RD53 investigation of CMOS radiation hardness up to 1Grad

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On behalf of the RD53 collaboration

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CENTRE DE PHYSIQUE DES PARTICULES DE MARSEILLE
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Outline

- RD53 collaboration
- Effect of radiation on CMOS
- Irradiation of 65 nm test transistors
  - Irradiation test at room temperature
  - Irradiation test at low temperature
  - Comparison across 2 different 65 nm processes
  - Comparison of results from different facilities (Xray, ^{60}CO, 3 MeV protons)
- Few results on ICs and blocks
- Summary and Conclusion.

RD53 collaboration

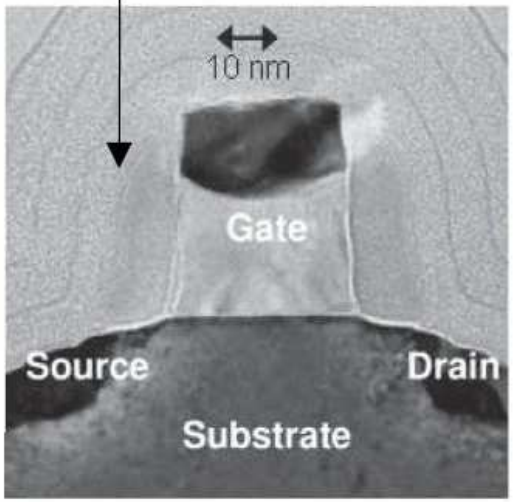
- "Development of pixel readout IC for extreme rate and radiation" : ATLAS-CMS-CLIC working group on small feature size electronics (focus on one 65nm techno so far)
- Goal:
  - Small pixels
  - Very high hit rates
  - Very high radiation levels

See Maurice GARCIA-SCIVERES: "RD-53 Progress on High Rate Pixel Readout chip"

- 6 working groups, among which one working on radiation effects (Bergamo-Pavia, CERN, CPPM, Fermilab, LPNHE, New Mexico, Padova, but also others)
- The work presented here essentially done in this framework

Radiation effects in CMOS

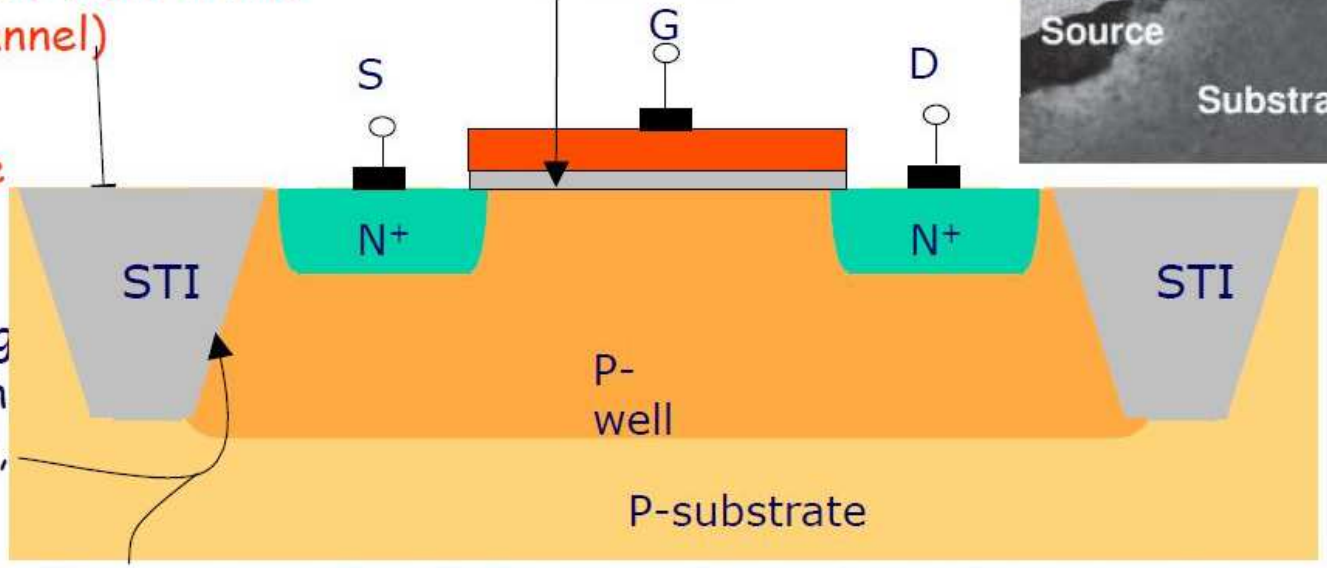
Spacer dielectrics may be radiation-sensitive



Thick Shallow Trench Isolation Oxide (~ 300 nm); radiation-induced charge-buildup may turn on lateral parasitic transistors and affect electric field in the channel)

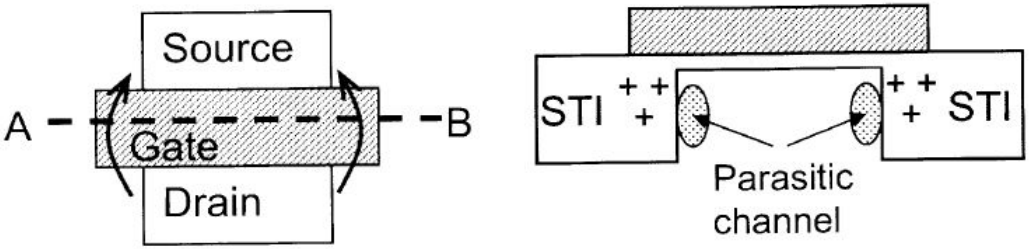
Thin (rad-hard) gate oxide for core devices, becomes thicker (and rad-softer) for I/O transistors

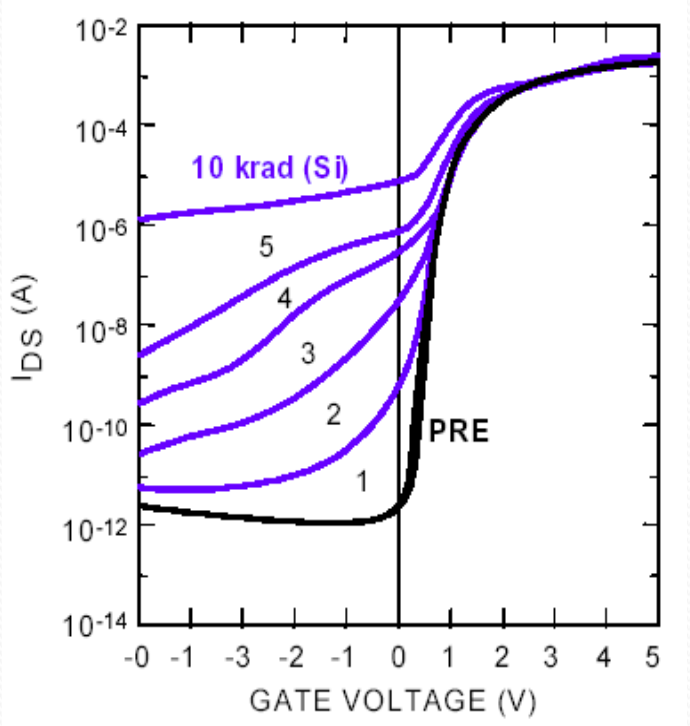
Doping profile along STI sidewall is critical; doping increases with CMOS scaling, decreases in I/O devices



Increasing sidewall doping makes a device less sensitive to radiation (more difficult to form parasitic leakage paths)

Radiation Induced Narrow Channel Effect (RINCE)

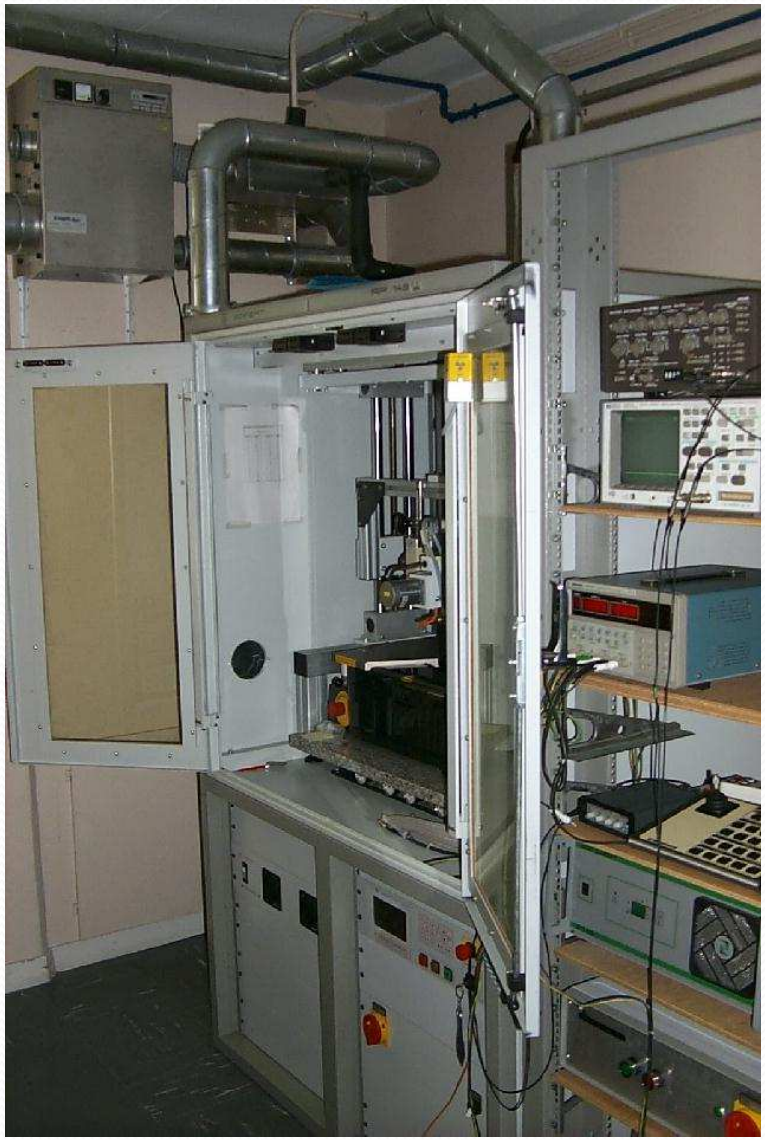




ref: Faccio (radiation induced edge effect in deep submicron CMOS transistors)

- Due to aggressive scaling into the deep sub-micron :
  - Threshold voltage shifts caused by charge buildup in the gate oxide has been reduced
- Trapping in in the isolation oxide (shallow trench – STI)
  - Radiation-induced positive charges opens inversion channel / parasitic transistor
  - The effect depends on the device width
  - Higher effect for narrow transistors
    - Parasitic transistor is a strong competitor to main channel
  - Increase in off-state leakage and Inter devices leakage
- Problem in IC design (power, overheating, and failure)

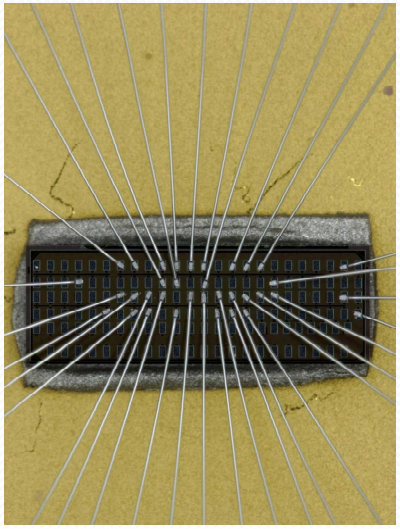
Xray Test Set up



- CERN Xray Tests : 10 keV
- A total dose of 1000 Mrad is reached in ~1 week following a Dose rate of 9 Mrad/hour (2.5krad/s)
- Measurement of devices characteristics takes 3-4 hours
- Evaluate the irradiation tolerance of digital devices (120nm/60nm to 480nm/60nm)
- Study the dependence of the irradiation hardbess on the device width
- Set device size suitable for digital library
- During irradiation and during annealing phase, pmos and nmos devices are set in :
  - Nmos : VG=VD=1.2V and VS=VB=0V
  - Pmos : VG=VD=0 V and VS=VB=1.2V

Tested Devices

Test chip designed by CERN

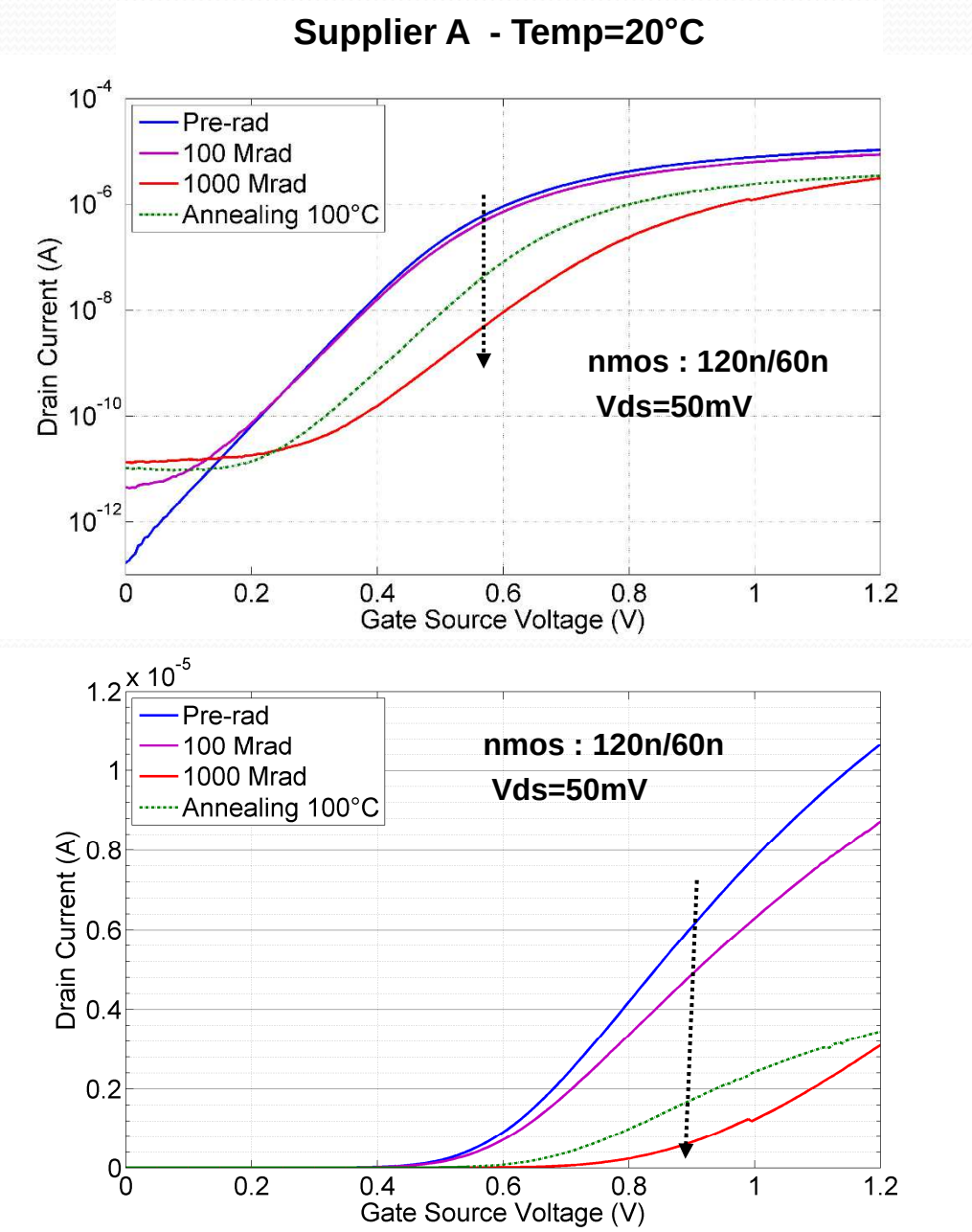


CERN frame contract foundry 65 nm

	Nmos devices	Pmos devices
	W/L (nm/nm)	W/L (nm/nm)
Regular nmos devices	120/60	120/60
	240/60	240/60
	480/60	480/60
	1000/60	1000/60
Regular enclosed devices (ELT)	800/60	1480/60
Hvt devices	200/60	200/60
Zvt devices (na)	500/300	
FOXFET devices	nw/nw, n+/n+, n+/nw	

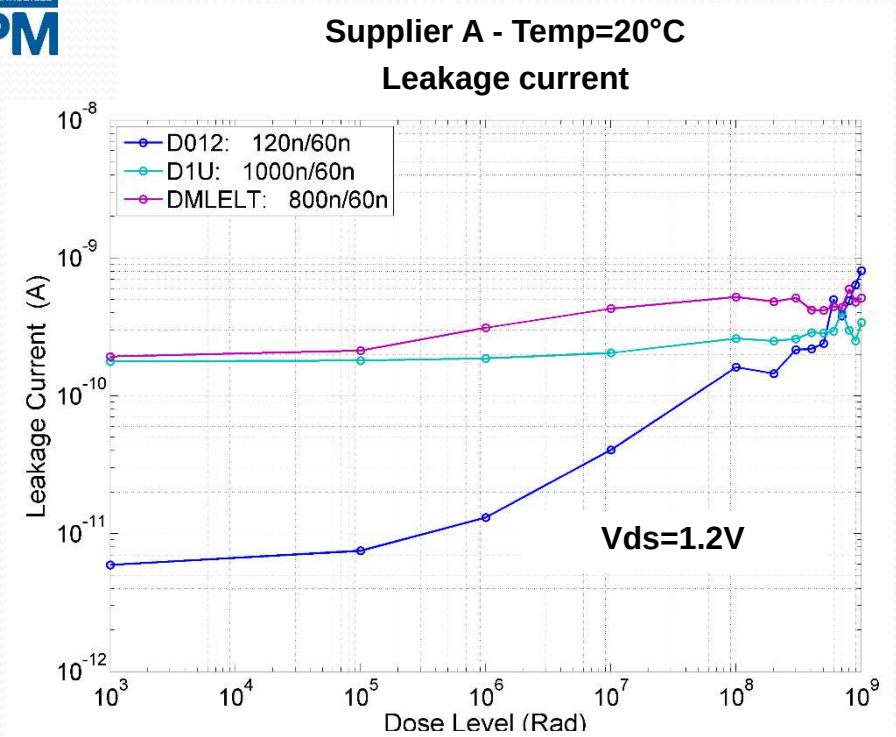
Room Temperature Irradiation Tests

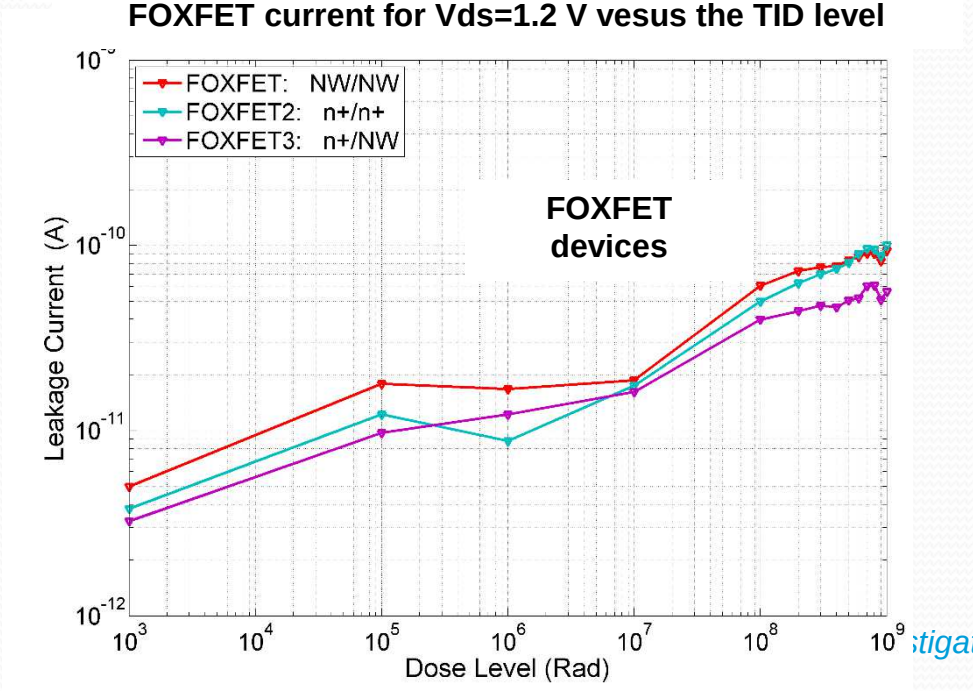
Ids(Vgs) variation for nmos device



- Test at room Temperature
- Only core transistors are considered
- Characteristics drawn for :
  - linear region (Vds = 50mV)
  - saturation (Vds =1.2V)
- Leakage current variation
- On state current variation
- Threshold voltage shift
- Transconductance variation
- Sub-threshold slope variation :
  - Allows to identify the effect of oxide traps Not and the effect of the interface traps Nit
- Annealing effect

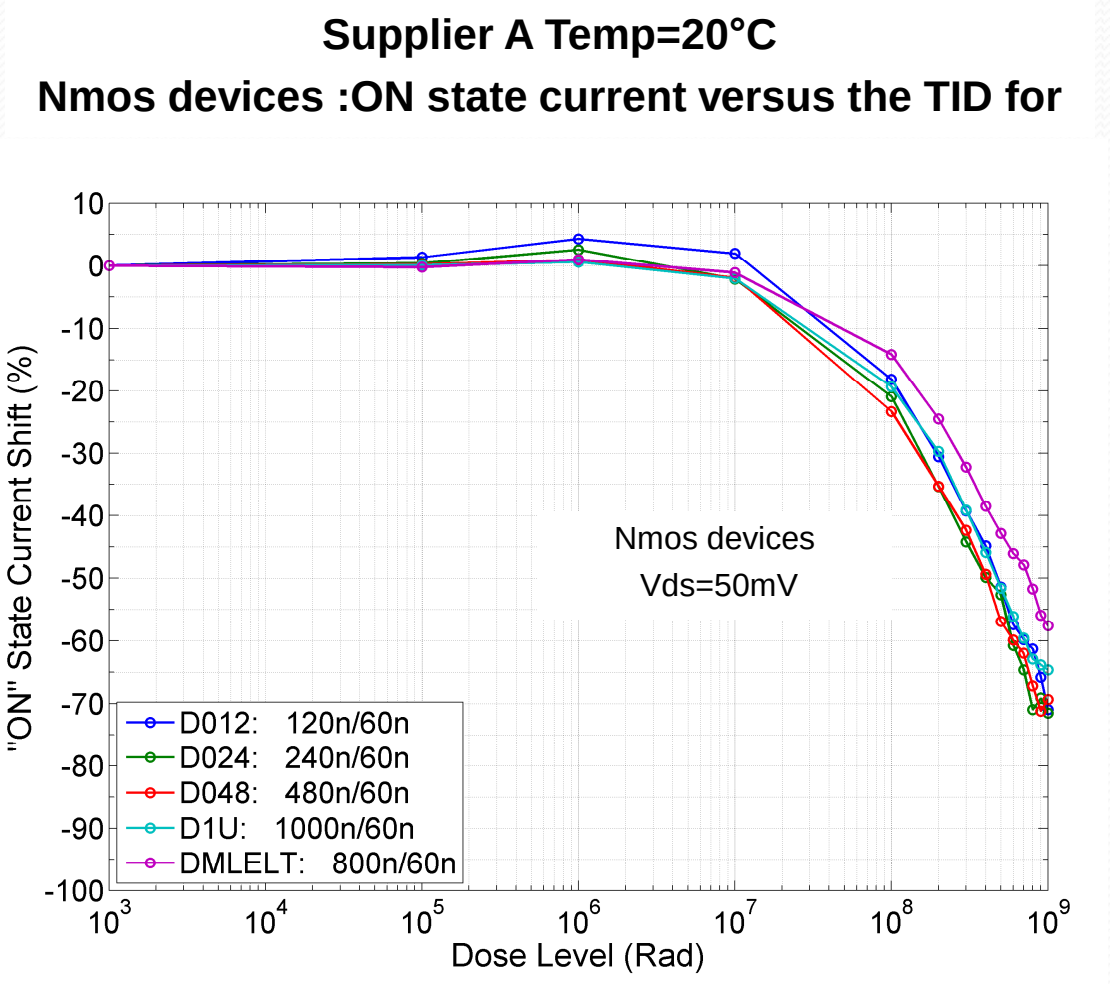
Leakage current





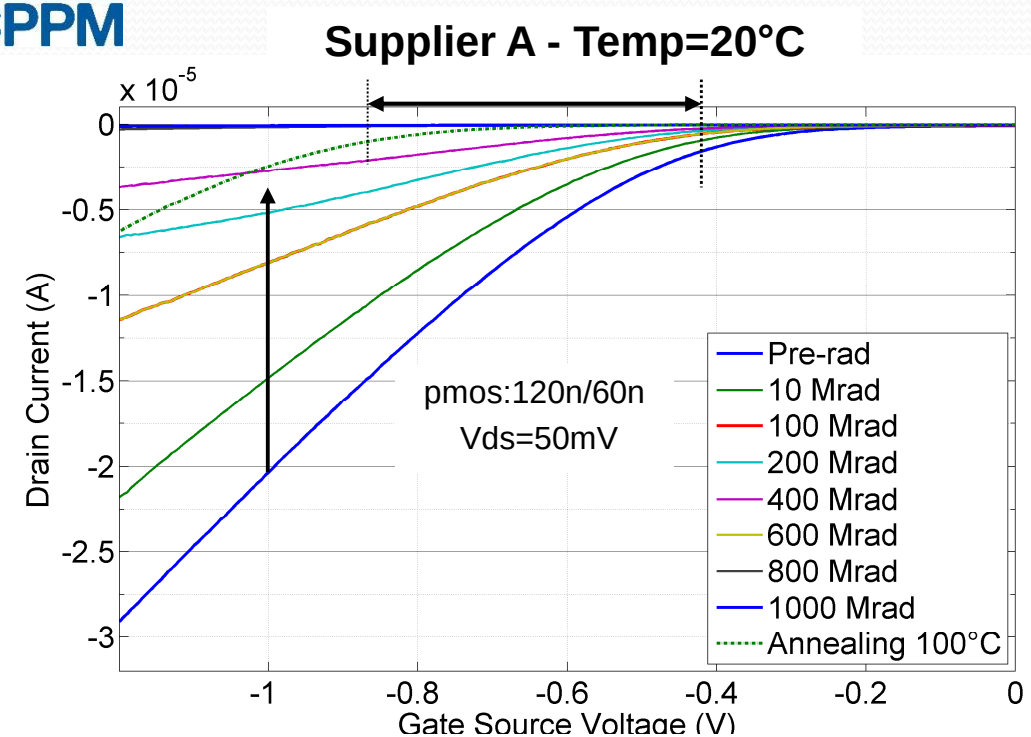
- Increase of the leakage is very limited
- Device with 120nm/60nm (the narrower one) shows the highest increase in leakage :
  - < 2 orders of magnitude for the level of 1000 Mrad
- Different FOXFET structures have been tested (NW/NW, n+/n+ and n+/NW)
  - The current variation still low at 1 Grad
  - The variation of the Inter-device leakage is also limited
- The 130 nm process used for the FEI4 design showed 3 order of magnitude variation for a dose level of 100 Mrad

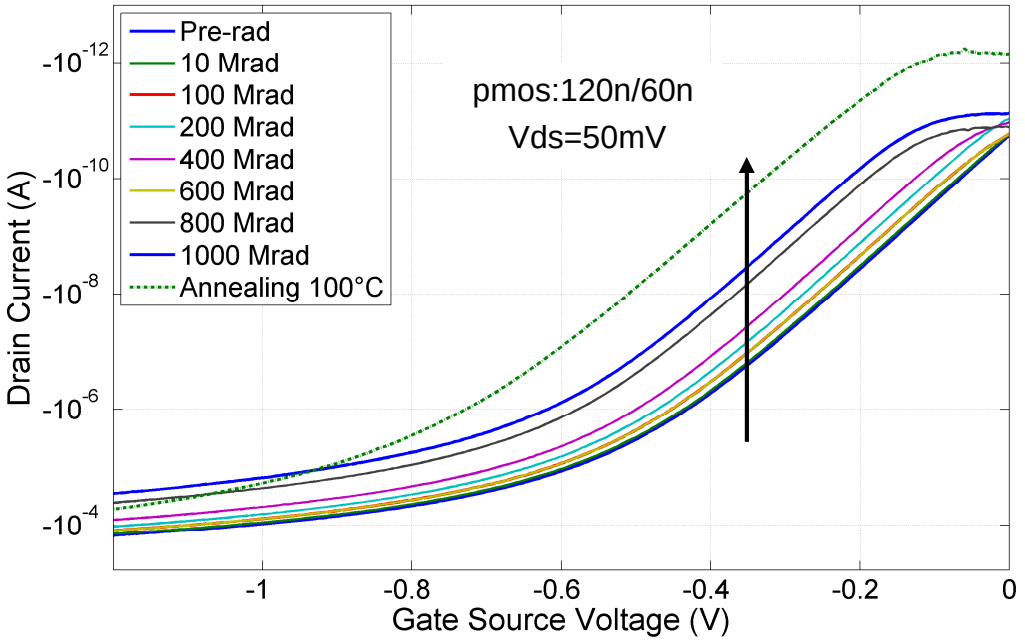
ON state current



- "ON" state current : Drain current measured for VGS = 1.2 V
- Driving current loss for all tested devices from a dose level of 200 Mrad
- In the linear region :
  - The loss is near 70 % for open geometry devices and does not depend lot on the width
  - ELTs degrade as well (10% less than open geometry)
  - The effect of W is not so clear for nmos devices
  - Parasitic device (STI) is not the unique explanation for this degradation
- Gate oxide still an issue ? Other effects ?
- Increase in subthreshold swing : Si/SiO2 interface traps
- 100°C annealing during 7 days reduces the loss to a value below 50% for all the devices

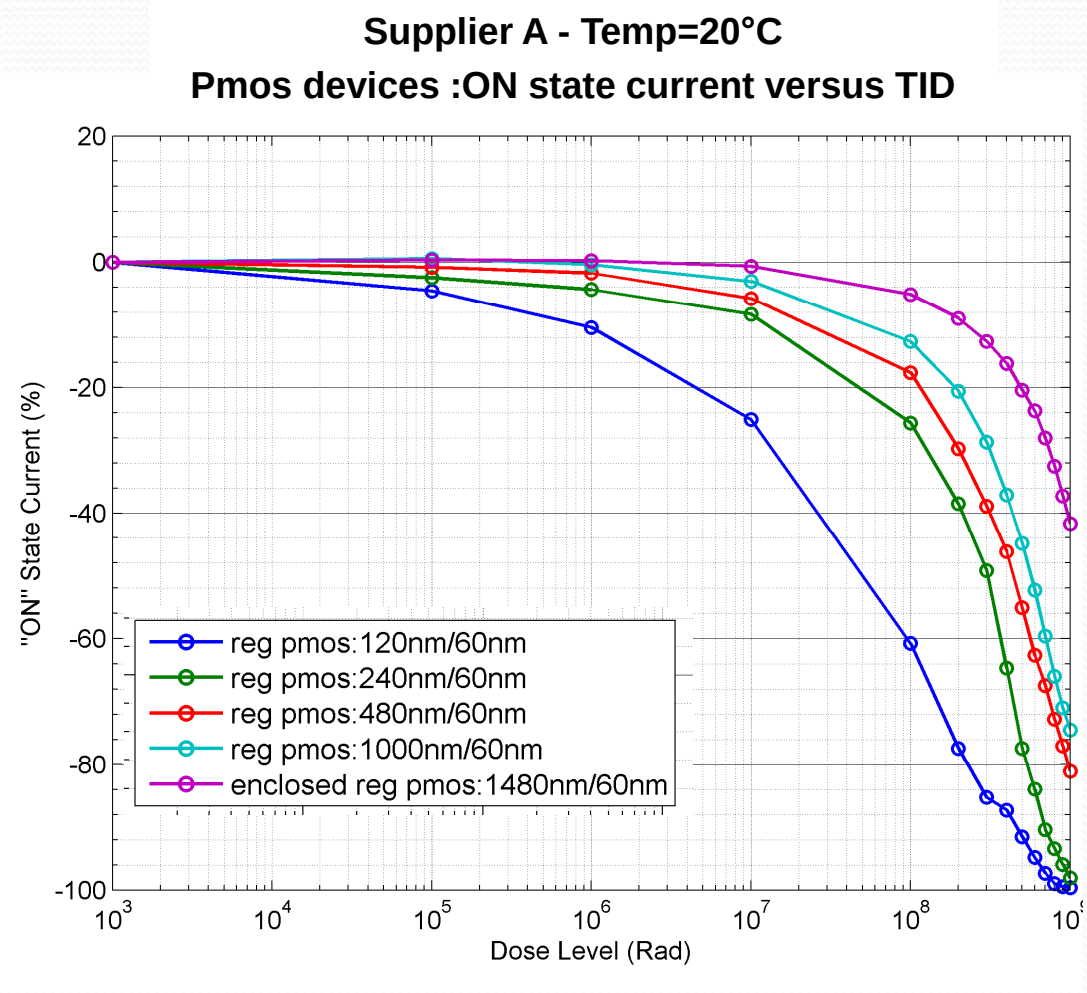
Ids(Vgs) variation for pmos device





- Id(Vg) for the narrower device (120nm/60nm)
- At the high level of dose, The device becomes completely “OFF”
- The GM factor (mobility) is more affected than the threshold voltage
- With annealing GM recovers well but Vth still increasing (reverse annealing)
- The Vth shift is ~ 0.45 V for the narrower device
- No issue with the leakage current
- No change in the subthreshold slope :
  - low effect of Interface traps
- Vth increases from a dose levels of 200 Mrad

pmos devices ON state current



- More degradation than the nmos device and depends more on the width
- At 1000 Mrad : “ION” decreases by 100% for W=120nm and 240nm
- ELTs (1480nm/60nm) degrade as well but “ION” loss is only 40%
- Annealing effect:
  - Slow recovery at room temperature
  - High temperature (100°C) helps recovering driving capability
  - Narrow devices recover more than large devices
  - The ION loss decreases from 100% to 78%
- Only a part of the degradation can be attributed to the parasitic STI device
- The other part ? Thin oxide still an issue at this level of dose ?

Summary table

		Supplier A Irradiation results		Supplier A Irradiation + 100 °C annealing	
		ION shift (%)	Vth shift	ION shift	Vth shift
Nmos device	120/60	-70%	0.35 V	-68%	0.15 V
	480/60	-70%	0.35 V	-42%	0.12 V
Pmos device	120/60	-100%	-	-78%	0.45
	480/60	-80%	0.1V	-68%	0.37

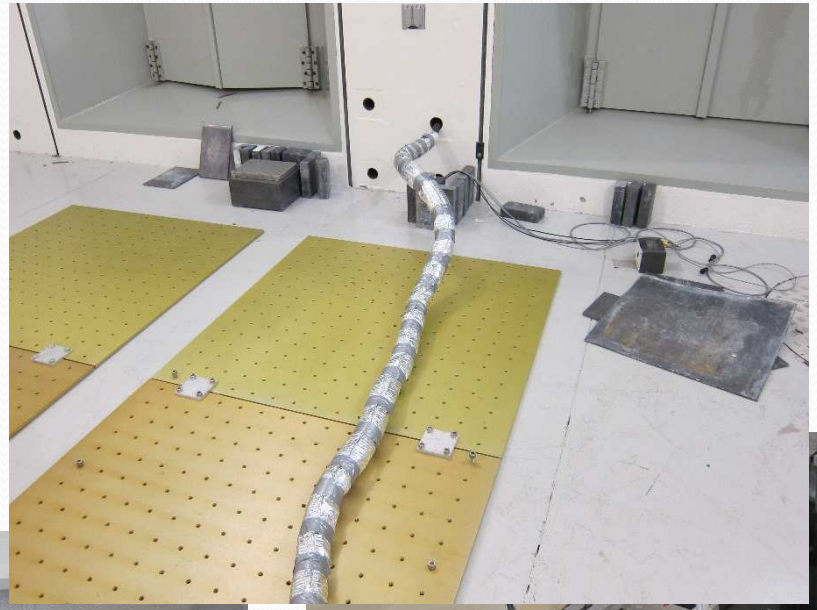
Extracted in the linear region (Vds=50mV)

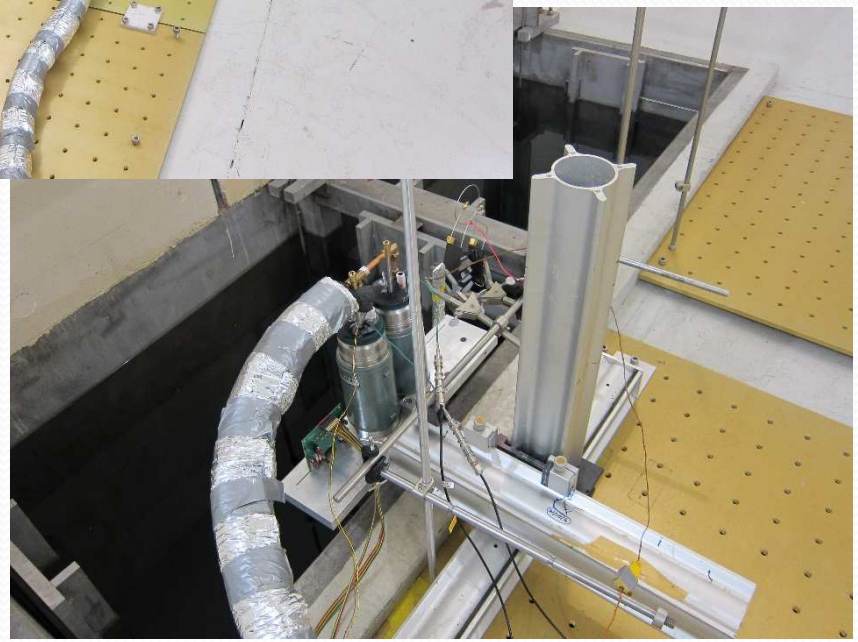
- Nmos device recovers with annealing
- Pmos device recovers GM but VTH increases

Low Temperature Irradiation Tests

Set-Up for low temperature irradiation at Sandia

David Christian et al, FNAL

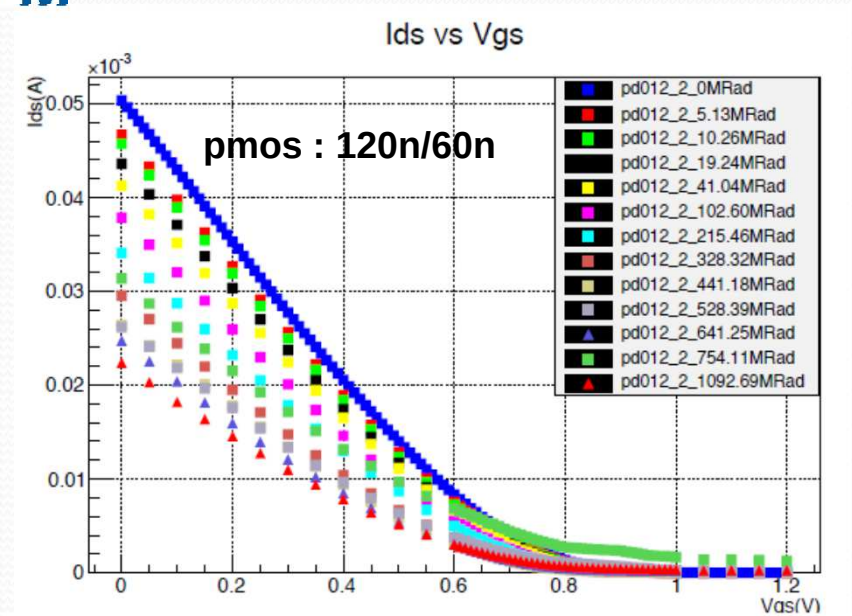


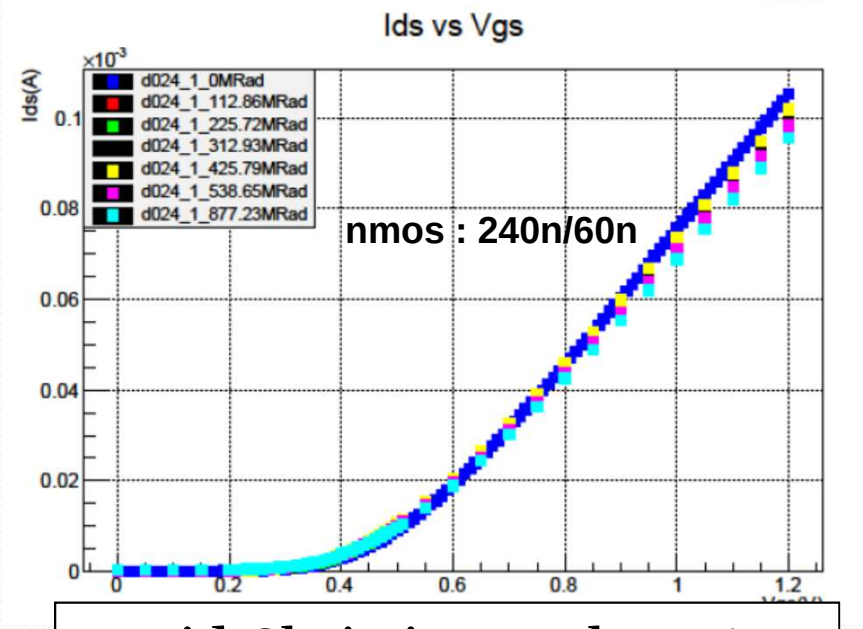


Irradiation Facility : Sandia

Source : 1 MeV γs from ^{60}Co

Low temperature tests





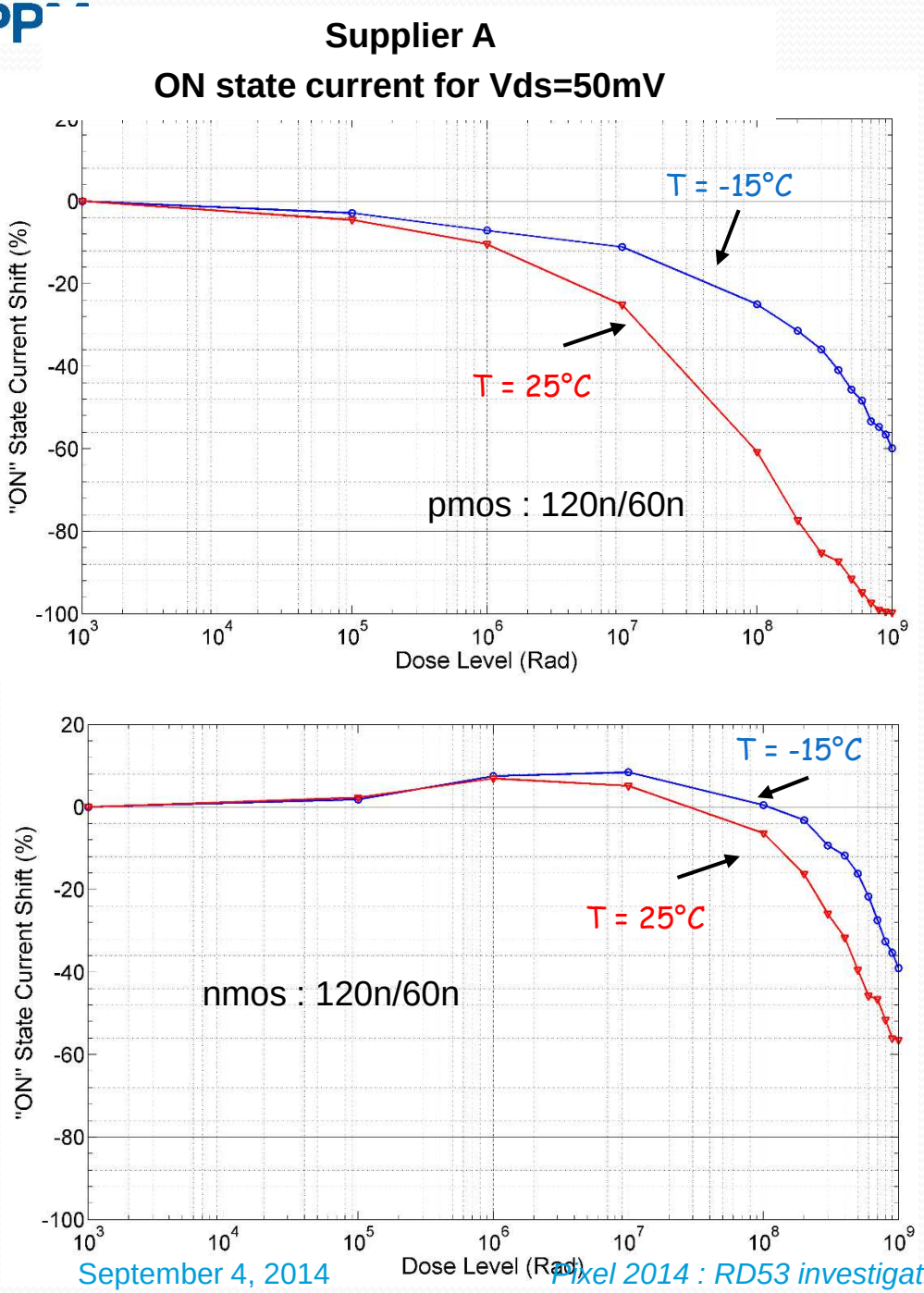
David Christian et al FNAL

- Sandia Gamma Irradiaton Facility
- Source : 1 MeV γs from ^{60}Co
- Dose rate =5.13 Mrad/hr (1.425krad/sec)
- Total dose = 1.1 Grad
- ICs kept at, or below, -20C except for ~10 minute periods while testing.
- Bias during Irradiation:
  - VG=1.2 V, VD=VS=VB=0 V (nMOS)
  - VG=VD=VS=1.2 V VB=0 V or VG=VB=0 VD=VS=1.2V (pMOS)
- Largest effect is loss of PMOS transconductance.
  - Biggest loss in smallest transistors.
  - Loss is not 100%
- No degradation for the nmos device !
- Benefic effect at low temperature ?

Comparison low/ambient temperature

- Low temperature irradiation test done using Xray CERN facility
- The same condition of the dose rate as for ambient temperature test
- The PCB is posed on a thermal chuck for which the temperature is set to -20°C
- Temperature of the devices estimated to -15°C
- Operational temperature for ATLAS-pixel is -13°C

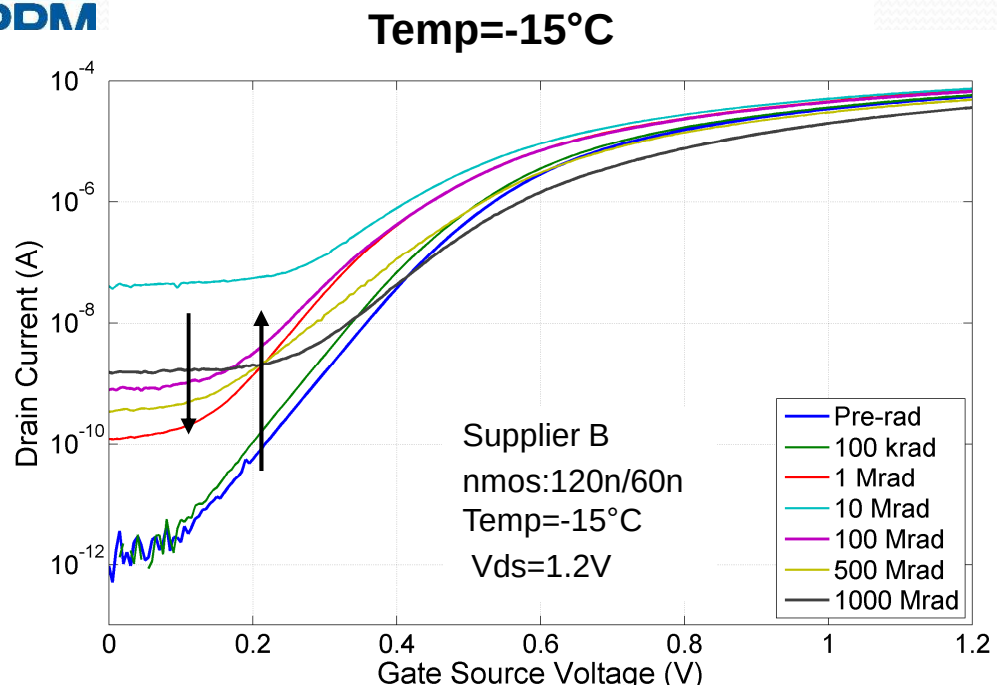
Comparison low/ambient temperature

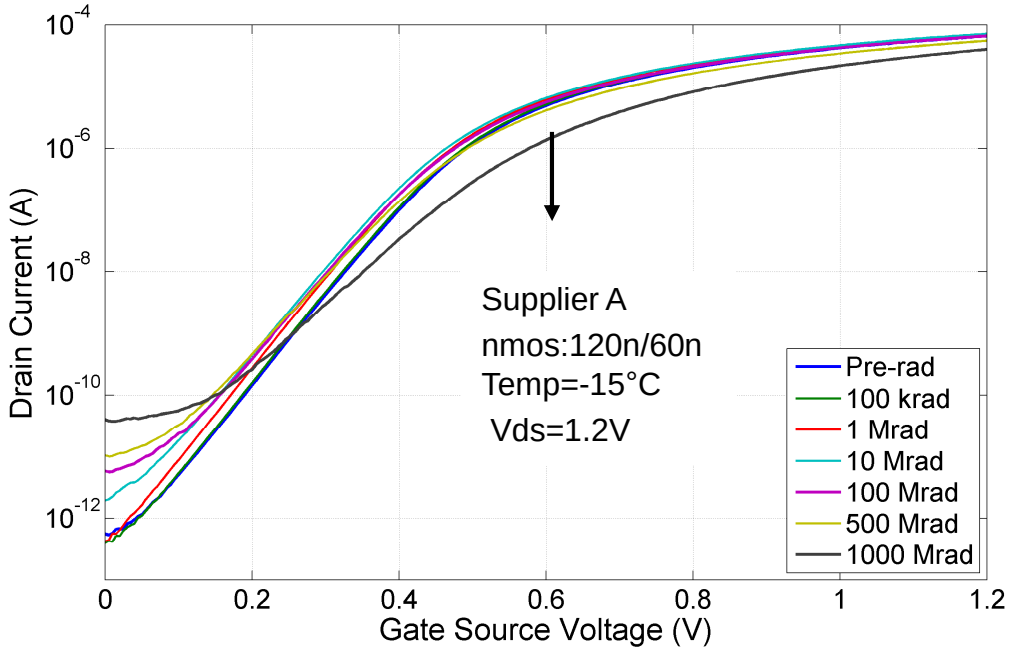


- Less degradation of the pmos transistors at -15°C than at room temperature
- 120nm/60nm pmos device is not completely 'off' at 1000 Mrad
- The ON current decrease is "only" 60% at -15°C
  - Compatible measurements given by the FNAL (55% loss)
- Nmos devices show also less degradation
- Leakage current :
  - Measurements show that the relative variation is similar as for the ambient temperature (2 orders of magnitude)

Comparison of 2 different processes

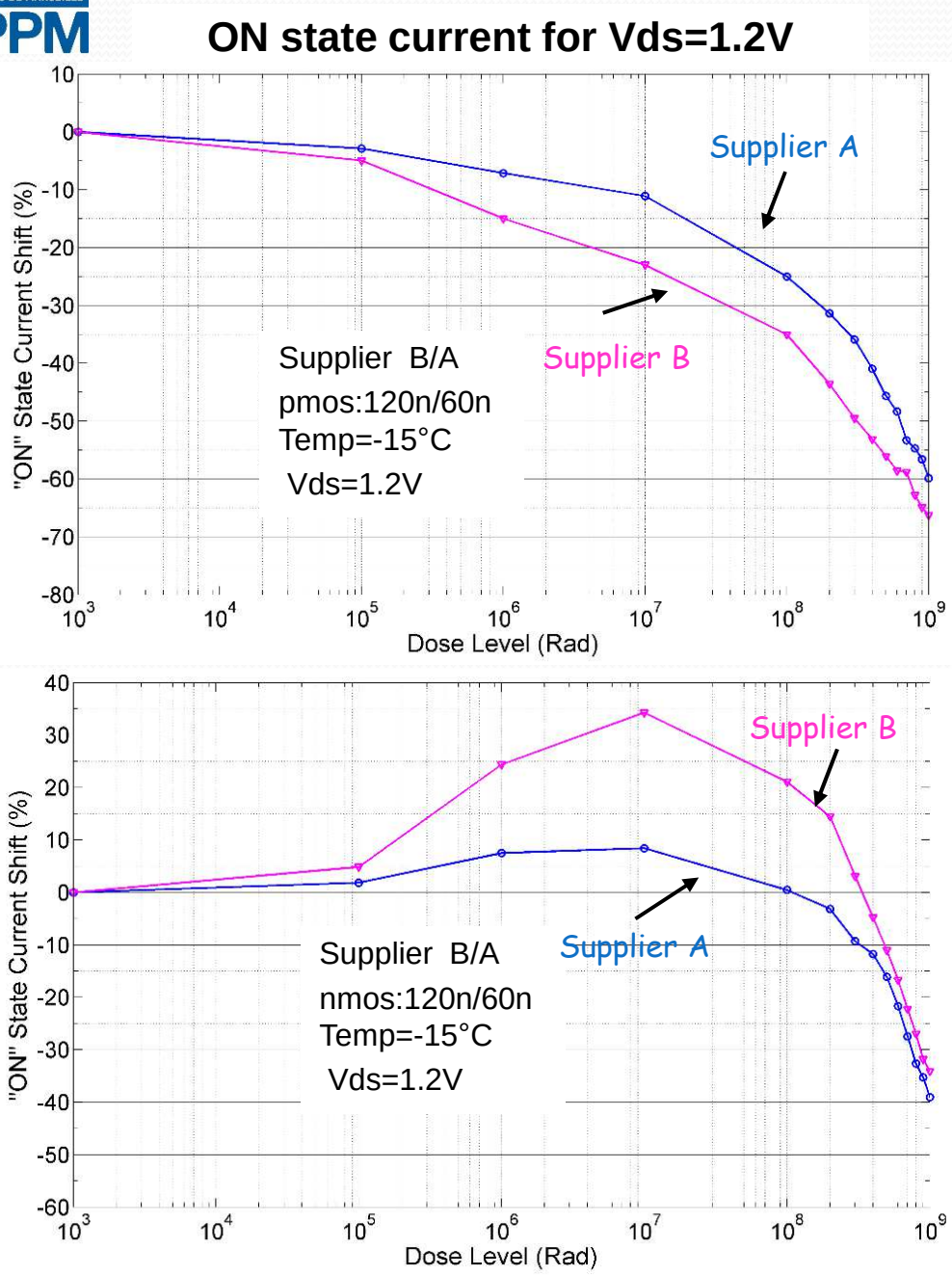
Comparison of processes A / B at -15°C





- A test chip provided by MOSIS through Berkeley
- Compared devices : L=60 nm and W : 120nm, 240nm, 480nm and 1um
- Leakage current is an issue for the process B
  - Parasitic transistor leaks much more than for the process A
  - The maximum value (~10 Mrad) is 200 nA
  - 10^5 times the pre-rad value

Comparison of processes A / B at -15°C



- The degradation at the high level of dose is not related only to the 65nm process from the supplier A (CERN contract)
- This degradation is observed for another 65nm process (supplier B)
- Pmos : Loss of transconductance in both cases
- Nmos : Larger rebound region between 100krad-100Mrad for the supplier B
- The degradation depends more on the device width for B than for A in this region
  - Confirms that the parasitic STI device is more influent for the process B

Summary table

		Supplier A Irradiation results at 20°C		Supplier A Irradiation results at -15°C		Supplier B Irradiation results at -15°C	
		ION shift	Vth shift	ION shift	Vth shift	ION shift	Vth shift
Nmos device	120/60	-70 %	0.35 V	-65 %	0.33 V	-52 %	0.08 V
	480/60	-70 %	0.35 V	-48 %	0.18 V	-50 %	0.18 V
Pmos device	120/60	-100 %	-	-60 %	0 V	-65 %	0.13 V
	480/60	-88 %	0.05 V	-52 %	0.023 V	-63 %	0.06 V

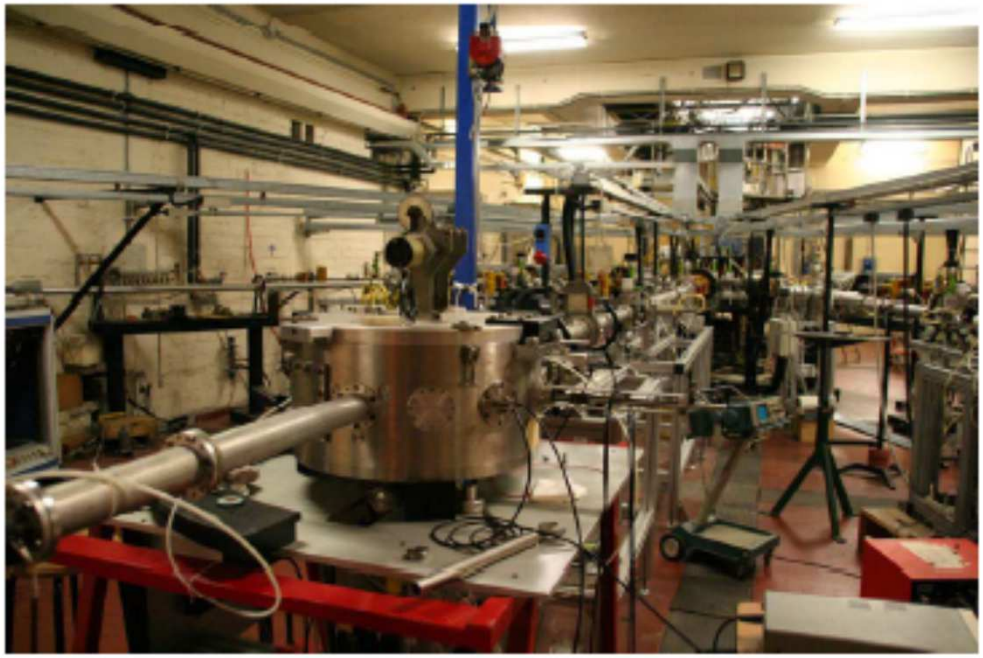
Extracted in the linear region (Vds=50mV)

- Degradation is smaller at low temperature
- Pmos device : The threshold shift after irradiation is now acceptable. The main effect is the loss of transconductance
- BUT, we need to wait for annealing results to conclude about hardness at low temperature

Proton Irradiation at Ambient Temperature

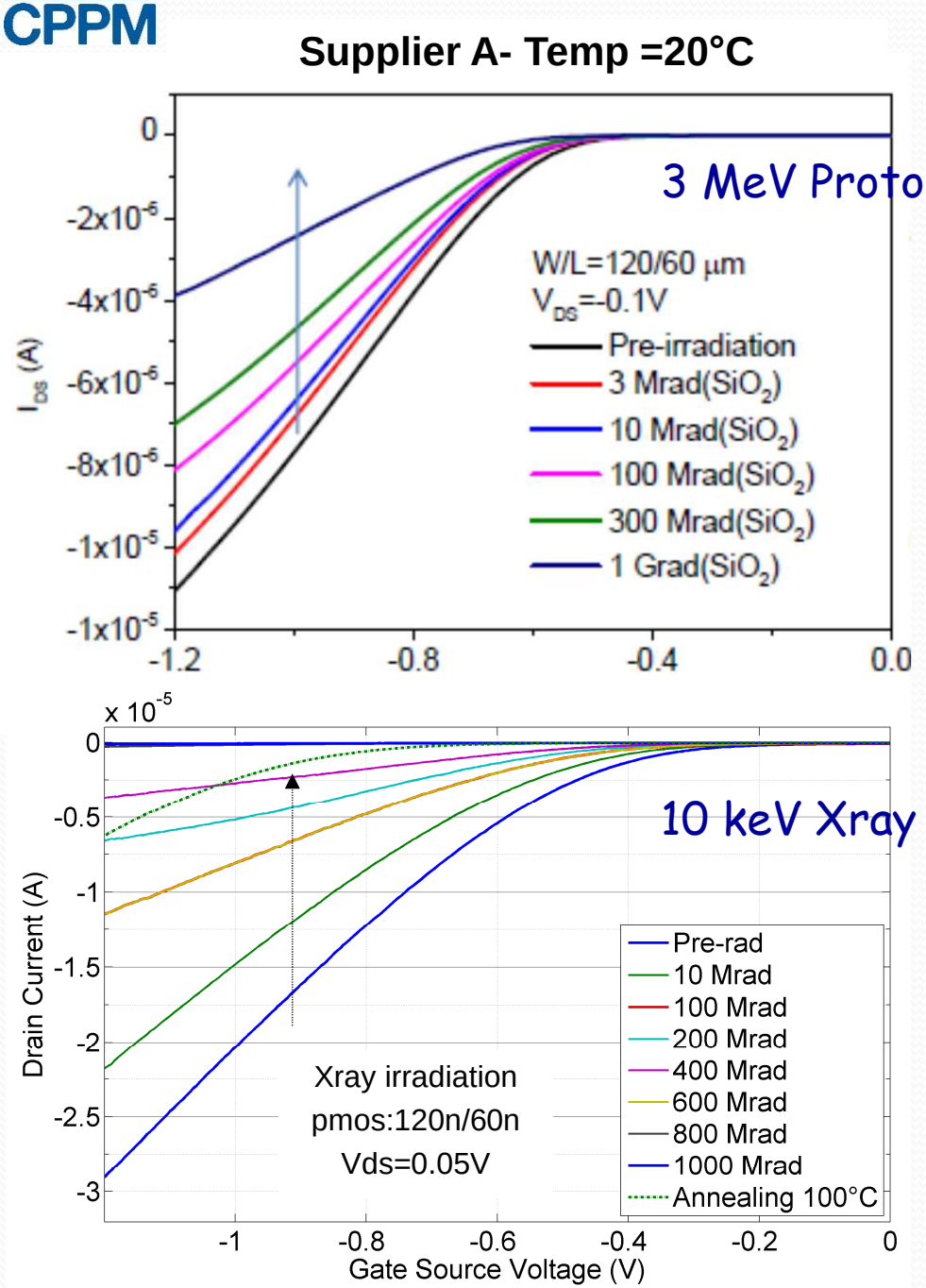
Proton irradiation

- 3 MeV proton beam
- CN accelerator, INFN-National Laboratory of Legnaro
- Dose rates up to 1 Mrad(SiO2)/s can be reached, suitable for 1 Grad(SiO2) fast irradiation test
- 60 krad(SiO2)/s until 100 Mrad
- 300 krad(SiO2)/s from 100Mrad to 1000 Mrad
- Only 2.5 krad/s used for Xray testing
- Bias during Irradiation:
  - VG=VDD, VD=VS=VB=0 V (nMOS)
  - VG=VD=VS=VB=0 V (pMOS)



Lili Ding et al, Padova.

Proton / Xray tests results



- at 1 Grad : 3 MeV proton : loss of 65 %. The device is still working (Xray : pmos device becomes off)
- nmos driving loss : -25 % for proton irradiation and -70% for Xray
- The increase of the pmos VTH after 100 °C annealing is observed for both tests
- After 100 °C annealing Vth shift (Xray) still higher than the Vth shift (3MeV proton) (450 mV/ 140 mV)
- Bias, Dose rate, Fractional yield ..
- Go even further at the annealing ?

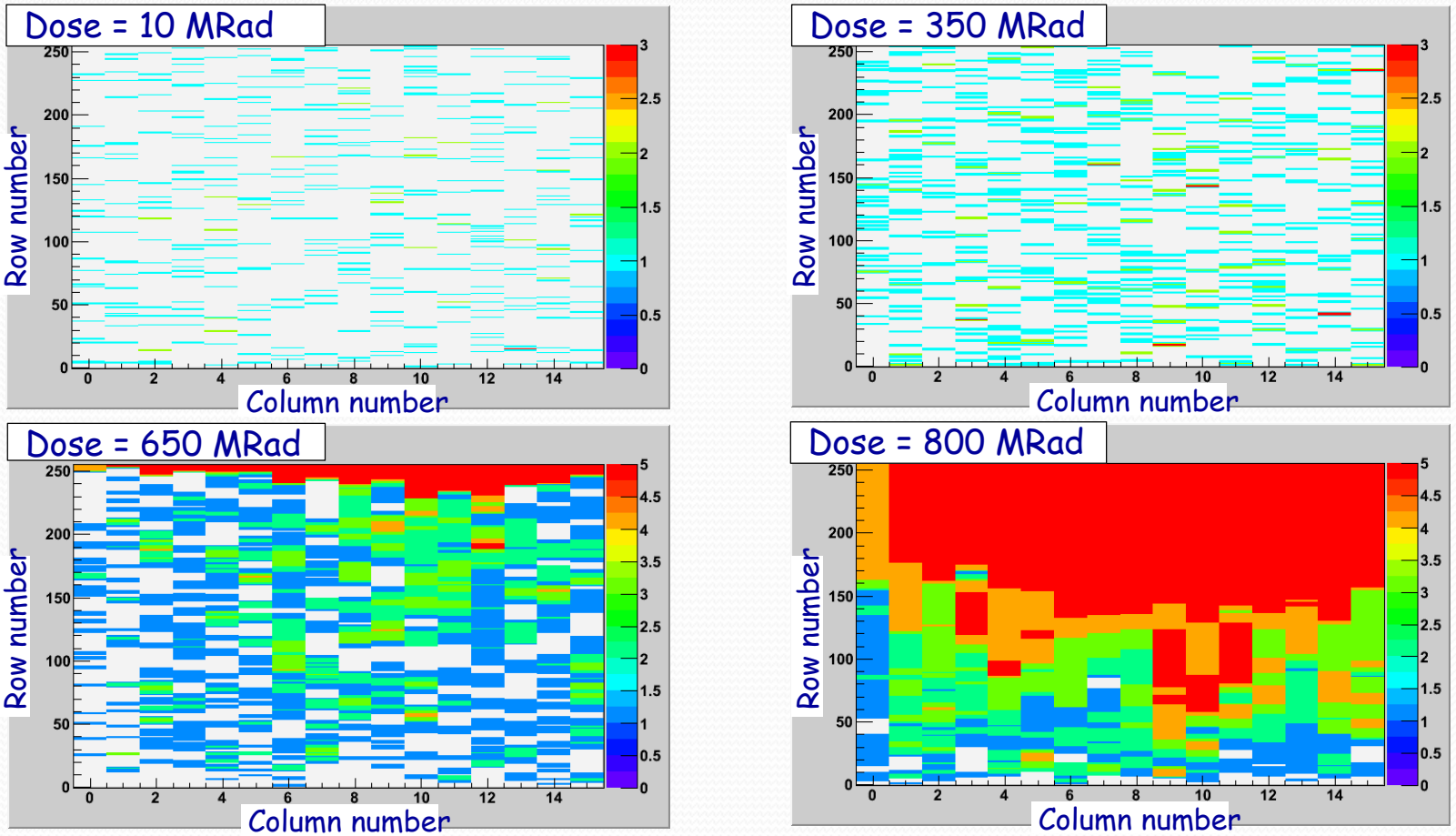
Summary table

		Supplier A 10 keV Xray 1 Grad + annealing at 100 °C		Supplier A 3 MeV proton 1 Grad + annealing at 100 °C	
		ION variation	Vth shift	ION variation	Vth shift
Nmos device	120/60	-68%	0.15 V		0.075 V
	480/60	-42%	0.12 V		0.05V
Pmos device	120/60	-78%	0.45 V		0.14 V
	480/60	-68%	0.37V		0.06 V

- The degradation (reverse annealing) of the pmos VTH after 100 °C annealing is observed for both tests
- Vth shift (Xray) still higher than the Vth shift (3MeV proton) (450 mV/ 140 mV)

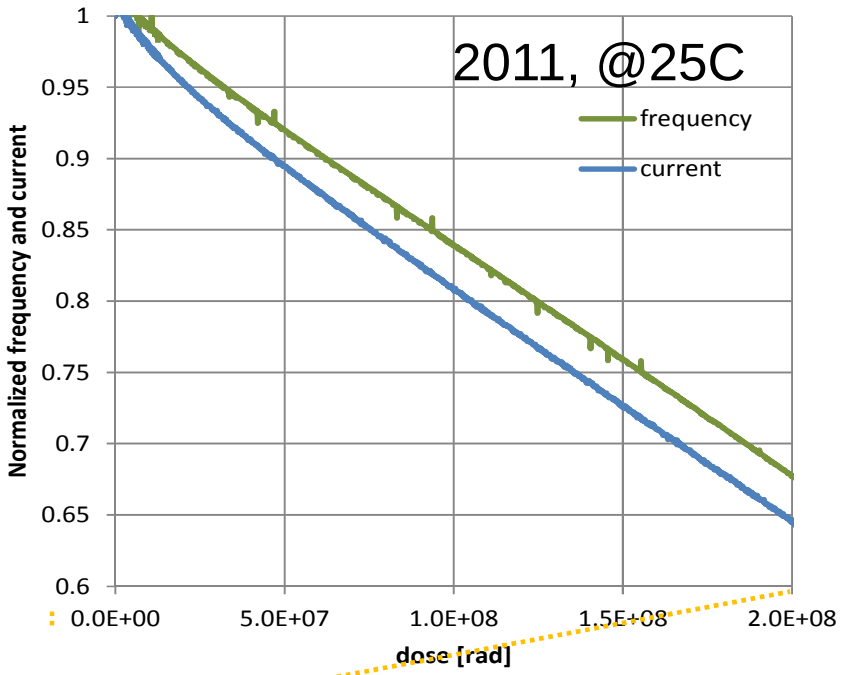
IC Irradiation Test Results

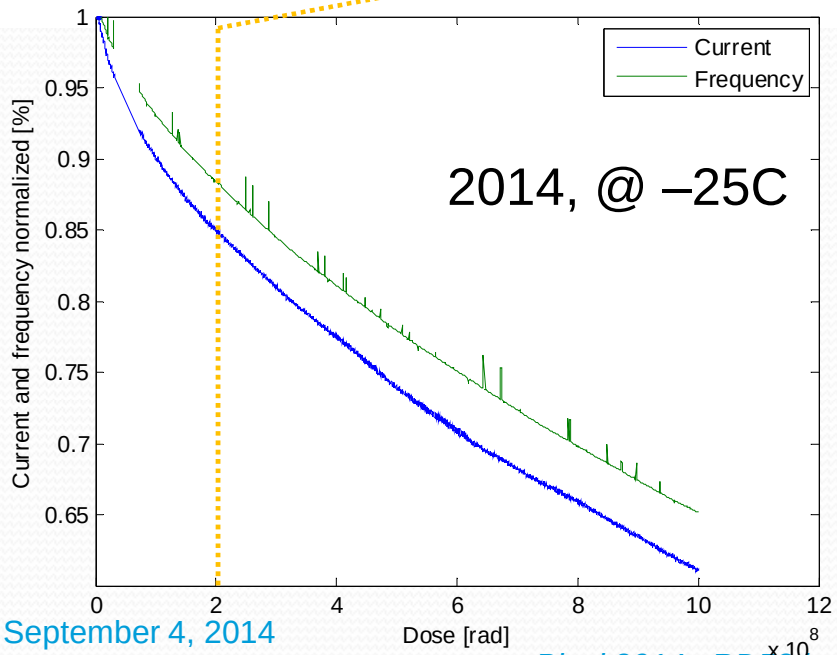
Dose effects on Shift register



- SEU tests carried out at the CERN PS with 24 GeV proton on the 65 nm Pixel array proto chip developed by LBL
- Observed localized bits stuck in shift register used for pixel config. Loading and Systematic errors begin to appear for the pattern “1111”
- The effect increases with the dose

Test IC developed by CERN



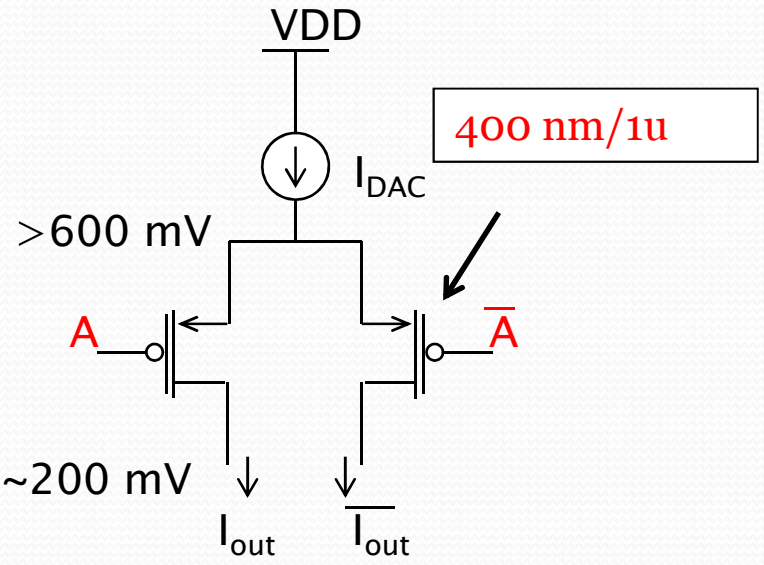


- 64 kbit Shift-register
  - Min W=150nm for both p and n
- 56 kbit SRAM (from foundry compiler)
  - MinW = 90nm
- Ring oscillator
  - 1025 inverters Wn=195nm, Wp=260nm
- Ring oscillator 2011 test at 25C
  - -32% @200Mrad
  - -13.8% after annealing
- Ring oscillator 2014 test at –25C
  - Uses the same sized inverter:
  - -12% @200Mrad
  - -35% @1Grad

Sandro Bonacini et al, CERN

CLICpix Test chip Irradiation Test

- XRay irradiation performed to 800 Mrads at 25 °C
- Digital Design : OK
- Analog Design :
  - Analog performances of the measured chip were found to be considerably degraded.
  - Loss of functionality at 400Mrad
  - Recovered with annealing, but strong impact on performance remains (noise, matching)
- TID / biasing effects in PMOS
  - DACs use PMOS switches to control a current mirror for each bit
  - At high rates switches irradiated while they are ON degrade more quickly than the ones irradiated while they are OFF
  - Above 200MRad, damaged switches are unable to let the nominal current pass (their driving current becomes too low).



Above 200 MRad.

Pierpaolo Valerio, CERN

Summary

- Unexplored territory in terms of process and radiation level
- CERN frame contract 65 nm process tested to 1 Grad at ambient and low temperature
- Limited variation of the Intra-device and inter-device leakage current
- Ambient temperature
  - PMOS device :
  - Strong drive loss for small W and narrowest devices completely off above few 100 Mrads
  - Recovers driving with annealing at 100°C But
  - Unacceptable increase on the threshold
  - NMOS device
  - shift of Vth and drive capability loss
  - 100 °C annealing seems to be benefic.
  - devices might be operated to close to ~1GRad TID down to small W
- Low Temperature
  - Results at low temperature are very promising – Less Degradation
  - We have to consider annealing effects
  - Define the annealing conditions compatible with the operational environment

Summary

- Differences between measures done by different groups at different facilities (10 keV Xray, ^{60}CO, 3 MeV protons) :
  - Device biasing, Dose rate, Fractional yield ...
- Test chips are provided from different Fab (Fab12 and Fab 14)
  - Good reproducibility from the same Fab
- The hardness of another 65nm process is explored
  - The degradation at high TID is probably common for the other highly scaled processes
  - Process from CERN contract foundry better in point of view leakage
- Most of the effects seeing in test IC seems compatible with device testing
- Other damages type (Xray / neutron/ proton … investigate if DD becomes an issue)
- Relation to other stresses: NBTI,…
- Still to come later: SEE studies / Statistical spread after irrad / etc…
- Define some rules and strategy for the chip design
- Define simulation models

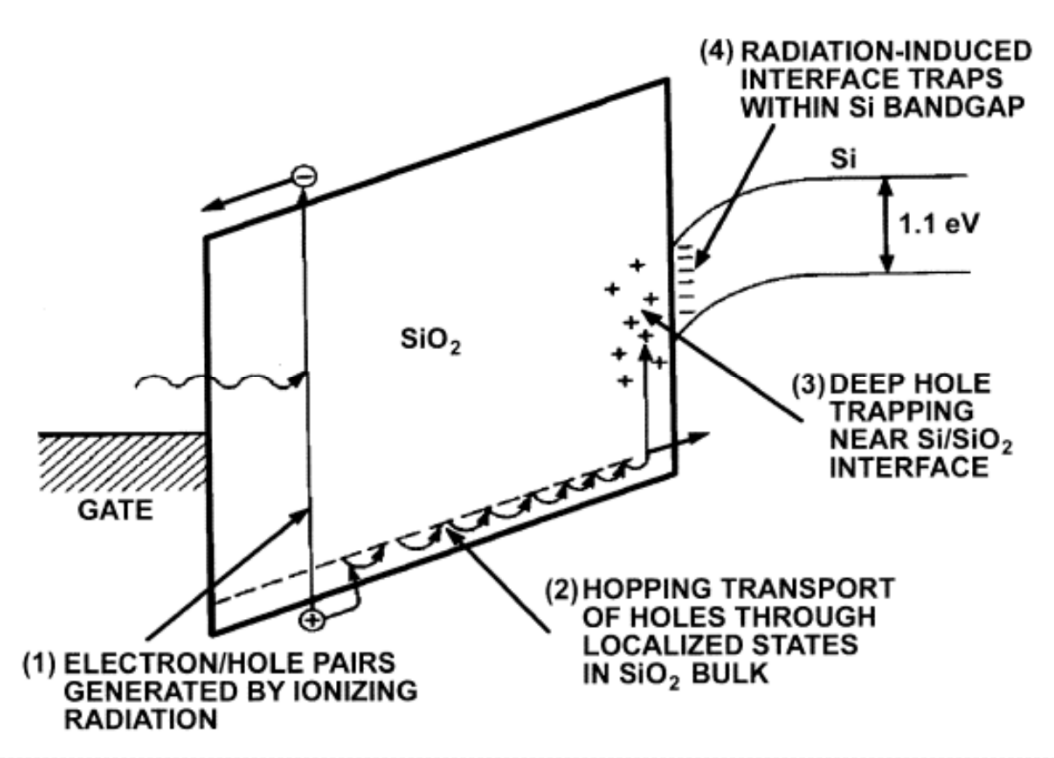
Thanks for your attention

Radiation effects in CMOS

Typical values (room T):

$$\mu_{e^-} \sim 20\,cm^2.V^{-1}.s^{-1}$$

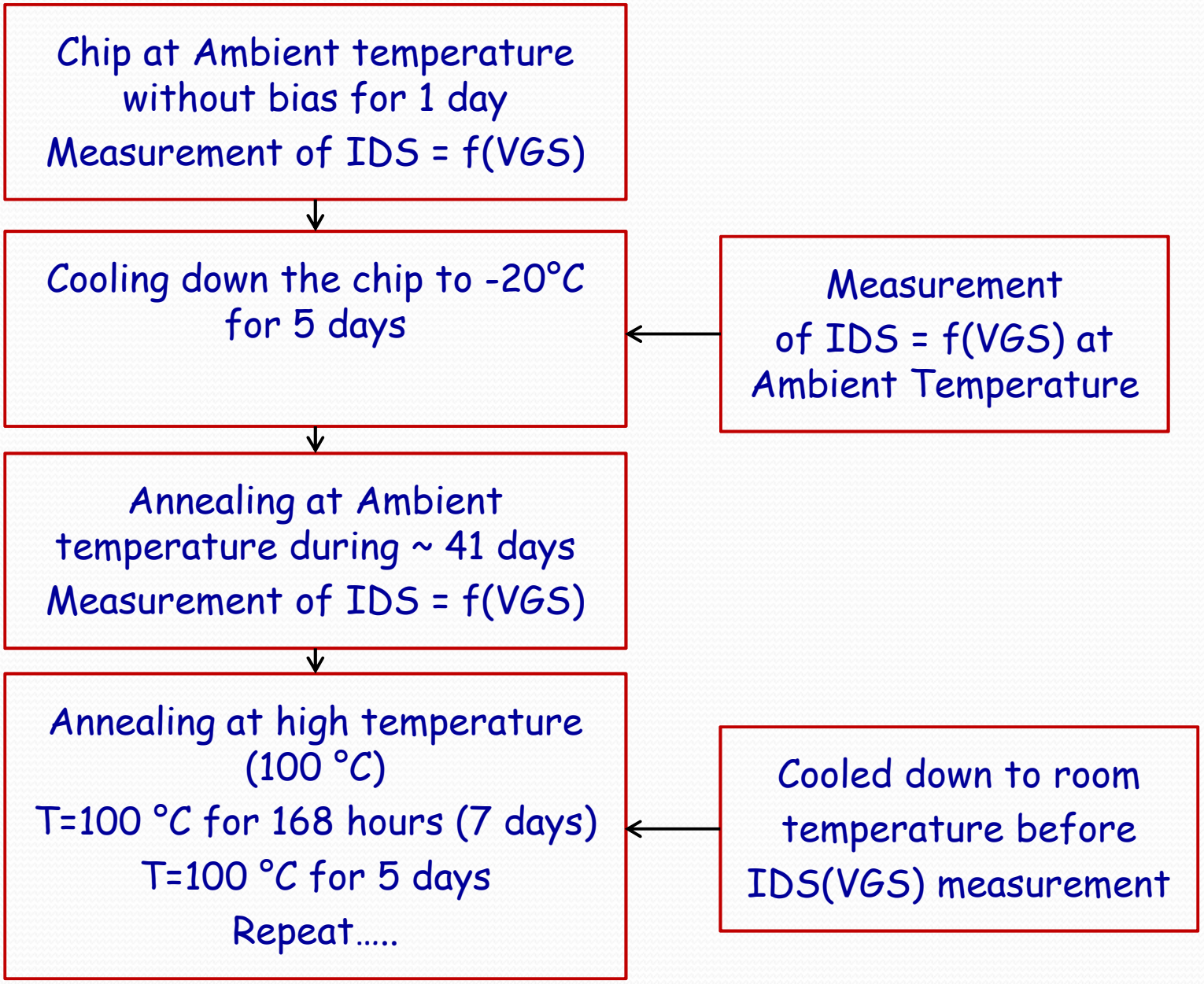
$$\mu_{hole} \sim 2.10^{-5} cm^2.V^{-1}.s^{-1}$$



(after McLean and Oldham, HDL-TR-2129 1987)

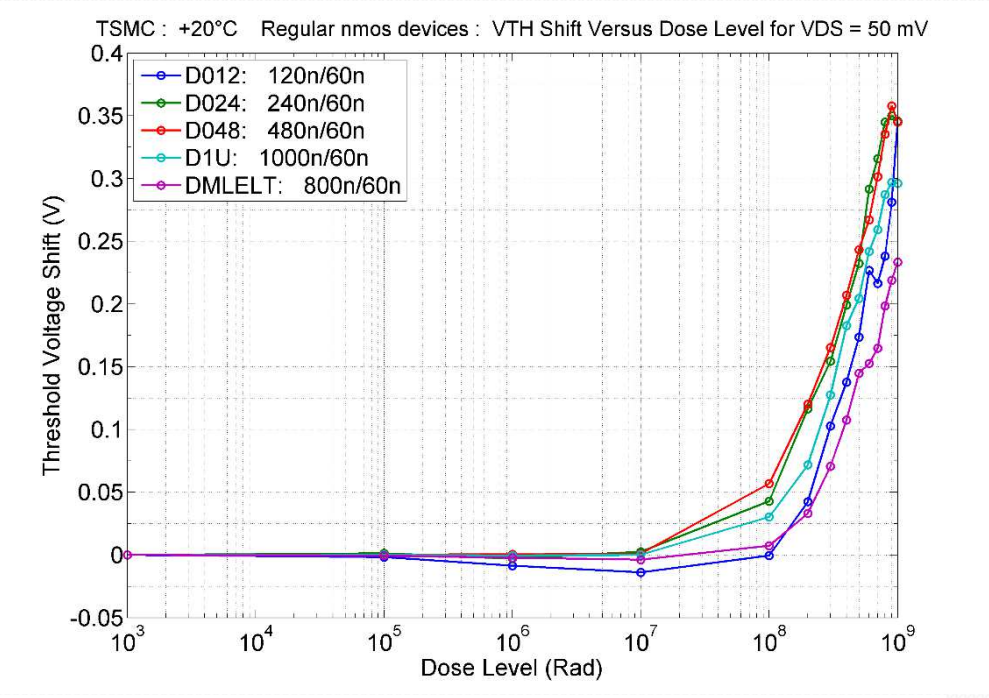
- 1st step: Ionizing Radiation → electron/hole pairs creation in oxide. Depending on biasing, electrons swept out in ~ps. Still fraction e- / holes recombine
- 2nd step: Hopping hole transport to Si/SiO2 interface
- 3rd step: Holes at interface → long-lived trap states -> Qot
- 4th step: Interface traps build-up : -> Qit
- Reminder:
  - gate thickness 2.6nm
  - hole mobility is << than e- mobility

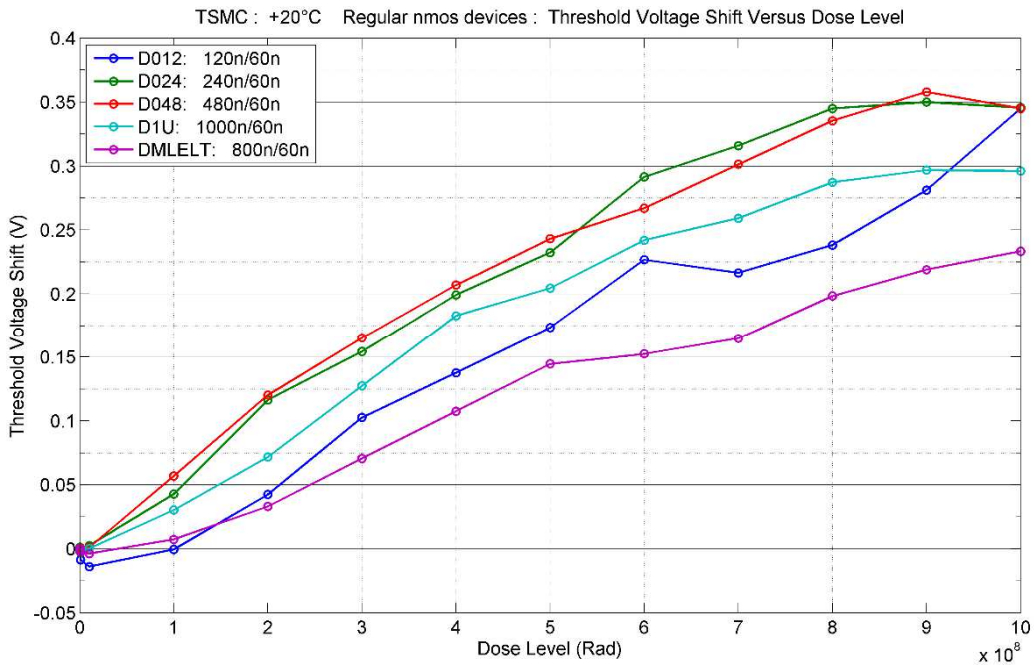
Post-irradiation tests



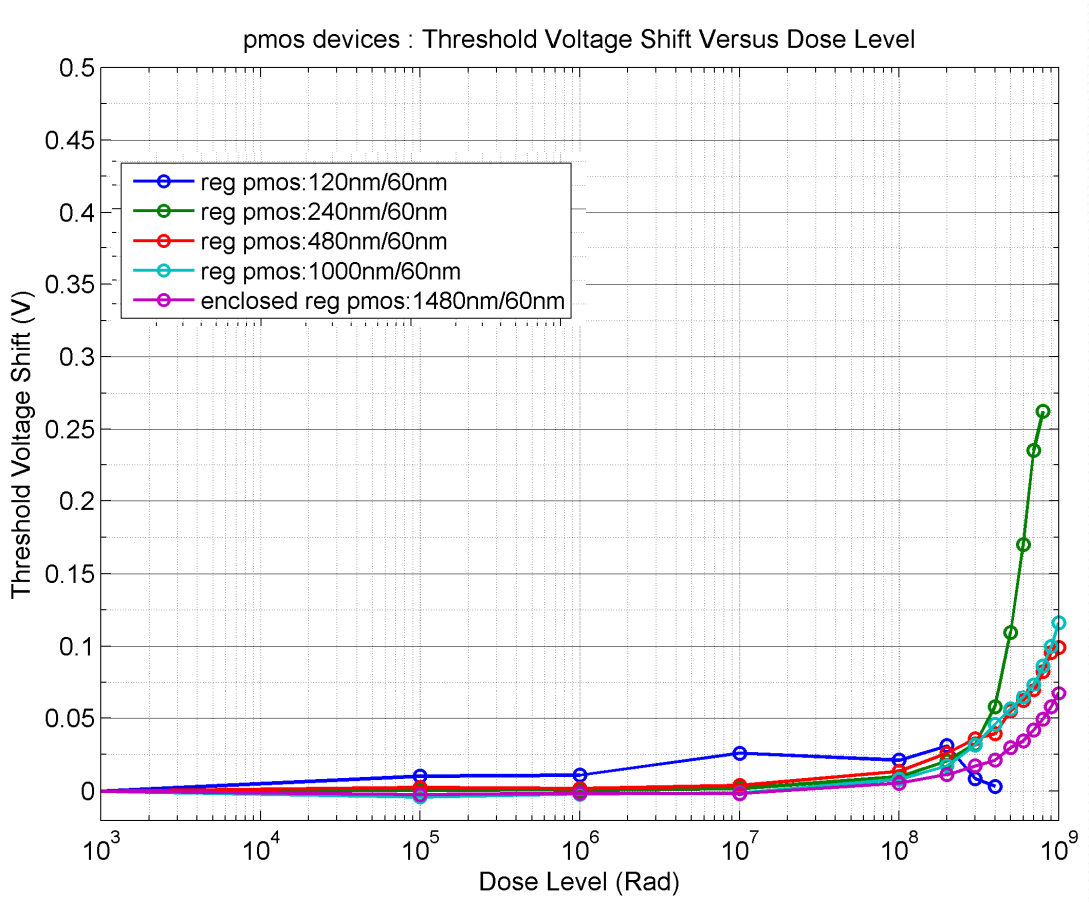
NMOS threshold shift

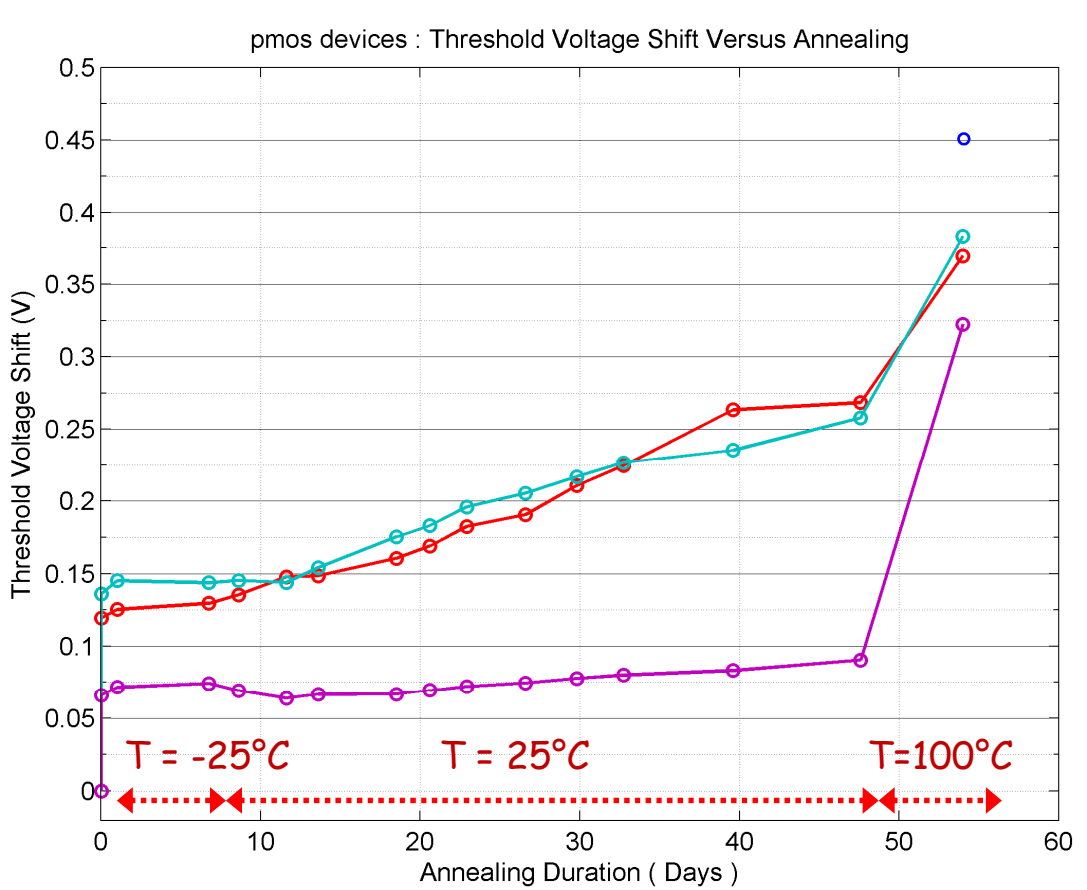
- A little decrease of the threshold for low dose level
  - 20 mV negative shift for the minimum width device
  - Concurrence between the Not positive charge and the Nit negative charge in parasitic devices
- For levels of dose > 200 Mrad, the absolute value of Vth increases
  - Interface states : Threshold shifts in the positive direction
  - At 1000 Mrad, the Vth shift is between 230mV to 350 mV
  - ELT device shows a Vth shift but less than open geometry devices
  - Qausi linear variation of the threshold versus the dose to 800 Mrad : 0.4mV/Mrad
- The Vth recovery at room temperature is very slow
- High Temperature annealing (100 °C for 7 days) :
  - The Vth recovery is accelerated and the global Vth shift is < 200 mV





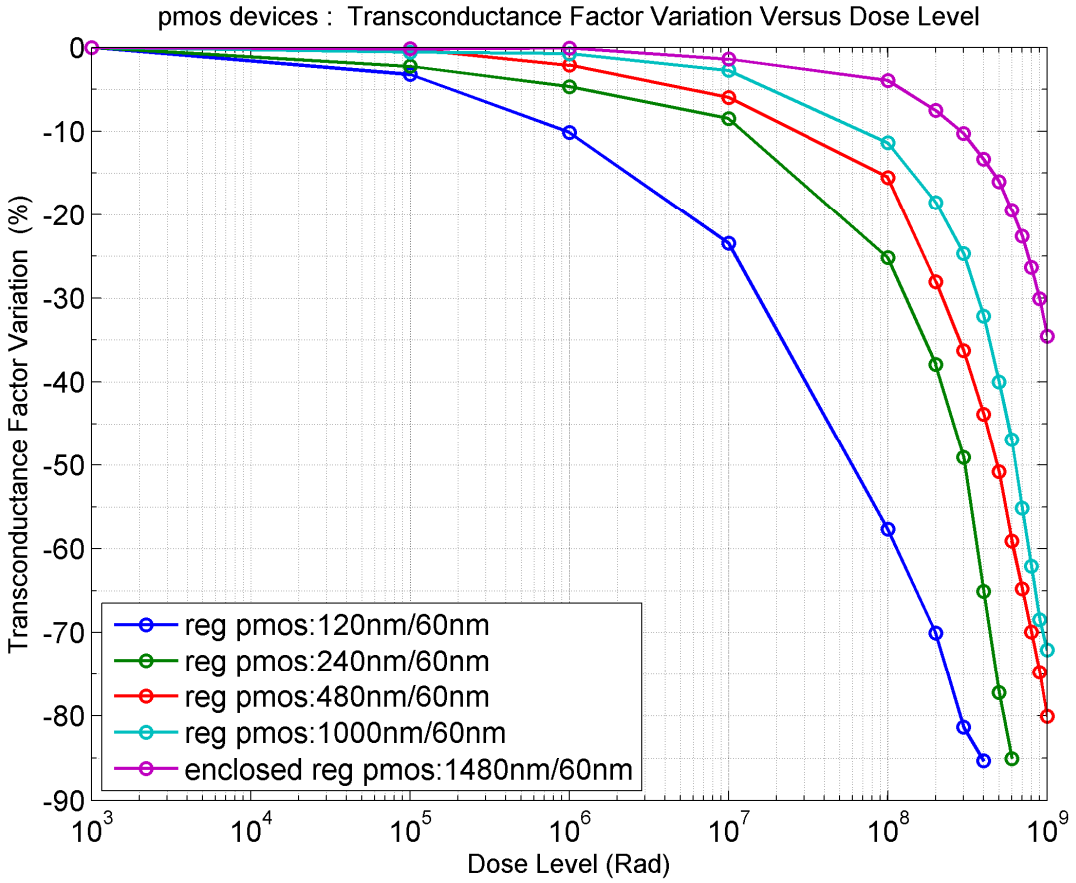
pmos threshold shift

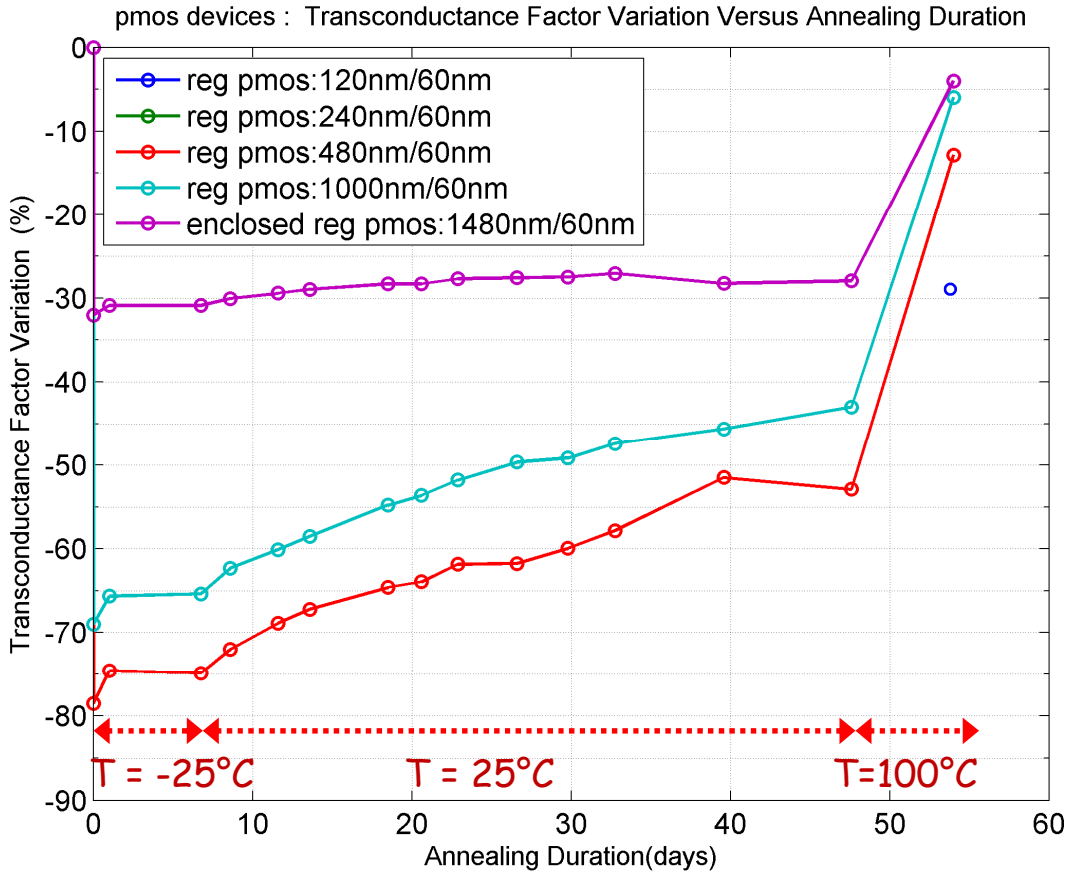




- Vth increases from a dose levels of 200 Mrad
- The device becomes 'OFF' essentially because of the decrease of the mobility (GM)
- With annealing GM recovers well but Vth still increasing (reverse annealing)
- The Vth shift is ~ 0.45 V for the narrower device

pmos transconductance variation





- For high level of dose (1000 Mrad), KPP decrease reaches 100% for 120 nm and 240nm devices
- With annealing, devices recover the most part of GM loss
- Wider devices recovers practically the pre-irradiation GM value
- For the narrowest device, KPN variation is only 32% compared to the pre-irradiation value