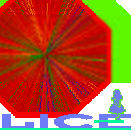


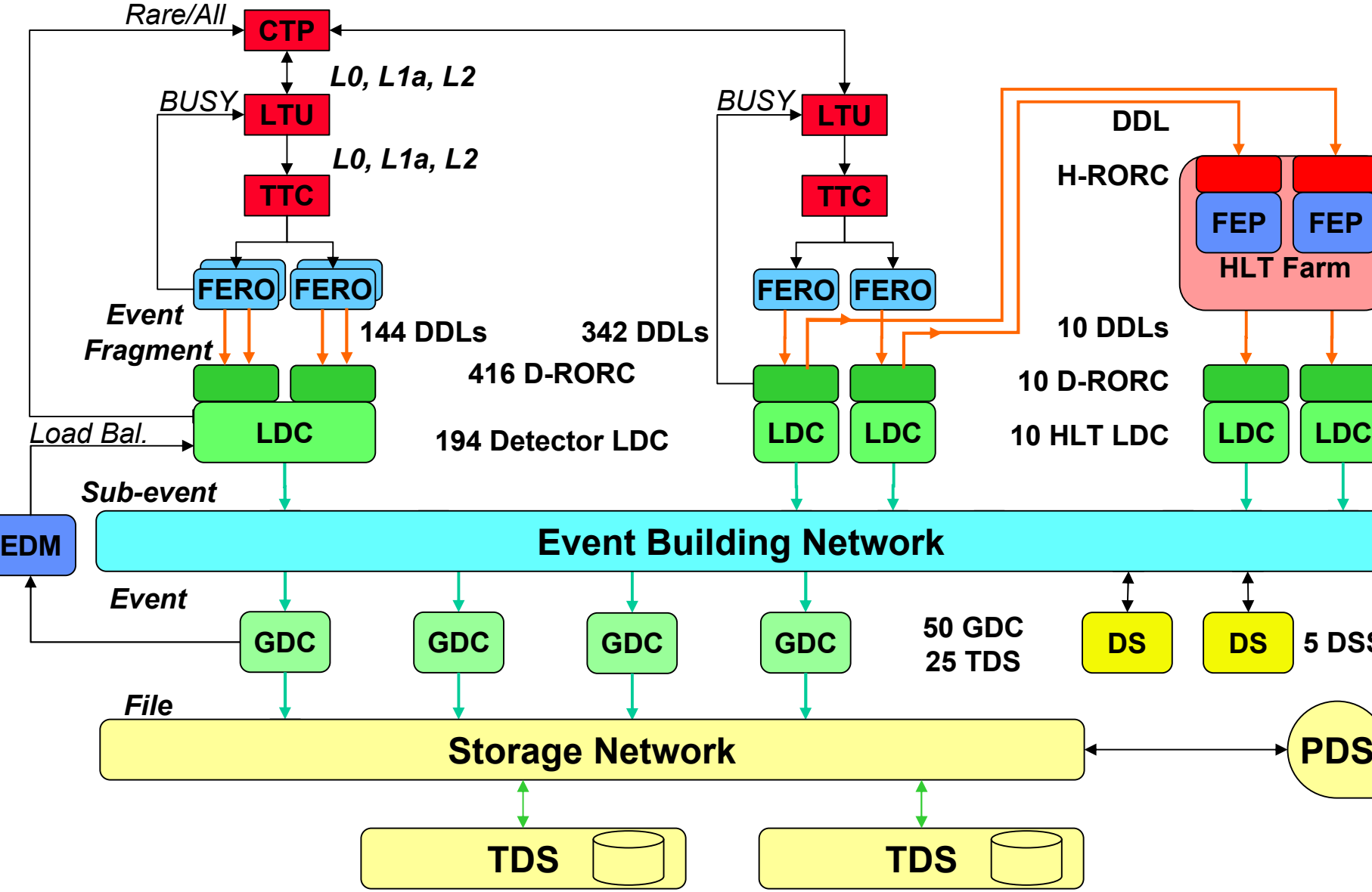
ALICE DAQ

Plans for 2006
Procurement, Installation, Commissioning

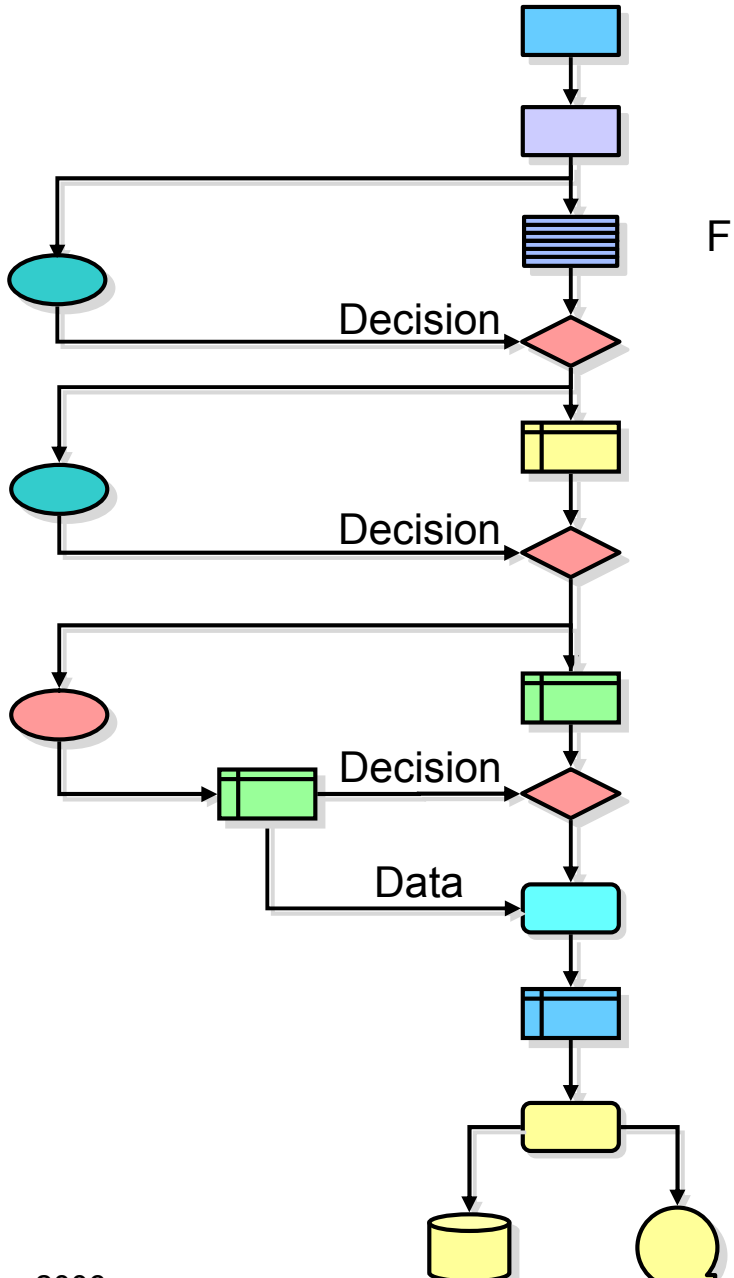
P. VANDE VYVRE – CERN/PH for

LHC DAQ Club - CERN - May 2006

DAQ architecture



ALICE online logical model



Detector

Digitizers

Front-end Pipeline/Buffer

Decision

Readout Buffer

Decision

Data transfer

Subevent Buffer

Decision

Event Building

Event Buffer

Storage

ALICE Terminology

Detector Data Link (DDL)

DAQ Read-Out Receiver Card (D-RORC)

Local Data Concentrator (LDC)

Global Data Collector (GDC)

Transient Data Storage (TDS)

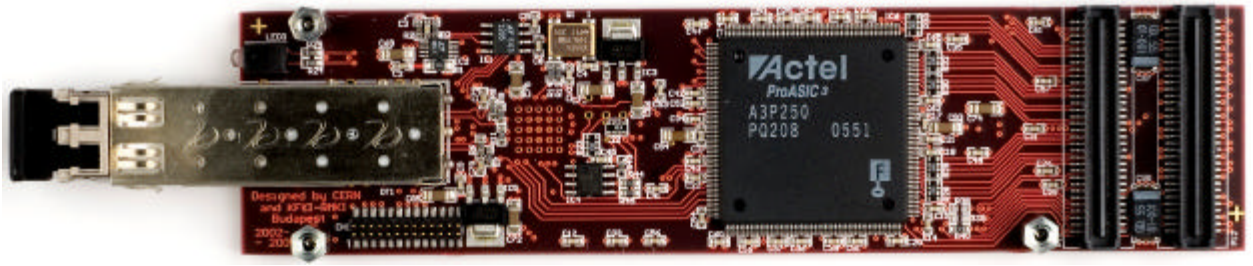
Permanent Data Storage (PDS)

DAQ Deployment

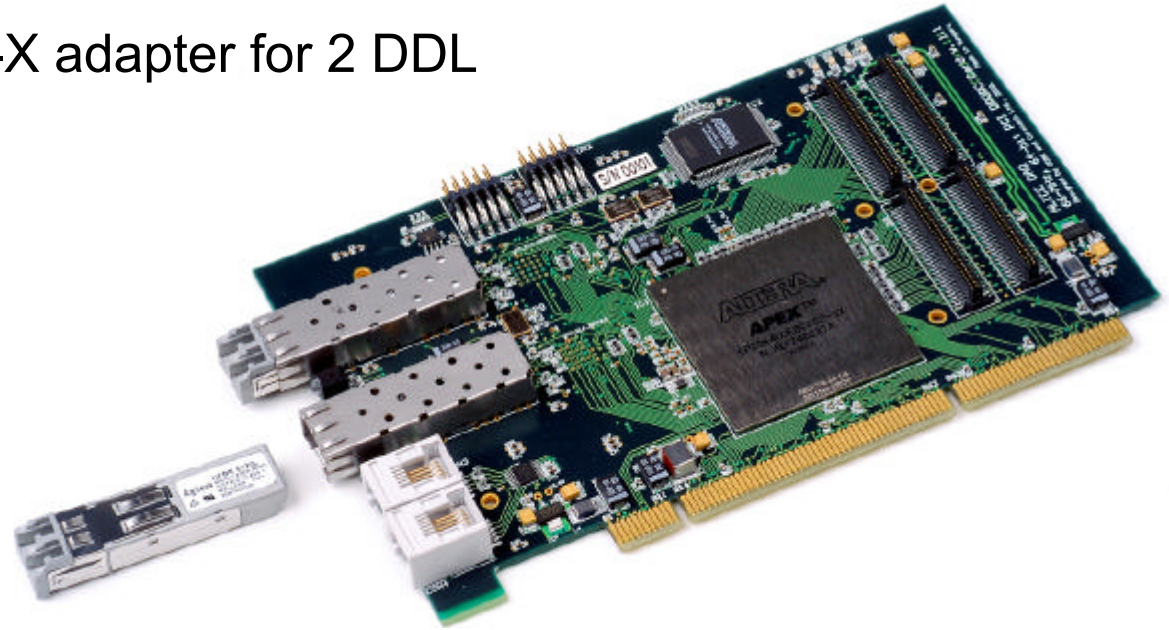
- Staged deployment of DAQ:
  - Full detector readout from the start (enough PCI slots for all DDLs)
  - 20/40/100 % of event building and storage bandwidth
- Jan 2006: DAQ Stage 0
  - DAQ for detector test and commissioning at CERN
  - Covers needs till June 06
- Jun 2006: DAQ Stage 1 (20%)
  - Equipment of present generation of hw (Supermicro X6, FC 2G) already qualified after extensive and competitive testing
  - Tender delayed till 20 February to include latest developments from industry
    - LDCs: dual-core Xeon CPUs, FB DIMM memory, I/O acceleration
    - Servers: dual-core AMD CPUs
    - Storage Fibre Channel 4 Gb (FC 4G)

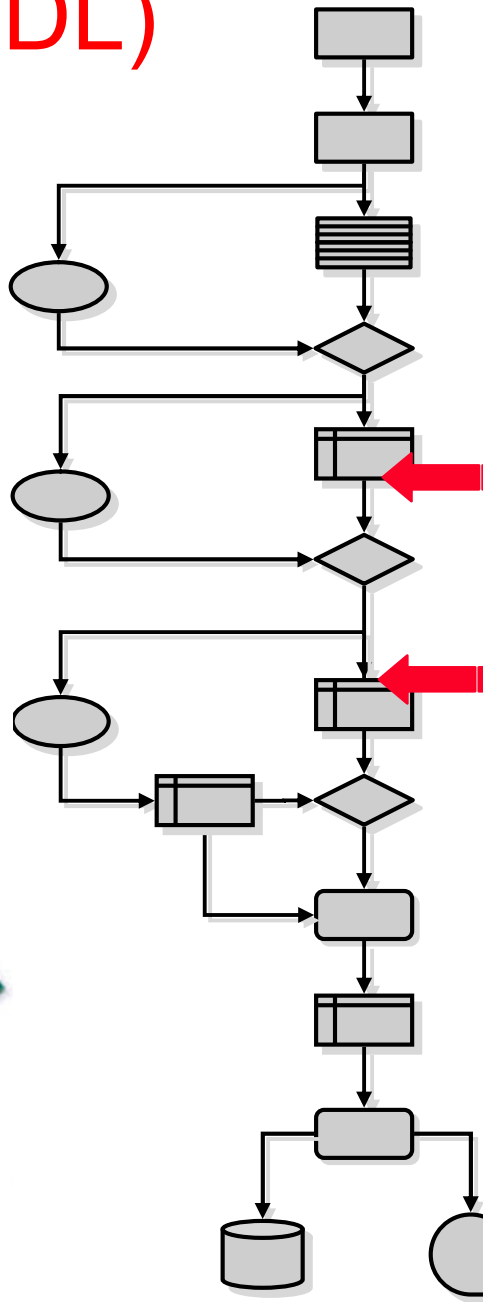
Detector Data Link (DDL)

- Two functions:
  - Detector readout: fast data transfer to PC memory
  - Electronics configuration: pedestals download



- PCI-X adapter for 2 DDL

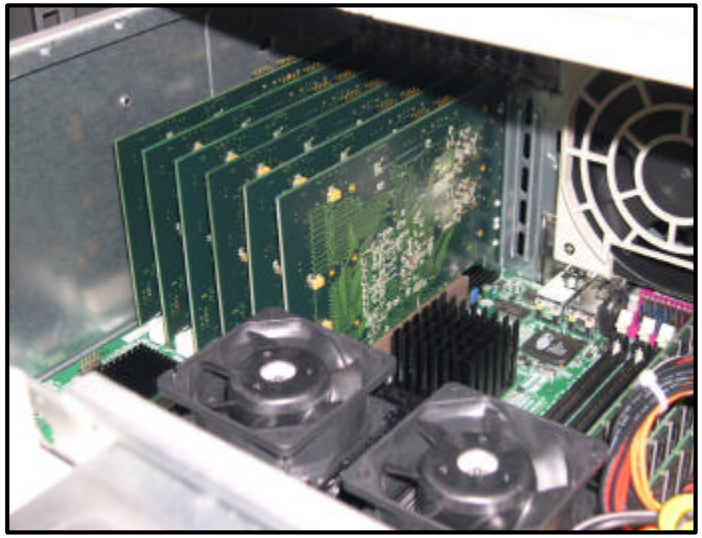




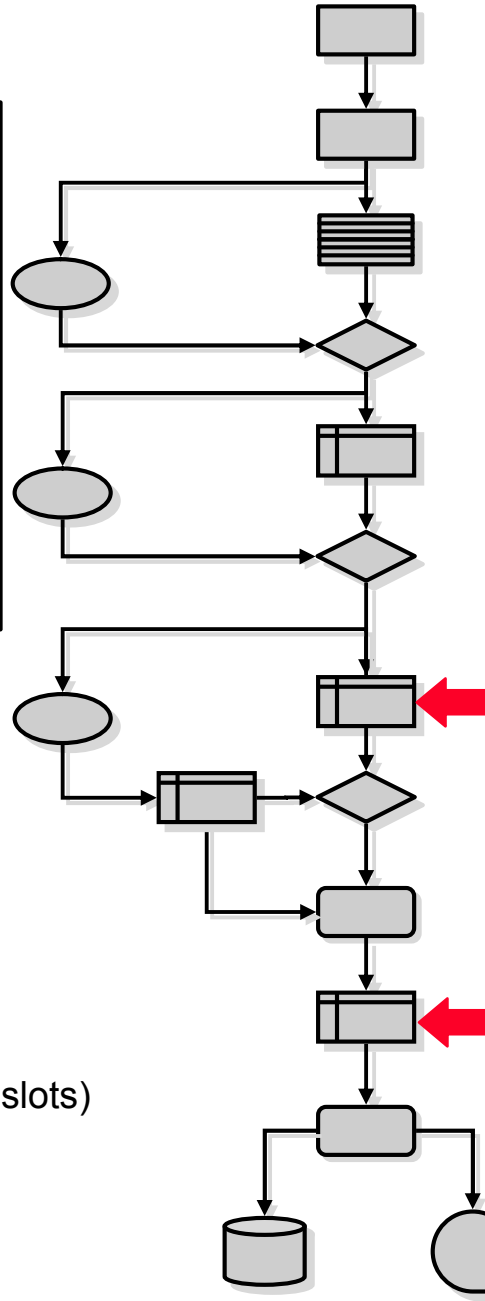
DDL SIU and D-RORC production

- Jan ’06: tender launched for production of
  - 550 DDL SIU cards
  - 460 D-RORC cards
- Mar ’06 – Jun ‘06: delivery of DDL SIUs in batches
  - So far 108 DDL SIUs cards produced, burnt in and tested by manufacture
  - Used to equip 1 side of TPC
  - Delay of delivery of ACTEL ProASIC 3
- May ’06 – July ’06: delivery of D-RORCs in batches

PCs



- LDC
  - 110 x 4U PCs
  - Dual Xeons
  - Up to 6 PCI-X slots
- GDC
  - 30 x 1U PCs
  - Dual Xeons
  - 1 PCI-X slot with Q-LOGIC FC-4G adapter
- DS
  - 5 x 1U PCs
  - Dual AMD Opteron 27x
- IT 3294/PH/ALICE (adjudication on 20 April ’06)
  - LDC:
    - Supermicro X6DHE-XB now (50 ordered)
      (CPU Nocona/Irwindale, Chipset Lindenhurst, DDR2 400, 6 PCI-X slots)
    - Supermicro X7DBE-XB not yet available
      (CPU Dempsey, Chipset Blackford, DDR2 FBD, 6 PCI-X slots)
    - Supermicro X7DB8-E under test
      (CPU Dempsey, Chipset Blackford, DDR2 FBD, 3 PCI-X slots)

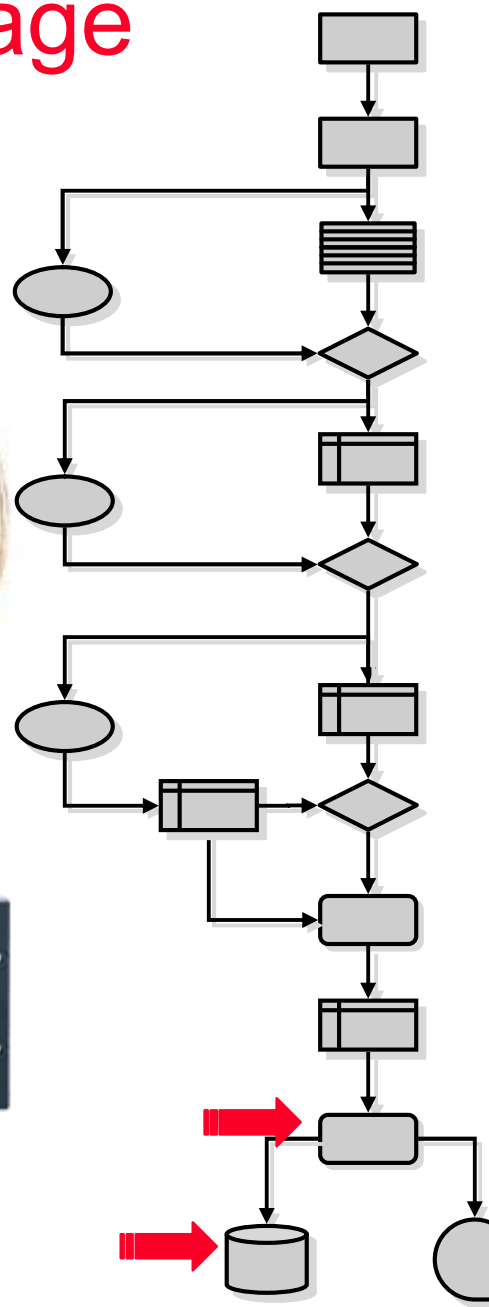


Transient Data Storage

- Local disk buffer at P2 (Fibre Channel 4G)
- Storage network:
  - 3 x QLogic SANbox 5602
    16 ports FC4G
    4 uplinks ports FC10G

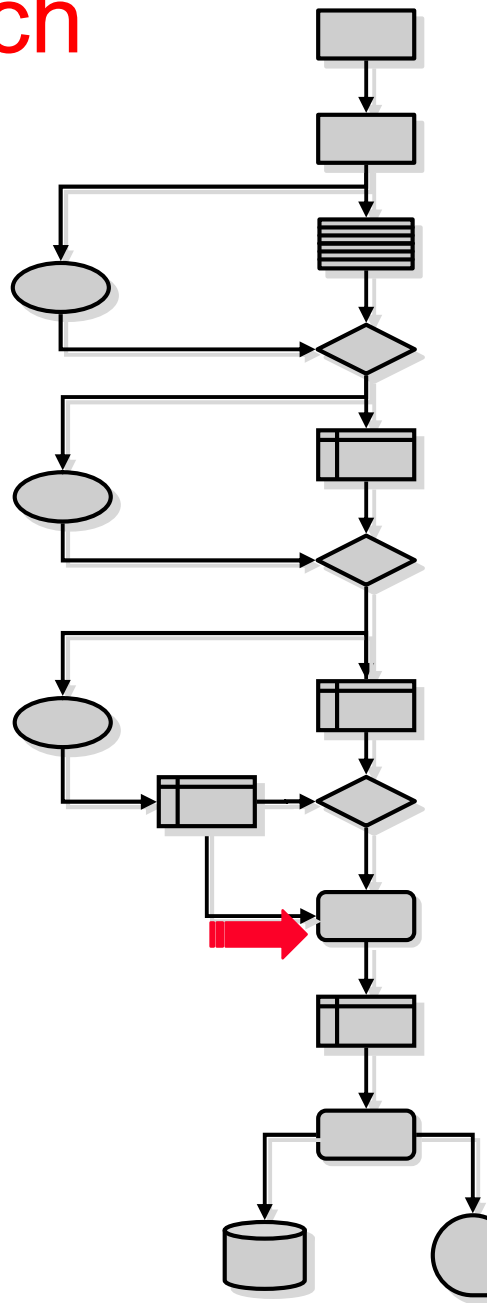
- Transient Data Storage
  - 18 x Infortrend INF-A16F-G2422
    2 ports FC 4G
    16 SATA II HD

- DO 23295/PH/ALICE (adjudication on 20 April '06)



Event Building Switch

- ALICE baseline:
  - TCP/IP over switched Ethernet
- Event-Building Switch
  - CERN frame contracts
  - Needs of IT and experiments
  - Good prices
  - On site maintenance (company+IT)
- Switch qualification test
  - Special set-up (IT): 60 PCs
  - DATE software used for benchmarking
- Force 10 Model 1200 delivered and installed



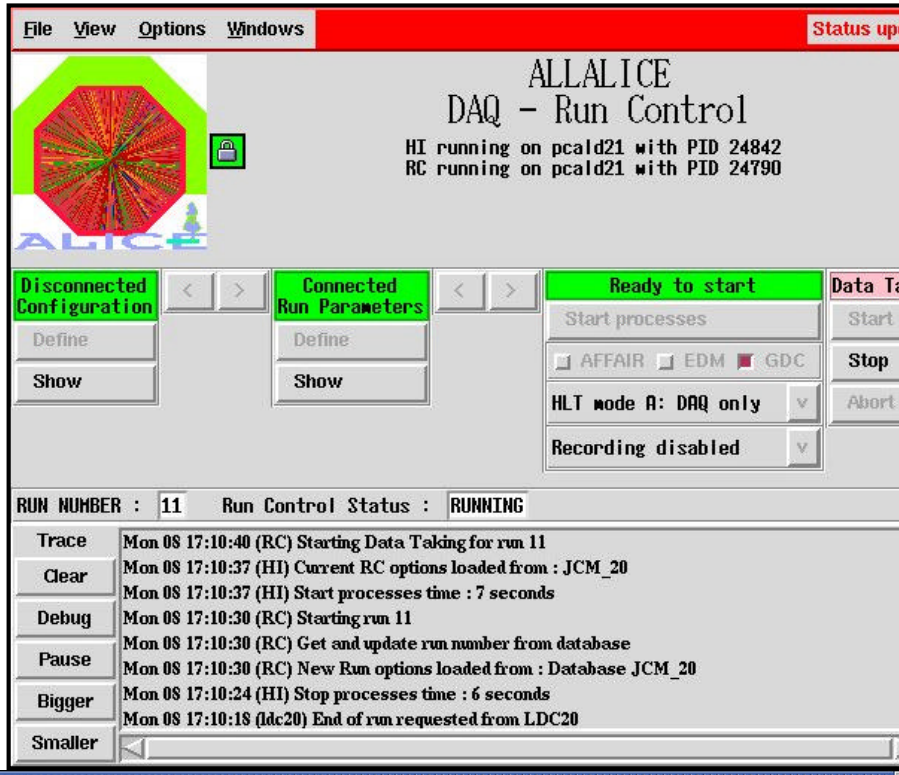
DAQ and ECS Software

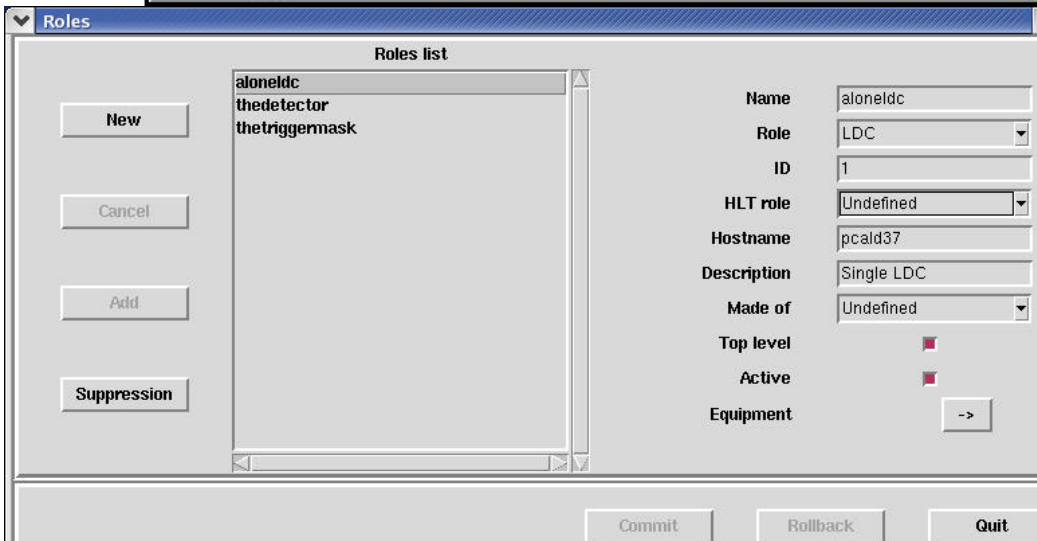
- DAQ software ready for startup
  - DDL software
  - DAQ framework (Control, configuration, dataflow) (DATE V5)
  - Performance Monitoring (AFFAIR)
  - Data quality monitoring (MOOD)
- Information dissemination
  - Documentation: 4 DAQ sw packages + ECS: fully documented.
    User's guide released and printed
  - Regular DAQ trainings (70 people in last 3 years)
- Linux
  - Linux SLC3 now.
  - ALICE DAQ contributing to Linux SLC4 certification.
    Transition to SLC4 scheduled before end '06.
- Process defined to produce, distribute, install new versions
  - Code management system: CVS. Release packaging and distribution: RPM (~20 MB)
  - Automatic installation of Linux and DATE on DAQ nodes

DATE V5

- Control
- Configuration
- Dataflow

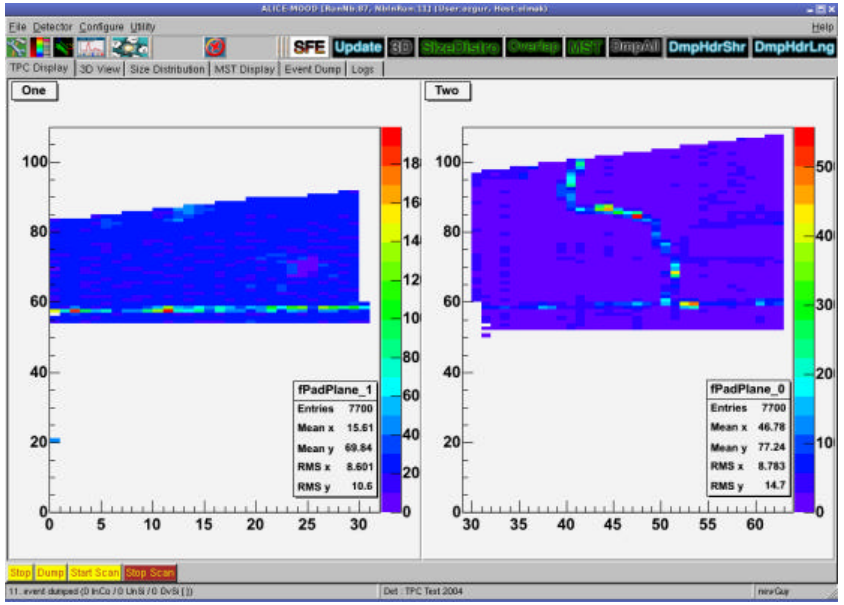
- Using
  - DIM, SMI++
  - Tcl/Tk
  - MySQL

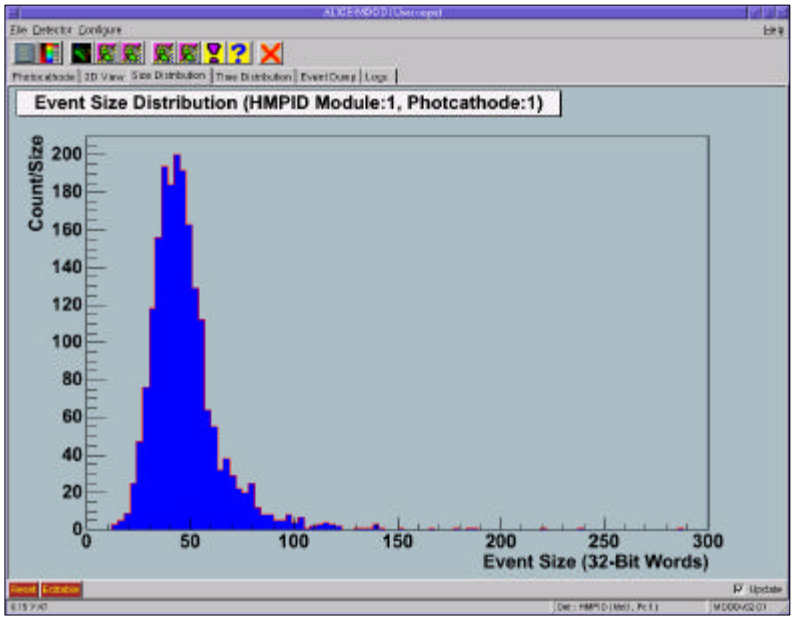


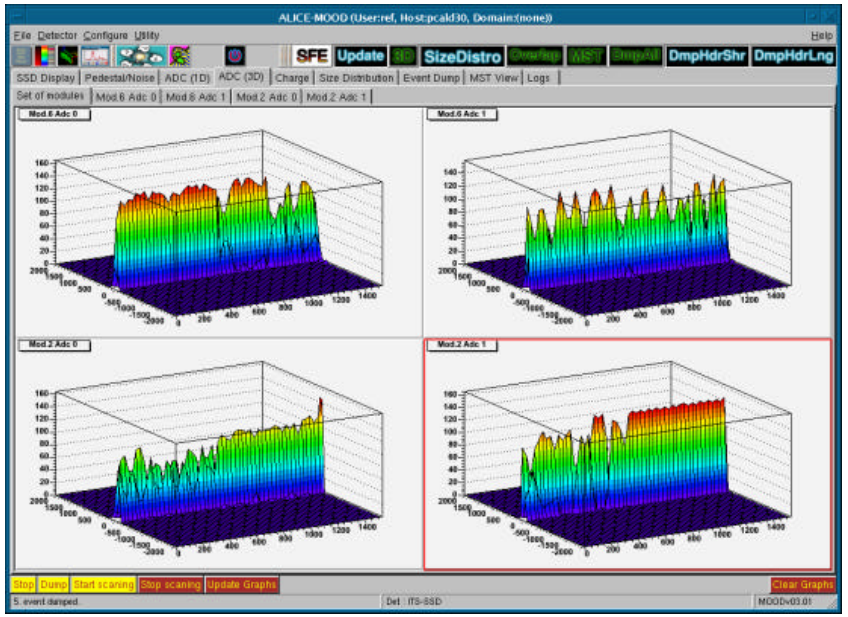


Data quality monitoring: MOOD

- Monitoring Of Online Data
  - Raw data integrity
  - Detector performance
- Using
  - DATE
  - ROOT

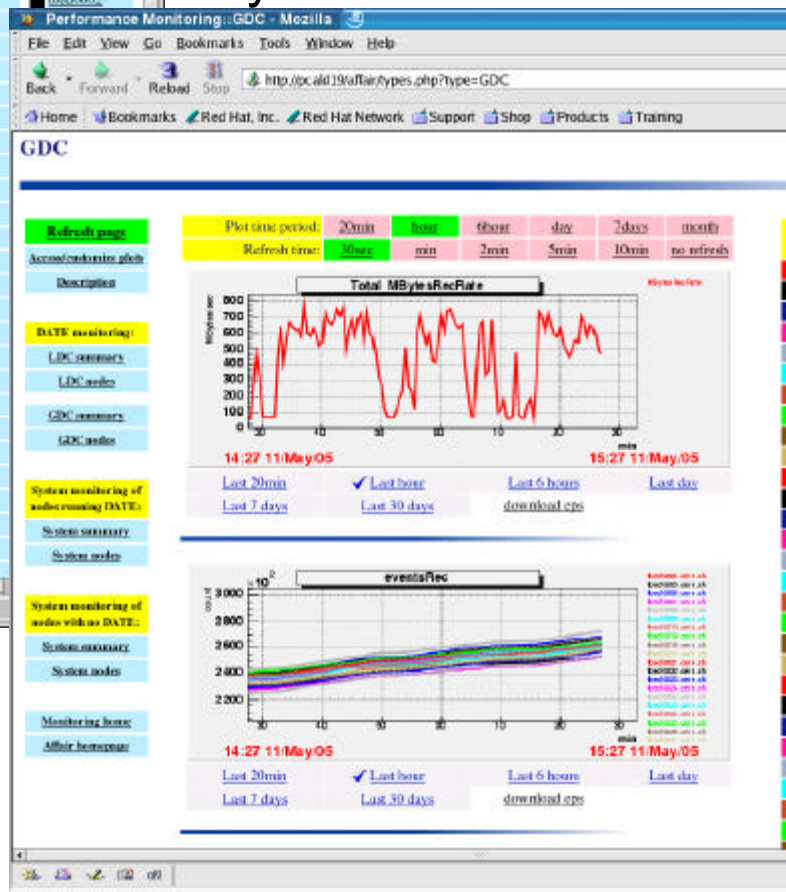






DAQ performance monitoring: AFFAIR

- DAQ performance monitoring
- Node view
- System view



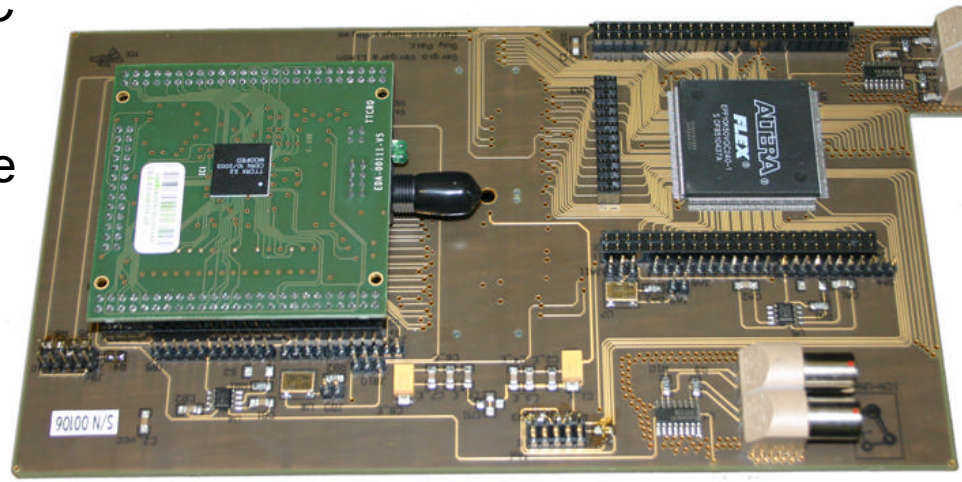
- Using
  - Apache
  - DATE, ROOT
  - DIM, SMI++

ECS

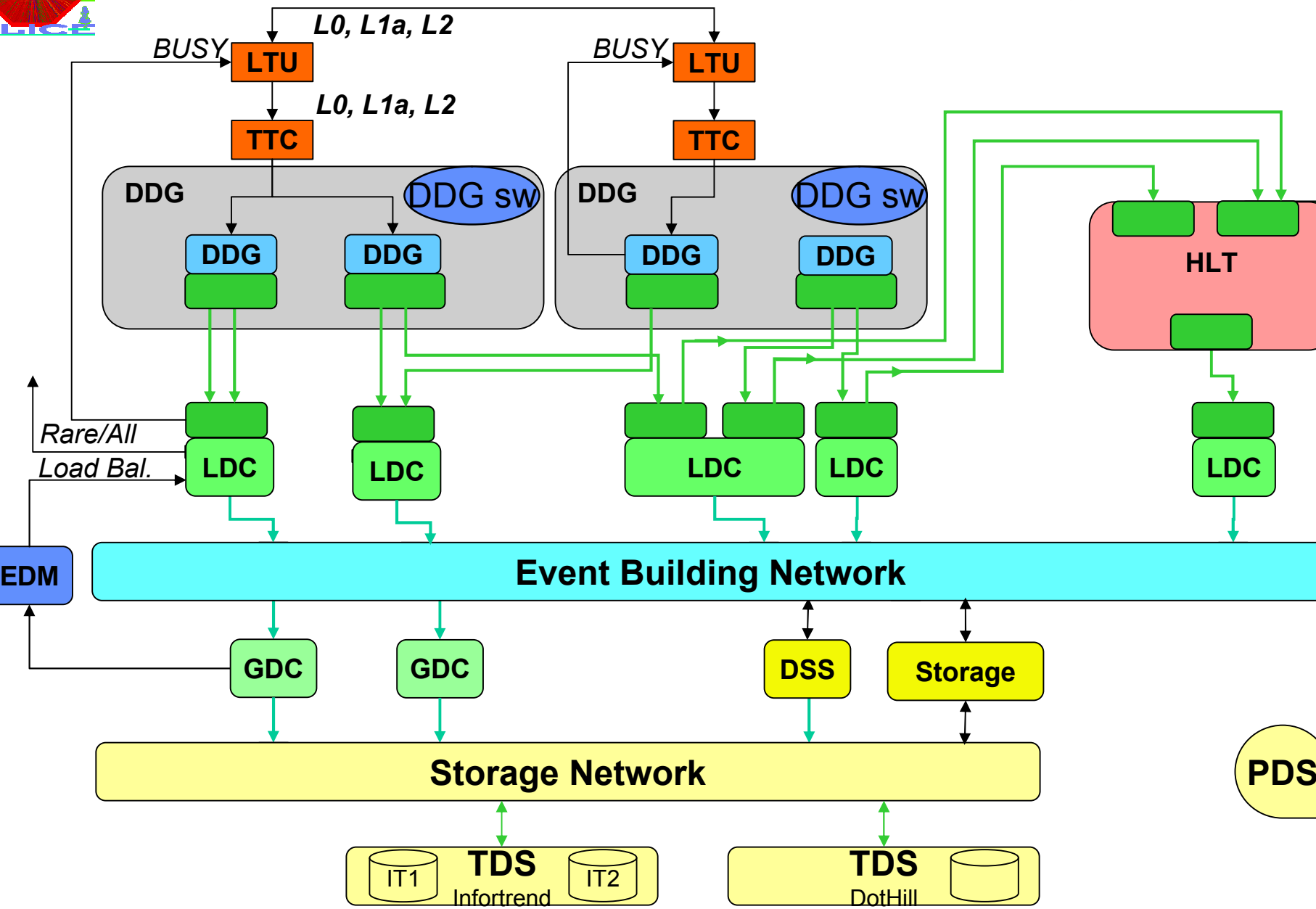
- Overall ALICE Control
  - TRG
  - DAQ
  - HLT
  - DCS
- Using
  - DIM, SMI++
  - Tcl/Tk
  - MySQL

DAQ Commissioning

- DAQ commissioning:
  - 1 system DAQ commissioning: “reference system” in DAQ lab
  - Test all functionalities
  - Running last released versions of DDL firmware, DAQ and ECS software
- Detector emulator
  - DDL Data Generator (DDG)
  - DDL data source triggered by TTC
  - Generation of busy
  - Uses the D-RORC as DMA engine to read data from PC memory
  - Send them over DDL



DAQ Reference System: hw data generator



DAQ systems for detector test & commissioning

- Detector tests with DAQ
  - Data transfer: 25 DDLs for tests (1 chain per detector delivered since 2002)
  - DATE sw
- Detector commissioning with DAQ
  - Hardware DAQ dedicated to detector tests:
    Distributed in different locations according to needs
  - Data transfer
    - CERN: 20 DDL SIUs, 16 D-RORCs, 8 DIUs
  - DAQ fabric
    - 12 LDCs (6 PCI slots)
    - 4 GDCs, 3 servers
    - 2 storage units 2 TB

DAQ systems for detector test & commissioning

- SPD — First sector with DAQ, TRG, ECS in DSF (CERN Bld 186)
- SSD — DAQ system (Utrecht)
- SDD — DAQ system (Torino)
- TPC — Electronics setup (Bergen, CERN Bld 13). Detector (SXL2 CERN)
- TRD — DAQ ready for super-module being assembled (Heidelberg)
- TOF — DAQ ready for module being assembled (Bologna, CERN Bld 156)
- Muon TRK — DAQ system (Orsay). Feb ’06: test SXL2
- Muon TRG — DAQ system (Nantes)
- HMPID — DAQ system (CERN Bld 581)
- PHOS — DAQ for electronics test, then module assembly (Bergen, CERN Bld 167)
- FMD — DAQ installed for test in March (NBI, CERN Bld 1)
- T0 — DAQ in TOF labs (Bologna and CERN)
- V0 — Test of CCIU (Lyon)
- ACORDE — DAQ system for detector (SXL2 CERN)
- EMCal — DAQ system used during TB (Fermilab)

Detector/DAQ integration (Mar 06)

	SPD	SSD	SDD	TPC	TRD	TOF	MUON TRK	MUON TRG	HMPID	PHOS	FMD	T0	V0	ZDC	PMD	ACORDE	EMCAL
DATE system																	
DDL with data gen.																	
Detector readout with DDL & DATE																	
Data quality monitor. (MOOD)																	

Must be done in the lab before starting commissioning at Point 2

DAQ Installation (CR1)

Grand Total Power not UPS (W)	84750
Grand Total UPS Level 2 (VA) [Allocation:10 kW]	7000
Grand Total UPS Level 3 (VA) [Allocation:17 kW]	19500

Sep-05	Test and Commissioning
Jan-06	Final system
	Services

Racks	Max Locat.	Racks in place	Racks Used	Spare Racks
Usage	35	35	32	3

		X		SPD	TRG - ZDC - ACORDE - SDD	SSD-FWD	TRD	TOF	TOF	HMPID - PMD	PHOS - CPV	MUON TRK - MUON TRG	HLT	Power Distrib. Control (TS-EL)	Hazen Mayer	X
				11	10	9	8	7	6	5	4	3	2	1	0	
			SPARE Rack	EMCal	TPC	TPC	TPC	TPC	TPC	TPC	TPC	TPC	TPC	TPC	TPC	TPC
	KVM User Station	Y	14	13	12	11	10	9	8	7	6	5	4	3	2	1
Operator Room (OR)			SPARE Rack	SPARE Rack			GDC	GDC	GDC	EB SW & KVM	GDC	GDC	DS	Test & Comm.		
	KVM User Station	Z	10	9			8	7	6	5	4	3	2	1		Z
							UPS Lv2-3	UPS Lv2-3	UPS Lv2-3	UPS Lv2-3	UPS Lv2-3	UPS Lv2-3	UPS Lv2-3			

Access door

Services

- Ready
  - 35 racks 56 U
  - Normal Power
  - Air conditioning
  - Cooling doors for 35 racks
  - Connections to chilled water
  - Chilled water circuits
  - Network
  - Access control
  - Optical fibres SXL-CR1
- In progress
  - Optical fibres between CR1 and other CRs and UX
- Quality and schedule critical

Some of the next steps

- Apr ’06 DAQ standalone commissioned in lab
- May ’06 ECS + DAQ + HLT at Point 2
- Jun ’06 ECS + TRG + DAQ test and commissioning in lab
  Installation DAQ Stage 1
- Jun’06 – Sep’06
  Data Challenge from Point 2 to IT

- May ’06 TPC commissioning on surface with cosmics
- Jul ’06 PHOS, TOF, TRD, HMPID, ACORDE
- Sep ’06 TPC
- Jan ’07 ITS
- Feb ’07 TOF, TRD
- Apr ’07 FMD, V0, T0, PMD

Conclusion

- Production of DDL and D-RORC in progress
  - Mar-Jul ’06. Enough DDL SIUs to equip 1 side of TPC
- DAQ fabric hardware
  - All hw elements qualified. Tenders include most recent equipment.
  - Procurement and delivery in progress.
- DAQ software ready
  - Software (DDL sw, DATE, AFFAIR, MOOD) released and documented.
  - Linux SLC3 now. Transition to SLC4 scheduled before end ’06.
- DAQ system deployment
  - Stage 0: small DAQ system for detector test and commissioning
  - Stage 1: deployed in June (full readout, 20% performance)
- Installation
  - Services for DAQ finished. Optical fibres progressing with detector installation.
- Commissioning of detectors in parallel