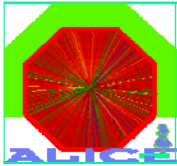


ALICE DAQ

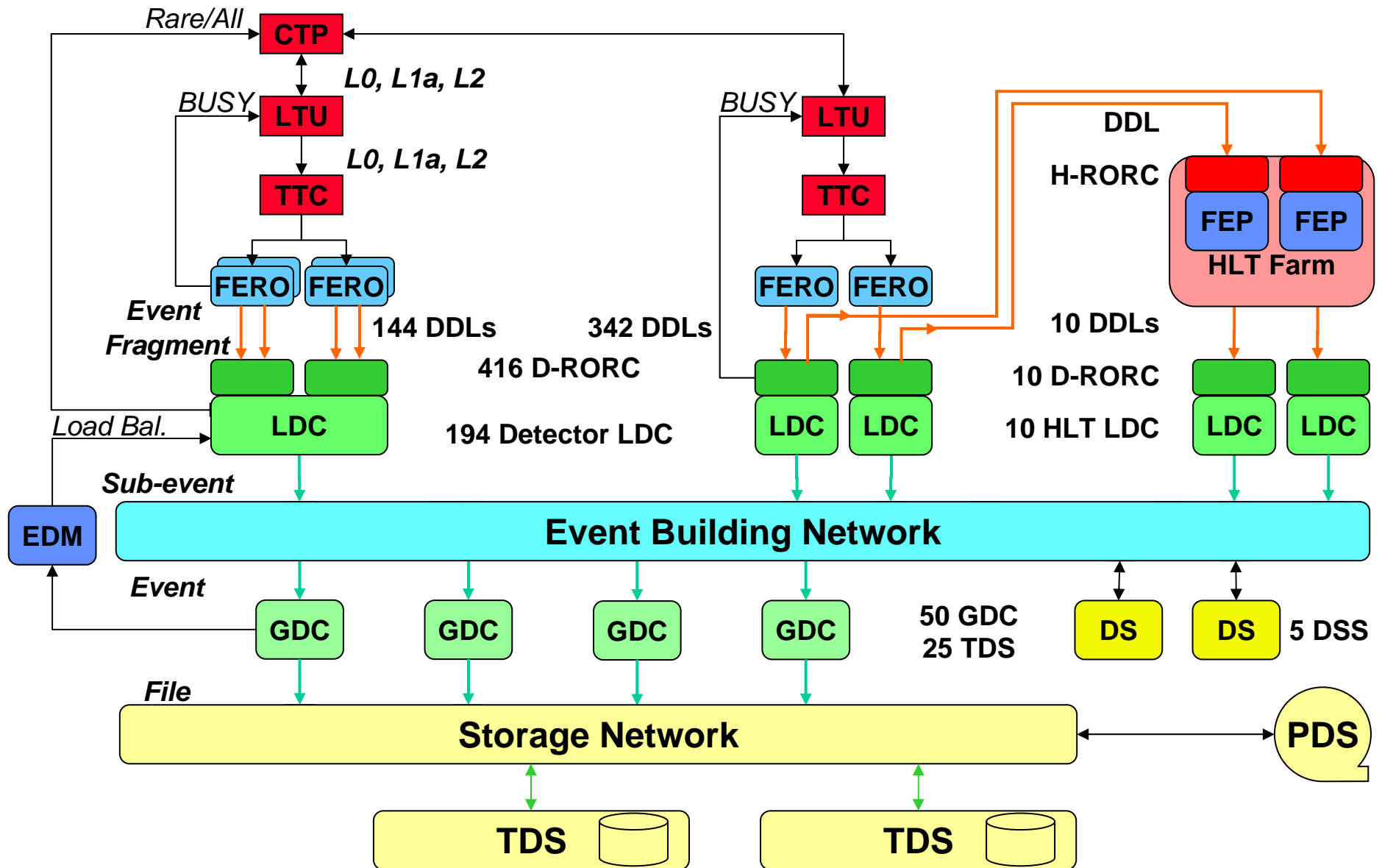
Plans for 2006
Procurement, Installation, Commissioning

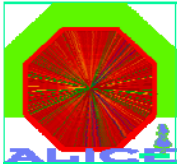
P. VANDE VYVRE – CERN/PH for

LHC DAQ Club - CERN - May 2006

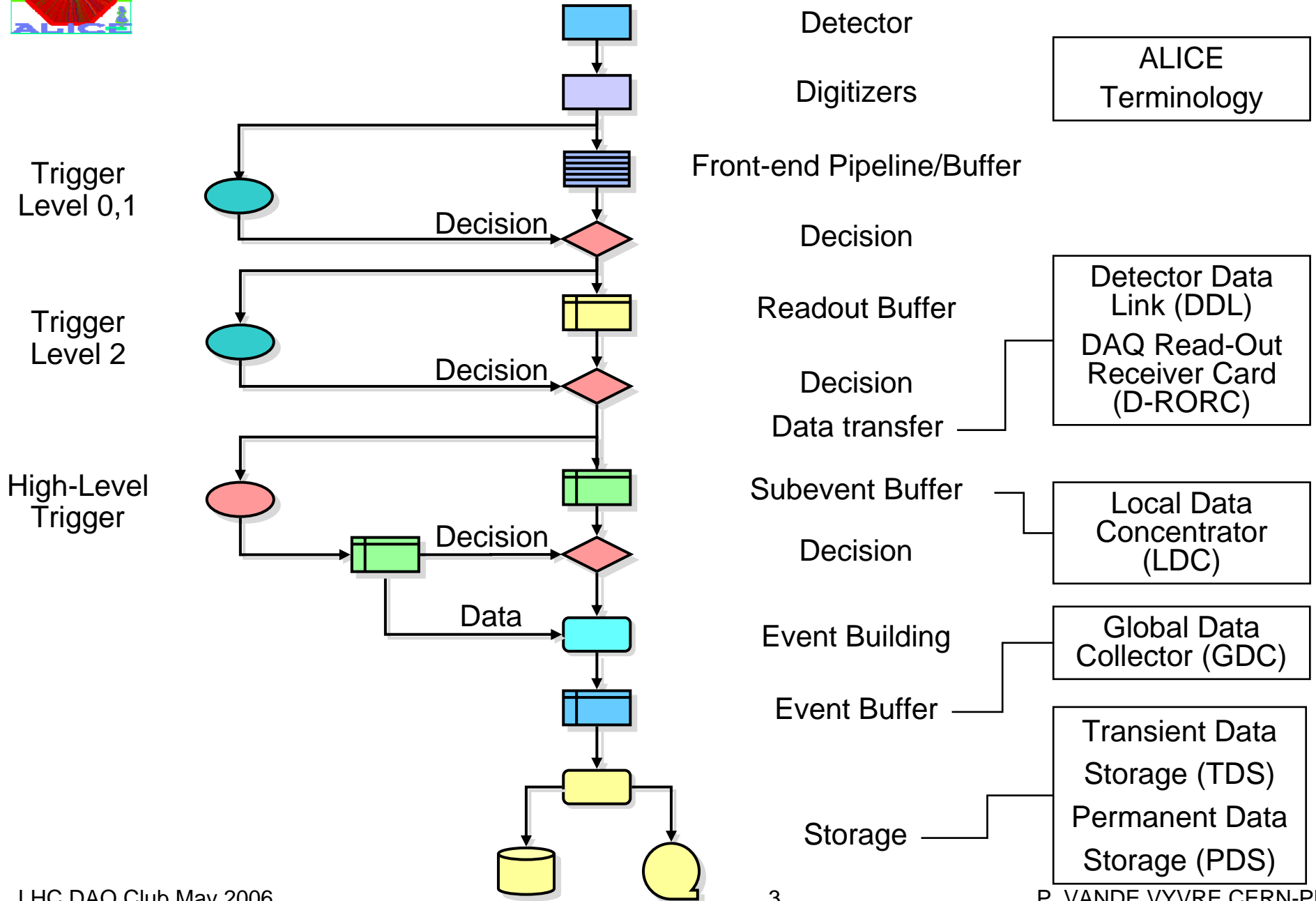


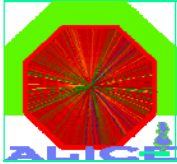
DAQ architecture





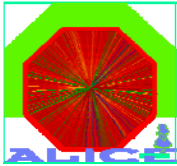
ALICE online logical model





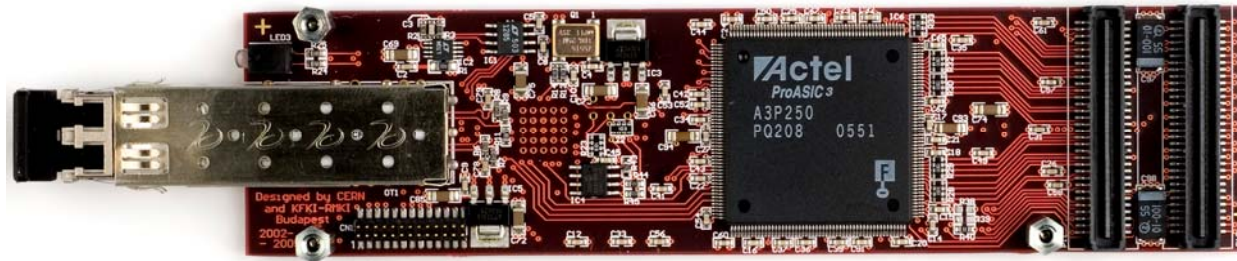
DAQ Deployment

- Staged deployment of DAQ:
 - Full detector readout from the start (enough PCI slots for all DDLs)
 - 20/40/100 % of event building and storage bandwidth
- Jan 2006: DAQ Stage 0
 - DAQ for detector test and commissioning at CERN
 - Covers needs till June 06
- Jun 2006: DAQ Stage 1 (20%)
 - Equipment of present generation of hw (Supermicro X6, FC 2G) already qualified after extensive and competitive testing
 - Tender delayed till 20 February to include latest developments from industry
 - LDCs: dual-core Xeon CPUs, FB DIMM memory, I/O acceleration
 - Servers: dual-core AMD CPUs
 - Storage Fibre Channel 4 Gb (FC 4G)

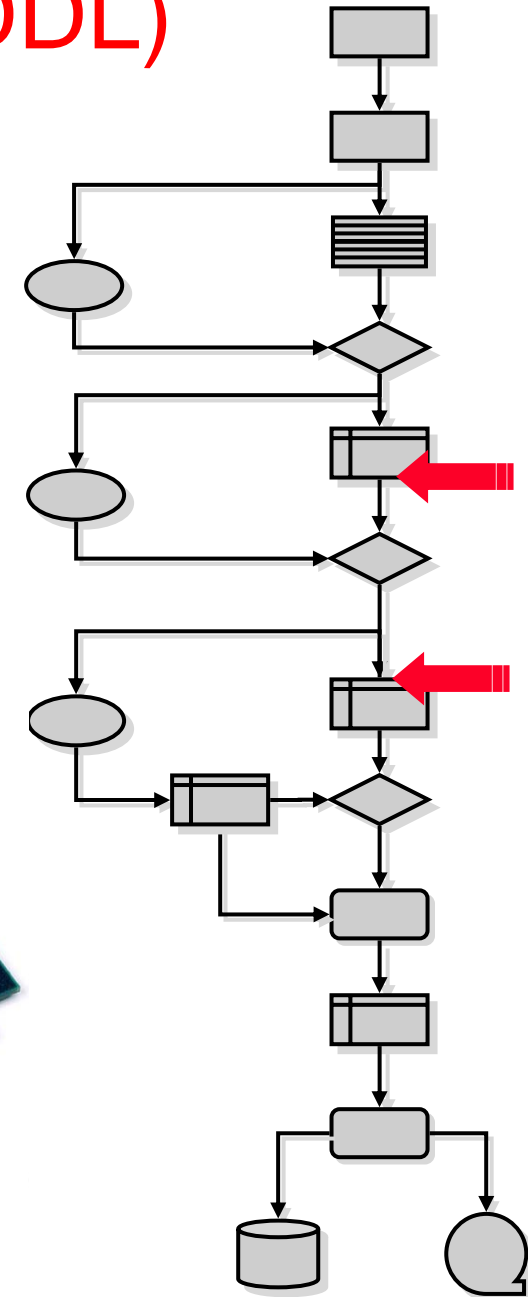
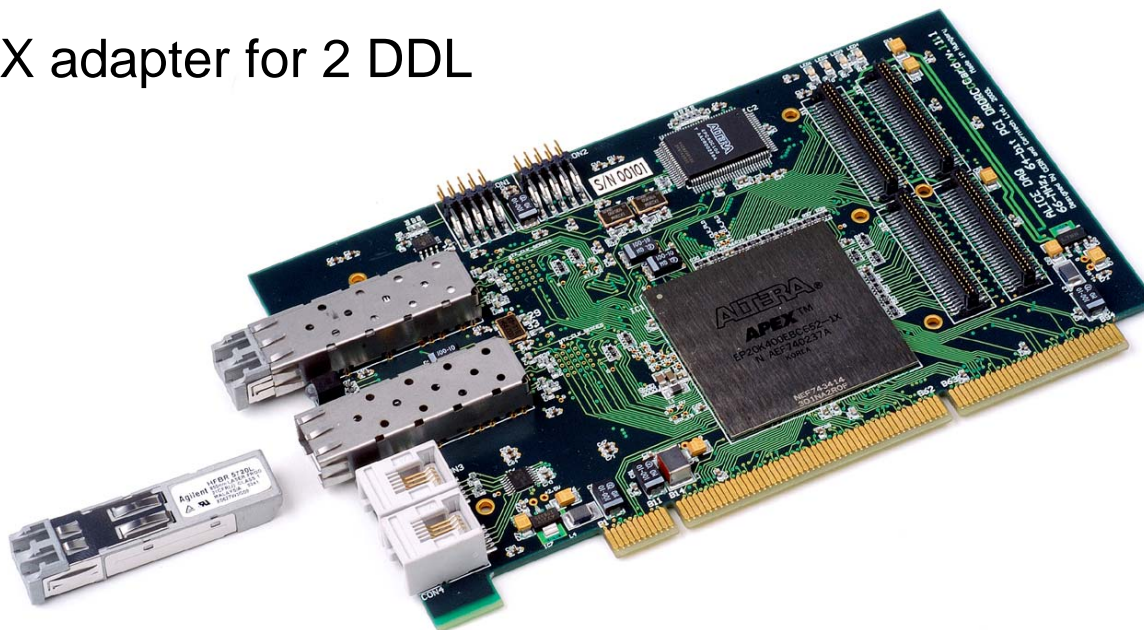


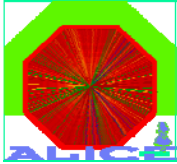
Detector Data Link (DDL)

- Two functions:
 - Detector readout: fast data transfer to PC memory
 - Electronics configuration: pedestals download



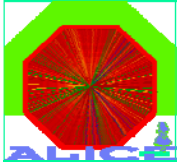
- PCI-X adapter for 2 DDL





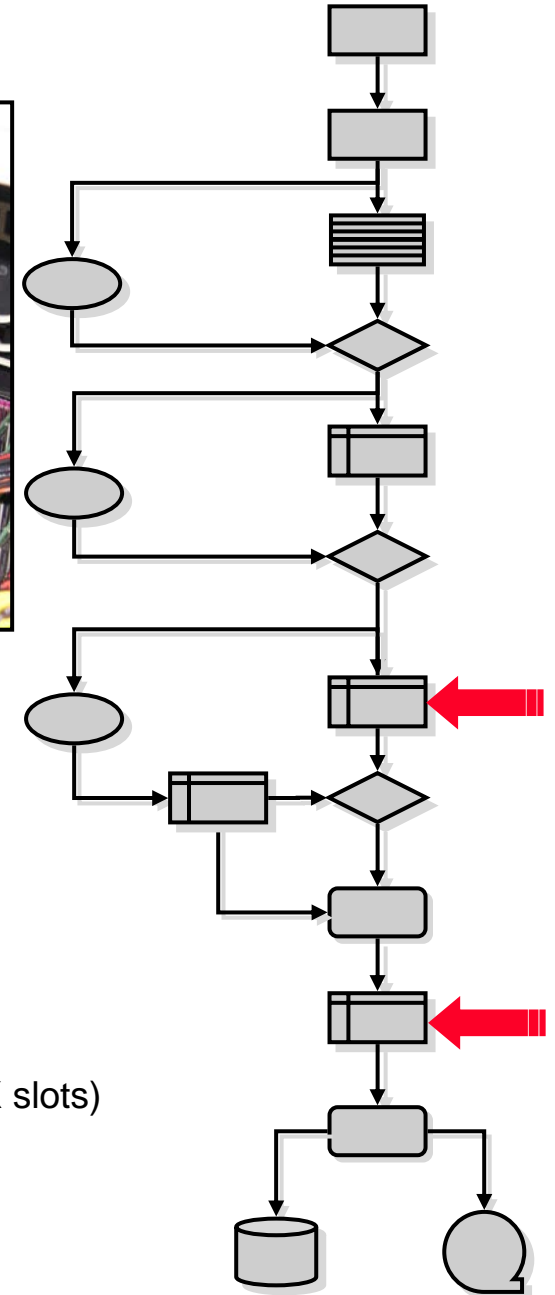
DDL SIU and D-RORC production

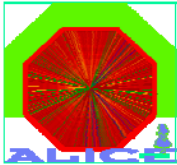
- Jan '06: tender launched for production of
 - 550 DDL SIU cards
 - 460 D-RORC cards
- Mar '06 – Jun '06: delivery of DDL SIUs in batches
 - So far 108 DDL SIUs cards produced, burnt in and tested by manufacturer
 - Used to equip 1 side of TPC
 - Delay of delivery of ACTEL ProASIC 3
- May '06 – July '06: delivery of D-RORCs in batches



PCs

- LDC
 - 110 x 4U PCs
 - Dual Xeons
 - Up to 6 PCI-X slots
- GDC
 - 30 x 1U PCs
 - Dual Xeons
 - 1 PCI-X slot with Q-LOGIC FC-4G adapter
- DS
 - 5 x 1U PCs
 - Dual AMD Opteron 27x
- IT 3294/PH/ALICE (adjudication on 20 April '06)
 - LDC:
 - Supermicro X6DHE-XB now (50 ordered)
(CPU Nocona/Irwindale, Chipset Lindenhurst, DDR2 400, 6 PCI-X slots)
 - Supermicro X7DBE-XB not yet available
(CPU Dempsey, Chipset Blackford, DDR2 FBD, 6 PCI-X slots)
 - Supermicro X7DB8-E under test
(CPU Dempsey, Chipset Blackford, DDR2 FBD, 3 PCI-X slots)





Transient Data Storage

- Local disk buffer at P2 (Fibre Channel 4G)

- Storage network:

- 3 x QLogic SANbox 5602
16 ports FC4G
4 uplinks ports FC10G

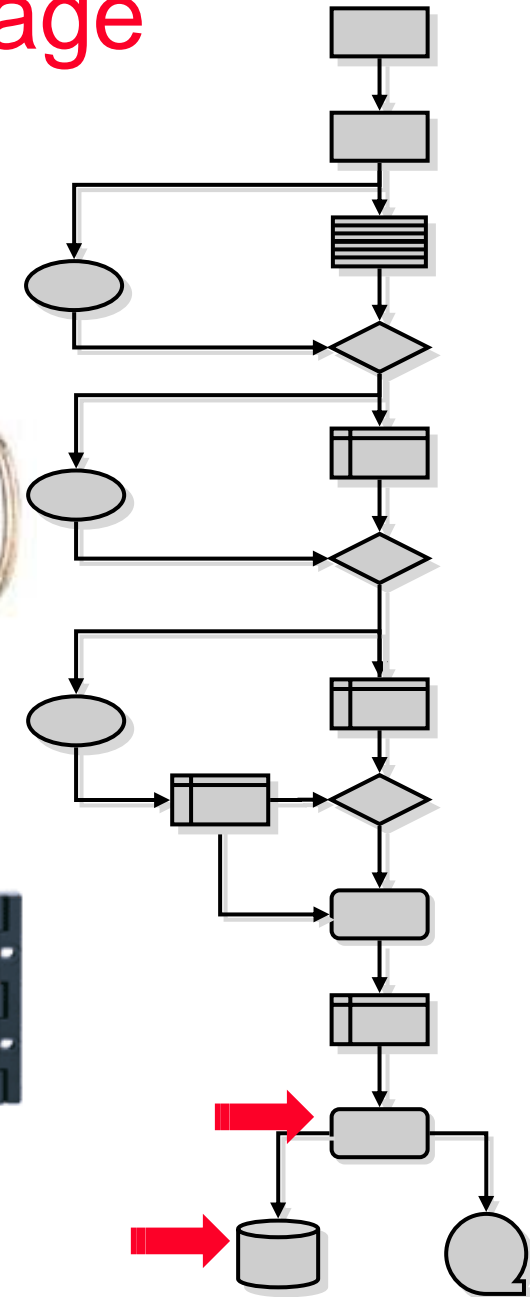


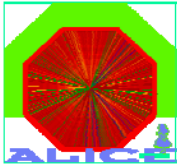
- Transient Data Storage

- 18 x Infortrend INF-A16F-G2422
2 ports FC 4G
16 SATA II HD



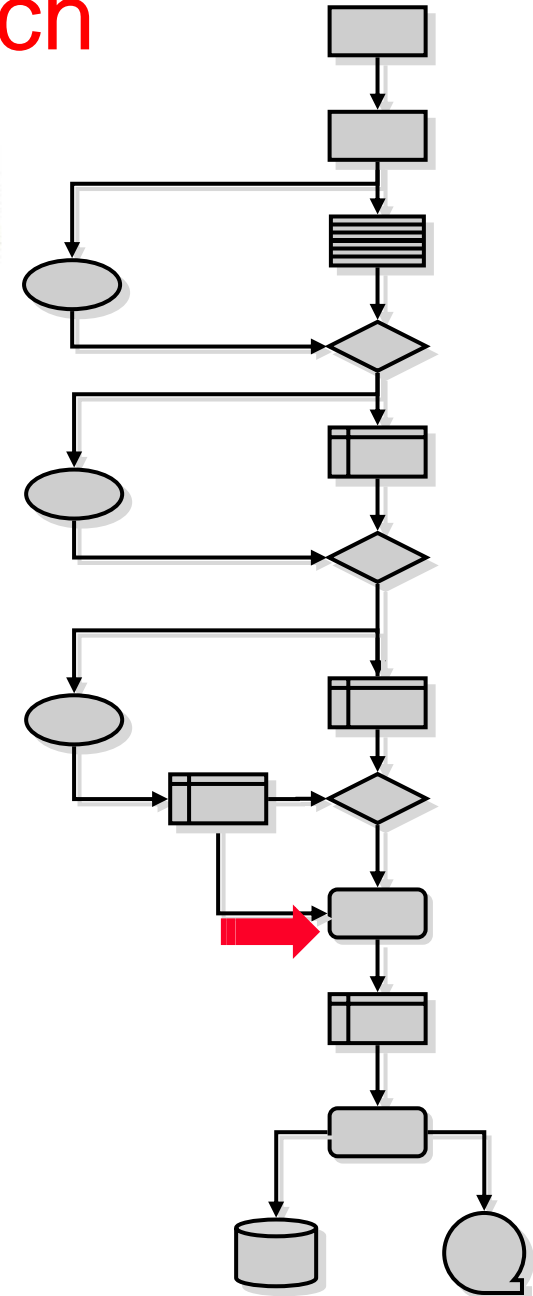
- DO 23295/PH/ALICE (adjudication on 20 April '06)

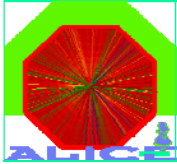




Event Building Switch

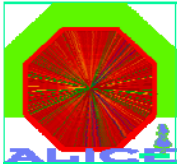
- ALICE baseline:
 - TCP/IP over switched Ethernet
- Event-Building Switch
 - CERN frame contracts
 - Needs of IT and experiments
 - Good prices
 - On site maintenance (company+IT)
- Switch qualification test
 - Special set-up (IT): 60 PCs
 - DATE software used for benchmarking
- Force 10 Model 1200 delivered and installed





DAQ and ECS Software

- DAQ software ready for startup
 - DDL software
 - DAQ framework (Control, configuration, dataflow) (DATE V5)
 - Performance Monitoring (AFFAIR)
 - Data quality monitoring (MOOD)
- Information dissemination
 - Documentation: 4 DAQ sw packages + ECS: fully documented. User's guide released and printed
 - Regular DAQ trainings (70 people in last 3 years)
- Linux
 - Linux SLC3 now.
 - ALICE DAQ contributing to Linux SLC4 certification. Transition to SLC4 scheduled before end '06.
- Process defined to produce, distribute, install new versions
 - Code management system: CVS. Release packaging and distribution: RPM (~20 MB)
 - Automatic installation of Linux and DATE on DAQ nodes



DATE V5

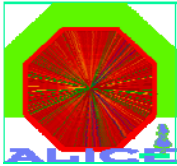
- Control
- Configuration
- Dataflow

- Using
 - DIM, SMI++
 - Tcl/Tk
 - MySQL

The screenshot shows the ALLALICE DAQ - Run Control interface. At the top, it displays 'ALLALICE DAQ - Run Control' and 'Status updated'. Below this, it indicates 'HI running on pcald21 with PID 24842' and 'RC running on pcald21 with PID 24790'. The interface is divided into several sections: 'Disconnected Configuration', 'Connected Run Parameters', and 'Ready to start'. The 'Ready to start' section includes buttons for 'Start processes', 'Start', 'Stop', and 'Abort', along with checkboxes for 'AFFAIR', 'EDM', and 'GDC'. A dropdown menu for 'HLT mode A: DAQ only' and a 'Recording disabled' dropdown are also present. The 'RUN NUMBER' is set to 11, and the 'Run Control Status' is 'RUNNING'. A log window at the bottom shows a series of events, including 'Starting Data Taking for run 11', 'Current RC options loaded from : JCM_20', 'Start processes time : 7 seconds', 'Starting run 11', 'Get and update run number from database', 'New Run options loaded from : Database JCM_20', 'Stop processes time : 6 seconds', and 'End of run requested from LDC20'.

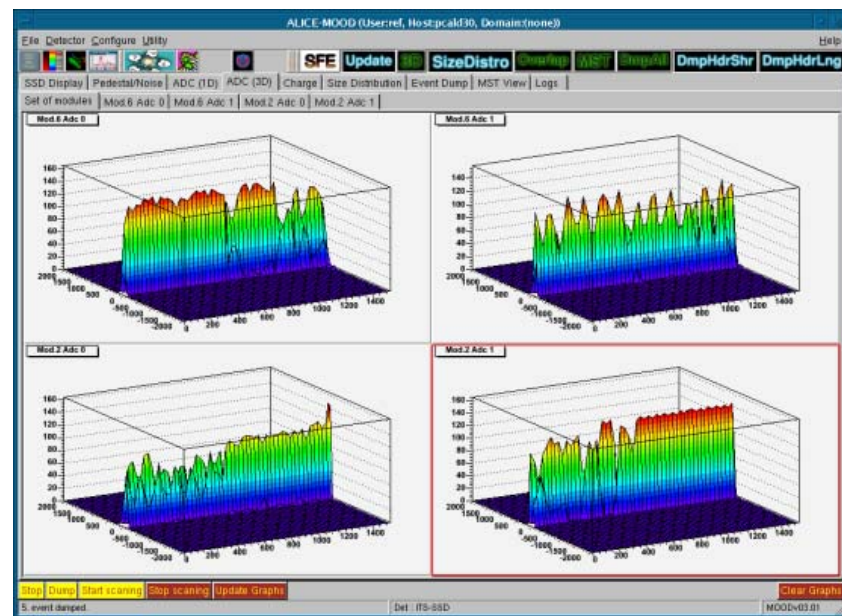
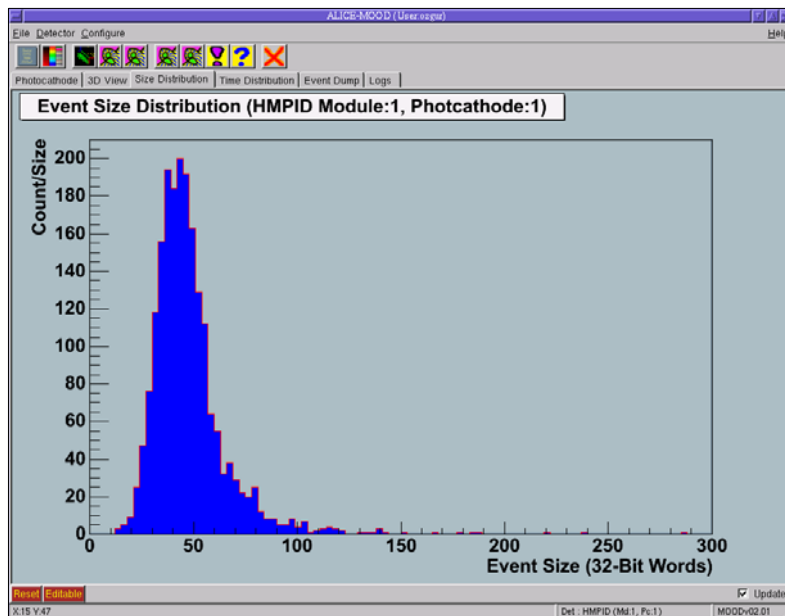
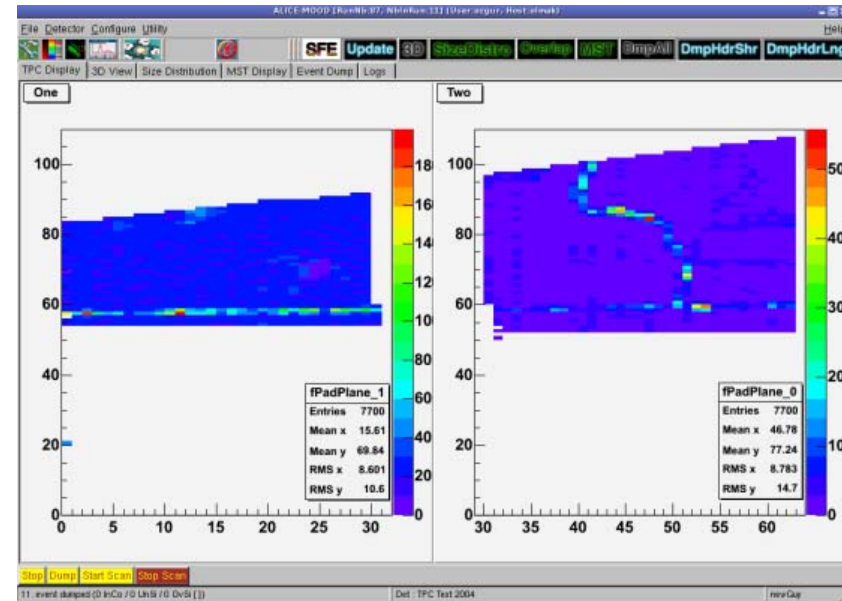
The screenshot shows the 'DATE database' menu. It contains several buttons: 'Roles', 'Detectors', 'Memory banks', 'Event building rules', and 'Quit'.

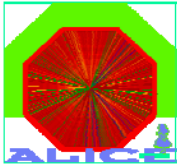
The screenshot shows the 'Roles list' dialog box. It has a 'Roles list' section with a list of roles: 'alonedc', 'thedetector', and 'thetriggemask'. There are buttons for 'New', 'Cancel', 'Add', and 'Suppression'. On the right, there are input fields for 'Name' (alonedc), 'Role' (LDC), 'ID' (1), 'HLT role' (Undefined), 'Hostname' (pcald37), 'Description' (Single LDC), and 'Made of' (Undefined). There are also checkboxes for 'Top level' and 'Active', and an 'Equipment' field with a right-pointing arrow. At the bottom, there are buttons for 'Commit', 'Rollback', and 'Quit'.



Data quality monitoring: MOOD

- Monitoring Of Online Data
 - Raw data integrity
 - Detector performance
- Using
 - DATE
 - ROOT



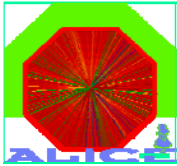


DAQ performance monitoring: AFFAIR

- DAQ performance monitoring
- Node view
- System view

The screenshot displays the AFFAIR performance monitoring interface. The main window shows a system overview with three charts: 'DATE CPU' (showing user, nice, sys, and idle percentages), 'DATE bandwidth in/out' (showing MB/sec for in and out), and 'DATE node status on/off' (a bar chart showing node activity over 20 minutes). A central table lists nodes grouped by LDC, GDC, and DATE. A secondary browser window on the right provides a detailed view of a GDC node, including a 'Total MBytesRecRate' chart and an 'eventsRec' chart, along with a list of nodes for that specific GDC.

- Using
 - Apache
 - DATE, ROOT
 - DIM, SMI++



ECS

- Overall ALICE Control

- TRG
- DAQ
- HLT
- DCS

- Using

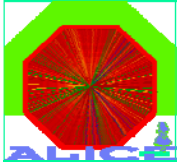
- DIM, SMI++
- Tcl/Tk
- MySQL

The screenshot displays several windows from the ECS control system:

- ITS Individual Detectors operations:** Shows status for SDD, SPD, and SSD, all currently INHIBITED.
- ITS DAQ details:** Shows status for ALLITS, SDD, SPD, and SSD. ALLITS is RUNNING, while SDD, SPD, and SSD are DISCONNECTED.
- ITS TRG details:** Shows status for TPA, LTU-SDD, LTU-SPD, and LTU-SSD. TPA is RUNNING, while the others are MASTER_RUNNING or SLAVE1/SLAVE2.
- LDC status display:** A table showing data for three LDCs (sddldc, spldc, ssldc).

LDC name	sddldc	spldc	ssldc
Number of equipments	1	1	1
Number of triggers	67449	67457	67457
Trigger rate	0	0	0
Number of events	67449	67457	67457
Event rate	0	0	0
Events recorded	67451	67459	67459
- GDC status display:** Shows data for GDC name eparbeam03gdc.

Number of events	202369
Event rate	354
Events recorded	67451
Events recorded rate	121
Bytes recorded	2084943168
Bytes recorded rate	3.739 M
- ITS Partition Control Agent:** Shows PCA status (PHYSICS) and FERD READY: TRUE. Includes buttons for DCS, DAQ, and TRIGGER.
- ALLITS DAQ - Run Control:** Shows the overall run control interface with buttons for Configuration, Run Parameters, and Data Taking Phase. The Run Number is 113 and the Run Control Status is RUNNING.



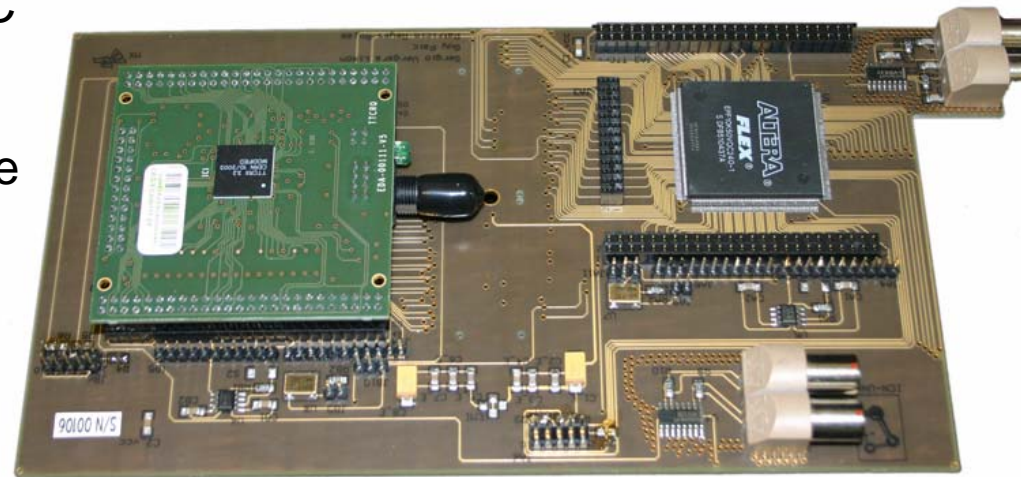
DAQ Commissioning

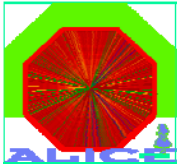
- DAQ commissioning:

- 1 system DAQ commissioning: “reference system” in DAQ lab
- Test all functionalities
- Running last released versions of DDL firmware, DAQ and ECS software

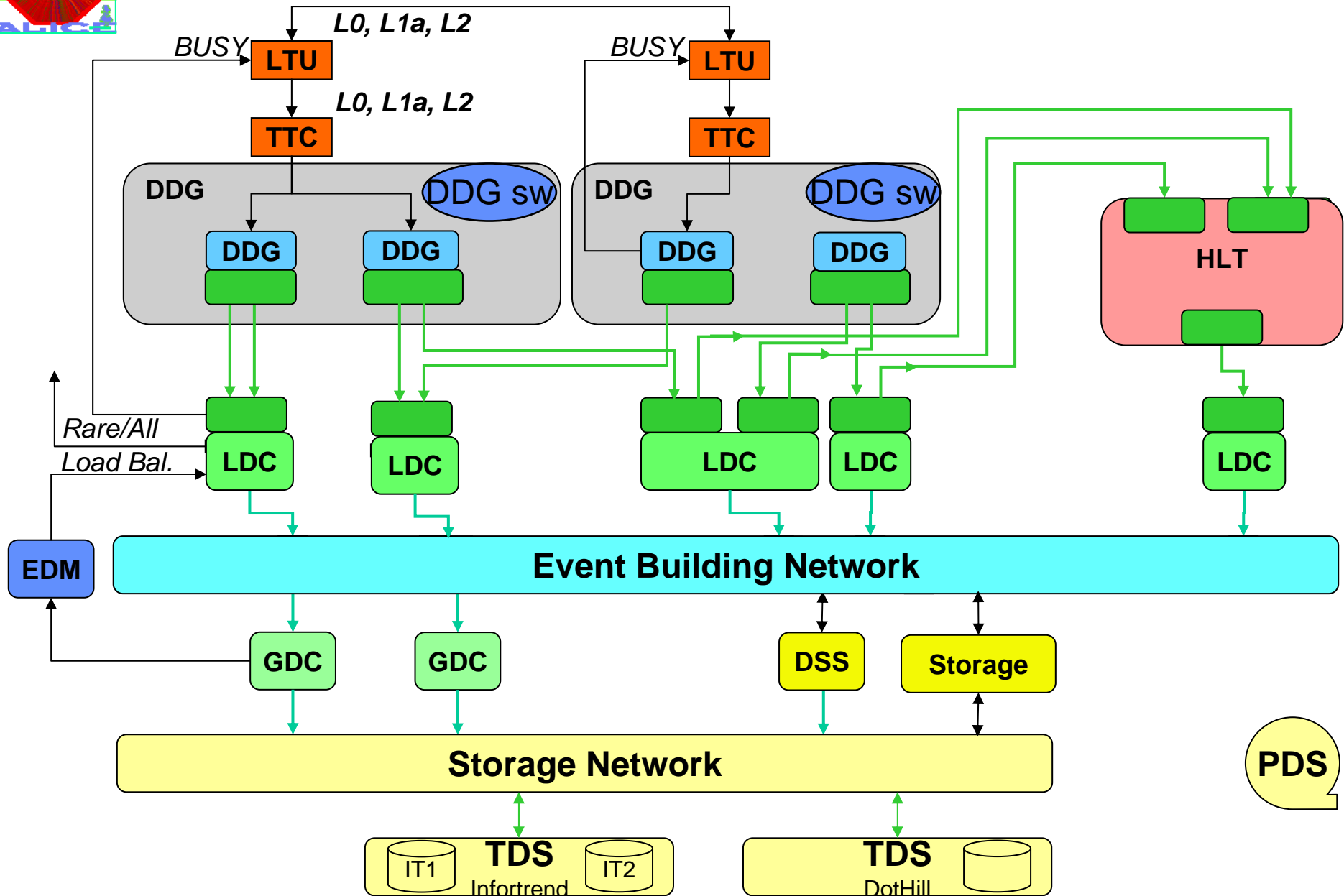
- Detector emulator

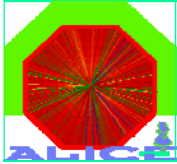
- DDL Data Generator (DDG)
- DDL data source triggered by TTC
- Generation of busy
- Uses the D-RORC as DMA engine to read data from PC memory
- Send them over DDL





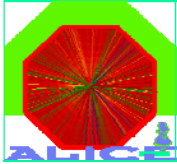
DAQ Reference System: hw data generator





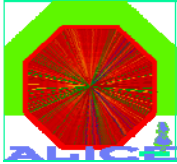
DAQ systems for detector test & commissioning

- Detector tests with DAQ
 - Data transfer: 25 DDLs for tests (1 chain per detector delivered since 2002)
 - DATE sw
- Detector commissioning with DAQ
 - Hardware DAQ dedicated to detector tests:
Distributed in different locations according to needs
 - Data transfer
 - CERN: 20 DDL SIUs, 16 D-RORCs, 8 DIUs
 - DAQ fabric
 - 12 LDCs (6 PCI slots)
 - 4 GDCs, 3 servers
 - 2 storage units 2 TB



DAQ systems for detector test & commissioning

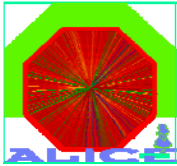
- SPD First sector with DAQ, TRG, ECS in DSF (CERN Bld 186)
- SSD DAQ system (Utrecht)
- SDD DAQ system (Torino)
- TPC Electronics setup (Bergen, CERN Bld 13). Detector (SXL2 CERN)
- TRD DAQ ready for super-module being assembled (Heidelberg)
- TOF DAQ ready for module being assembled (Bologna, CERN Bld 156)
- Muon TRK DAQ system (Orsay). Feb '06: test SXL2
- Muon TRG DAQ system (Nantes)
- HMPID DAQ system (CERN Bld 581)
- PHOS DAQ for electronics test, then module assembly (Bergen, CERN Bld 167)
- FMD DAQ installed for test in March (NBI, CERN Bld 1)
- T0 DAQ in TOF labs (Bologna and CERN)
- V0 Test of CCIU (Lyon)
- ACORDE DAQ system for detector (SXL2 CERN)
- EMCal DAQ system used during TB (Fermilab)



Detector/DAQ integration (Mar 06)

	S P D	S S D	S D D	T P C	T R D	T O F	M U O N T R K	M U O N T R G	H M P I D	P H O S	F M D	T O	V O	Z D C	P M D	A C O R D E	E M C A L
DATE system	Green	Green	Green	Green	Green	Green	Green	Green	Green	Green	Green	Green	Green	Green	Green	Red	Green
DDL with data gen.	Green	Green	Green	Green	Green	Green	Green	Green	Green	Green	Green	Green	Green	Red	Red	Red	Green
Detector readout with DDL & DATE	Green	Green	Green	Green	Green	Green	Green	Green	Green	Red	Red	Green	Green	Red	Red	Red	Green
Data quality monitor. (MOOD)	Green	Green	Green	Orange	Green	Orange	Green	Green	Green	Red	Red	Red	Red	Red	Red	Red	Red

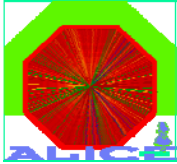
 **Must be done in the lab before starting commissioning at Point 2**



Services

- Ready
 - 35 racks 56 U
 - Normal Power
 - Air conditioning
 - Cooling doors for 35 racks
 - Connections to chilled water
 - Chilled water circuits
 - Network
 - Access control
 - Optical fibres SXL-CR1
- In progress
 - Optical fibres between CR1 and other CRs and UX
- Quality and schedule critical

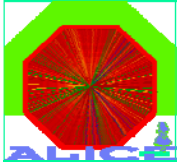




Some of the next steps

- Apr '06 DAQ standalone commissioned in lab
- May '06 ECS + DAQ + HLT at Point 2
- Jun '06 ECS + TRG + DAQ test and commissioning in lab
Installation DAQ Stage 1
- Jun'06 – Sep'06
Data Challenge from Point 2 to IT

- May '06 TPC commissioning on surface with cosmics
- Jul '06 PHOS, TOF, TRD, HMPID, ACORDE
- Sep '06 TPC
- Jan '07 ITS
- Feb '07 TOF, TRD
- Apr '07 FMD, V0, T0, PMD



Conclusion

- Production of DDL and D-RORC in progress
 - Mar-Jul '06. Enough DDL SIUs to equip 1 side of TPC
- DAQ fabric hardware
 - All hw elements qualified. Tenders include most recent equipment.
 - Procurement and delivery in progress.
- DAQ software ready
 - Software (DDL sw, DATE, AFFAIR, MOOD) released and documented.
 - Linux SLC3 now. Transition to SLC4 scheduled before end '06.
- DAQ system deployment
 - Stage 0: small DAQ system for detector test and commissioning
 - Stage 1: deployed in June (full readout, 20% performance)
- Installation
 - Services for DAQ finished. Optical fibres progressing with detector installation.
- Commissioning of detectors in parallel