Experience with DAQ for ATLAS SCT

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On behalf of ATLAS SCT collaboration
Vertex '08

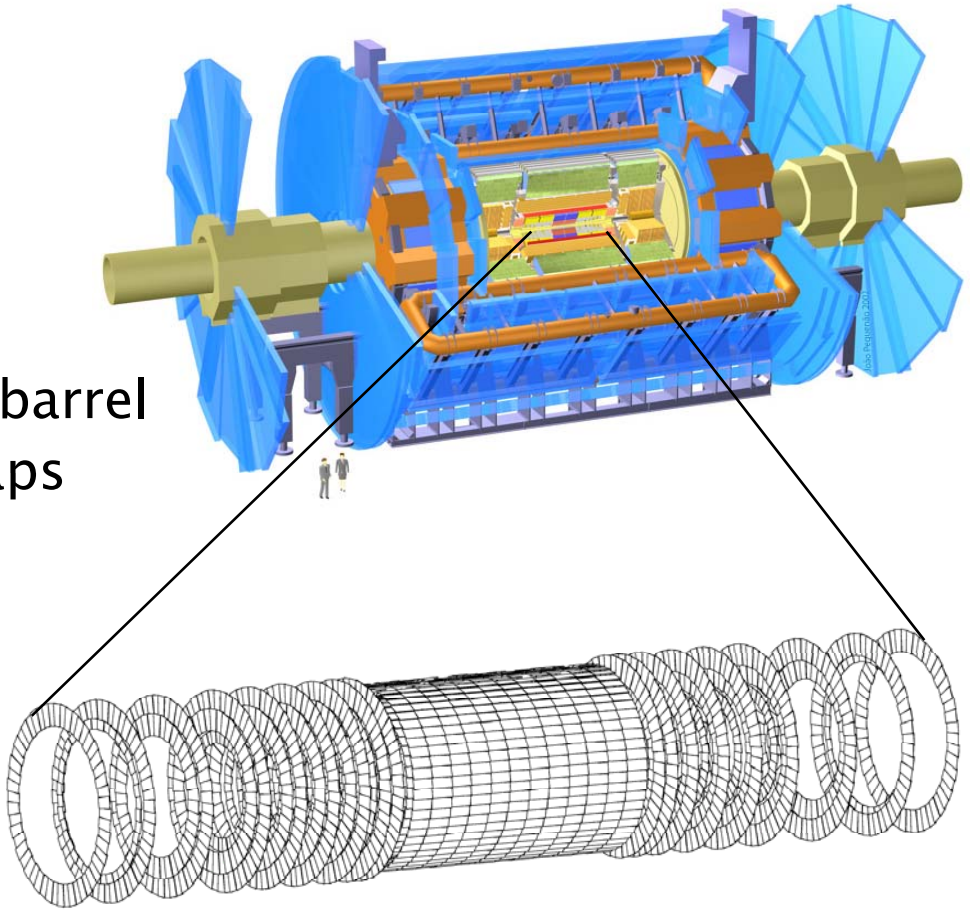
ATLAS SCT

Part of the inner tracking detector in ATLAS

Silicon strips
- 6.3 M channels

4088 modules
- 2112 on 4 cylinders in the barrel
- 1976 on 9 disks in 2 endcaps
- Each double sided
- 40 mrad stereo angle
- Up to 12 cm strips
- 80μm pitch

Bunch crossing at 40MHz
- Level 1 trigger at up to 100kHz

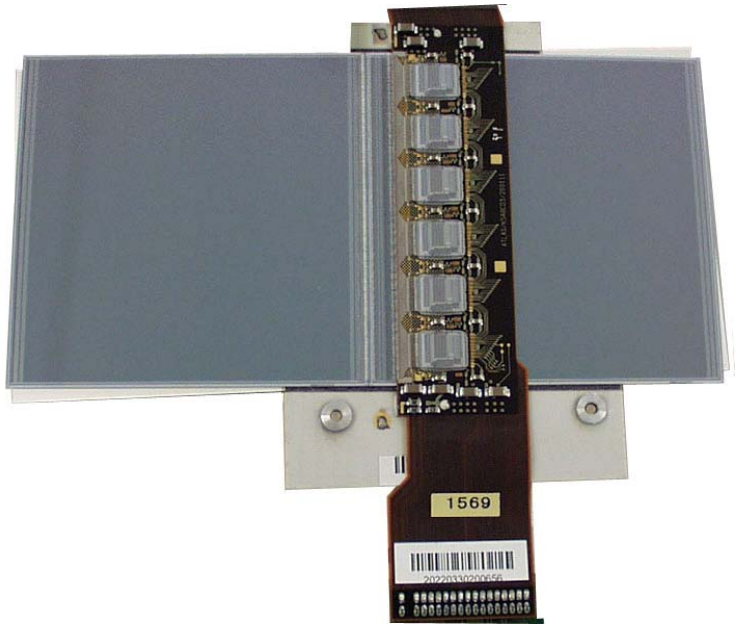


SCT Modules

1536 strips per module

12 ABCD front-end chips

- Binary pipeline 132 deep
- Waiting for level 1 trigger
- Read out 3 time-bins on trigger



Optical link to/from module

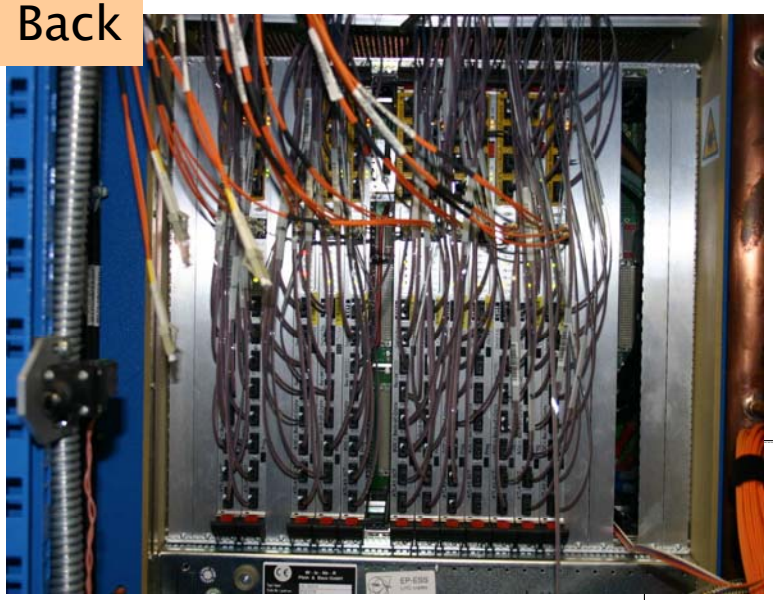
- Clock and control on one fibre using BPM (bi-phase mark) encoding
- Two fibres for read-out ½ module each
- Redundancy options for control and read-out

Off-detector Hardware

Front

- 8 VME Crates
  - 6-U SBC
    - Ethernet connection
    - External control
  - 11(2) * ROD, BOC pairs
  - TIM

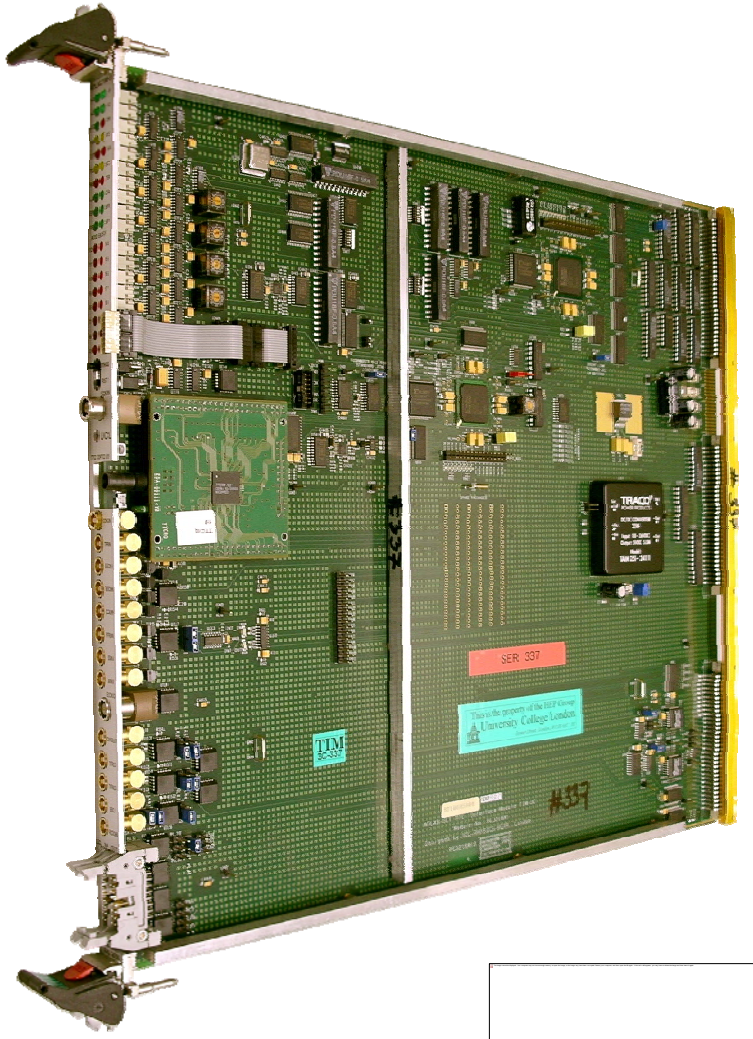
Back



- Each ROD controls up to 48 modules
- Receives timing information from TIM
- 9 rack mounted monitoring hosts

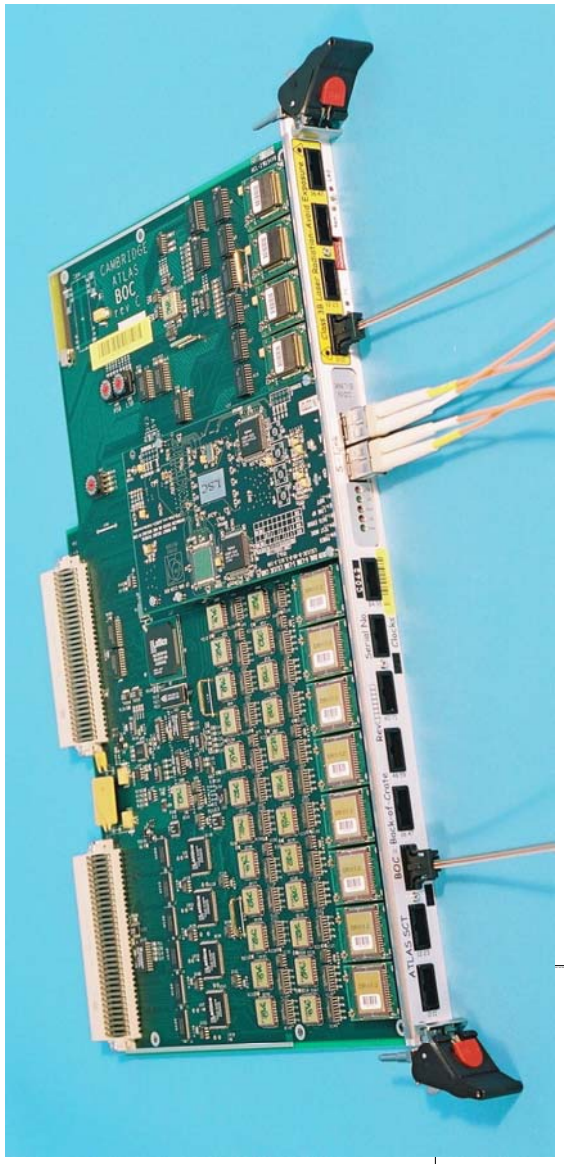
TIM – Timing Interface Module

- Distributes clock and trigger from ATLAS trigger system (TTC) to RODs using custom crate backplane
- Generate counters for event synchronisation (TTCrq)
- Transmit BUSY signal from RODs
- Generate BUSY to veto fixed frequency triggers
  - Avoid bond-wire resonances
- Standalone mode
  - External or pseudo-random trigger with delays



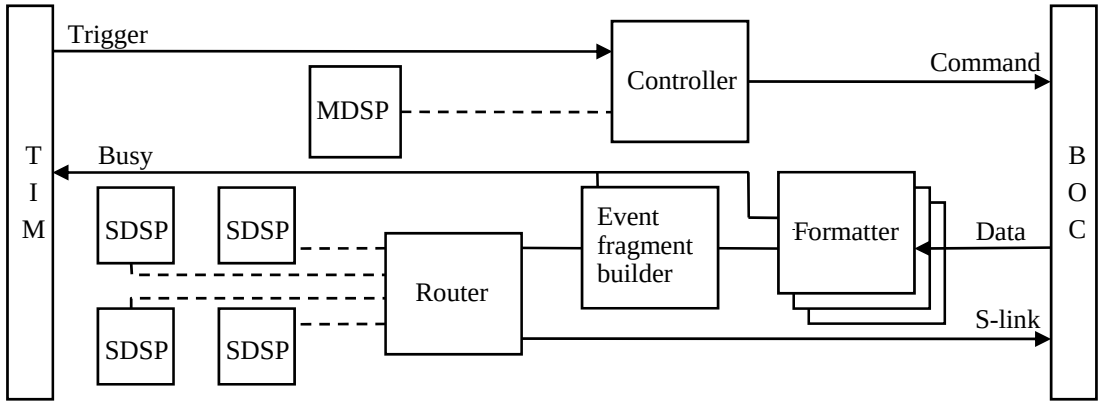
BOC – Back of Crate

- Optical interface to front-end modules and data flow
- Tx clock and command -> BPM
  - Adjust timing of trigger to modules
  - Programmable parameters of BPM
- Rx, one fibre from each side of a module
  - Programmable threshold and timing
- Distribute clock from TIM to ROD and modules
- S-link to ATLAS event builder
- Configurable via serial port to ROD



ROD – Readout Driver

- Generate command and parse data signals for 48 modules
- Triggers and resets come from TIM
- Data formatted into events goes to ROS via S-link
- FPGAs implement data path
- DSPs for setup and monitoring



Physics Data-taking Mode

System design was optimised for physics mode

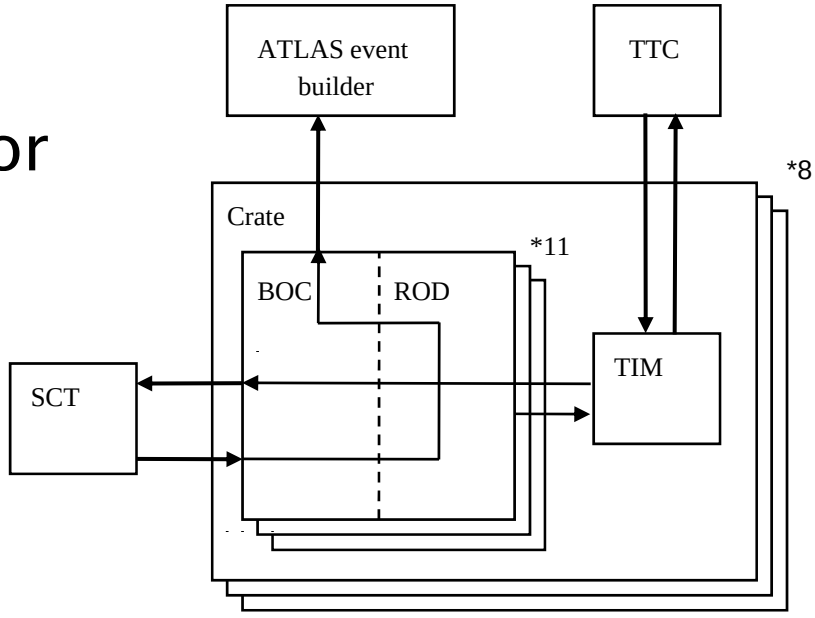
SBC used to configure modules

After that the ROD FPGAs do all the work

- Data is built into events
- Sent to S-Link

Busy from ROD when not ready for triggers

Once running, the job of the SBC becomes one of monitoring



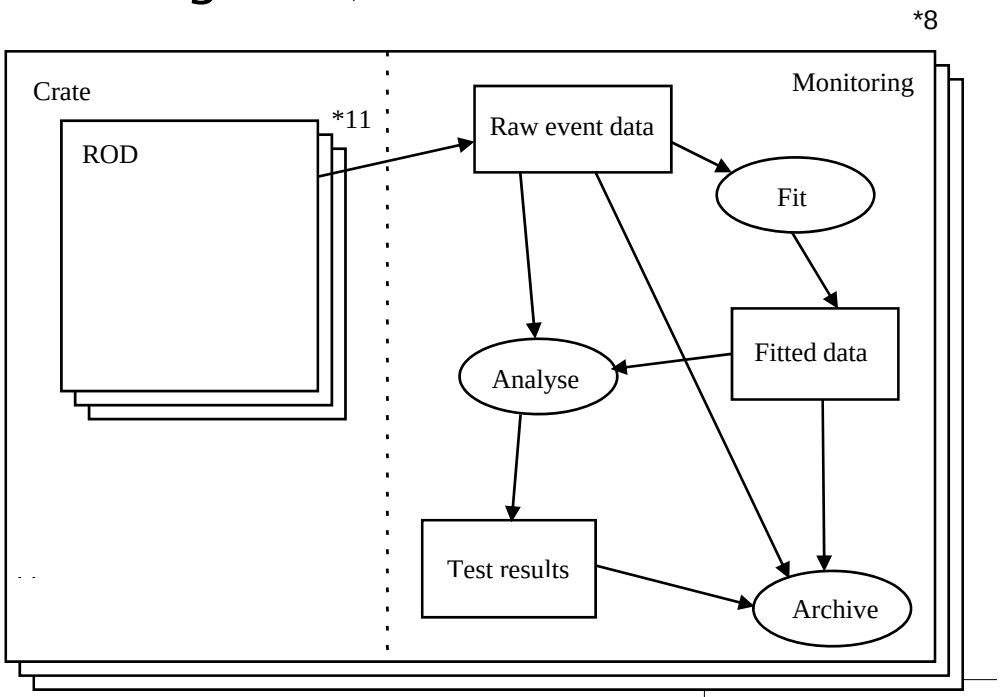
DAQ Calibration Software

Software on crate

- SctApi provides interface to RODs, BOCs and TIMs
- Configuration of VME cards and SCT modules
- Generate histograms (by controlling ROD) for calibration and monitoring

Off-crate, calibration infrastructure

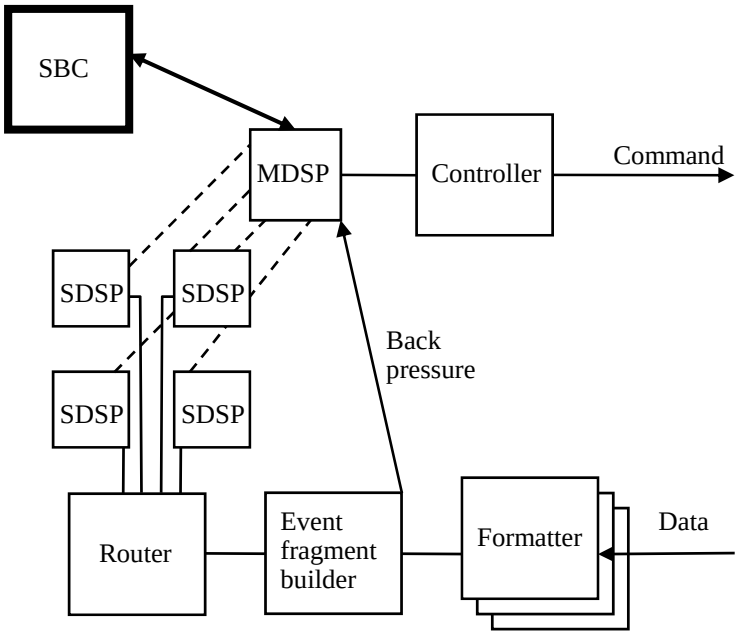
- Description of tests
- Fit S-curves
- Analysis of tests
- Change configuration based on results

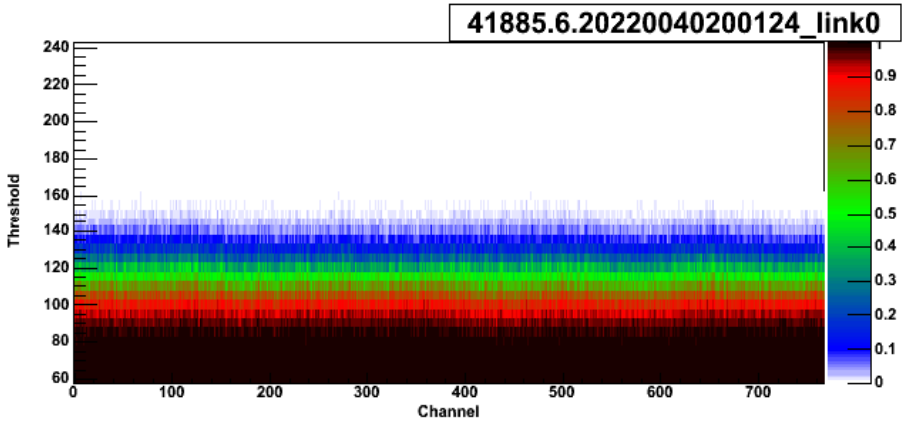


Calibration Scans

Produce scan using DSPs on the ROD

- Set module parameters
- Pick one variable to change
- Send sequence of triggers to read out module
- Histogram the hits in the resulting events



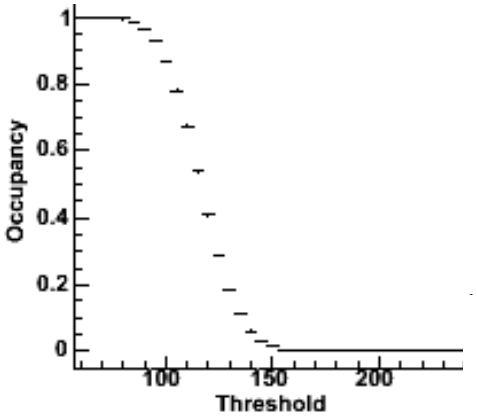


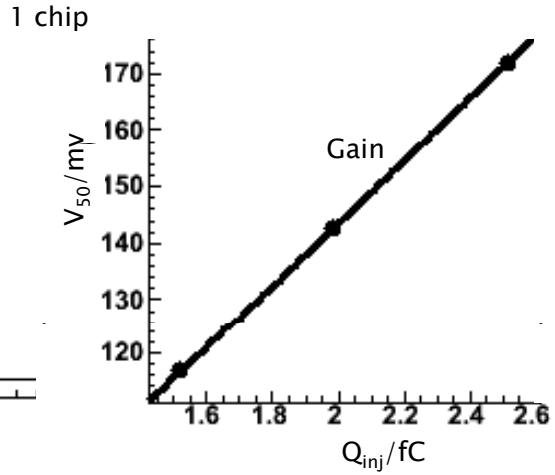
If one module produces errors, suppress from the scan so others can continue

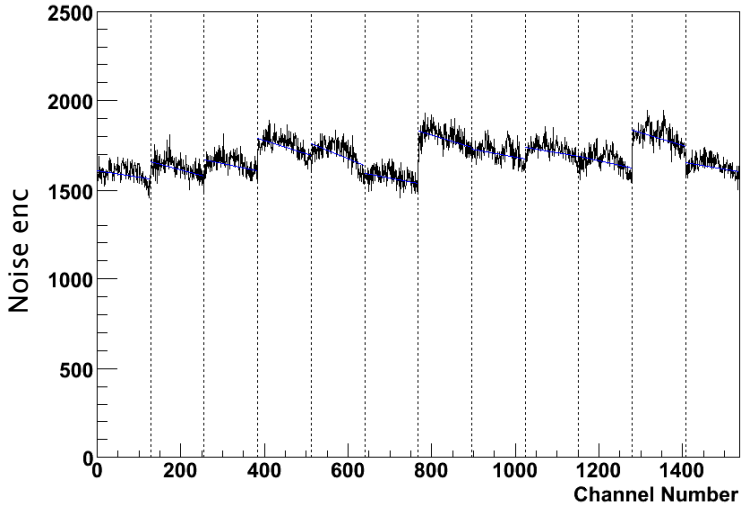
Calibration Tests

A calibration test is made up of a series of scans, each with different parameter settings

- The scans are analysed together to produce a calibration result
  - Pipeline test => pipeline defects
  - Threshold scans => bad channel maps
  - 3-pt gain => response curve, noise estimation







Optical Links

For each module, one Tx and 2 Rx fibres

Rx needs thresholds set correctly

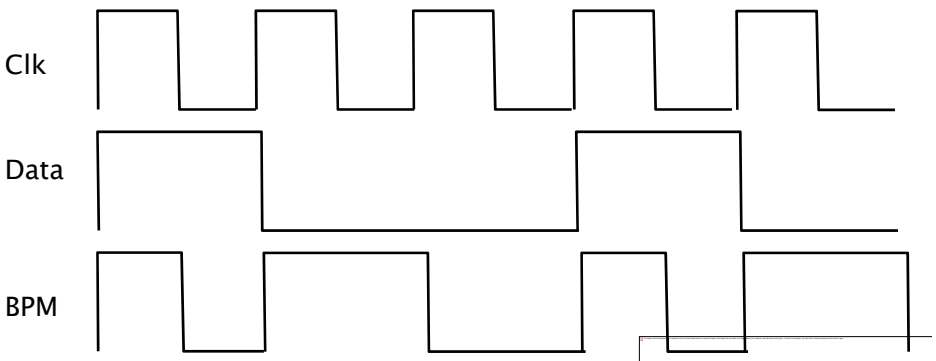
- Assumes valid Tx settings
- Scan using ABCD clock pass-through (clock/2)

Changing Tx amplitude can remove clock from chips

- Best procedure so far is to set high value and lower until doesn't work (assumes valid Rx)
- Current through PiN device indicates reception of signal

Changeable mark-space ratio

- Minimise jitter in clock derived from BPM signal
- Have had problems scanning MSR as when clock becomes invalid the scan can fail



2D Rx Scan

Optimise both Rx threshold and delay

Run in clock by 2 mode

For each setting

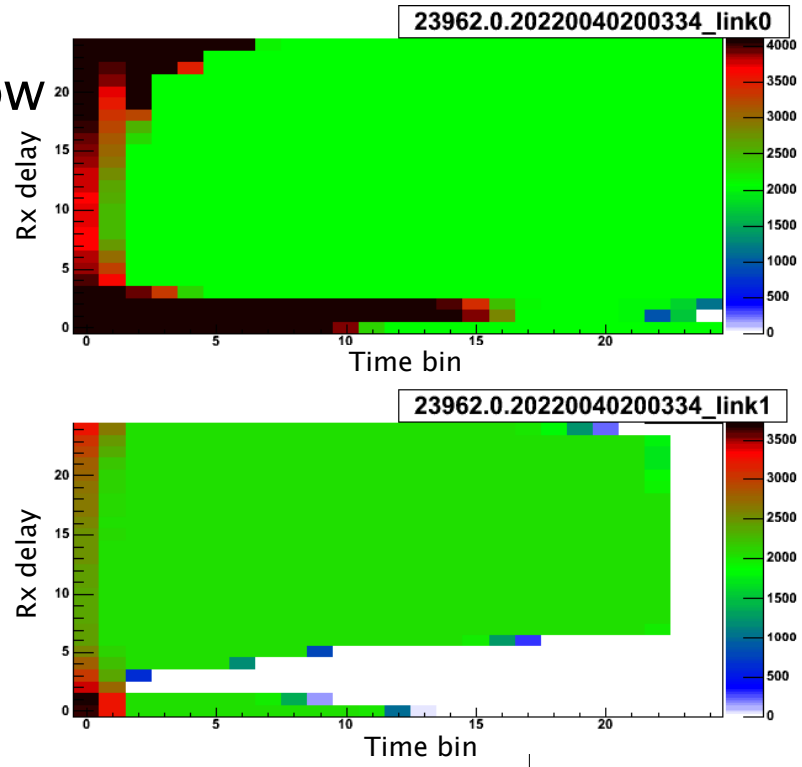
- Count number of 1s in time window

Use counters added to ROD firmware for this purpose

Fast, majority of time spent switching parameters

No trigger sent so don't worry about fixed frequency

But fails to find correct values for slow turn on lasers (return to zero protocol)

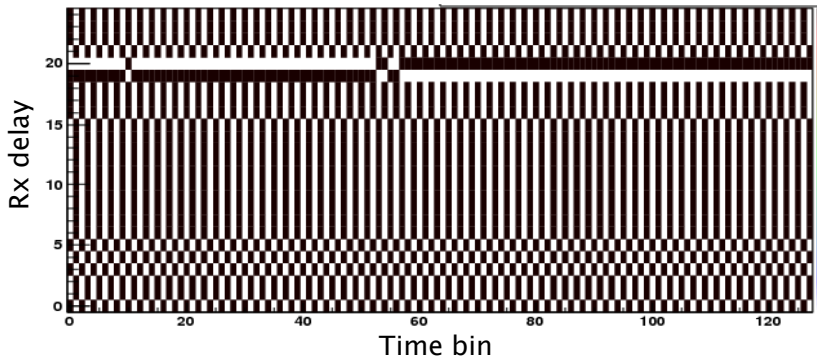


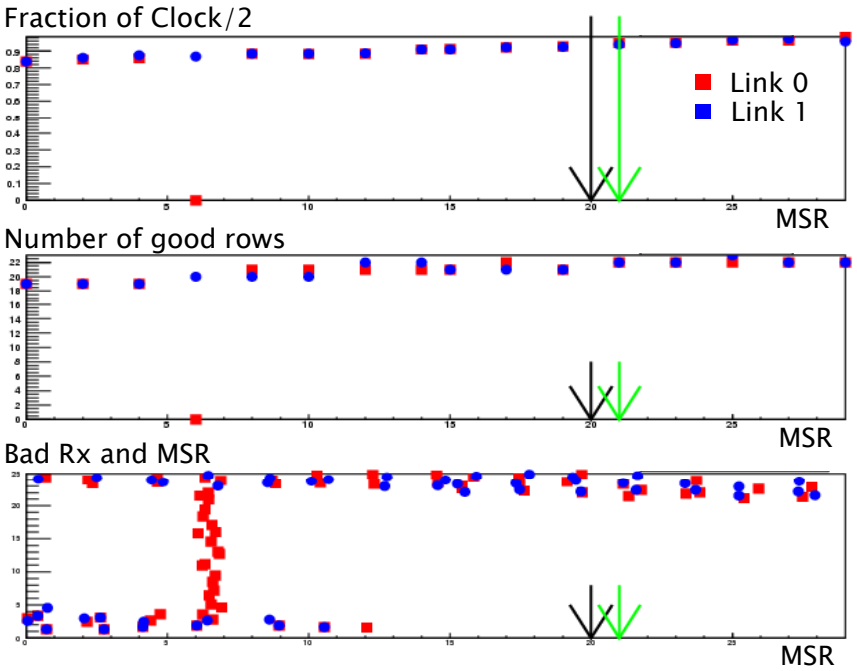
Mark-space Ratio Test

Poor mark-space introduces jitter in reconstructed clock

Scan before and after bit-flip

- Try using ROD counters for this





Scanning mark-space affects clock transmission

- BPM decoder on module can find half clock, test should fail

New method

- Send bit-flip during capture
- Send configuration stream for clock reconstruction

Better results on test modules

ROD Busy

BUSY caused by data volume close to or over limit

Normally due to few modules malfunctioning

- Don't want to affect whole system

Monitor for occupancy close to limit (e.g. loss of bias)

- Identify hot links in DSP code
- If occupancy too high, take appropriate action

If ROD trigger buffer overflows, data for ROD is lost

- BUSY can only be cleared by reset of ROD FPGAs
- Need to catch BUSY before data is lost

Work in progress to identify causes at module link level

Simulation of ABCD

Recent RODs have spare space in FPGA

- Run simulation of chips when modules not available
- When trigger arrives, generate bit-stream at input
- Exercise whole data chain
- Programmable number of hits on random channels

Very useful

- Haven't used much for development yet
- Would have been useful at an earlier stage

Minor problem

- Doesn't receive reset signals so counters are not implemented

DAQ Monitoring

A shifter needs to know what is happening in the system

When working, the system receives triggers and sends out events

Online event monitoring

- Histogram events sampled from ATLAS event path
  - At crate level within sub-detector
  - ATLAS level using analysis infrastructure
- Also possible in RODs, so far not a priority

Monitoring of BUSY signals at TIM and ROD level

Many more things could be monitored

- Need balance between which are useful and amount of information to read out

BC Reset and BCID

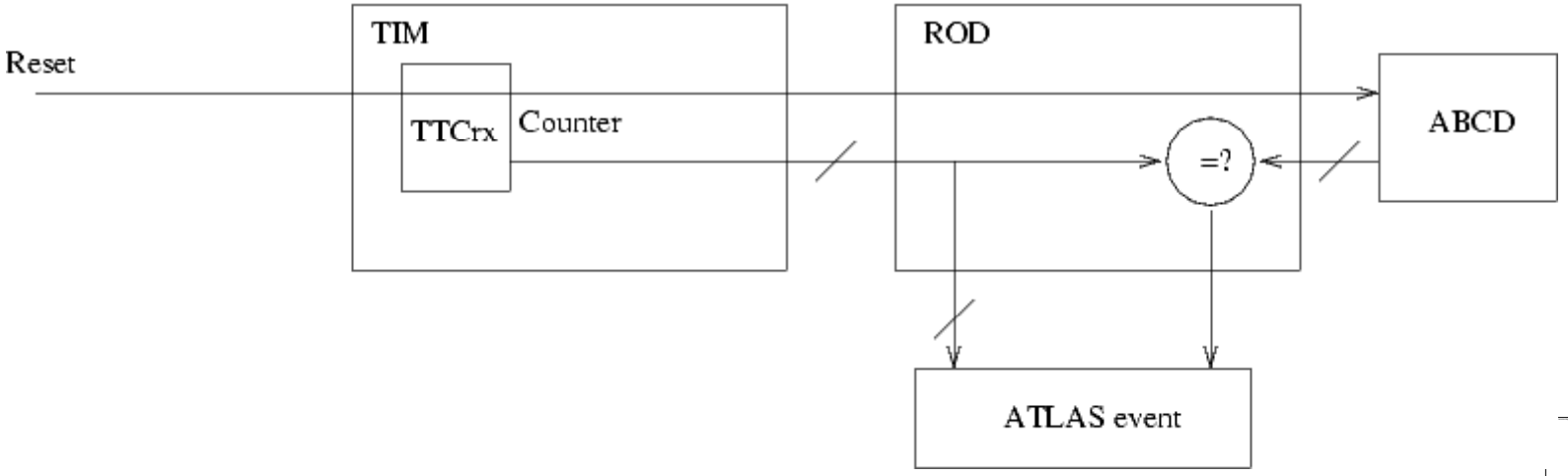
Bunch crossing counter for synchronisation

SEU recovery, need regular reset every orbit

- In the long gap before each bunch of triggers

TIM arranges for minimal transmission latency

But, BC reset to ABCD can't be at the same time as L1A and takes several cycles to transmit to ABCD



Correction of BCID

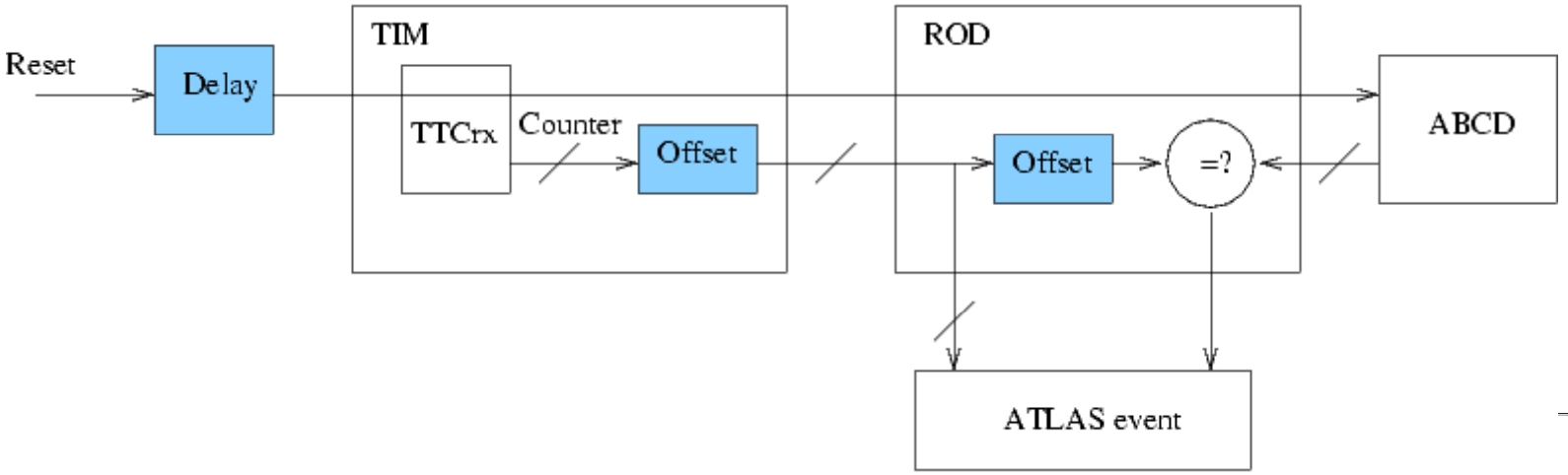
Need to veto trigger during BC reset

Bunch crossing counter, first bunch is 0

Delay arrival of BCR into region of no triggers

Correct to make BCID=0 match first bunch, in TIM

Compensate in ROD for check against module



Milestone Runs

Series of milestone runs with all ATLAS

- M5 run with small number of modules in test box
  - Exercise trigger system and real event timing
- Full SCT barrel in M6
  - Time in by dead reckoning
  - Cosmic tracks through muon chamber
- M7
  - Run using simulator for one day
- M8
  - Run up to ~70kHz using simulated data
  - Use new BC reset scheme, instead of trigger veto

Summary

The system has been tested with over half the SCT

- Has flagged problems with BC counters, monitoring

Need more experience of running with real modules

- Main area is monitoring so we don't flag BUSY unnecessarily

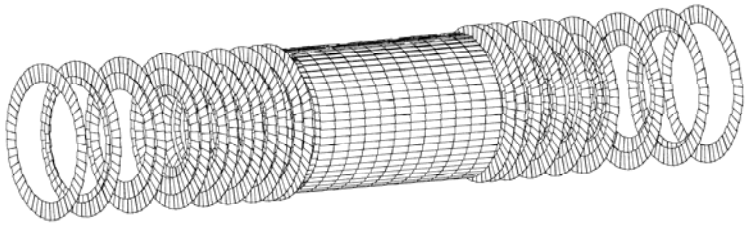
Simulation of modules is a useful feature that would have helped at an earlier stage

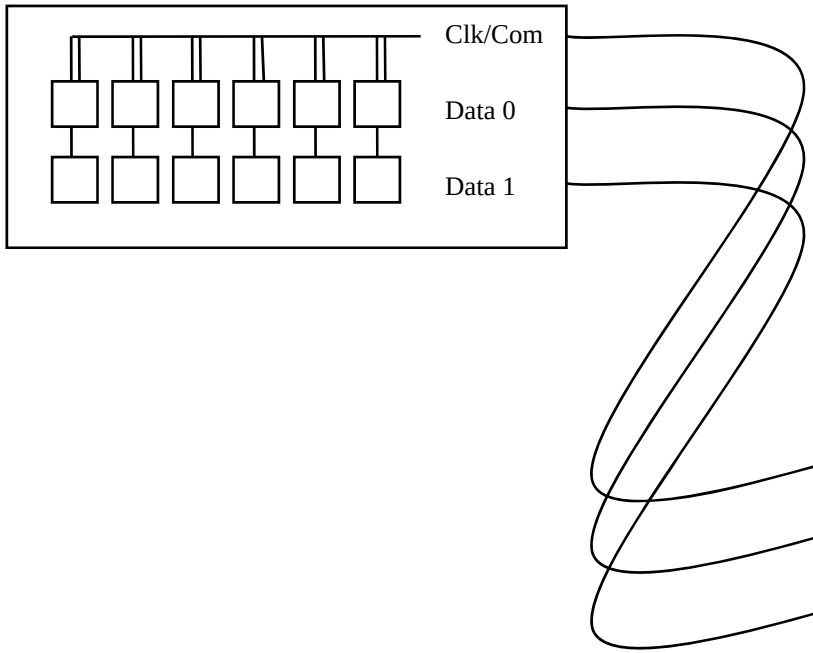
- Can't assume the infrastructure is going to work all the time

For the future

- Non-return to zero encoding would be a good thing both ways
- Having "dead-time" for resets causes problems

DAQ Overview





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  - Clock and control on one fibre using BPM (bi-phase mark) encoding
  - Two fibres read out ½ module each
  - Redundancy options for control and read-out