Optimization of the New Vertex Detector for (Super) Belle

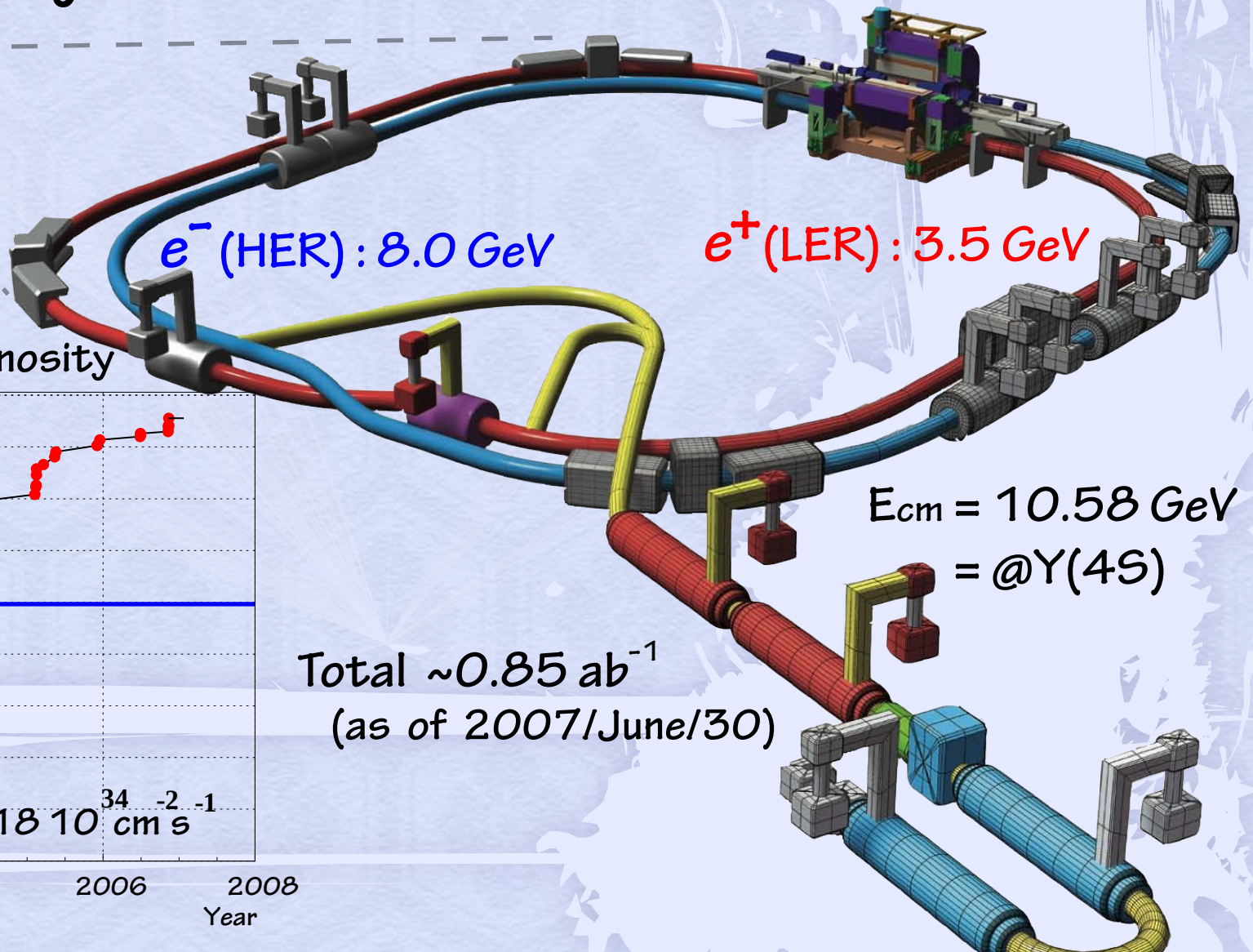
T.Hara (Osaka U) for Belle SVD group

– Contents –

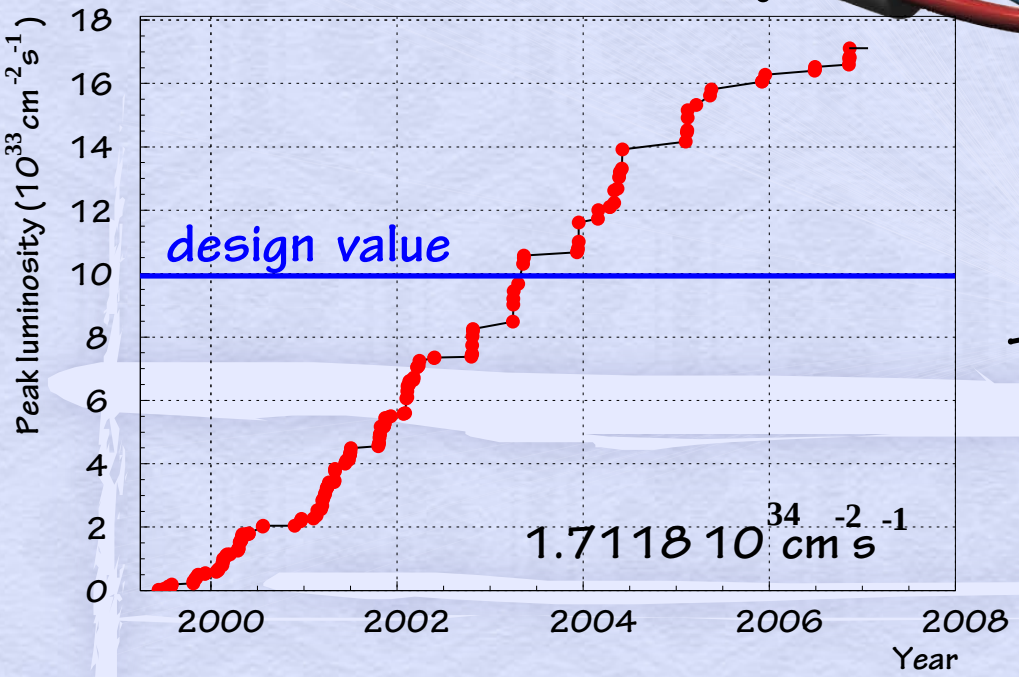
. Status of the current Silicon Vertex Detector
. Super KEKB/Belle
. Optimization of the Baseline design
. Optimization of the Final (LoI) design
. Summary

KEKB

Asymmetric e^+e^- Collider



Increase of KEKB Peak Luminosity

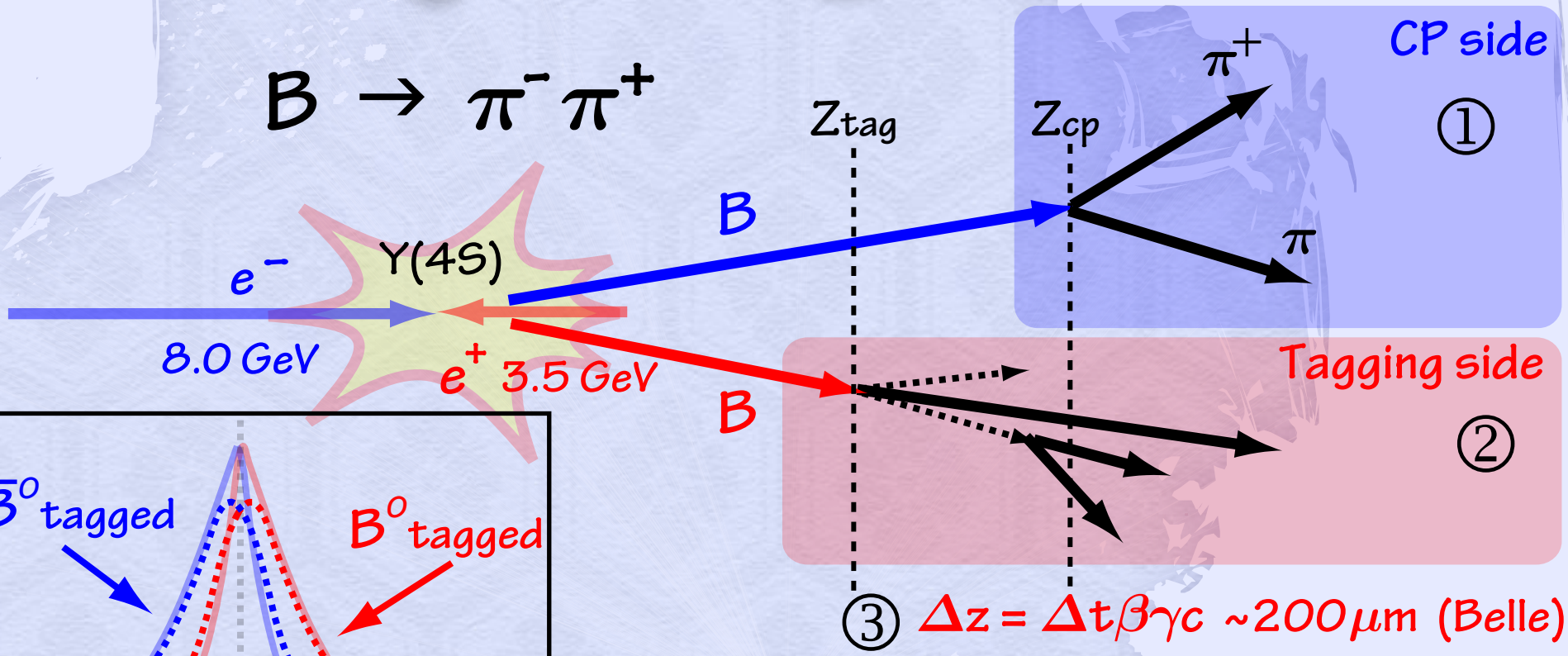


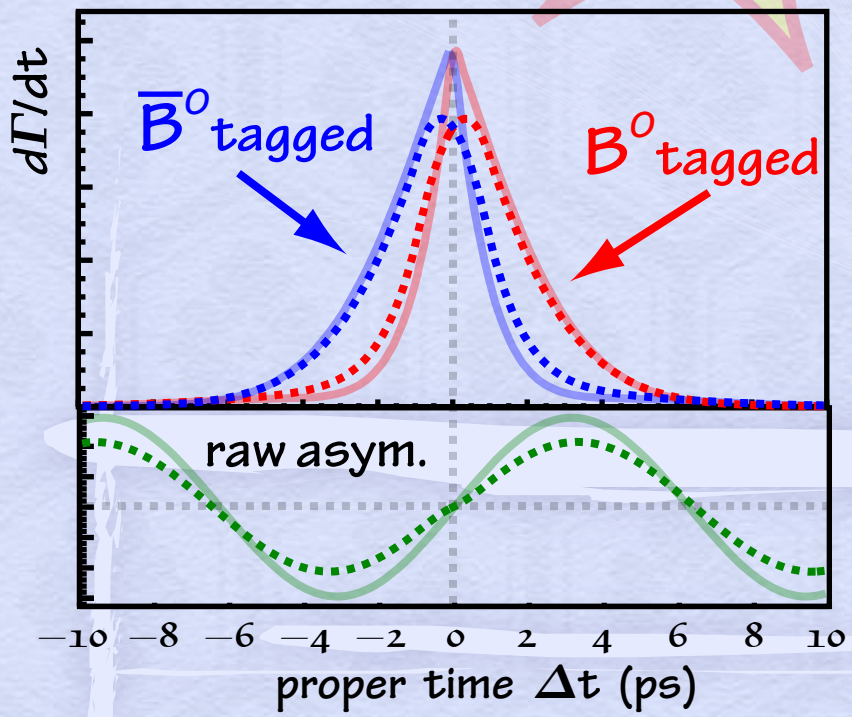
E_{cm} = 10.58 GeV
= @Y(4S)

Total ~0.85 ab^{-1}
(as of 2007/June/30)

Physics @ Belle

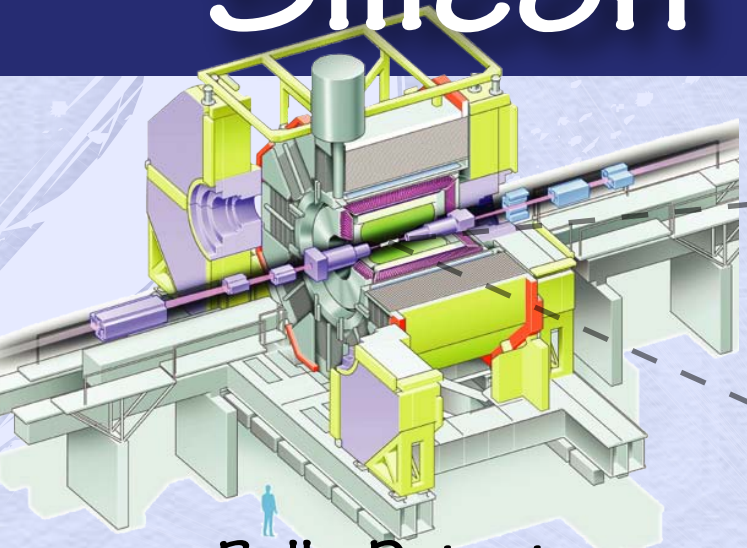
$B \to \pi^- \pi^+$





①CP-side Reconstruction
②Flavor Tagging
③$\Delta z(=\Delta t \beta\gamma c)$ Measurement

Silicon Vertex Detector



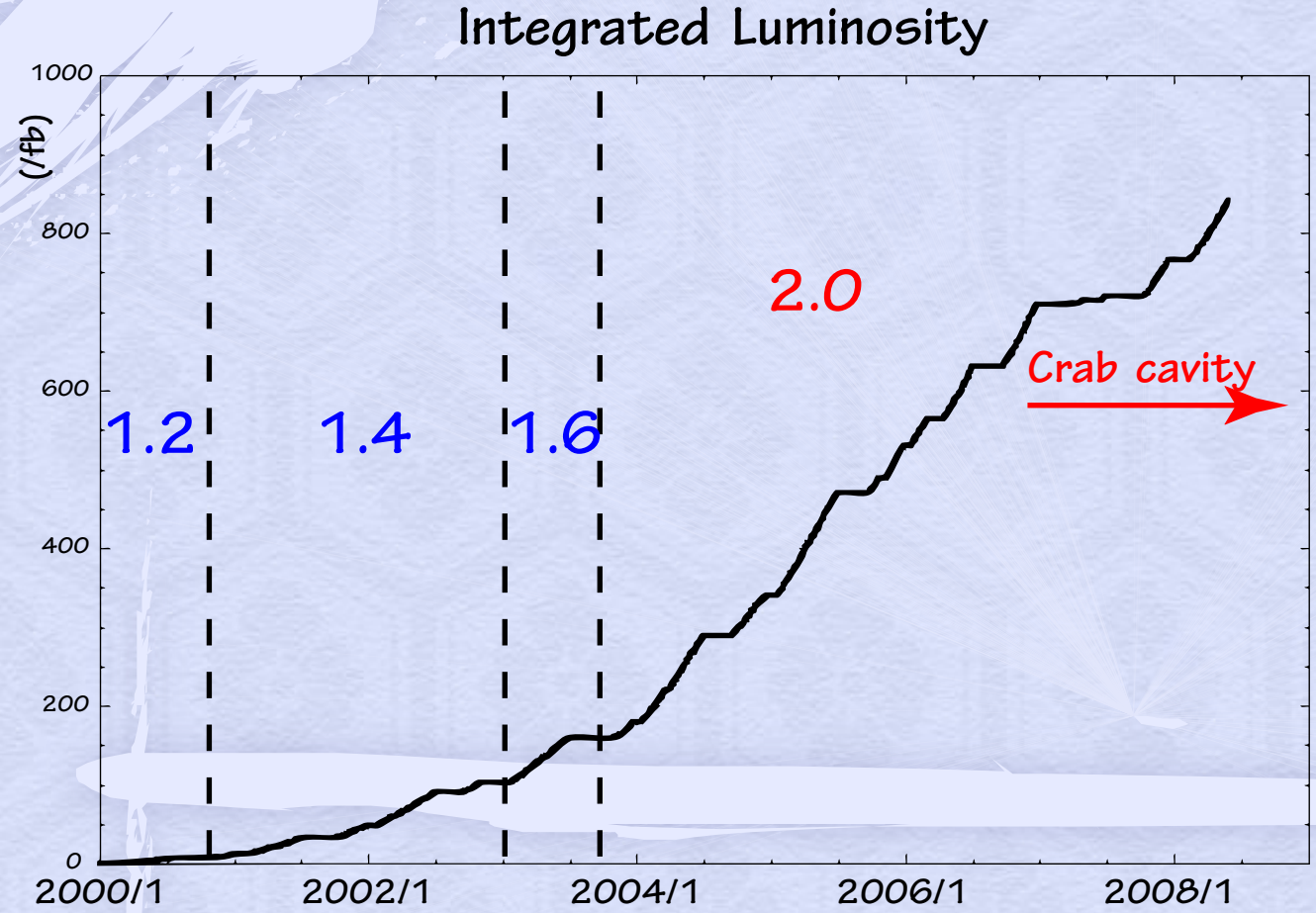
Belle Detector

over 20 institutes
~ 100 members

SVD2

SVD1 (upto 2003 summer)	SVD2 (upto now)	
3-layer (R_{3rd} = 6.0cm)	4-layer (R_{4th} = 8.8cm)	better low P tracking
2.0 (3.0) cm radius of beam pipe (1st lyr)	1.5 (2.0) cm radius of beam pipe (1st lyr)	better vertex resolution
23°< θ < 139°	17°< θ < 150°	larger acceptance
VA1 (0.8 μm) : < 1MRad	VA1TA (0.35 μm) : < 20MRad	rad. hard

SVD History



SVD1.0 : VA w/ 1.2μm process
(up to 200 kRad)
demaged by soft X-rays

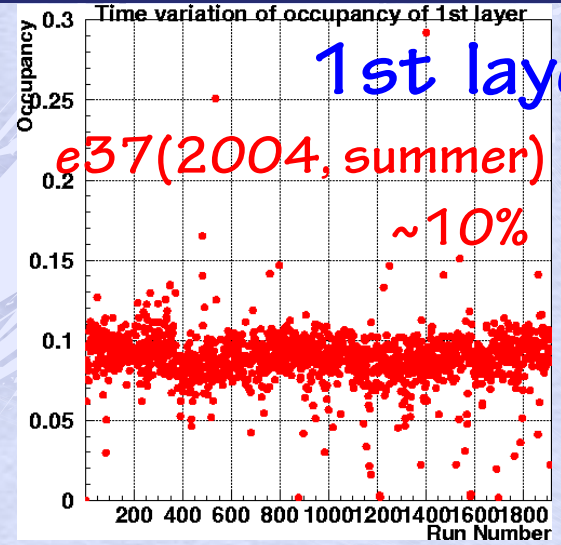
SVD1.2 : a gold foil was wrapped
on the beam pipe to stop X-rays

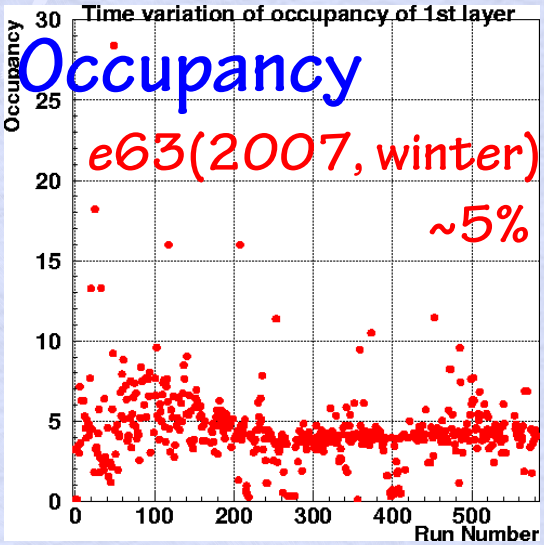
SVD1.4 : VA w/ 0.8μm process
(up to 1MRad)

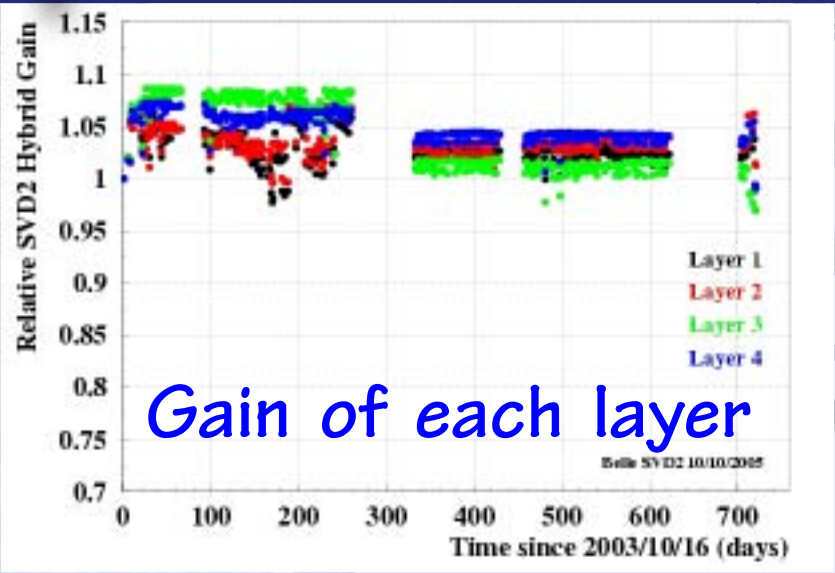
SVD1.6 : degraded ladders
were replaced

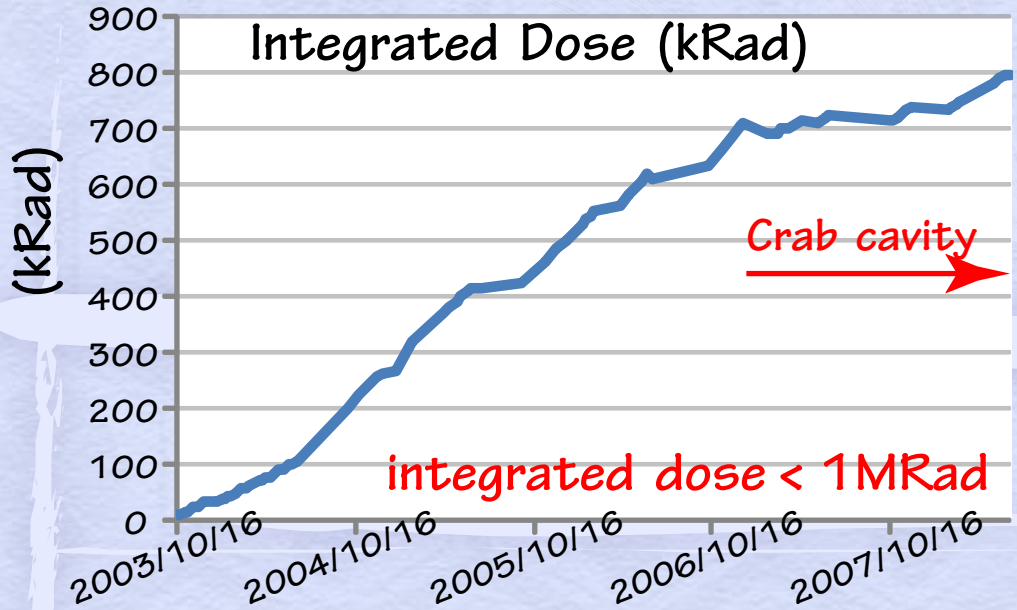
SVD2.0 : VA w/ 0.35μm process
(up to 20MRad)

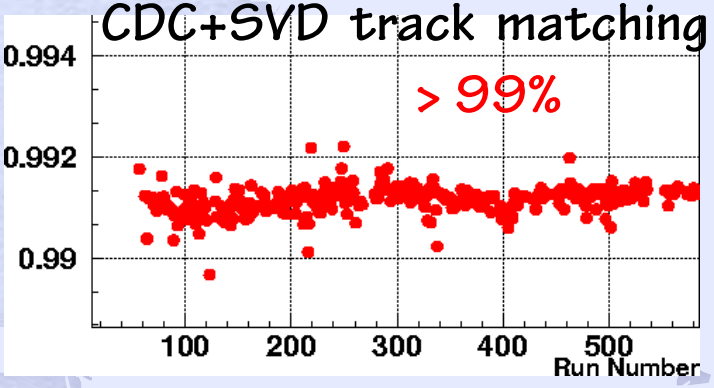
SVD Stable Operation











Belle operation will continue!

2009 fiscal year : ~5 months

(Not fixed yet)

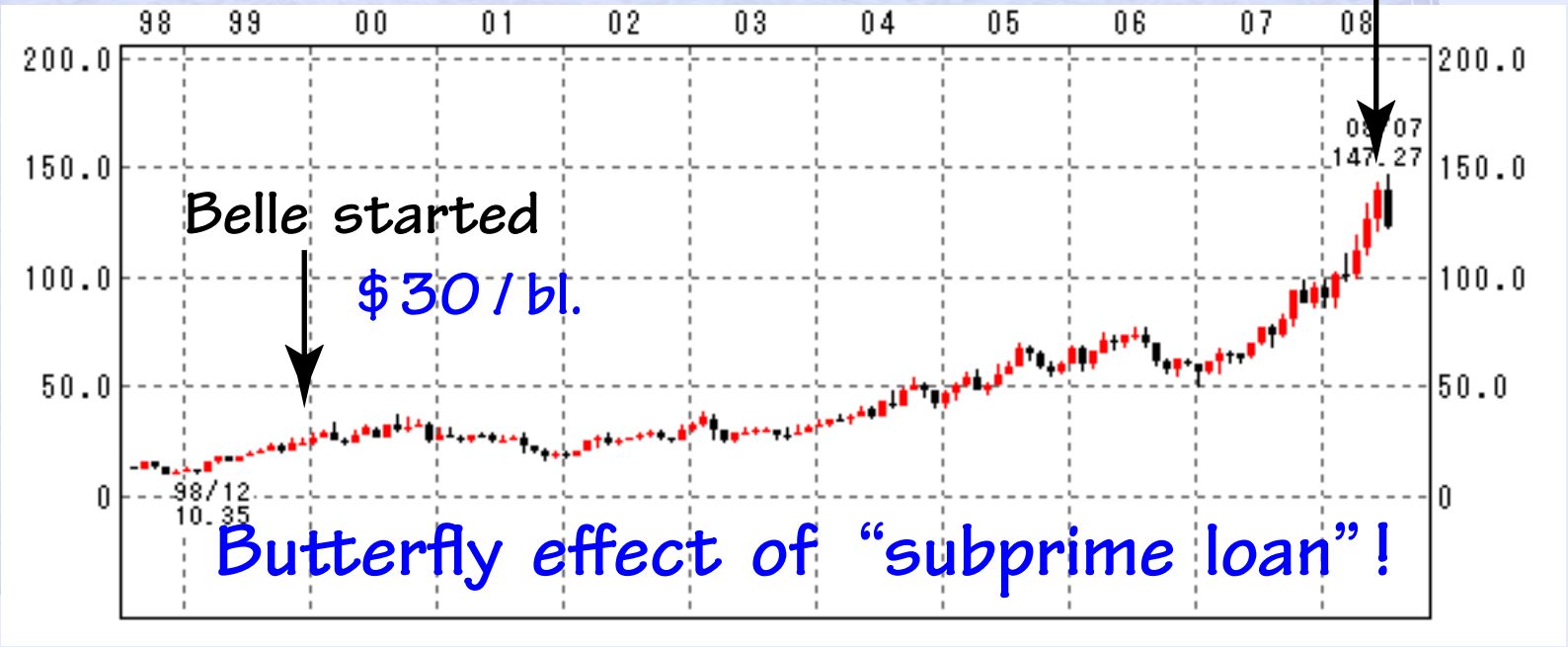
Price of crude oil

Belle operation will continue!

2009 fiscal year: ~5 months

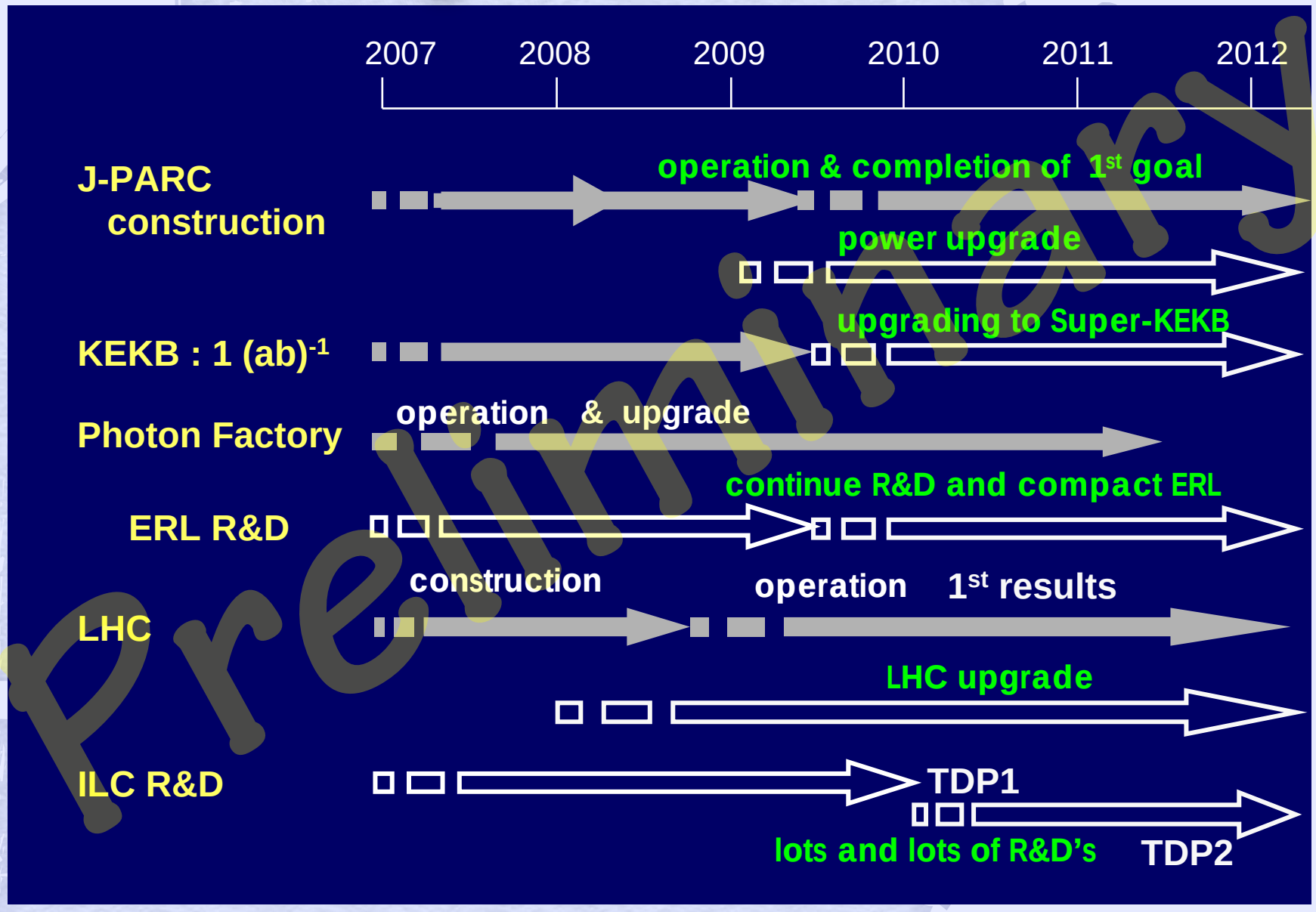
(Not fixed yet)

~$150/bl.



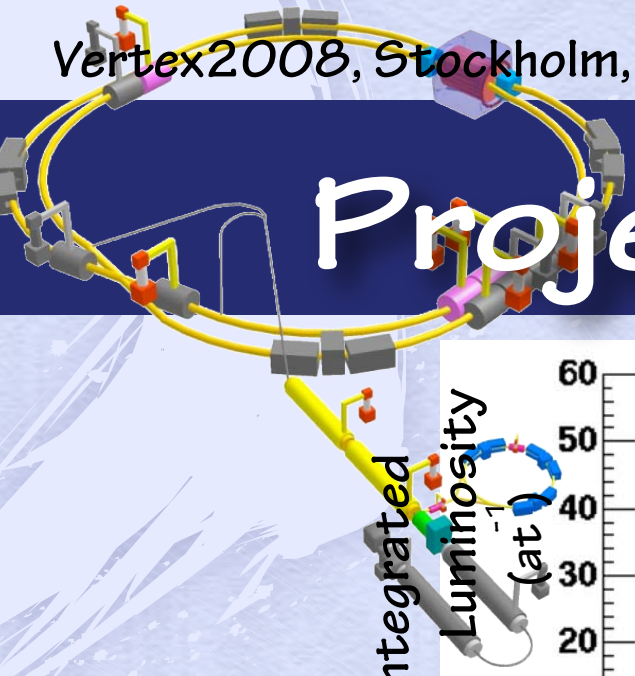
Running cost is getting higher and higher these days!!

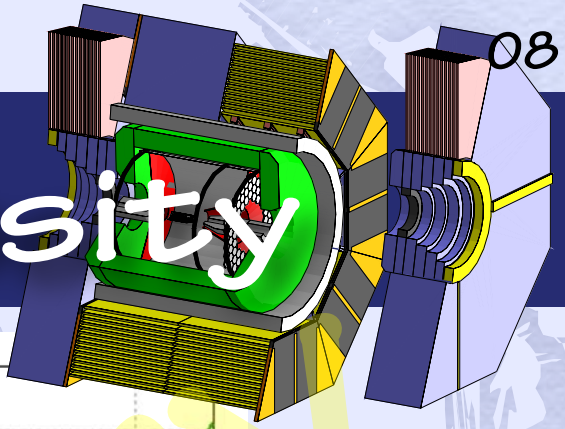
Summary of KEK Roadmap

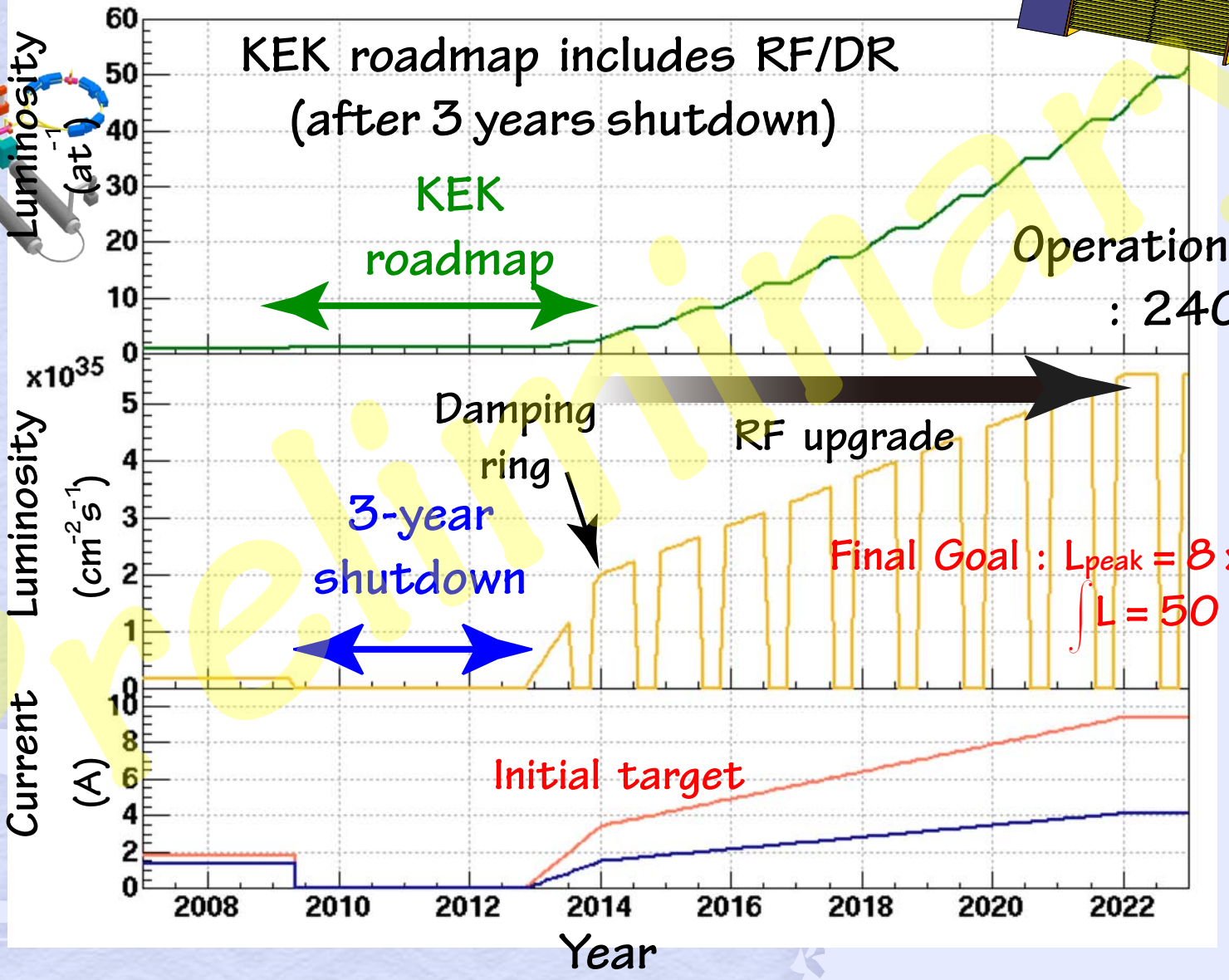


A.Suzuki
July,4,2008

Projected Luminosity







Upgrade Strategy

For commencement of operation on 2012,

schedule is so tight !

We decided to upgrade the detector in two steps

Baseline design	LoI design
From the beginning up to 2×10^{35} cm^{-2} s^{-1} (~2014?) (For Initial target)	after a few years operation ~ 8×10^{35} cm^{-2} s^{-1} (to the end?) (For Final goal)
6-layer strip-type	2-layer pixel-type + 4-layer strip-type
1.5 cm radius beam pipe	1.0 cm radius beam pipe

Requirement for "Baseline"

(1.5cm radius beam pipe + 6-layer SVD)

For trigger rate

. ~10kHz (c.f. ~400Hz @ Belle)

For inner layers

. better vertex resolution (at least, SVD2 performance should be kept)

$\sigma_{\Delta z} < 100\ \mu m$

. beam BG tolerant

x 15 BG is expected

@ $2 \times 10^{35} cm^{-2} s^{-1}$

SVD2 Occupancy(%)

	L1	L2	L3	L4
SVD2	10	3	1	1

VA1TA(Tp=800nsec)

For outer layers

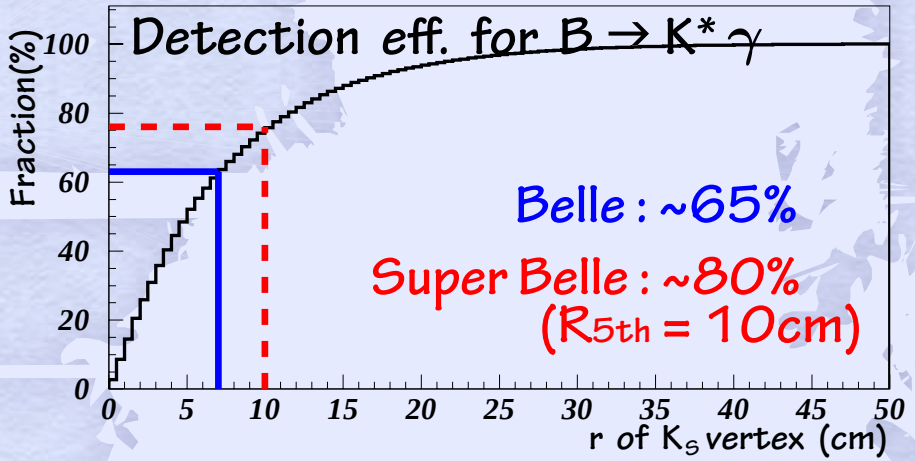
. better detection eff. for $B \to K^* \gamma$

. S/N ratio

. Readout pitch

. Material thickness

. Slanted sensors



Readout Chip for inners

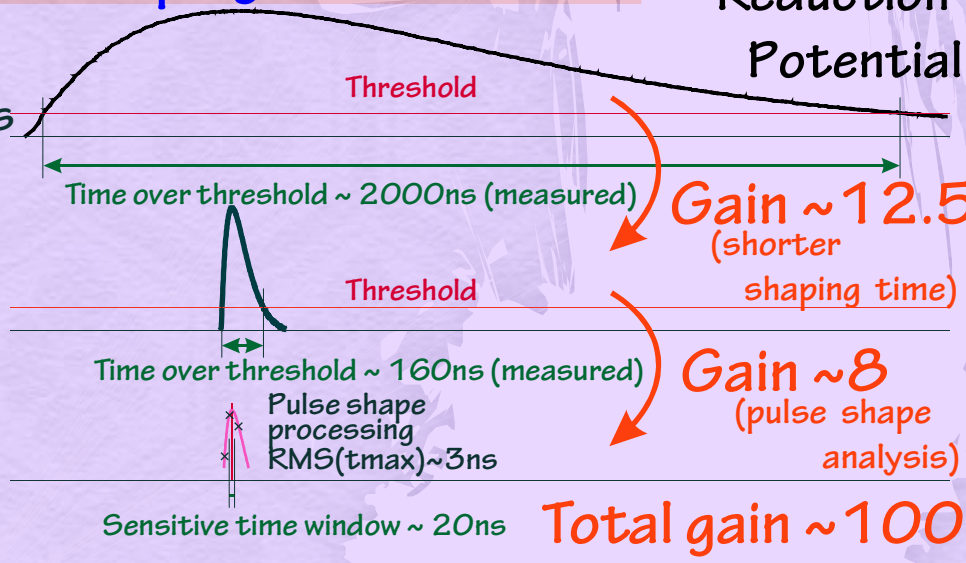
High trigger rate (~10kHz) : Pipeline readout

beam BG tolerant (x15 BG) : Shorter shaping time

Occupancy Reduction Potential

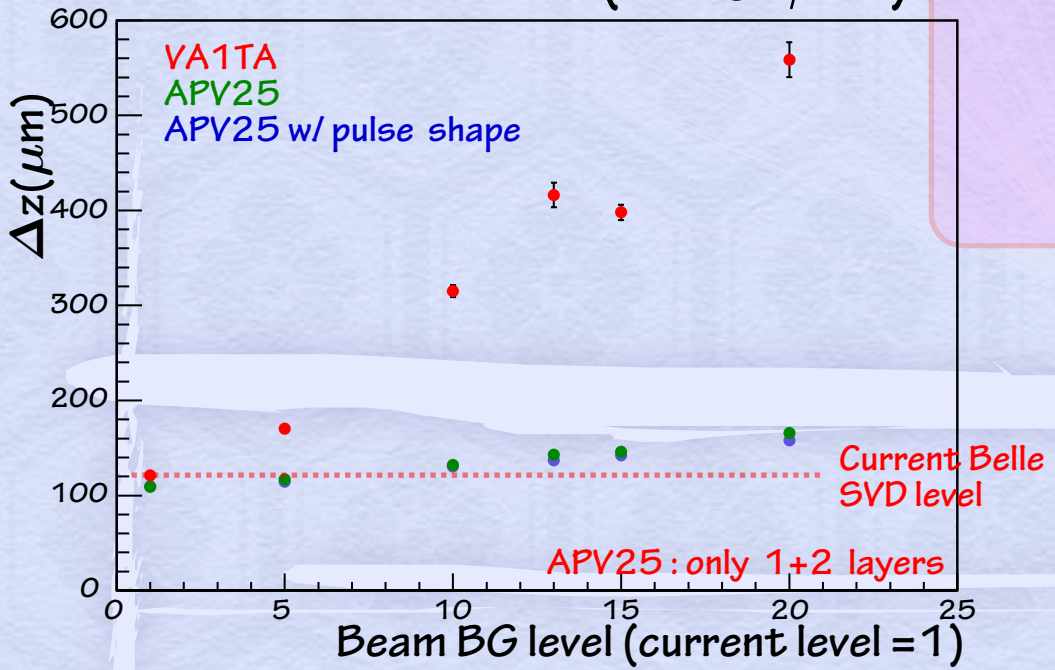
VA1TA
Tp~800ns

APV25
Tp~50ns



But, Data size ↑↑

Δz vertex resolution (B → J/ψ Ks)



APV25 is applicable to Super Belle !

S/N gets worse by a factor ~4
but, not critical for inner layer

(VA1TA : ~35)

Inner Layers

A study report "http://belle.kek.jp/~ushiroda/sbelle/StudyReport2008/draft/" will be released soon!

To achieve better vertex resolution → $\sigma_{\Delta z} <\sim 100\ \mu m$

Innermost layer should be located as close to the beam pipe as possible

Innermost layer should be operable under harsh beam background (x15 higher BG than Belle)

High trigger rate (~10kHz)

Shorter shaping time

Pipeline readout

VA1 → APV25 equivalent chip, S/N gets worse

~10% Occ. (inner) for Belle VA1

~35 (inner), ~16 (outer) for Belle VA1

APV25 : ~4times worse

but DSSD + APV25 can be used

VA1 → APV25 is the key

Readout Chip for outers

High trigger rate (~10kHz) : Pipeline readout → APV25

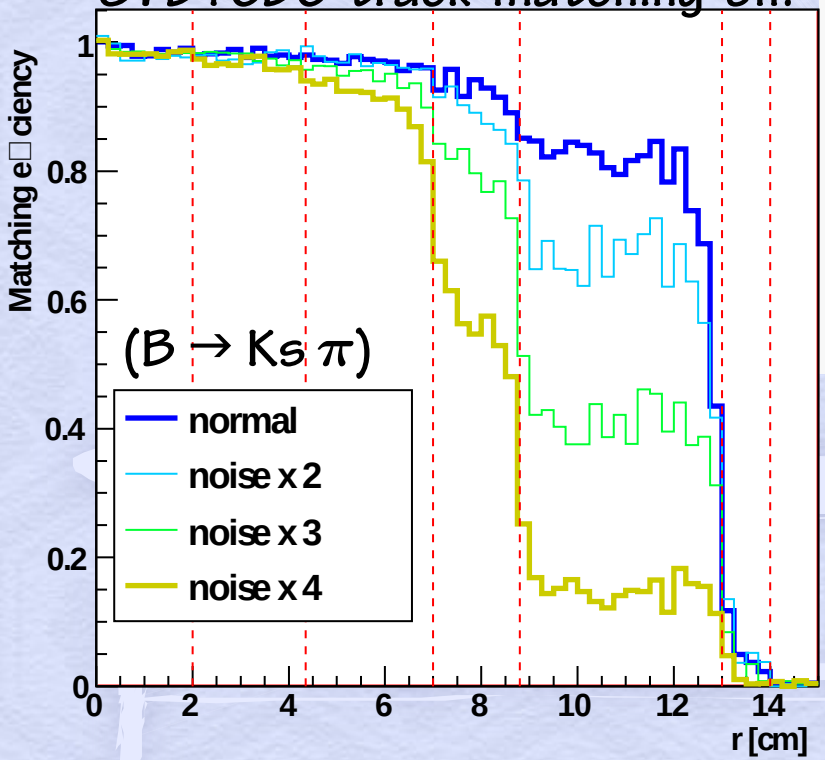
beam BG tolerant : Shorter shaping time is preferred, but not critical

longer sensor + APV25 → worse S/N (VA1TA ~16 for outer layer)

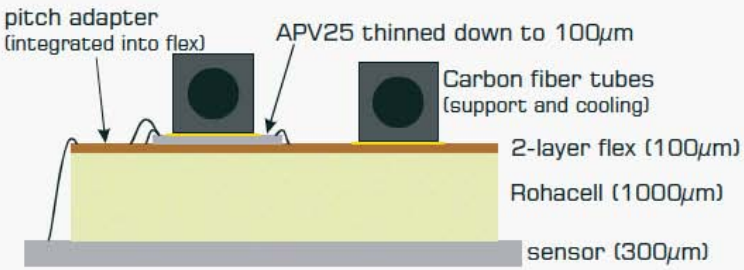
R=16cm

$17° < \theta < 150°$

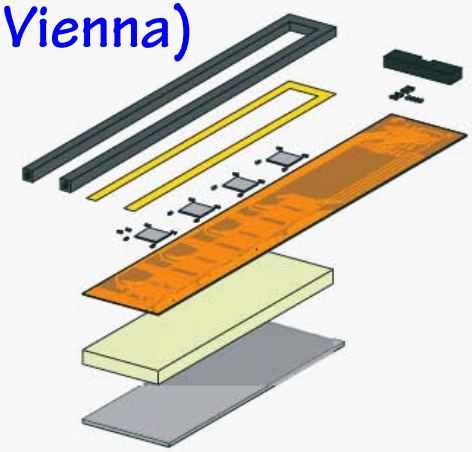
SVD+CDC track matching eff.



Chip-on-Sensor (proposed by Vienna)



(Drawings not to scale)



Outer Layers

A study report "http://belle.kek.jp/~ushiroda/sbelle/StudyReport2008/draft/" will be released soon!

High trigger rate (~10kHz)

↓

Pipeline readout is needed

"APV25"

To increase the eff. for $B \to K^*\gamma$

↓

SVD should be expanded in the radial direction

R=16cm

(sensor woudl be longer to keep the same acceptance)

$17° < \theta < 150°$

channel increases

↓

Slanted sensor (not yet optimized)

wider pitch (unacceptable)

S/N gets worse

↓

CDC+SVD matching eff. gets worse

($B \to K^* \gamma$ eff. decreases)

↓

To make S/N better, chip-on-sensor is proposed

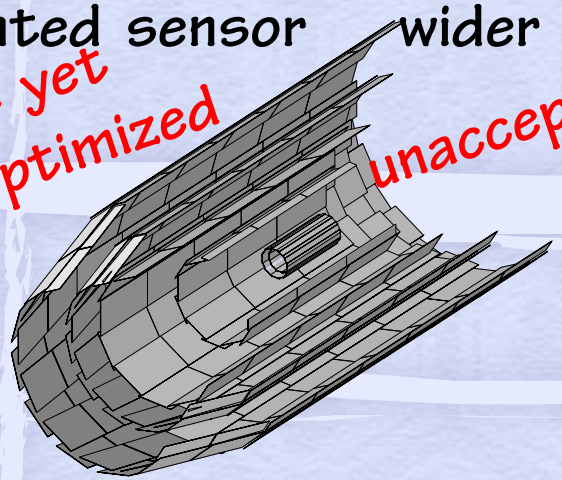
↓

Material increases

↓

vertex resolution for $B \to K^*\gamma$ gets worse

Unavoidable



Hurdles we face

. DSSD sensors from HPK (Hamamatsu)

HPK stopped the DSSD production !!

. Micron → Several samples in hands.
. Kyungpook → DC coupled DSSD was produced.
Test in progress.
. Tata → Waiting for the first test production.
Double-sided, double-metal and AC-coupled sensor
. Other vendors... Canberra, SINTEF ?

. # of readout chips will be >10 times larger than SVD2

Space for cables, repeaters and backend electronics.
Larger power supply, cooling system.

. Chip-on-sensor

leakage of coolant, system test, ...

Milestones

2008

Demonstrate APV25 readout chain

. Design optimization (Osaka, Niigata)

. APV25 front-end, repeater and FADC (Vienna)

. Data acquisition board : COPPER/FINNESE (Cracow)

DSSD test production

2009

Fix the design of Silicon Vertex Detector

Requirement for "LoI" design

(1.0cm radius beam pipe + 2-layer PXD + 4-layer SVD)

For trigger rate

. ~10kHz

For inner 2 layers

R_{bp} = 1.5cm → 1.0cm

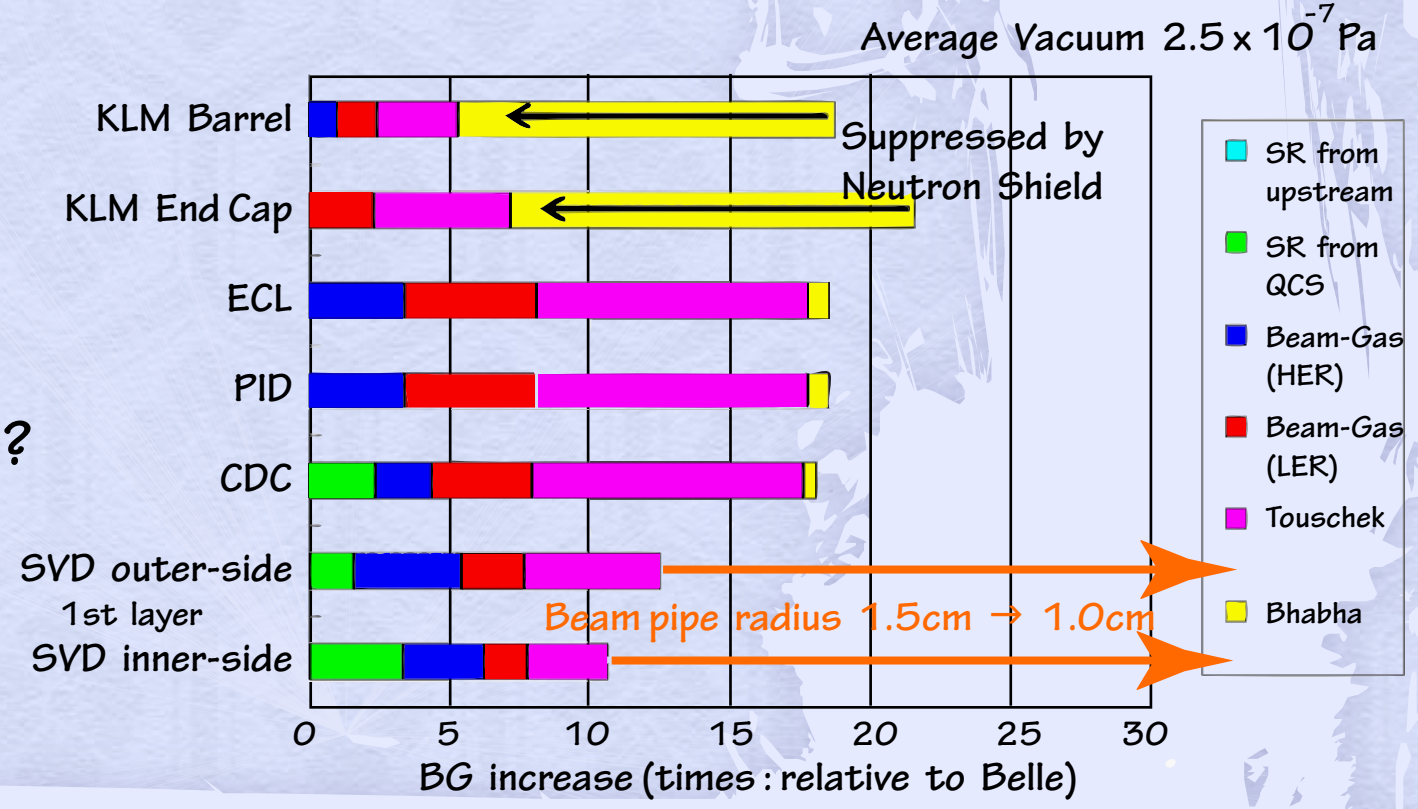
R_{1st} = 2.0cm → 1.3cm

x 33 BG is expected !?
(several MRad/yr)

@ 8×10^{35} cm^{-2} s^{-1}

. beam BG tolerant

. high occupancy

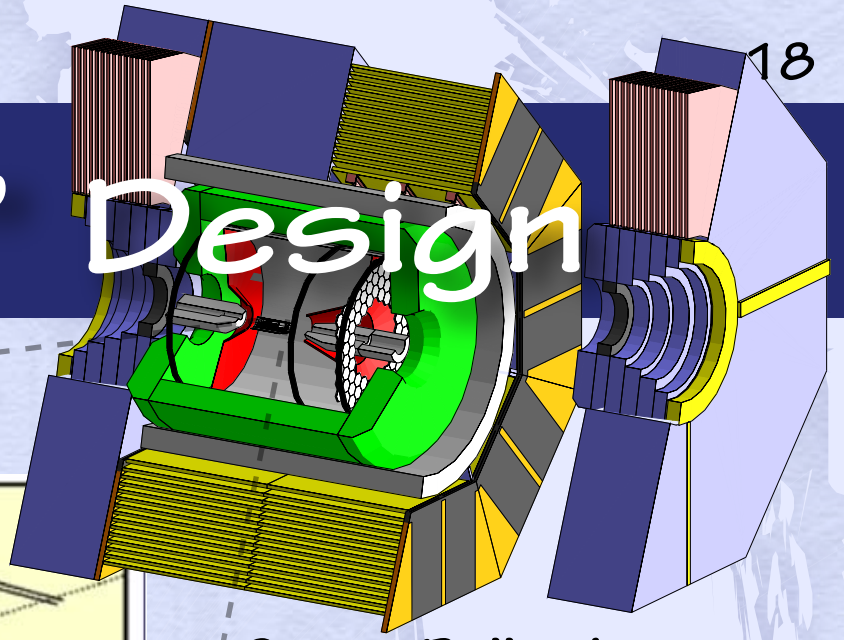


DSSD can not survive anymore ! → pixel-type

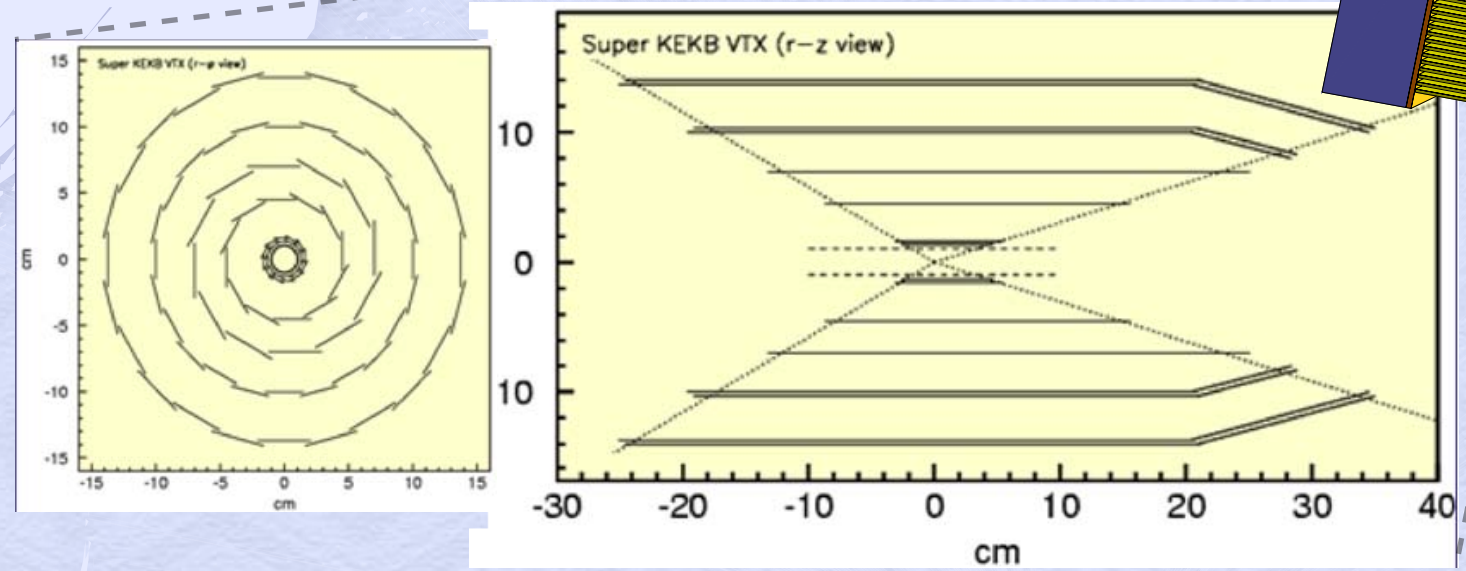
For outer 4 layers

DSSD w/ APV25 can still survive.

Tentative "LoI" Design



Super Belle detector



likewise as Baseline

. Acceptance : $17^\circ < \theta < 150^\circ$

. Radius (for better vertex resolution)

. Beam pipe = 10 mm

. Innermost = 13 mm

. Outermost = 150 mm

. 6-layer (2-lyr pixel + 4-lyr DSSD)

. Inclined sensors in Layer5 and 6

. reduce readout channels

. reduce material budget

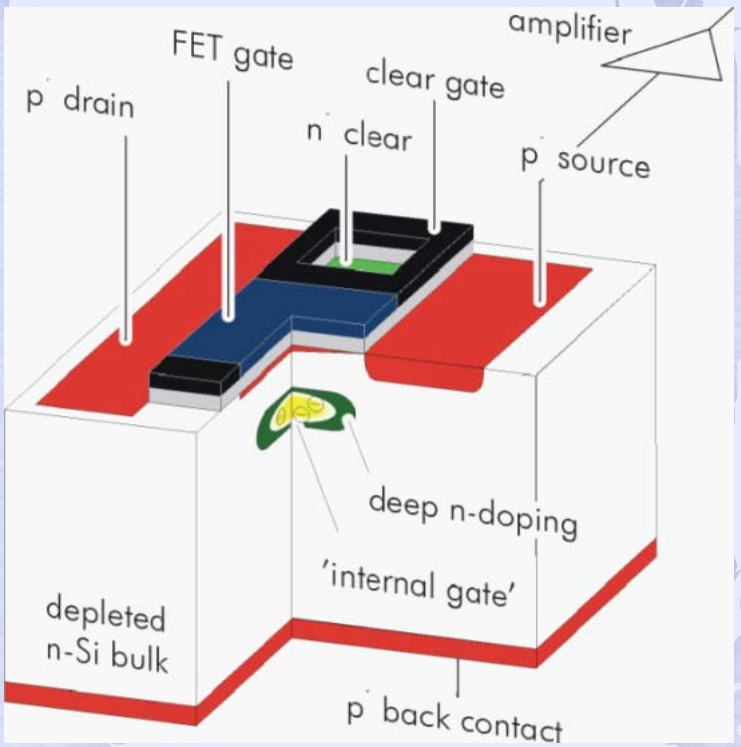
. reduce ladder length (w/o ~75cm)

. Technology options

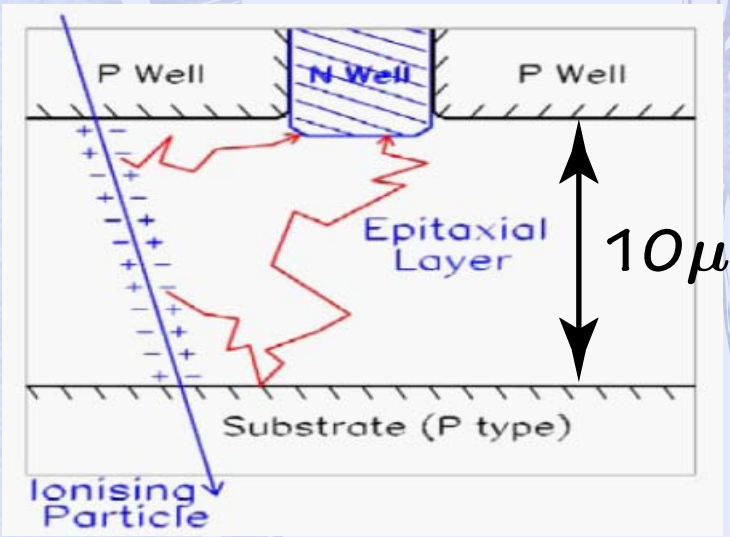
DEPFET / CMOS / SOI

DEPFET

. Intense R&D has been done for ILC pixel sensors
has been used in several experiments already!
. Technology is available in MPI only
. Sensor size is limited by wafer size
50 μm x 75 μm : 215 x 512 pixel (adjustable)
almost no gap in the acceptance
. Not very rad-hard (tested up to 1Mrad)
OK up to 8Mrad ??
. Small power consumption
. Reset switcher chip: Voltage swing > 8V
. Thickness 20μm ~ 100μm (adjustable for experiments)
. Doubly-correlated sampling can be done → low noise
. 10kHz trigger rate, 0-suppression, ~4pixels/hit, 32 bits/pixel includiing address
Disadvantage: ~1% inefficiency
. Data processing is done in subsequent chips
on repeater system or in backend system



CMOS pixel (CAPS/MAPS)



. The same technology as commercial CMOS cameras
  5-10M -pixel chips are in production
. Sensor size is limited by reticle size (21 x 21 mm^2)
  22.5 μm x 22.5 μm
  gap in the acceptance
. Intrinsic rad-hard (deep sub-micron technology)
  > 30 MRad
. Sensor is a thin epitaxial layer (5~10μm thick)
  signal si small → No problem as the detector capacitance is also small
  <= 50μm
. N-well is used to collect charge from the epitaxial layer
. 100kHz frame rate is achieved (132 x 48 pixel)
  Full-size detector (928 x 128 pixel)
  10kHz trigger rate ???

SOI

. Activity started as
one of KEK detector R&D project in 2005

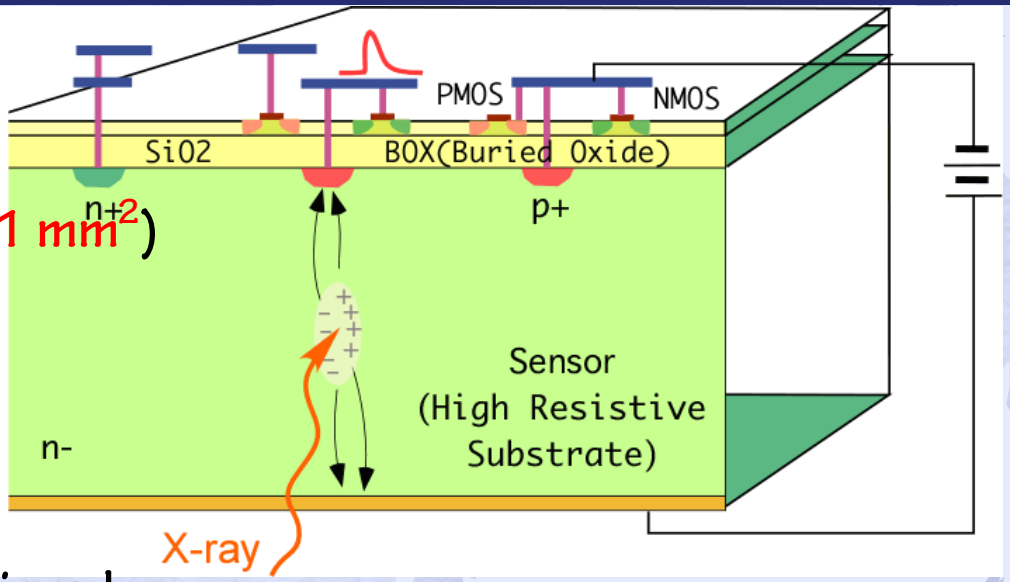
. Sensor size is limited by reticle size (21 x 21 mm^2)
20μm x 20μm : 128 x 128
gap in the acceptance

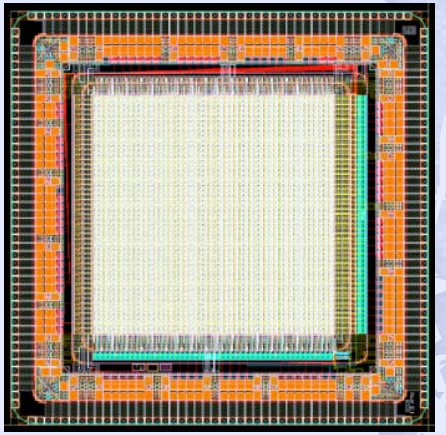
. rad-hard (deep 0.2 μm technology)
tested > 30 MRad

. Depletion depth of 50-100μm has been achieved
thinning after silicon process
<= 50μm

. Signal induced in the sensor can be processed by the CMOS circuit
Complex/rad-hard circuit can be made
DEPFET/CAP type readoout is also possible
10kHz trigger rate ???

. R&D in progress
Evaluation of Belle PIXEL chip will start soon
(pixel-shaper-discrimination-digital pipeline)





Technology options

	DEPFET	CMOS (CAPS/MAPS)	SOI
Material budget	20 ~ 100 μm (adjustable)	<~50 μm (sensitive area 5~10 μm)	50~100 μm (could be <~50 μm)
Size	limited by wafer (50×75 mm^2)	limited by reticle (21×21 mm^2)	limited by reticle (21×21 mm^2)
Power consumption	small (0.5w) (reset switcher chip : Voltage swing > 8V)	small	small
Rad.-hardness (3MRad/yr ?)	tested < 1MRad (up to 8MRad? : irradiation test)	intrinsic rad. hard (must be > 30MRad)	tested > 30MRad
10kHz trig. rate	estimated ~1% ineff.	? (CAP3 too slow)	not proved
Availability	MPI only (already used in other exp.)	R&D in progress	R&D in progress

One possible solution

(Subject to Optimization)

. improve $B \to K^*\gamma$ eff.

. perform self-tracking

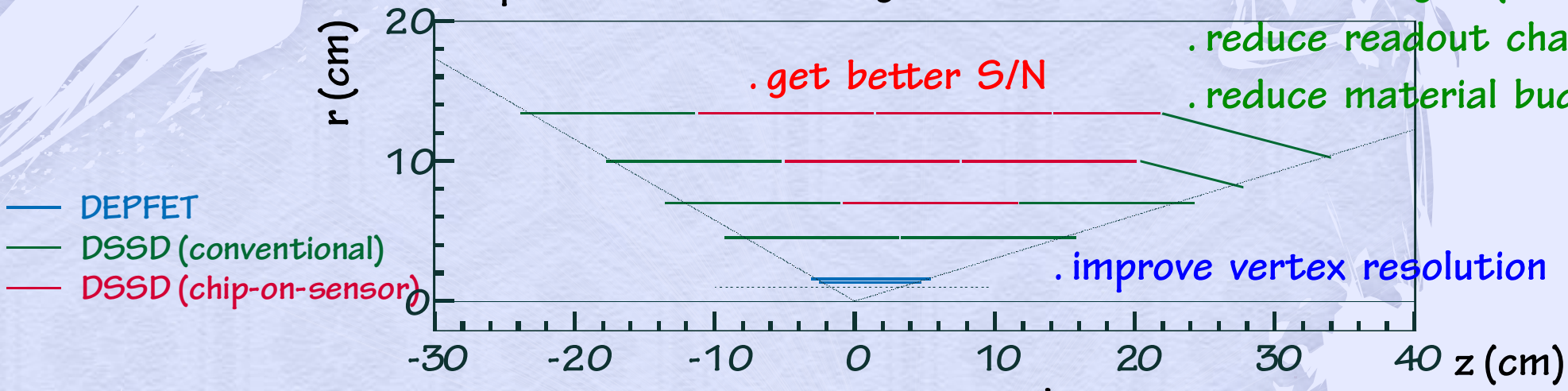
. reduce ladder length (w/o ~75cm)

. reduce readout channels

. reduce material budget

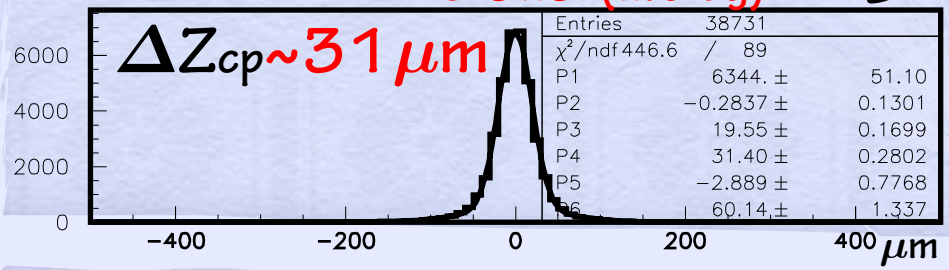
. get better S/N

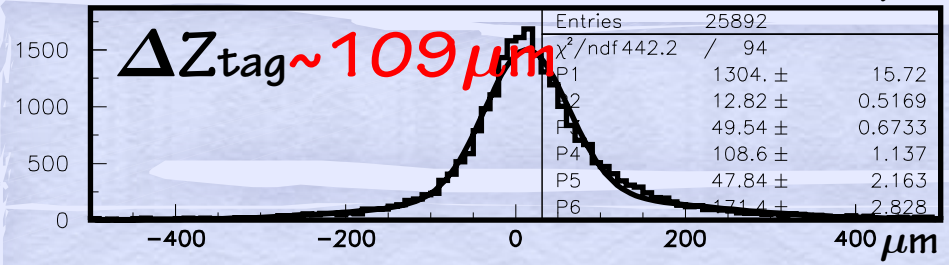
. improve vertex resolution



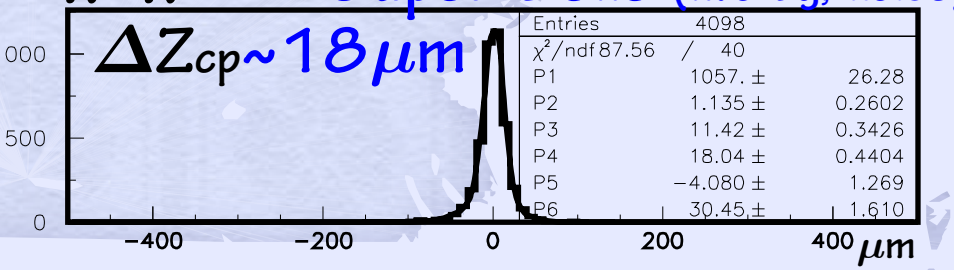
$B \to \pi^-\pi^+$

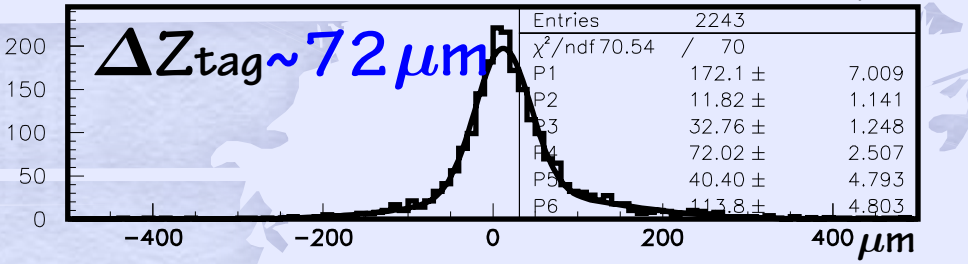
Belle (w/o bg)



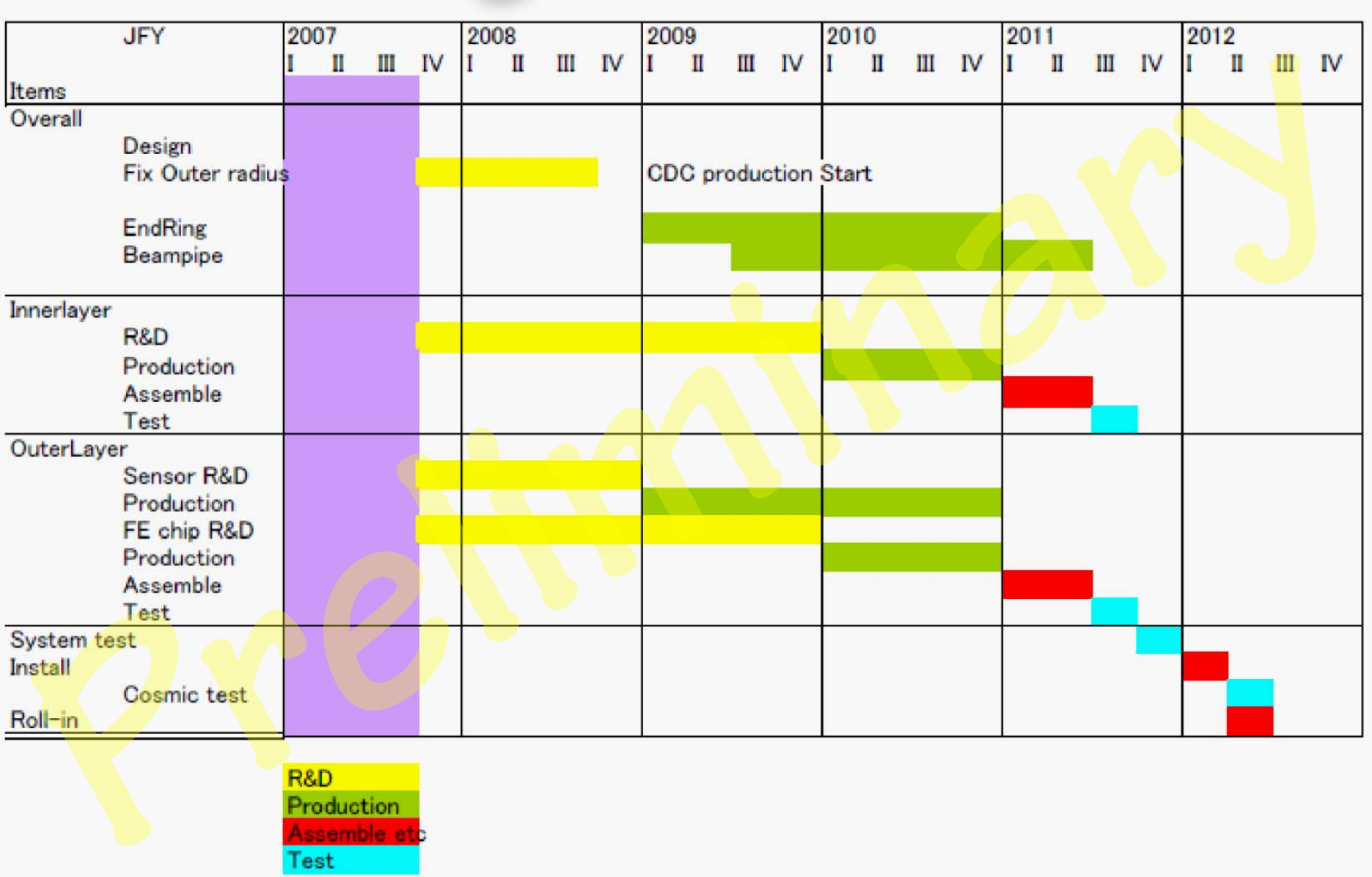


Super Belle (w/o bg, noise)





So Tight Schedule



Summary

For current SVD in Belle

. operated stably and efficienctly for almost ~5 years

. will continue in the next fiscal year (2009 : ~5 months : not fixed yet)

For "Baseline" design (for $2 \times 10^{35} cm^{-2} s^{-1}$ peak lum. : 2012 ~)

. optimization is still going on.

. high trigger rate (~10kHz)

. beam BG tolerant (x 15 BG is expected) } → APV25

can keep a SVD2-equivalent vertex resolution ($\sigma \Delta z < 100\ \mu m$)

. better detection eff. for $B \to K^* \gamma$ → realize a larger volume detector w/ chip-on-sensor for outer layers

. many hurdles, e.x. DSSD production, system test, tight schedule ...

For "LoI" design (for $8 \times 10^{35} cm^{-2} s^{-1}$ peak lum. : 2014 ~)

. concrete optimization has just started. (esp, for two inner layers)

. we have to determine which technology option we can use in real !

. again many hurdles, e.x. system test, tight schedule ...

Technology and Instrumentation in Particle Physics

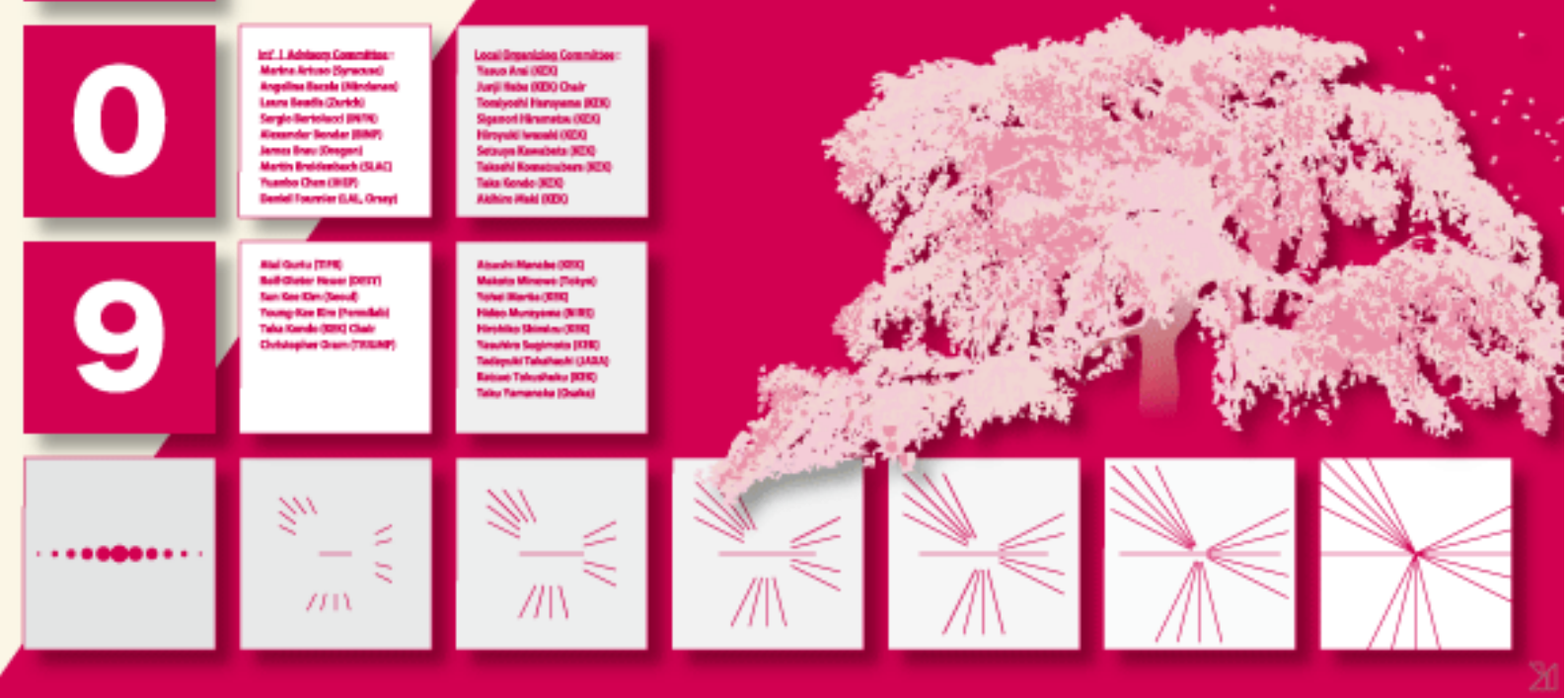
TIPP09

The 1st International Conference on
Technology and Instrumentation in Particle Physics

March 12-17, 2009

Tsukuba, Japan

http://tipp09.kek.jp



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— Topics —

- Gaseous/liquid detectors
- Semi-conductor detectors
- Trigger & data aquisition systems
- Accelerator and beam instrumentation
- Experimental detector system
- Calorimeters
- Particle identification and photon detectors
- Instruments for non-accelerator physics
- Astrophysics and space instrumentation
- Front-end electronics