Fermilab

Vertical Integration of Integrated Circuits and Pixel Detectors

Grzegorz DEPTUCH

Fermi National Accelerator Laboratory, Batavia, IL, USA

on behalf of the FERMILAB ASIC design group:

R. Yarema Idr.,

G.Deptuch, J.Hoff, A.Shenai, M.Trimpl, T.Zimmerman

and:

M.Demarteau, R.Lipton, M.Turqueti, R.Rivera and others

- **focus of this presentation is**
  1) **introduction to 3D integration technology**
  2) ***design of first 3D integrated device for HEP (including results)***
  3) ***discussion***

email: deptuch@ieee.org

Fermilab

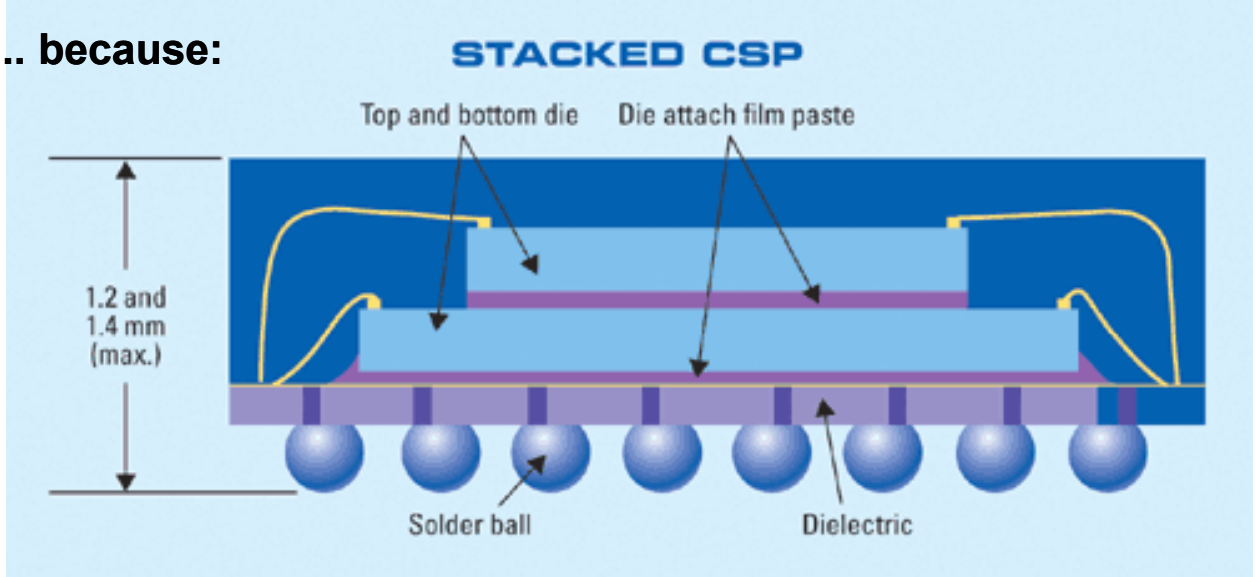
Is 3D (vertical integration) new?

- For decades, semiconductor manufacturers have been shrinking transistors sizes in ICs to achieve the yearly increases in speed and performance described by Moore's Law (chip performance will double every ~18 months)
  - Moore's Law exists only because the RC delay has been negligible in comparison with signal propagation delay. It turns ou that for submicron technology, RC delay becomes a dominant factor! (the change to Cu interconnects, low-k ILDs and CMP is not giving answer to the questions: how to reduce RCs?)

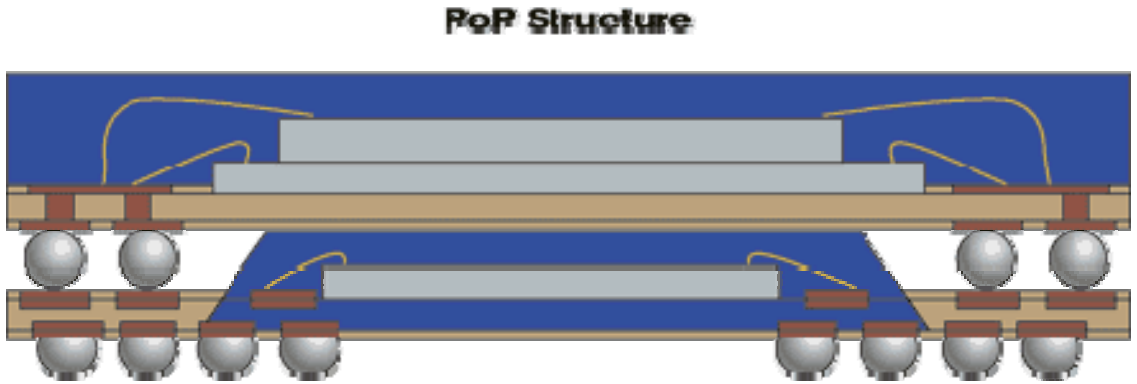
Fermilab

Is 3D (vertical integration) new?

- not really... because:



Stacked CSP – stacked chip-scale package **(example source: Amkor)**



1. A typical three-chip PoP solution.

PoP – Package-on-package **(example source: Amkor)**

Fermilab

Is 3D (vertical integration) new?

3D-TSV – 3D Through Silicon Via

3D integration is undergoing evolutionary change from peripheral vertical connectivity involving bonding pads to the interconnectivity at the block, gate or even transitor level

- **reduced interconnect delays, higher clock rates,**
- **reduced interconnect capacitance, lower power dissipation,**
- **higher integration density,**
- **high badwidth μ-processors**
- **merging different process technologies, mixed materials, system integration,**
- **advanced focal planes**

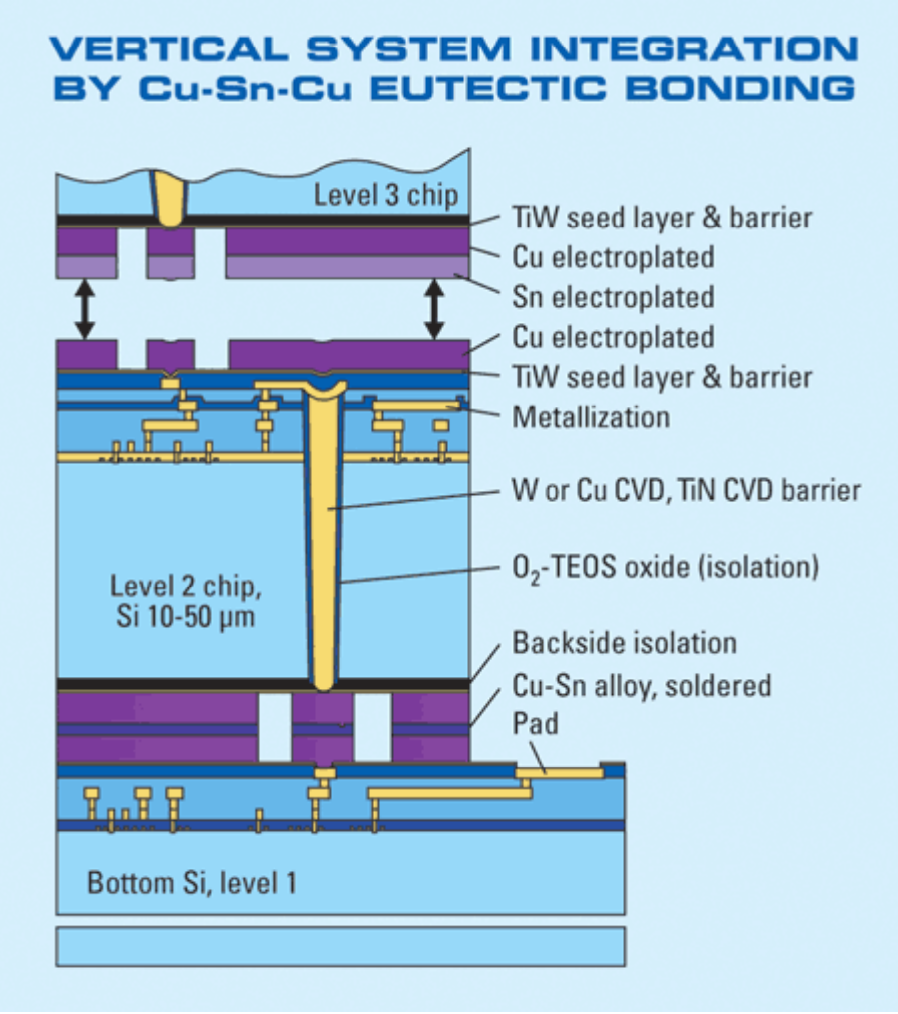


Illustration TSV with 3D stack mounting using direct bonding technique
(example source: Fraunhofer-Munich)

Fermilab

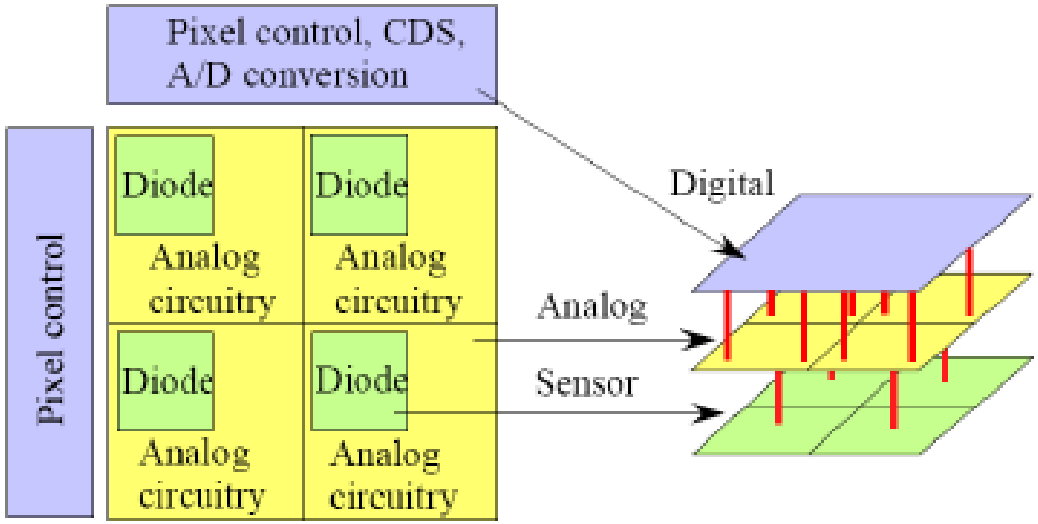
Challenges for 3D-TSV technology:

3D-TSV will be adopted , but to what extend and how quickly depends on:

- **Commercial availability of EDA tools and design methodologies,**
- **Thermal concerns caused by the increased power densities,**
- **Vendor adoption of TSV technology**
  - **Via first - foundries**
  - **Via last - 3rd party vendors**
- **Testability methods, known good die are availability**

Fermilab

What 3D-TSV mean for pixel designs:



Conventional MAPS 4 Pixel Layout

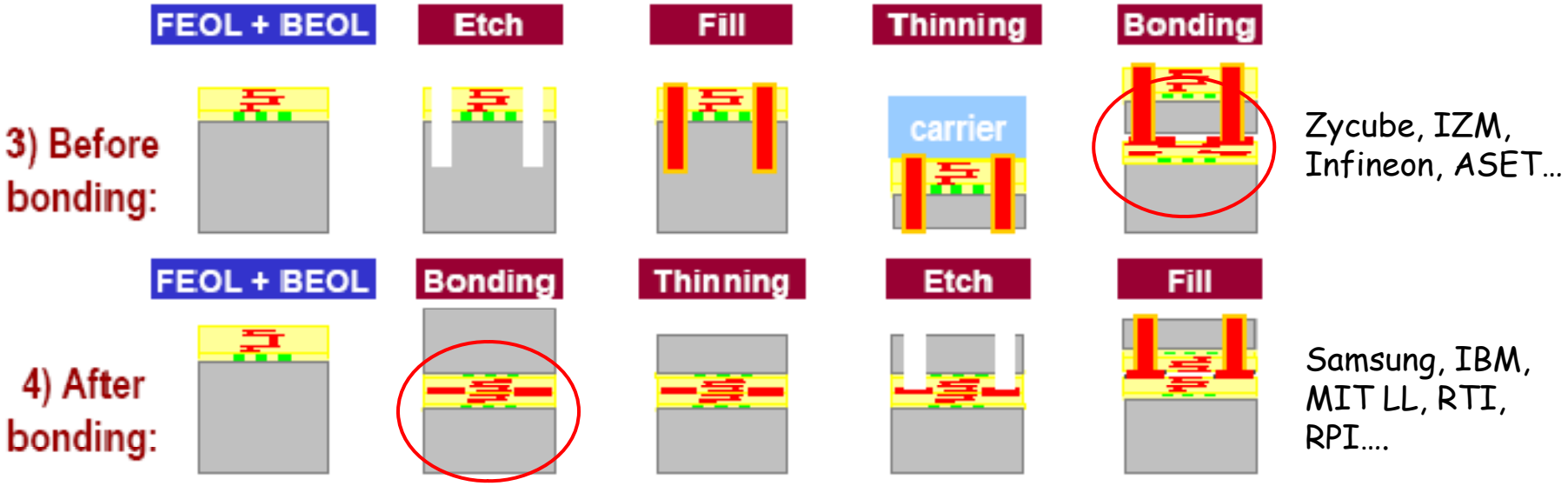
3D 4 Pixel Layout

Fermilab

When 3D-TSV are inserted in the fabrication:

VIA LAST

approach occurs after wafer fabrication and either before or after wafer bonding



Notes: Vias take space away from all metal layers. The assembly process is streamlined if you don't use a carrier wafer.

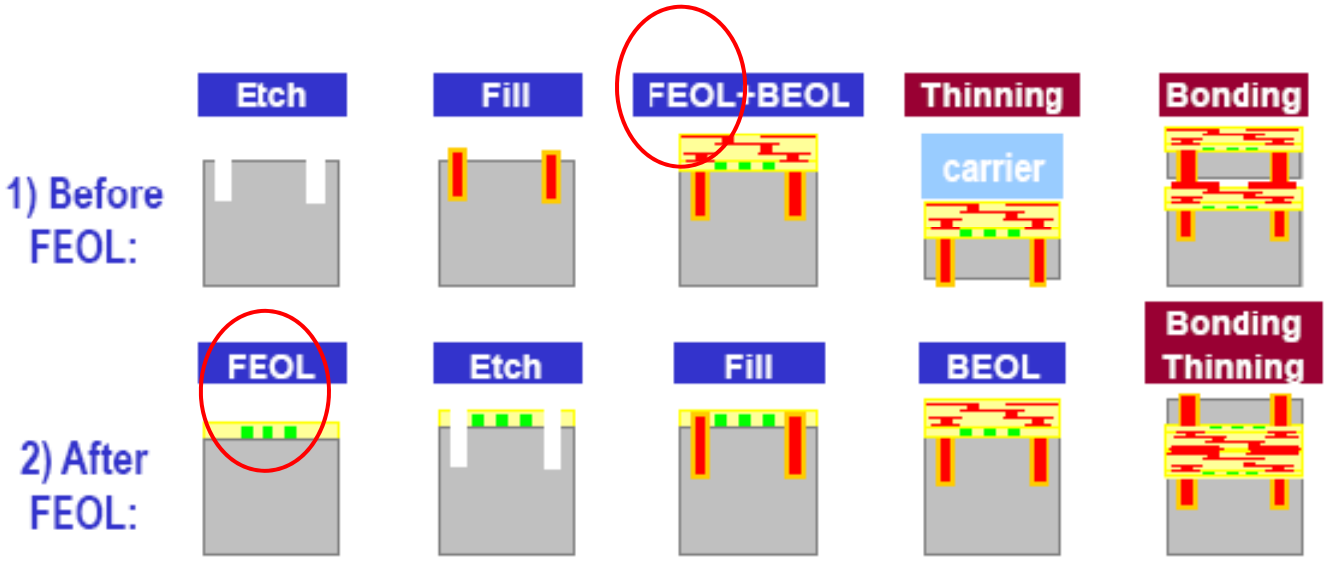
Basically wafers from different processes/vendors could be used as via creation is a postprocessing operation.

Fermilab

When 3D-TSV are inserted in the fabrication:

VIA FIRST

formation is done either before or after CMOS devices processing; is part of the process done on the production line



IBM, NEC, Elpida, OKI, Tohoku, DALSA….

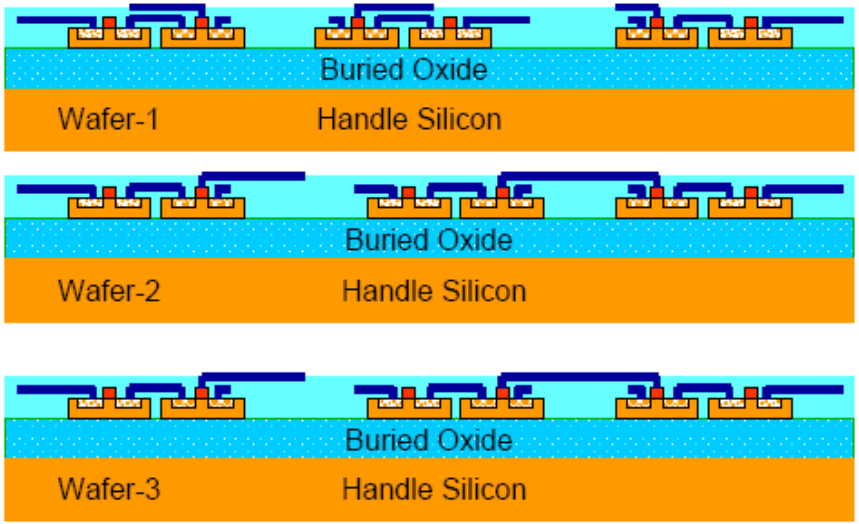
Tezzaron, Ziptronix Chartered, TSMC, RPI, IMEC……..

Fermilab

MITLL 3DM2 vertical integration process flow (VIA LAST):

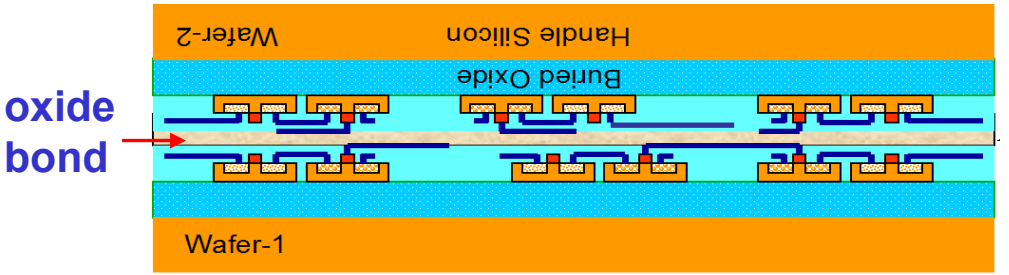
- 3 tier chip; 3DM2 includes 2 *"digital"* 180-nm FDSOI CMOS tiers and 1 RF 180-nm FDSOI CMOS tier
- 11 metal layers including: 2-µm-thick RF backmetal, Tier-2 backmetal

Step 1: Fabricate individual tiers

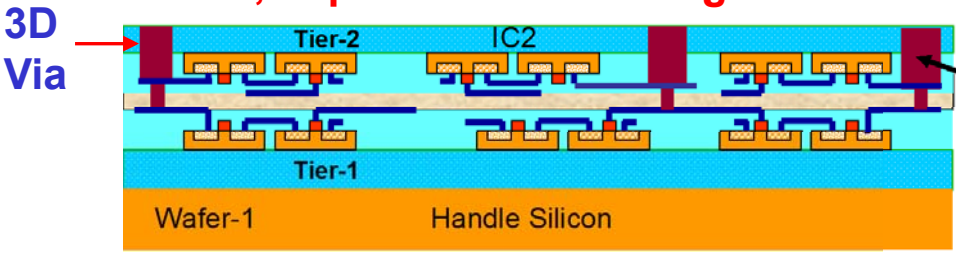


In principle wafer 1 could also be bulk

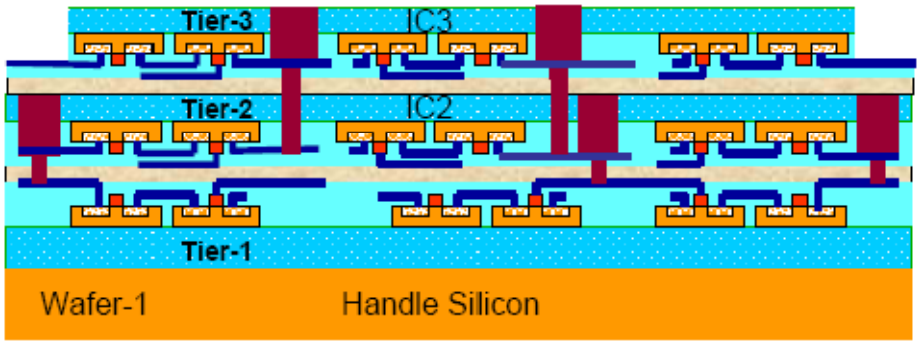
Step2: Invert, align, and bond wafer 2 to wafer 1



Step 3: Remove handle silicon from wafer 2, etch 3D Vias, deposit and CMP tungsten



Step 4: Invert, align and bond wafer 3 to wafer 2/1, remove wafer 3 handle wafer, form 3D vias from tier 2 to tier 3, etch bond pads

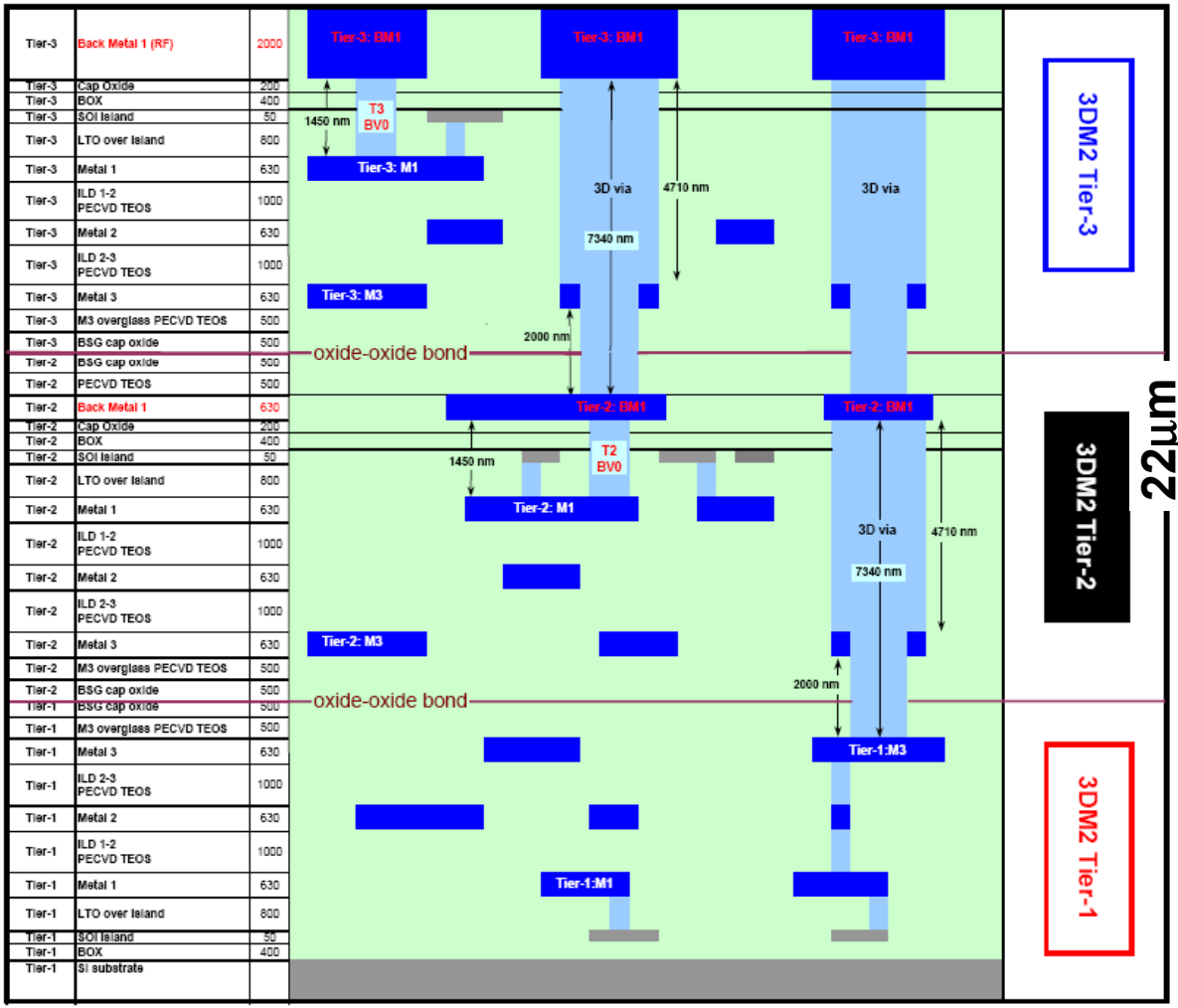


Fermilab

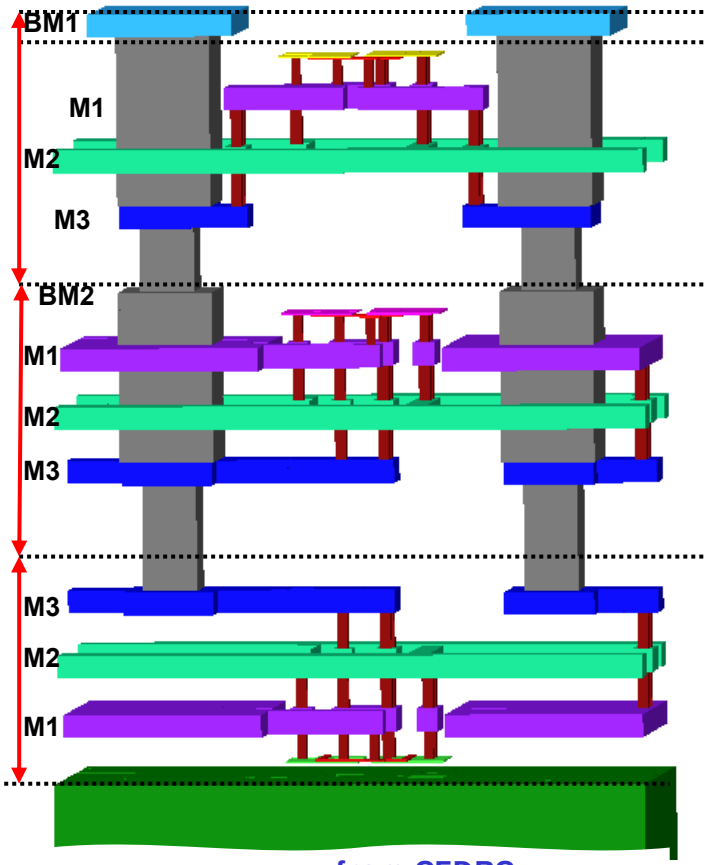
Description of the MITLL 3DM2 process:

MIT-LL 3D IC Technology (SOI) - Layer Description

Tier-3	Back Metal 1 (RF)	2000
Tier-3	Cap Oxide	200
Tier-3	BOX	400
Tier-3	SOI Island	50
Tier-3	LTO over Island	800
Tier-3	Metal 1	630
Tier-3	ILD 1-2 PECVD TEOS	1000
Tier-3	Metal 2	630
Tier-3	ILD 2-3 PECVD TEOS	1000
Tier-3	Metal 3	630
Tier-3	M3 overglass PECVD TEOS	500
Tier-3	BSG cap oxide	500
Tier-2	BSG cap oxide	500
Tier-2	PECVD TEOS	500
Tier-2	Back Metal 1	630
Tier-2	Cap Oxide	200
Tier-2	BOX	400
Tier-2	SOI Island	50
Tier-2	LTO over Island	800
Tier-2	Metal 1	630
Tier-2	ILD 1-2 PECVD TEOS	1000
Tier-2	Metal 2	630
Tier-2	ILD 2-3 PECVD TEOS	1000
Tier-2	Metal 3	630
Tier-2	M3 overglass PECVD TEOS	500
Tier-2	BSG cap oxide	500
Tier-1	BSG cap oxide	500
Tier-1	M3 overglass PECVD TEOS	500
Tier-1	Metal 3	630
Tier-1	ILD 2-3 PECVD TEOS	1000
Tier-1	Metal 2	630
Tier-1	ILD 1-2 PECVD TEOS	1000
Tier-1	Metal 1	630
Tier-1	LTO over Island	800
Tier-1	SOI Island	50
Tier-1	BOX	400
Tier-1	SI substrate	



CFDRC Full 3D Model with active elements in all layers



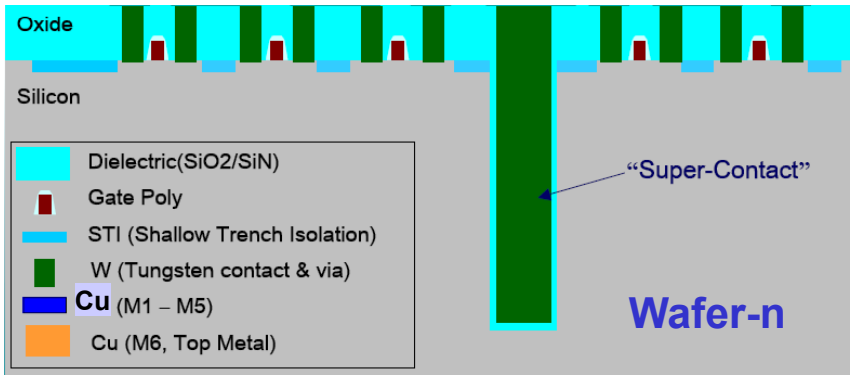
from CFDRC

Fermilab

Tezzaron vertical integration process flow (VIA FIRST):

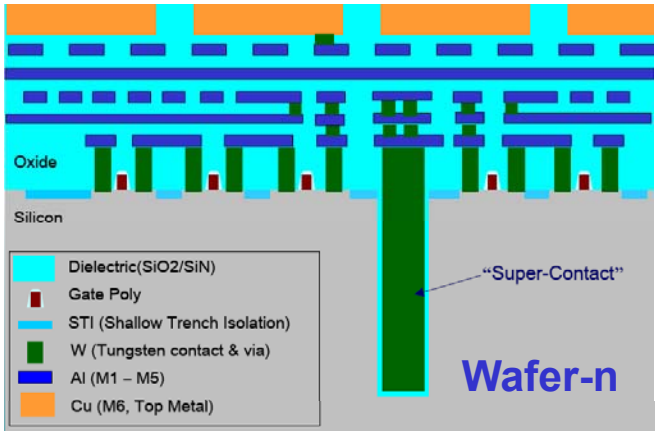
- multi-tier tier chip; Tezzaron includes standard CMOS process by Chartered Semiconductor, Singapore.

Step 1: Fabricate individual tiers; on all wafers to be stacked: complete transistor fabrication, form super via Fill super via at same time connections are made to transistors

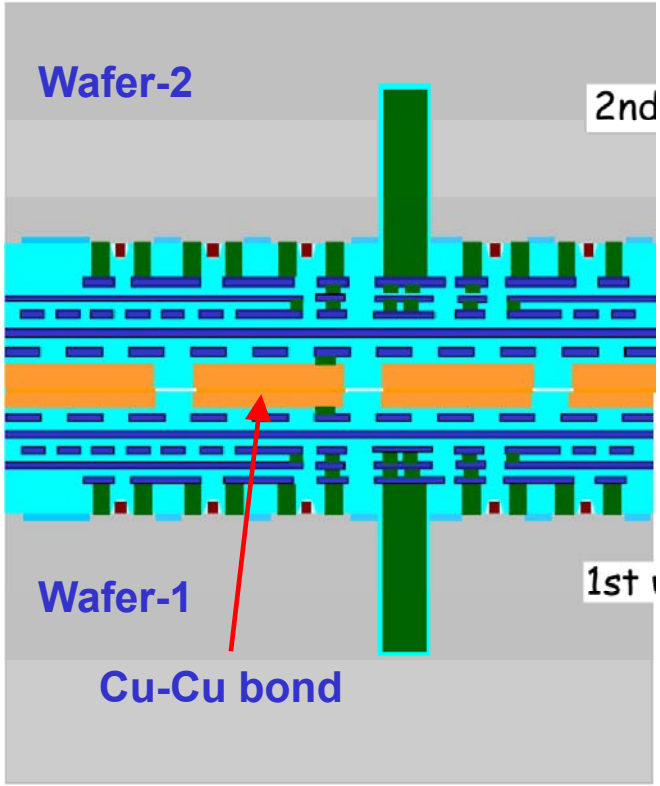


All wafers are bulk

Step2: Complete back end of line (BEOL) process by adding Al metal layers and top Cu metal (0.7 μm)



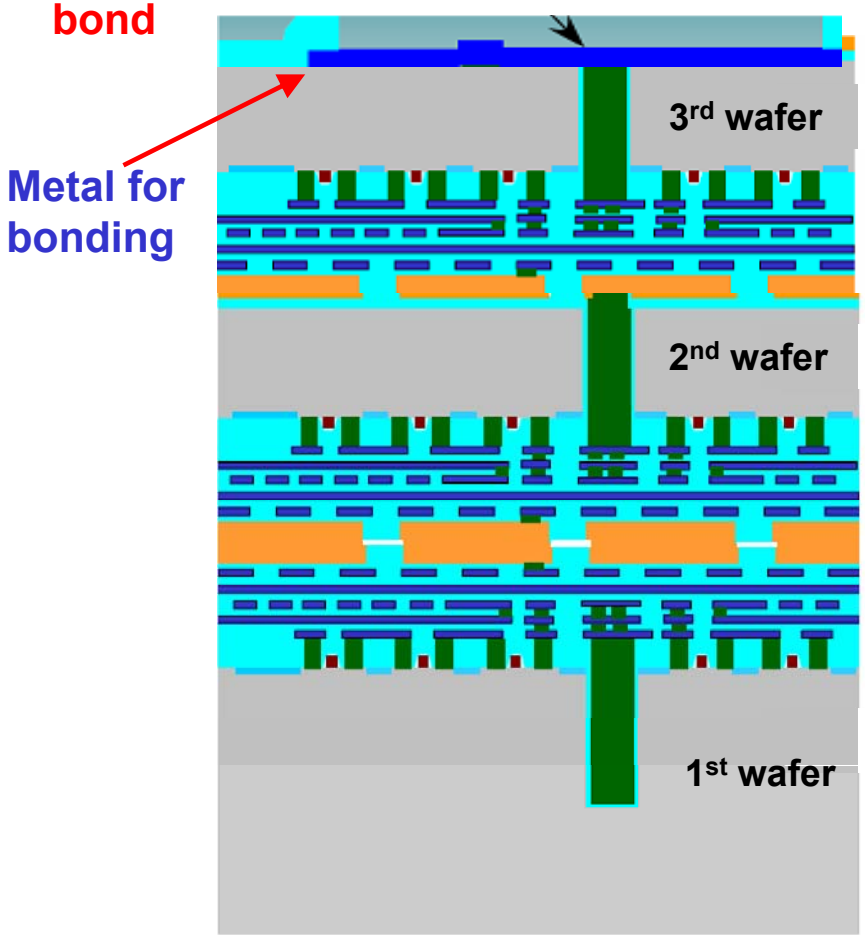
Step 3: Bond wafer-2 to first wafer-1 Cu-Cu thermo-compression bond

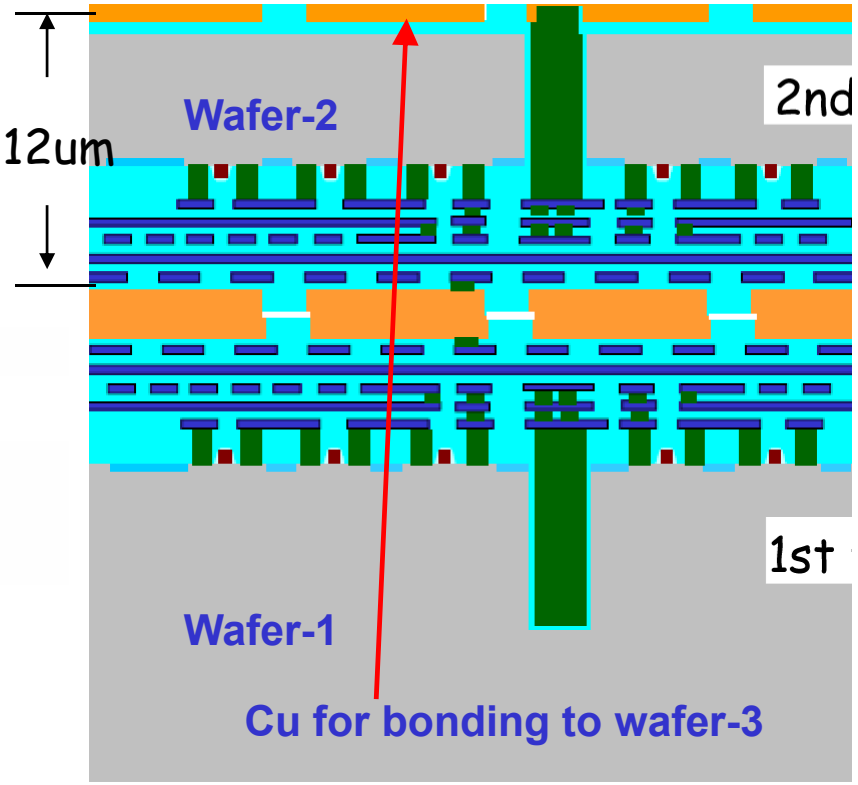


Fermilab

Tezzaron vertical integration process flow:

Step 4: Thin the wafer-2 to about 12 um to expose super via. Add Cu to back of wafer-2 to bond wafer-2 to wafer-3
OR stop stacking now! add metallization on back of wafer-2 for bump bond or wire bond





Step 5: Stack wafer-3, thin wafer-3 (course and fine fine grind to 20 um and finish with CMP to expose W filled vias) Add final passivation and metal for bond pads

Fermilab

3D-Integration activities at FERMILAB

- **FERMILAB work on vertical integration technologies started in 2006.**
- **Efforts include:**
  - **design of 3D integrated circuit exploitng 3D TSV,**
  - **wafer thinning and investigations of interconnectivity RO/detector (low profile, low material budget, high density, interconnects),**
  - **design of monolithic detector/readout systems in SoI on HR handle wafer.**
- **3D - integration related work:**
  - **design of 3D integrated readout circuit with architecure for ILC *(VIP vertically integrated pixel) in 0.18 μm MITLL 3DM2 process (Oct. 2006) – tests performed,***
  - **new VIP2, *0.15 μm MITLL 3DM3 process (tape out Sept. 30 2008)***
  - **new 3D design exploring commercial 3D integration technology by Tezzaron *built on Chartered Sem. 0.13 μm CMOS process – FERMILAB hosts MPW (reticle shared between interested users)***
  - ***wafer thinning and laser annealing for low material budget detectors – underway with different vendors (IZM, RTI, Ziptronix, MITLL),***
  - ***investigation of low mass, high density bonding.***

Fermilab

VIP: floorplan

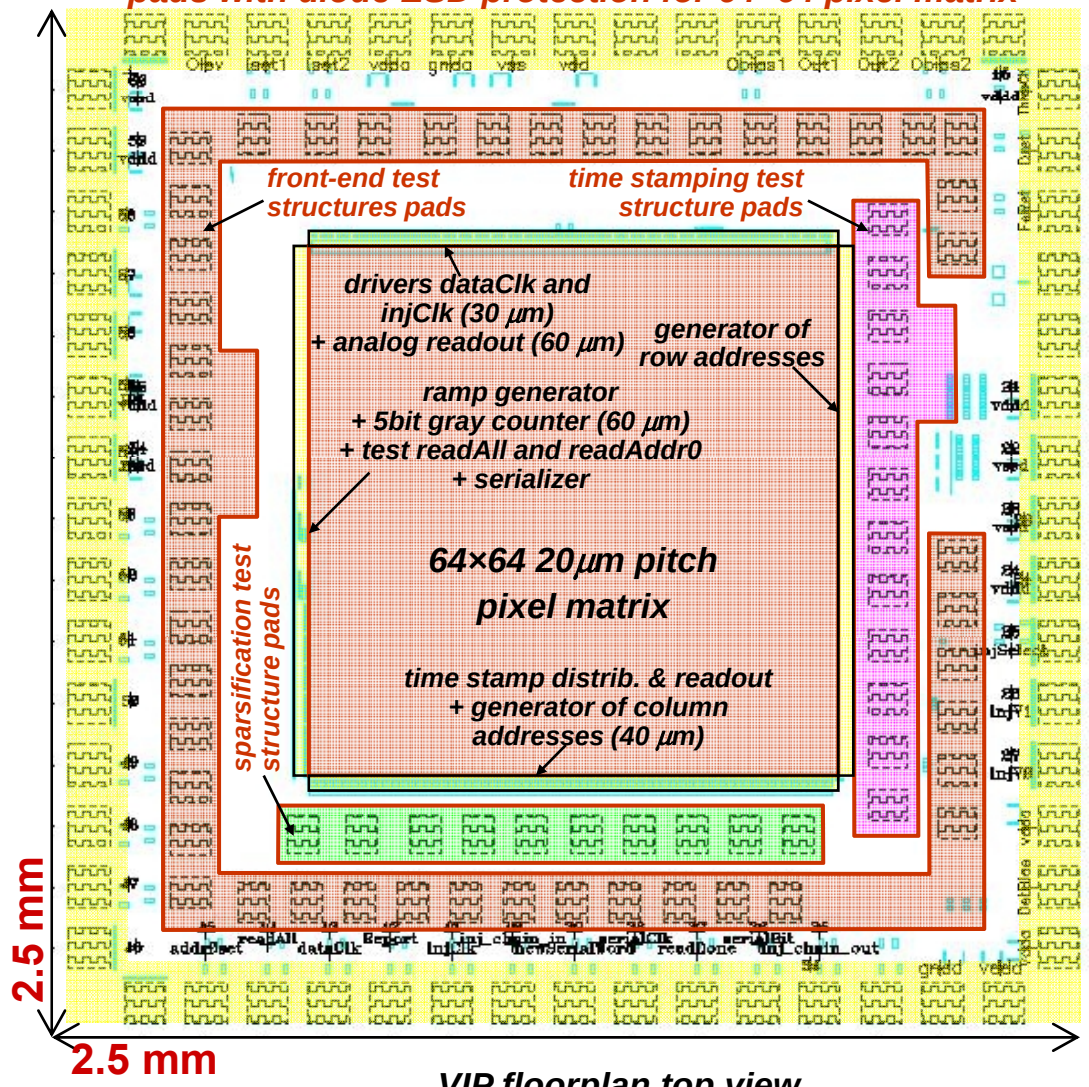
VIP = Vertically Integrated Pixel
64×64 20mm² pixel prototype

- **fully functional matrix of 64×64 pixels including zero suppresed readout,**
- **single pixel test structures, placed on corresponding layers using internal ring of pads, reduced, or NO ESD protection.**

Tests accomplished recently

Yield problems faced in tests – looks like process problems – problems are not related to 3D integration but processing of individual layers

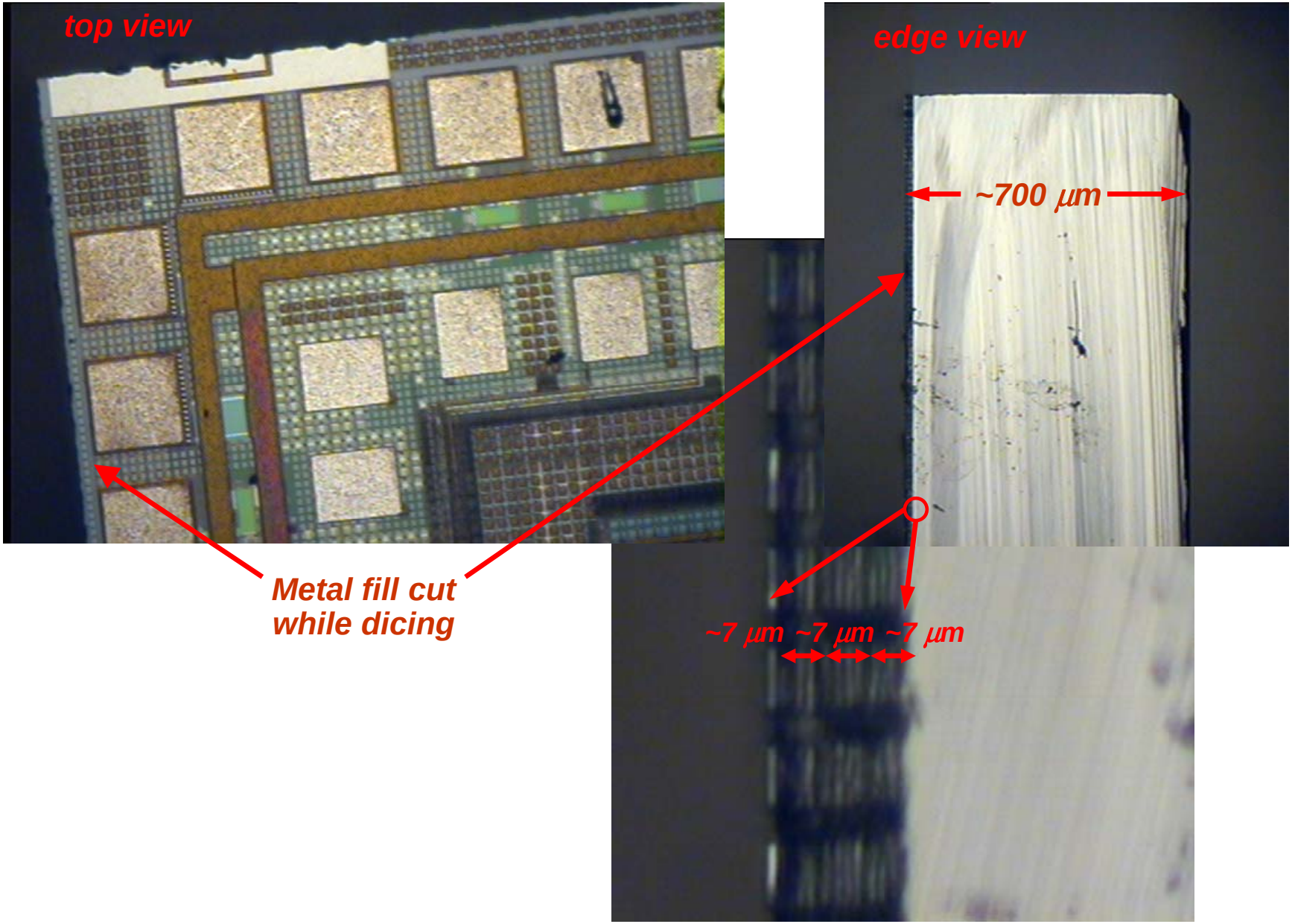
pads with diode ESD protection for 64×64 pixel matrix



VIP floorplan top view

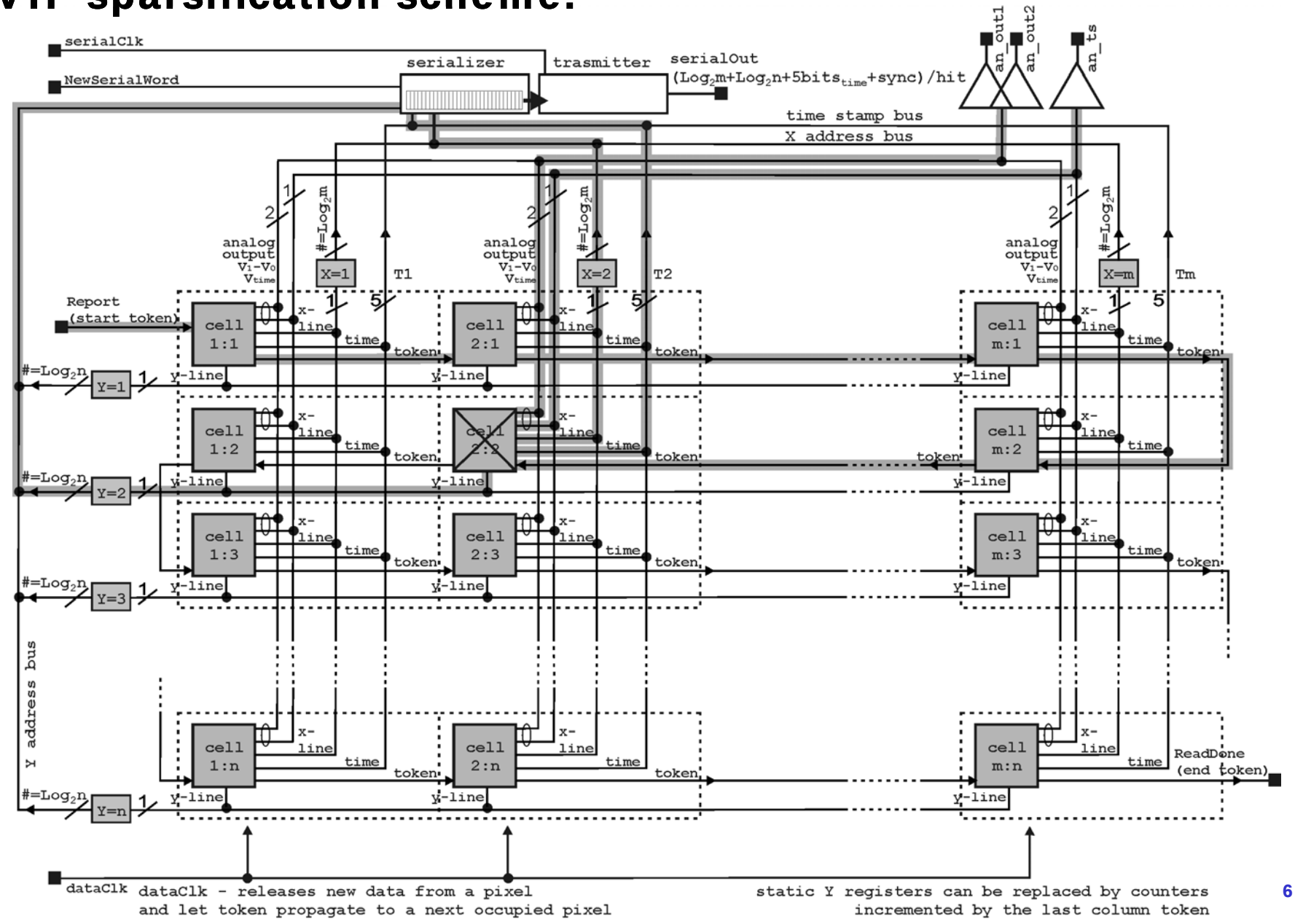
Fermilab

VIP:



Fermilab

VIP sparsification scheme:



Fermilab

VIP: distribution between layers

38 transistors

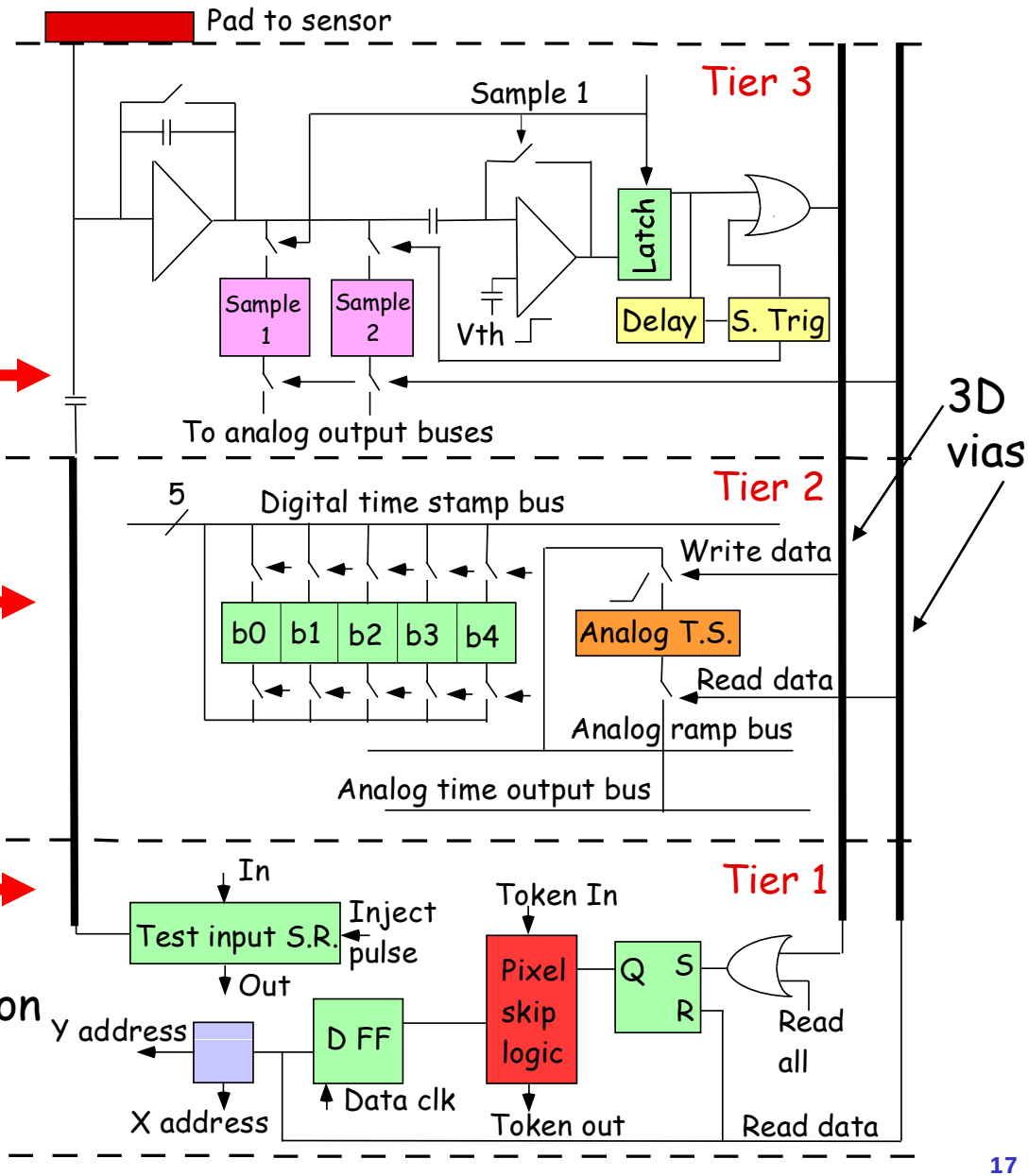
Tier 3 analog

72 transistors

Tier 2 Time Stamp

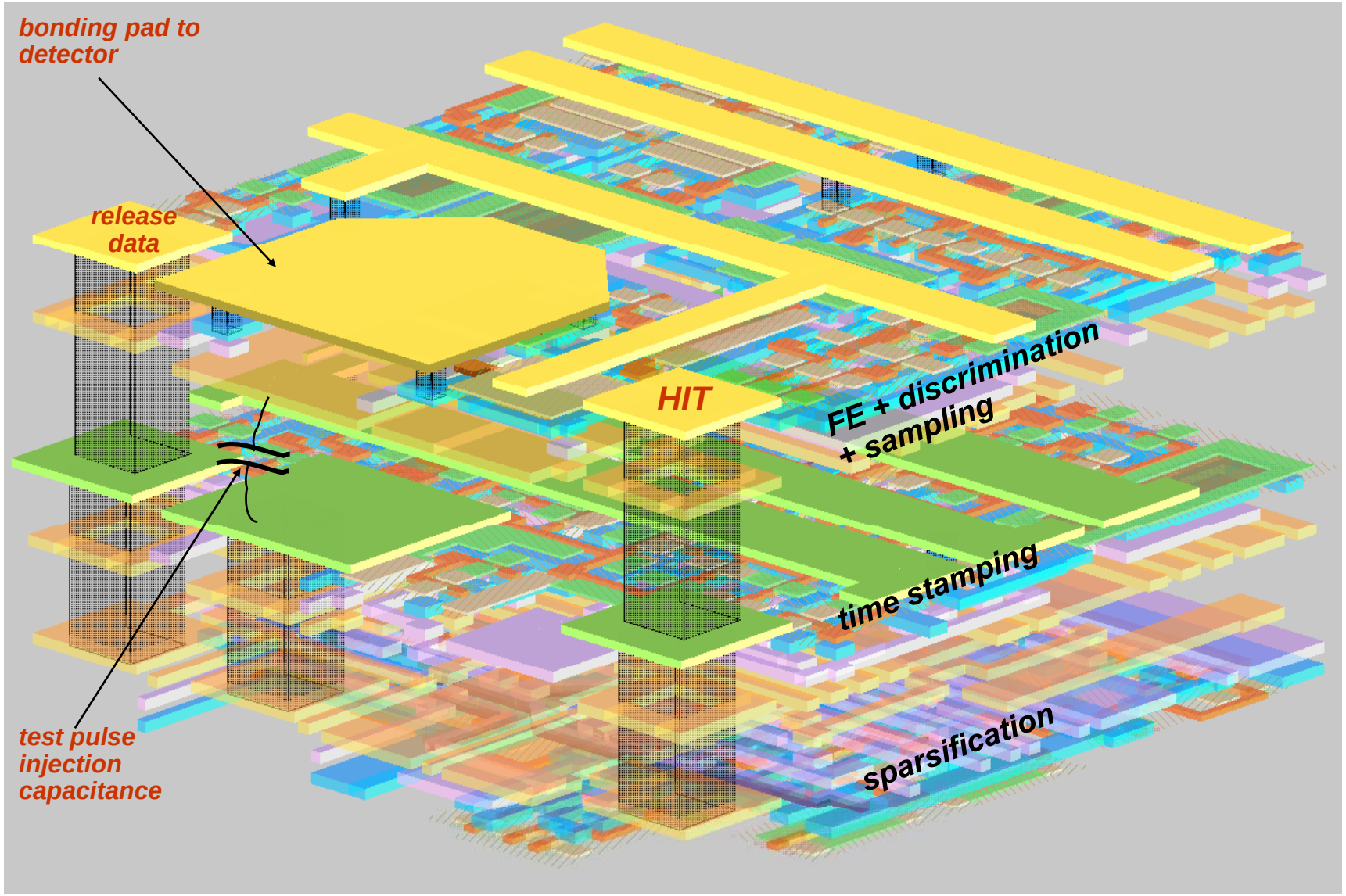
65 transistors

Tier 1 Data sparsification



Fermilab

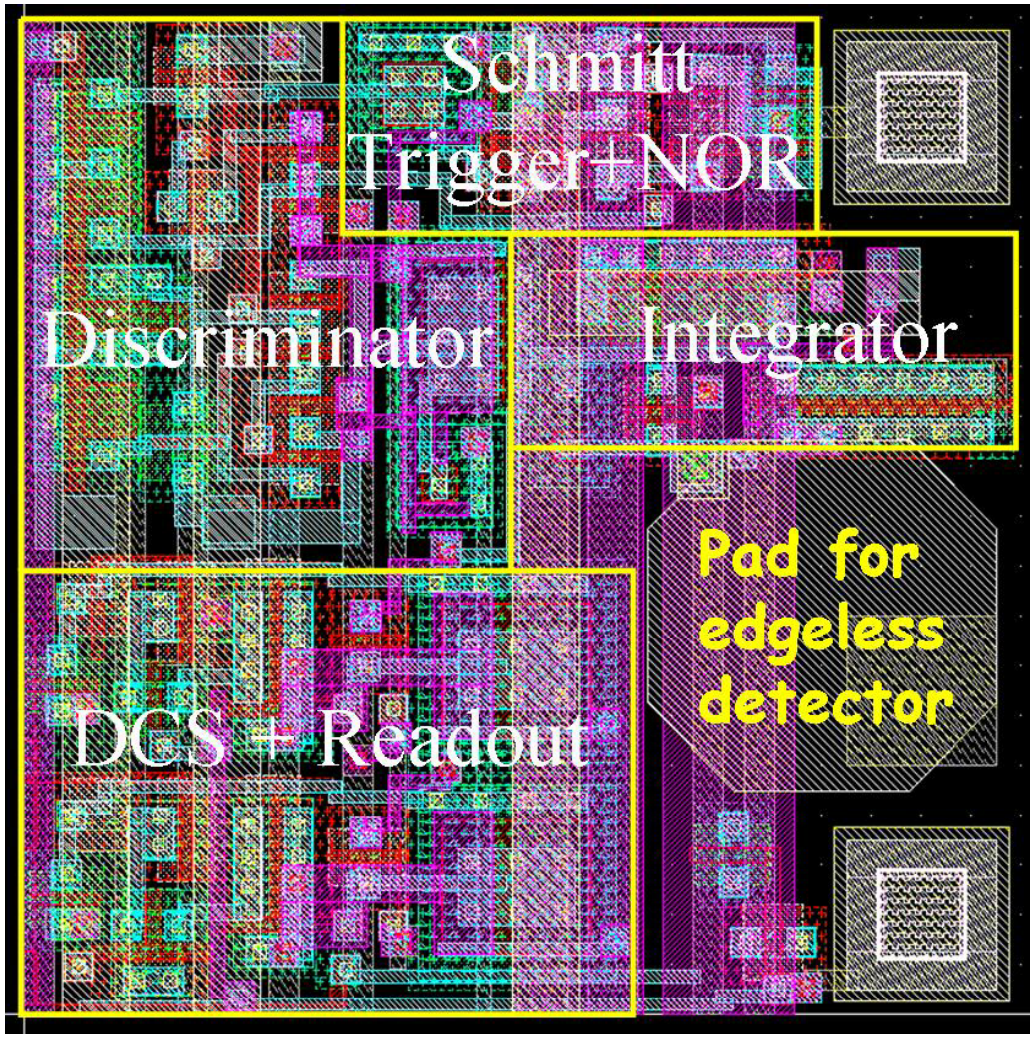
VIP: layout view with 3D Design Tool by Micro Magic:



http://www.micromagic.com/MAX-3D.html

Fermilab

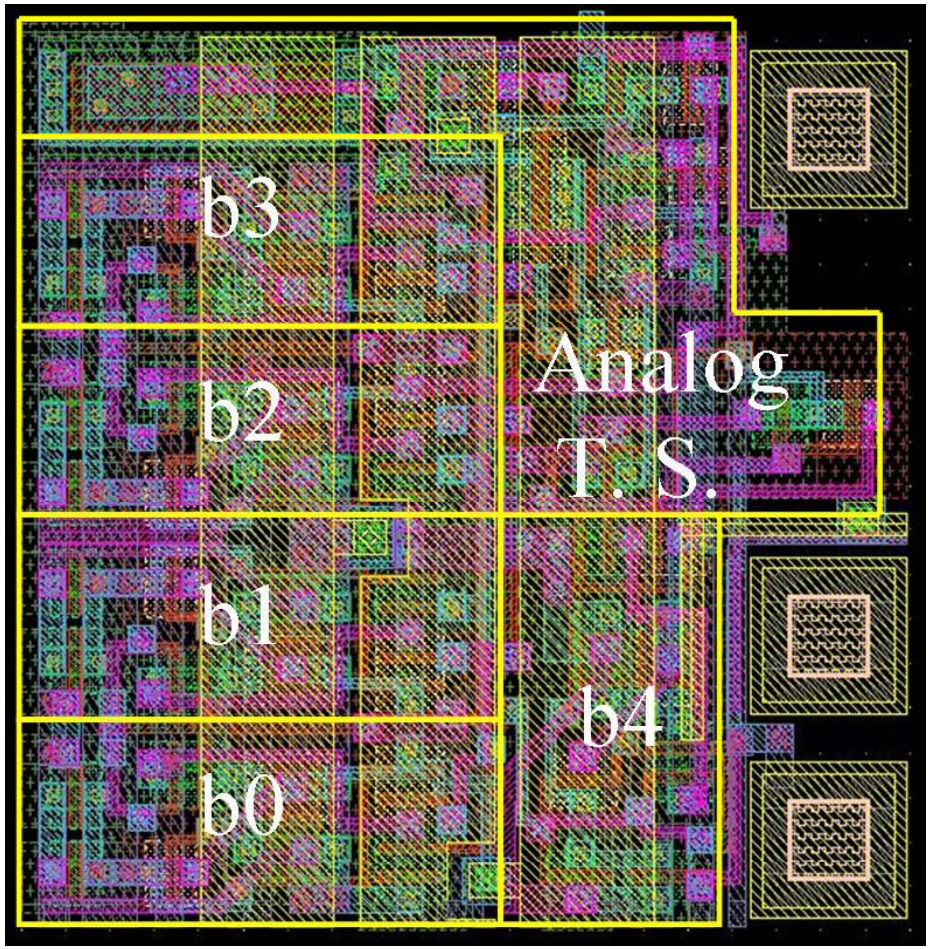
VIP: analog layer layout



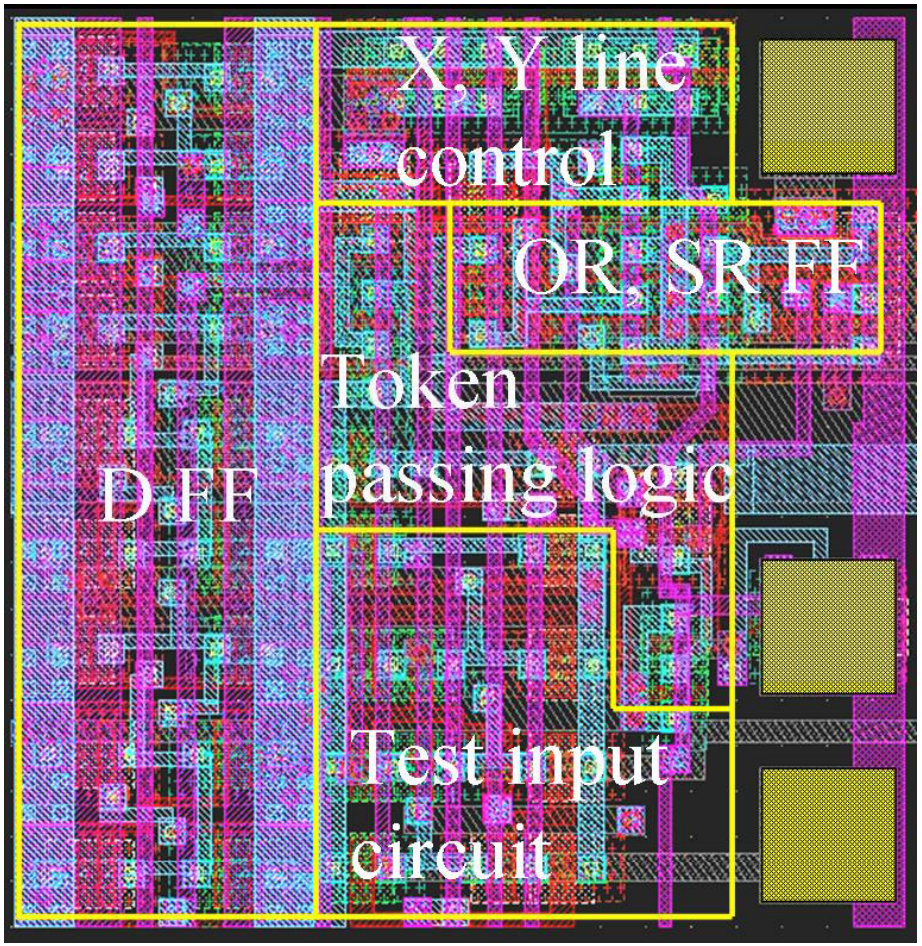
tier3

Fermilab

VIP: time stamping and sparsification layouts



tier2



tier1

Fermilab

Full array results:

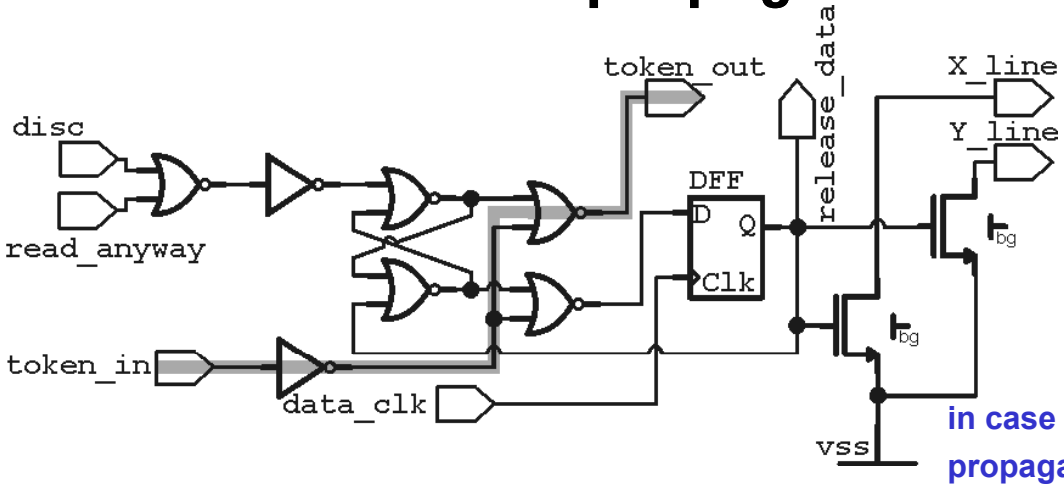
- poor fabrication yield: 1 testable chip among 23 tested
  (problem seems to be related to fabrication of individual tiers,
  3D TSV and 3D assembly seem to be successful,

- tests performed:
  - propagation of readout token,
  - threshold scan,
  - input test charge scan,
  - digital and analog time stamping,
  - full sparsified data readout,
  - Fixed Pattern Noise and temporal noise measurements (limited due to S/H)

- tests used in definition of guidelines for submission of VIP2 MIT-LL 3DM3 09/30/08.

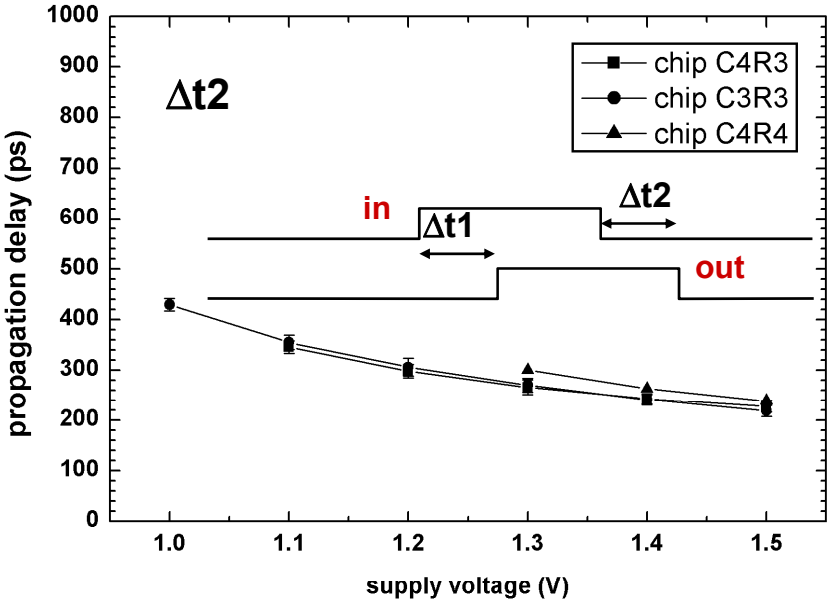
Fermilab

VIP: readout token propagation

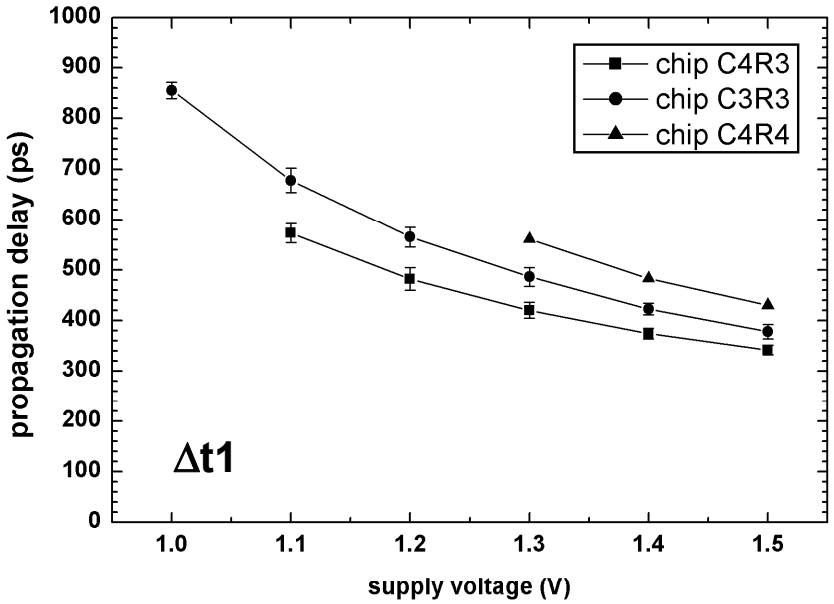


token propagation circuitry is part of sparsification circuitry; if pixel has data to send out high level at the token_in is not transmitted to token_out until the readout of the pixel address, time stamp and signal amplitude is not accomplished.

in case of lack of any hits recorded high level propagates through all pixels without interruption



propagation of falling edge:
NMOS transistors work; faster and less spread between chips



propagation of raising edge:
PMOS transistors work; slower and more spread between chips

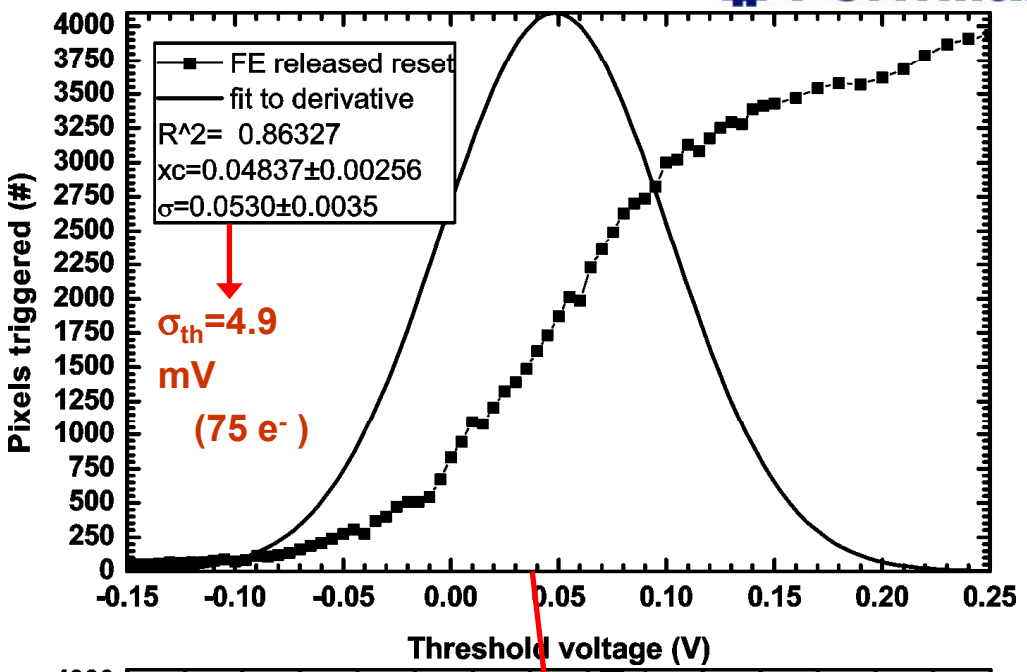
Fermilab

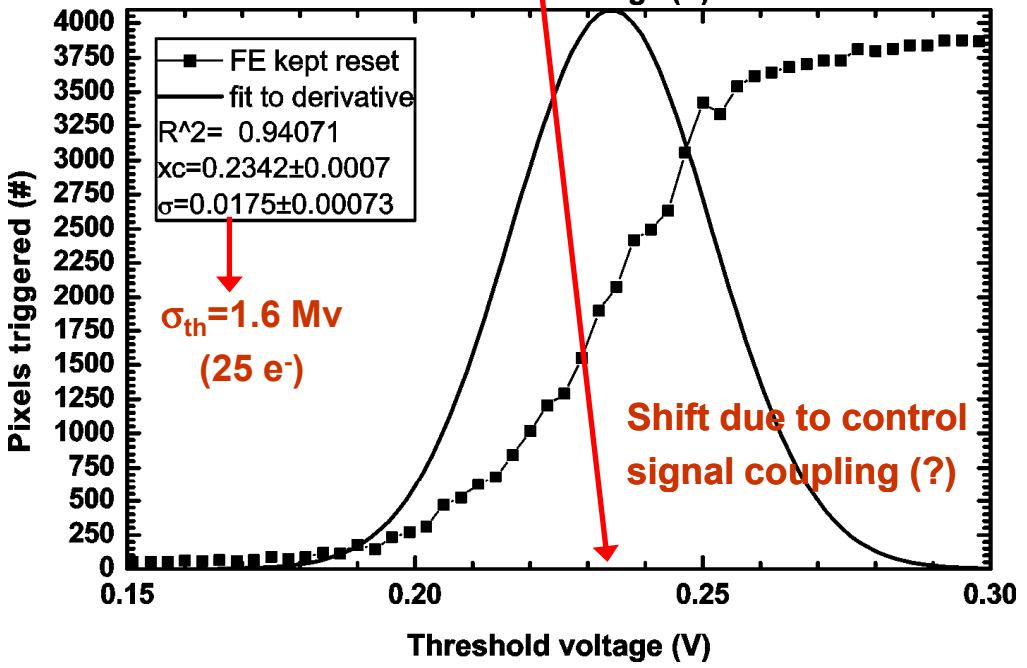
VIP: pixel-to-pixel threshold dispersion scan

- normal operation conditions, sequence: integrator reset and released, discriminator reset (autozero), threshold adjusted (lowering threshold below baseline), readout based on sparsification scheme

- operation with integrator kept reset (inactive),

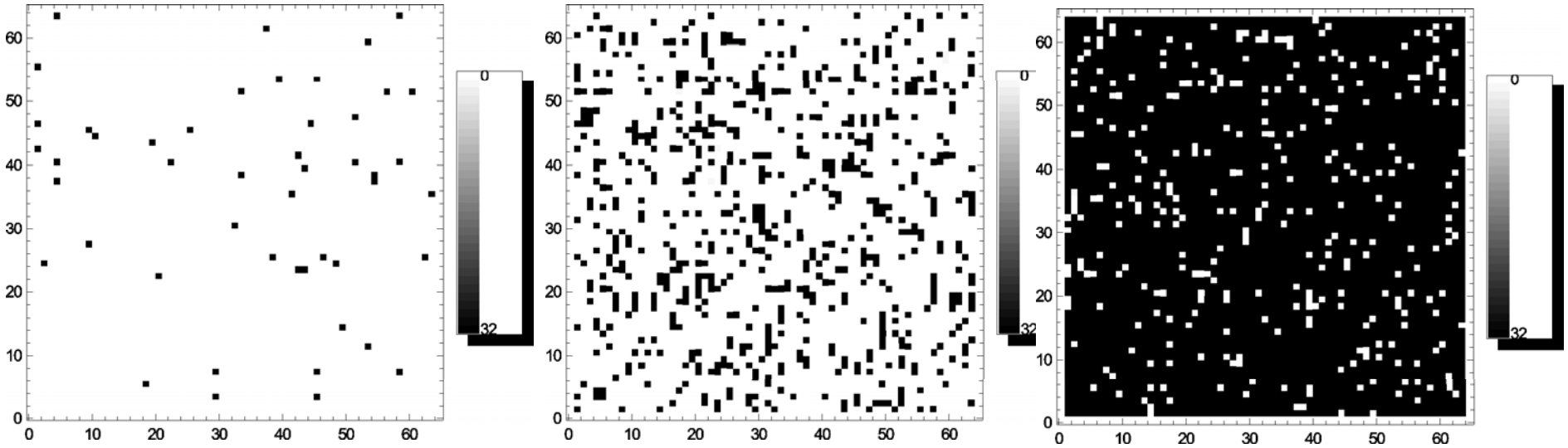
capacitive divider by 11 at the dicriminator input





Fermilab

VIP: pixel-to-pixel threshold dispersion scan



Maximum threshold

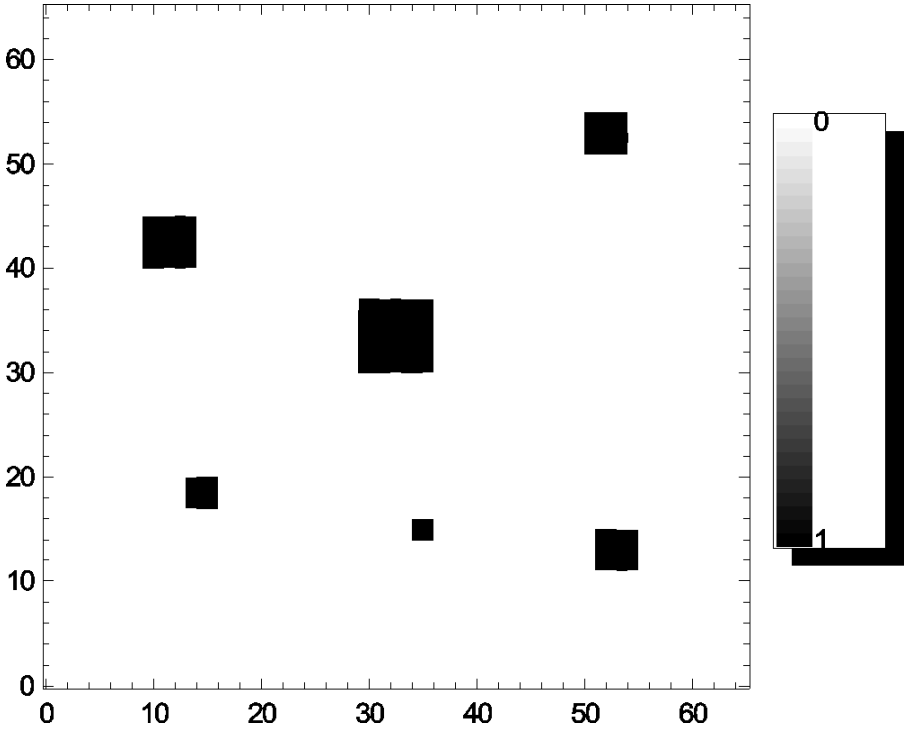
Intermediate threshold

Negative threshold

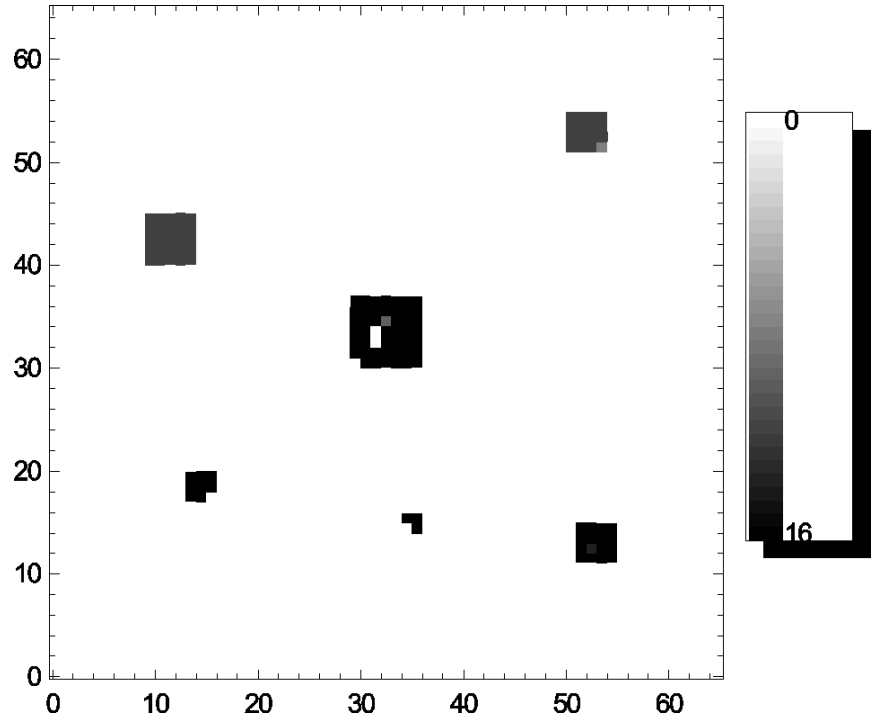
Lowering threshold

Fermilab

VIP: injection of test charge to the integrator input



***Preselected pattern** of pixels for the injection of signal to the front-end amplifiers; pattern shifted into the matrix, than positive voltage step applied accross the injection capacitance; threshold levels for the discriminator adjusted according to the amplitude of the injected signal*

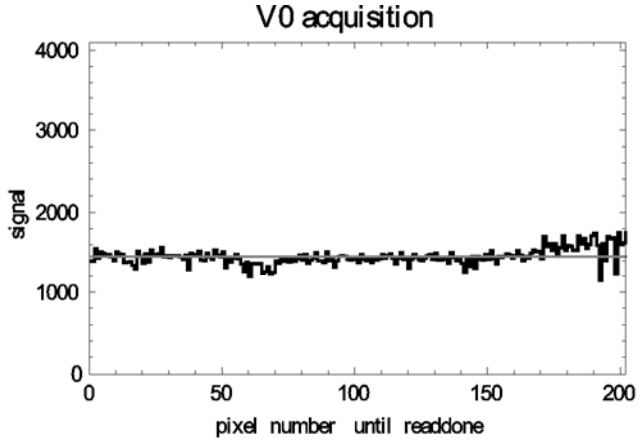


Pattern of pixels from the preselected injection pattern that after injection of tests charge reported as hit (grey level represents number of repetition – 8 times injection)

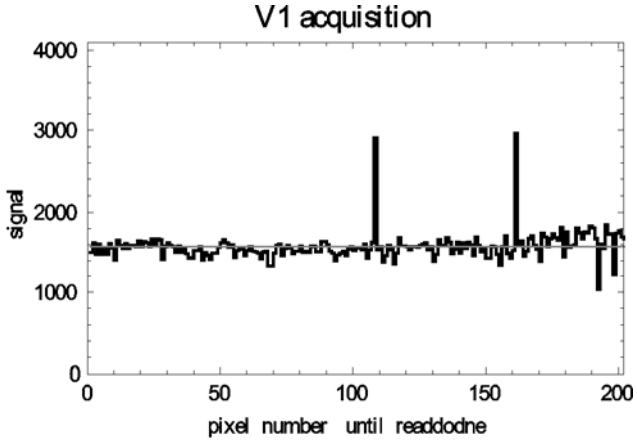
Fermilab

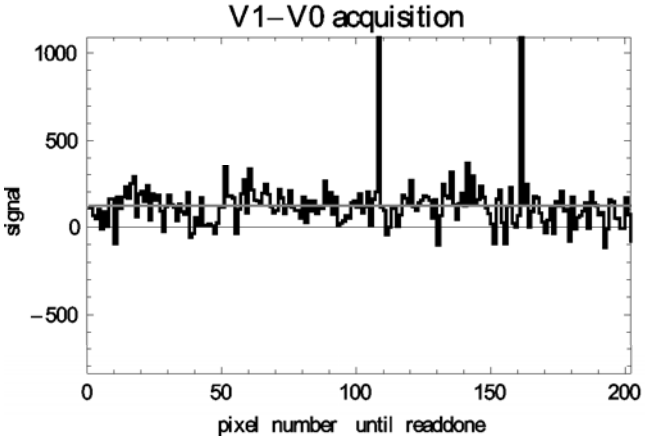
VIP: analog signals

after reset of integrator

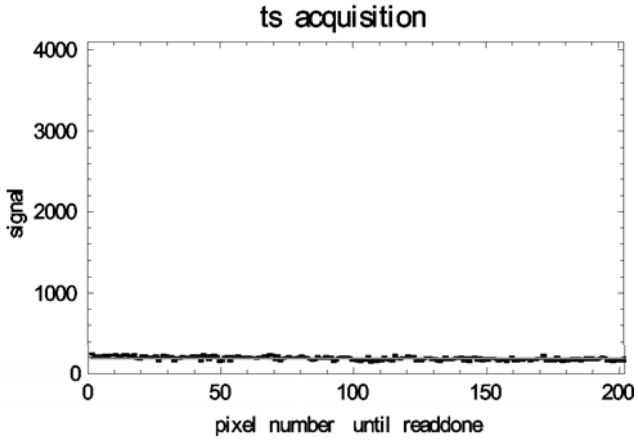


samples after discriminator trigger





difference



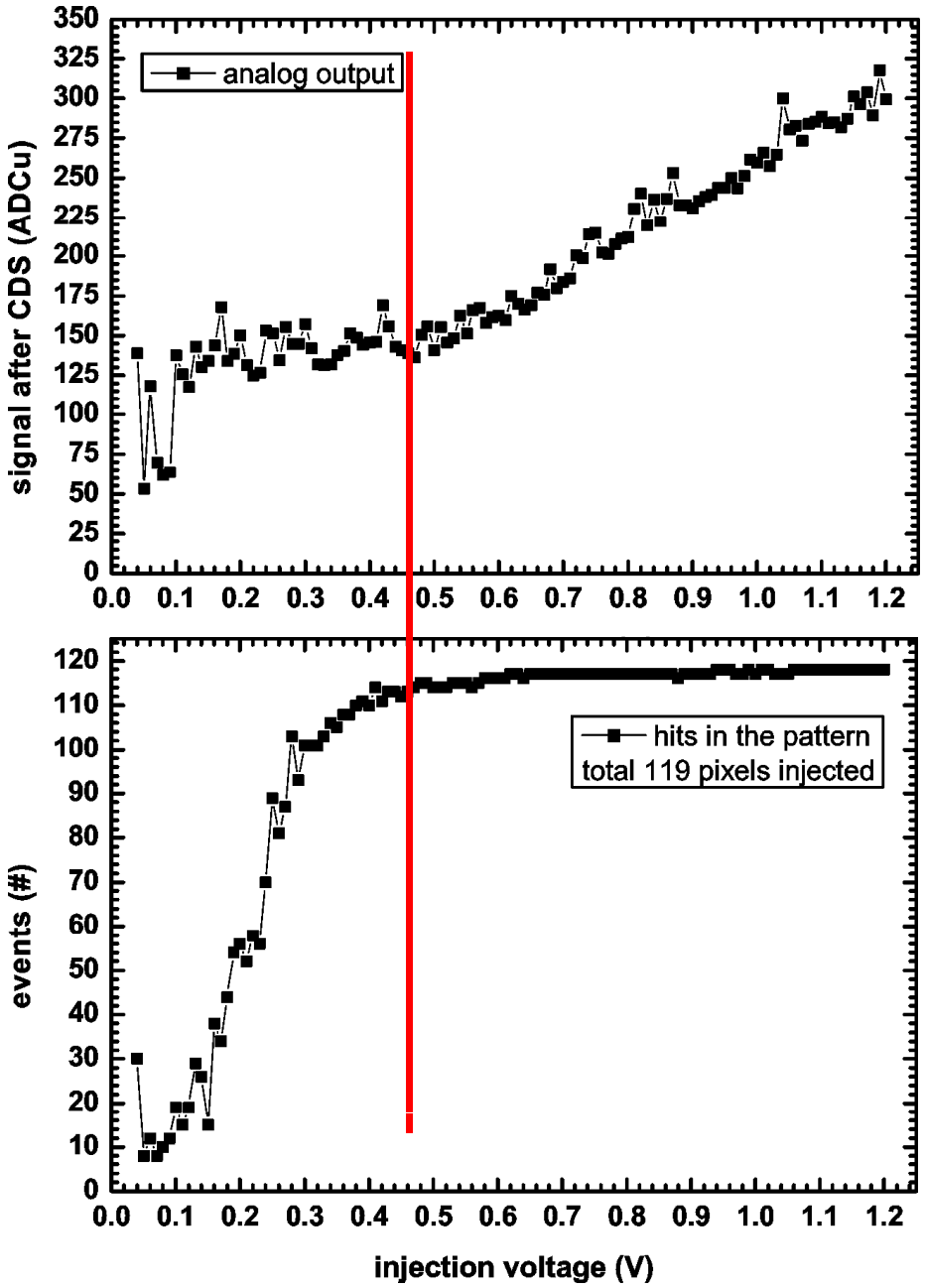
analog time stamping

Fermilab

VIP: analog signals

- scan of test charge injected through test capacitor placed between tier3 and tier2

Test capacitor value smaller than expected, however functionality demonstrated



Fermilab

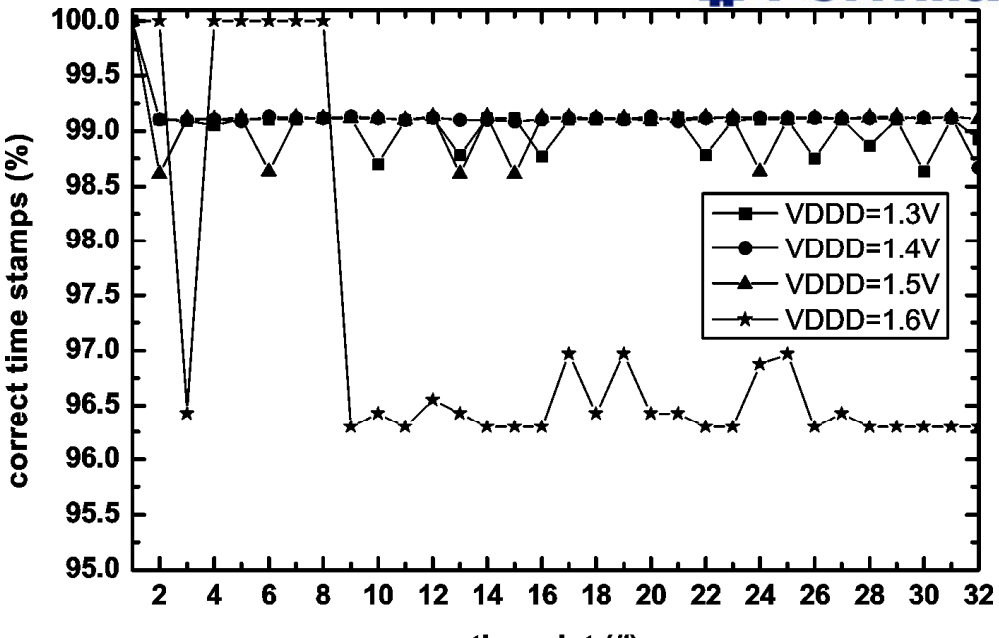
VIP: time stamping operation

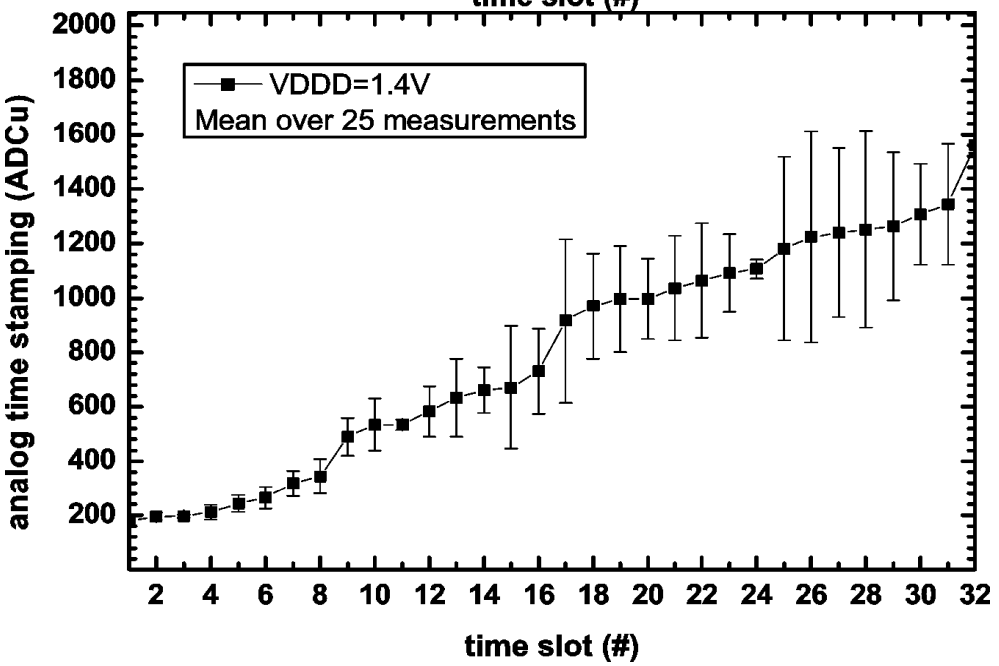
- digital time stamping (time stamping coded in inverted Gray code 5 bits)

Digital time stamping:
- 1 or 2 time stamps corrupted

Analog time stamping:
- Suffers from strong I_{off} in S/H

- analog time stamping (data taken in group of 8 acquisitions)





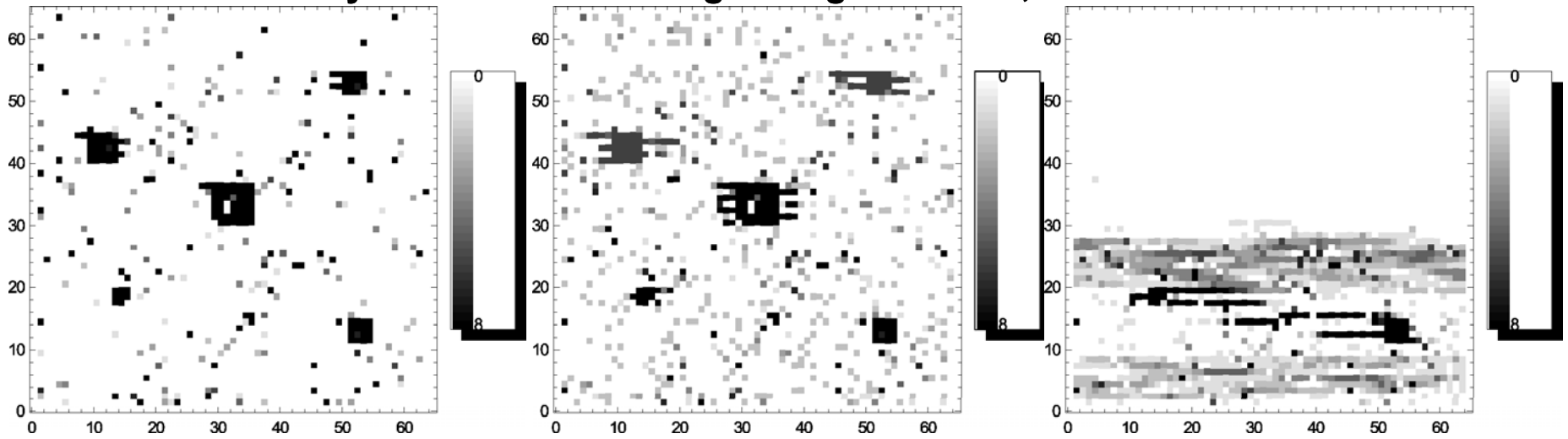
Fermilab

VIP: achievement

- First design of 3D pixel ROIC designed and fabricated,
- Operation demonstrated in ubiased measurement: input signal injection, amplification, discrimination, hit storage, time stamping, sparisified readout,

VIP: problems

- yield problems related to the fabrication technology (3D TSV seem OK),
- very high leakage currents (I_{off} corrupting stored signal in S/H),
  - Current mirror problems due to lack of statistical models,
  - Very leaky protection diodes,
- difficulty in selecting pixels for test pulse injection – missfunction of shift register due to use of dynamic DFF under big leakage currents,



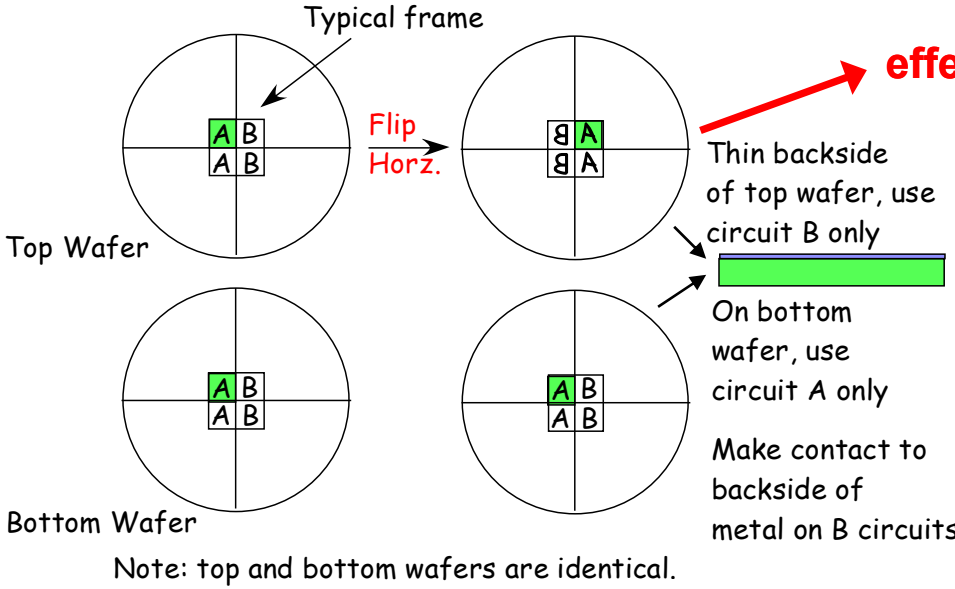
understood and correction under preparation for the Sept. 30 2008 run

Fermilab

3D integration plans with commercial vendors

- deep N-wells, MiM capacitors, single poly up to 8 levels of routing metals, variety of transistors (VT optimized) nominal, low power, high performance, low voltage, 8" wafers, reticle 24×32 mm^2;
- Tezzaron vias are very small: Φ_{via}=1.2 μm, $\Phi_{landing\_pad}$=1.7 μm, d_{min}=2.5 μm

3D MPW run using Tezzaron/Chartered open for collaborators (France, Italy). Cost-efficient option is considered with only 2 layers of electronics fabricated in the Chartered 0.13 um process, using only one set of masks



effective reticle 16×24 mm^2)

Face to Face Bonding

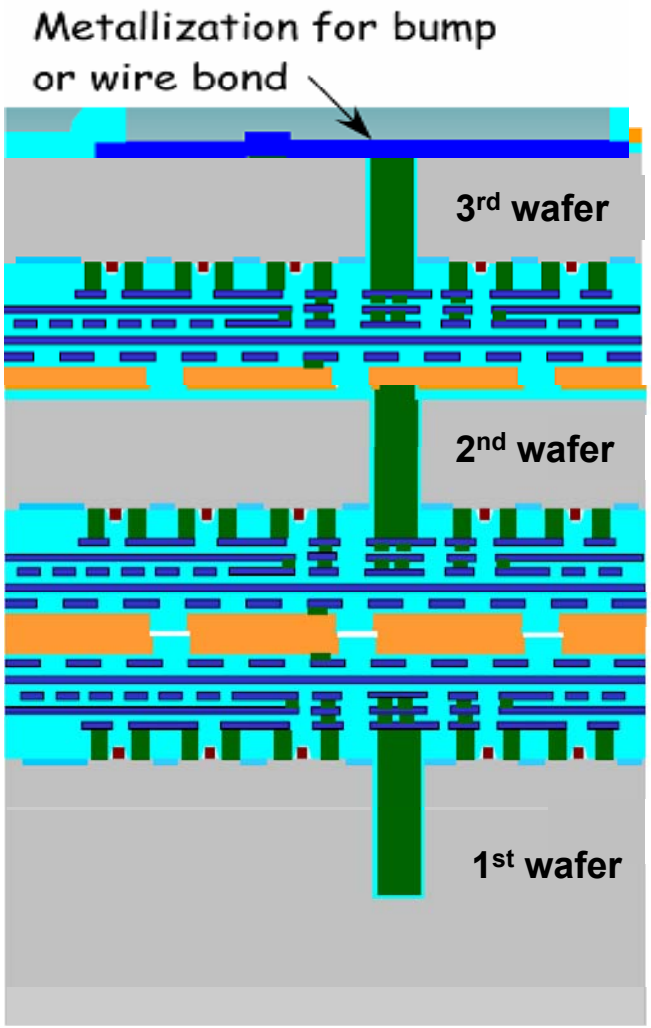
Planned submission Spring 2009 (delivery 12 weeks after ☺)

Fermilab

3D integration plans with commercial vendors

- Advantages of the Tezzaron/Chartered process:

- No extra space allotment in BEOL for 3D TSV,
- 3D TSVs are very small, and placed close together,
- Minimal material added with bond process,
- 35% coverage with 1.6 μm of Cu => Xo=0.0056%,
- No material budget problem associated with wafer bonding,
- Advanced process 0.13 μm and below
- Good models available for Chartered transistors,
- Thinned transistors have been characterized,
- Process supported by commercial tools and vendors,
- Fast assembly + Lower cost (12 3D processed wafers @ $250k in 12 weeks),



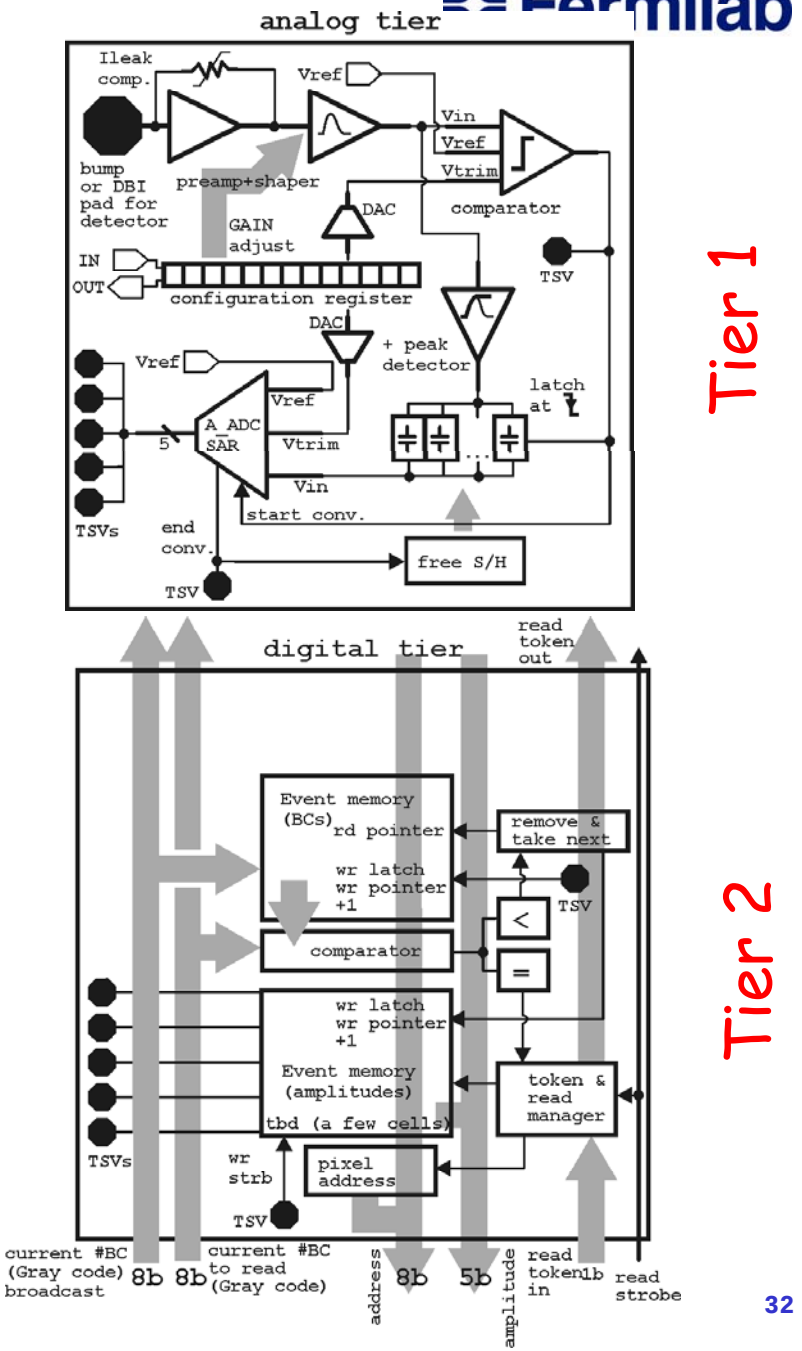
Fermilab

3D integration plans

- FNAL is exploring 3D Integration technology for pixel readouts in upgrade of CMS, development for ILC and imaging,

- Going from 1 layer in 0.25μm to 2 layers in 0.13 μm can increase circuit density × 7, density can by traded for smaller pixel size (if needed?).

- the key points of new design(s) are:
  - low power consumption (no increase),
  - high speed and data throughput, reduction of data loss (large digital storage – no storage at the periphery),
  - radiation hardness,
  - parallel processing in-situ (in pixel A-to-D conversion triggered by radiation event), sparsification,
  - reduction of peripheral circuitry,
  - can pixels have trigger capability?



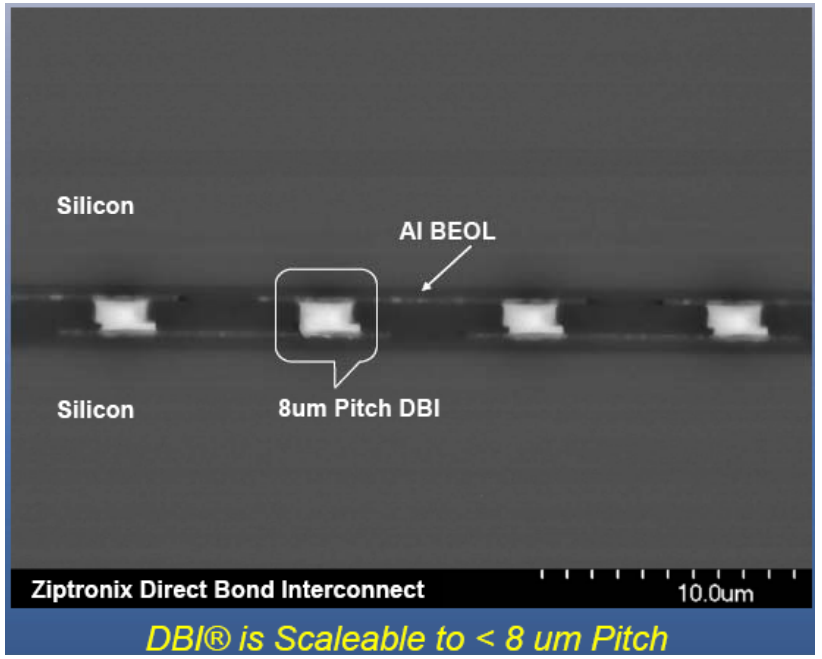
Fermilab

3D integration plans with commercial vendors

- Another demand for 3D assembly comes from detector/ROIC bonding; Fermilab is working with Ziptronix to do low mass bonding with DBI to detectors. (FPIX chips to 50 um thick sensors.);
- Conventional solder bumps or CuSn can pose a problem for low mass fine pitch assemblies

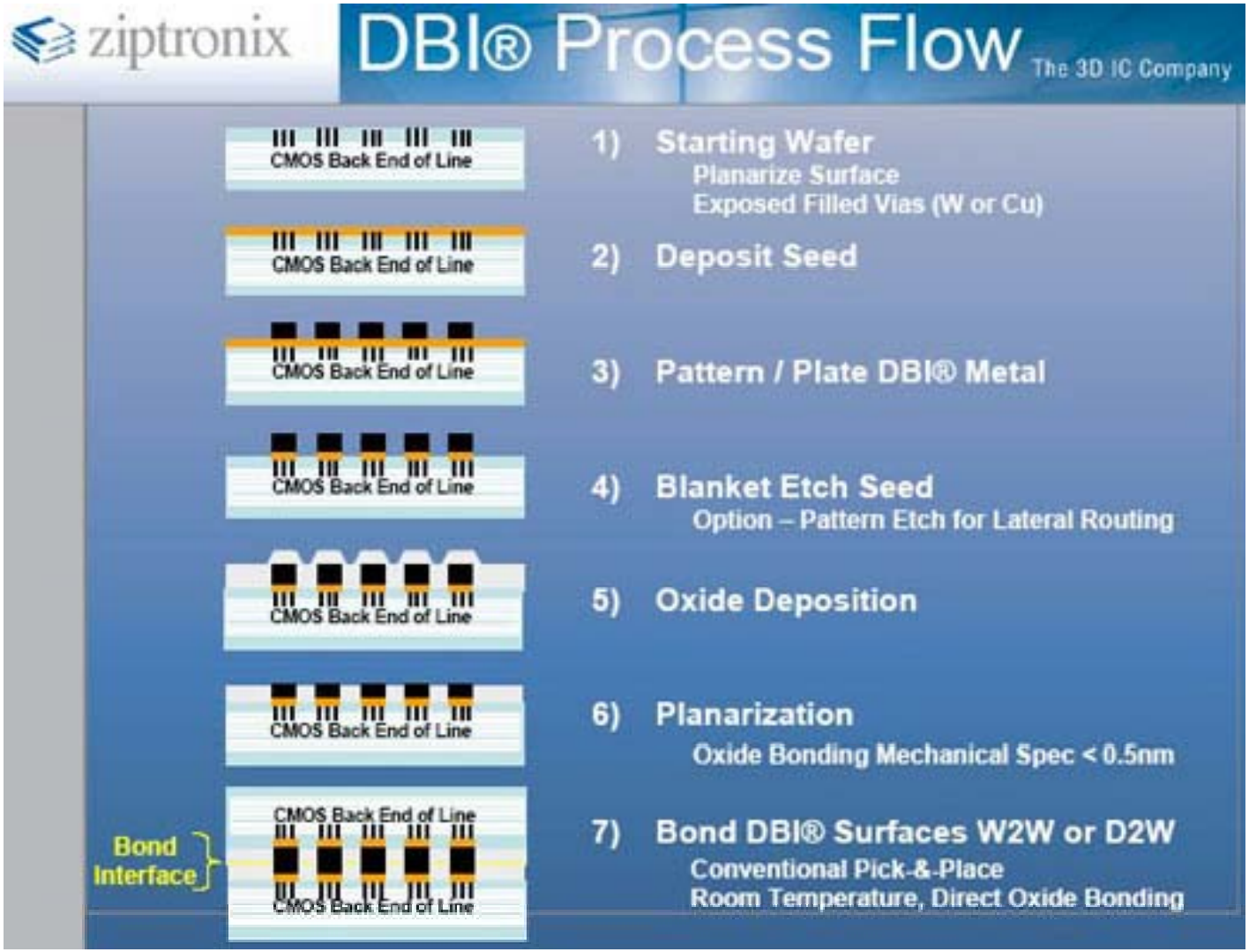
Ziptronix - uses Direct Bond Interconnect (oxide bonding)

- Ziptronix is located in North Carolina
- Fermilab has current project with Ziptronix to bond BTEV FPIX chips to 50 um thick sensors.
- Orders accepted from international customers



Fermilab

3D integration plans with commercial vendor



Fermilab

Conclusions:

- 3D Integration is very attractive for highly granular detector systems,
- Bonding is low temperature process, adds limited amount of high-Z material,
- 3D-Integration may extend use of certain detector type (MAPS),
- 3D-Integration is starting to be available in industry,
- Commercial vendors like Tezzaron-Charted lead to lower costs, faster fabrication cycle, high yield,
- The proposal from Fermilab, to use commercial vendors, received considerable attention and is leading to a collaboration between various groups within HEP to explore the Tezzaron 3D process,
- Groups in Italy, France, and the United States will be designing chips in the Tezzaron 3D process for possible application ILC, SLHC, etc.

- First run exploiting 3D-Integration technology with MIT-LL (SOI based) process showed feasibility of the design,
- One more submission in MIT-LL is envisaged, however main effort will be allocated to Tezzaron/Chartered process,
- Dedicated EDA tools required – will our community be able to afford?

Fermilab

Back up

3-D PROCESSES									
	RPI	Fraunhofer-Munich	ASET Japan	Tohoku University Japan	IBM	Infineon	MCNC-RDI	Toshiba	Tezzaron
Wafer to wafer	X			X				X	X
Chip to wafer		X				X	X		
Chip to chip			X				X		
SOI or bulk wafer	SOI		Bulk		SOI		Bulk	Bulk	
Via size (μm)	2 × 2	2.5	10	2.5			4	30	
Via etch process	SF_6		SF_6	SF_6			SF_6	SF_6	SF_6
Peripheral vias			X					X	
Area array vias	X	X				X	X		X
Via dielectric	SiO_2	SiO_2	SiO_2	SiO_2		SiO_2	Polymer	SiO_2	SiO_2
Barrier layer	TiN	TiN	TiN			TiN	TiN	TiN	TiN
Metal plug	Cu	W or Cu	Cu	Poly-Si or W	Cu	Cu	Cu	Cu	Cu
Handle wafer	No	Yes	Yes	Yes	Yes	No			No
Bonding scheme	Polymer	Cu-Sn eutectic	Cu-Sn eutectic	In/Au bumps	Si fusion	Cu-Sn-Cu	Polymer or bumps	Bumps	Cu-Cu