Fine Pixel CCD for ILC Vertex Detector

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for ILC-FPCCD vertex group

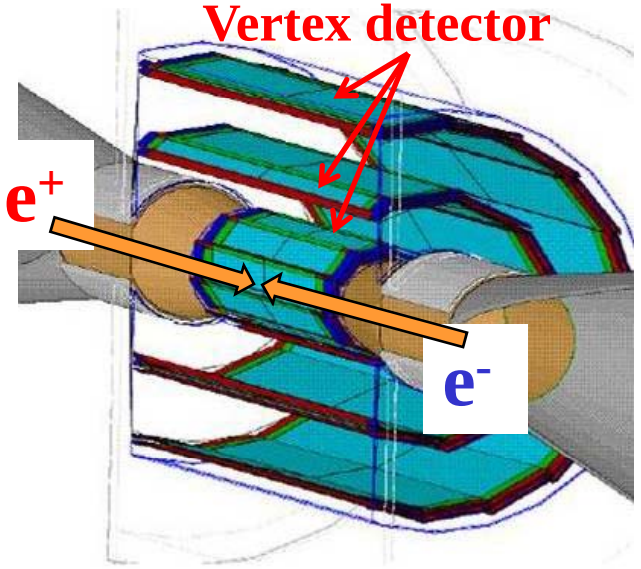
Contents

- ILC vertex detector
- Fine Pixel CCD (FPCCD)
- Test-sample for the FPCCD
- FPCCD readout ASIC
- Summary & Next step

ILC vertex detector

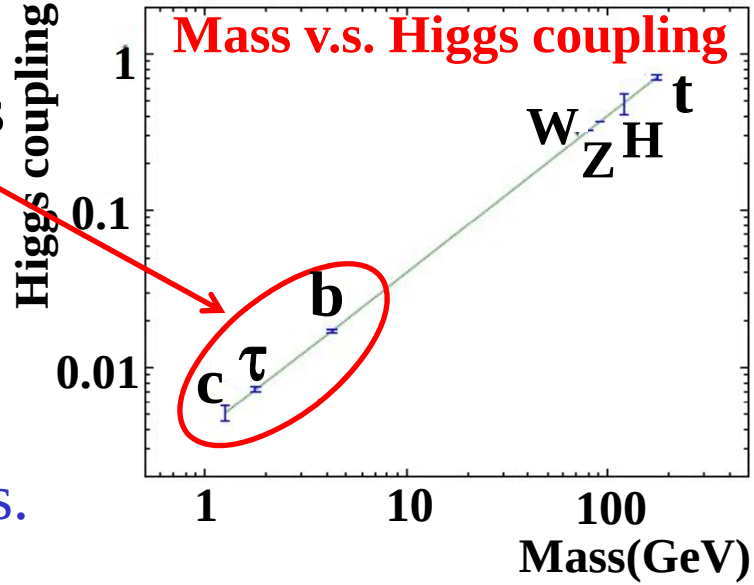
ILC (International Linear Collider)

- e^+e^- linear accelerator in the future
- CM energy : 500GeV
- Precise measurement for Higgs and new physics is planed.



ILC vertex detector

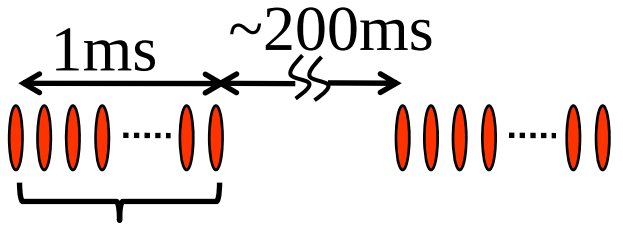
- Necessary to study Higgs coupling to mass
- Excellent impact parameter resolution is required.
  - $\sigma_{IP} = 5 + 10/(p\beta \sin^{3/2}\theta)$ (μm)
- ILC-VTX detector is studied in >10 groups.



Requirement to ILC vertex detectors

The readout scheme is key issue for ILC vertex detectors.

- Readout in the inter-train (200ms) is easy.
  - It is ideal to keep all hit data in one train.



- The hit occupancy in the pixels is problem.
  - There are huge e^+e^- pair B.G. from beam crossing.
  - The occupancy will be ~10% for the pixel size of 20μm
    - ✓ Required pixel occupancy < 1%

Prescription

- Readout many times in one train
  - Difficult to achieve
- To use the very fine pixel sensor
  - Current CCD technology can realize it.

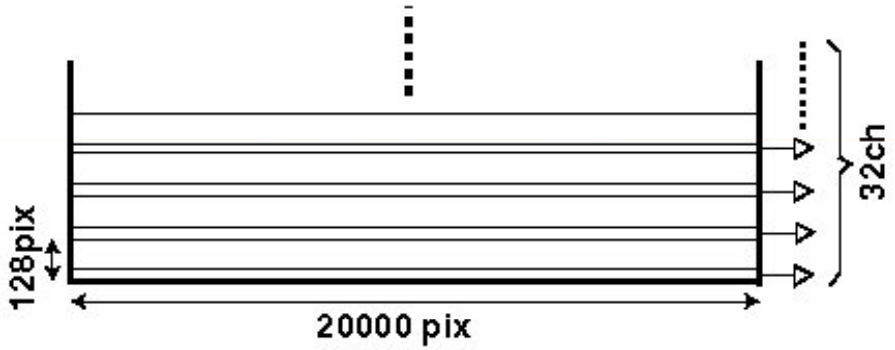
→ **FPCCD**
(Fine-pixel CCD)

Fine Pixel CCD (FPCCD)

FPCCD vertex detector

- Pixel size : 5 x 5 μm^2
- Thickness (epi) : 15μm
  - Total Si-thickness : 50 μm
- # of readout channels: ~6,000ch
  - ~20,000 x 128 pix/ch
- Fully depleted to compact the clusters
- FPCCDs will be equipped on the both side of the sensor layer.

ILC-FPCCD ladder



Wire-bonding

We started to develop FPCCD vertex detector

- FPCCD sensor
- Readout ASIC

} **Today's my talk**

Development of FPCCD Sensor

Development of FPCCD sensor

Requirement to FPCCD sensor

- Pixel size : 5 x 5 μm^2
- Total thickness : 50 μm
- Readout rate : 10Mpix/s
- Noise level : <30e
- Power consumption : <10mW/ch
- The horizontal transfer-register is embedded between the readout pixels.

→ FPCCD test-sample is developed to establish the technology.

- The test-sample is produced twice in 2008.
- The 1nd test-sample was delivered.

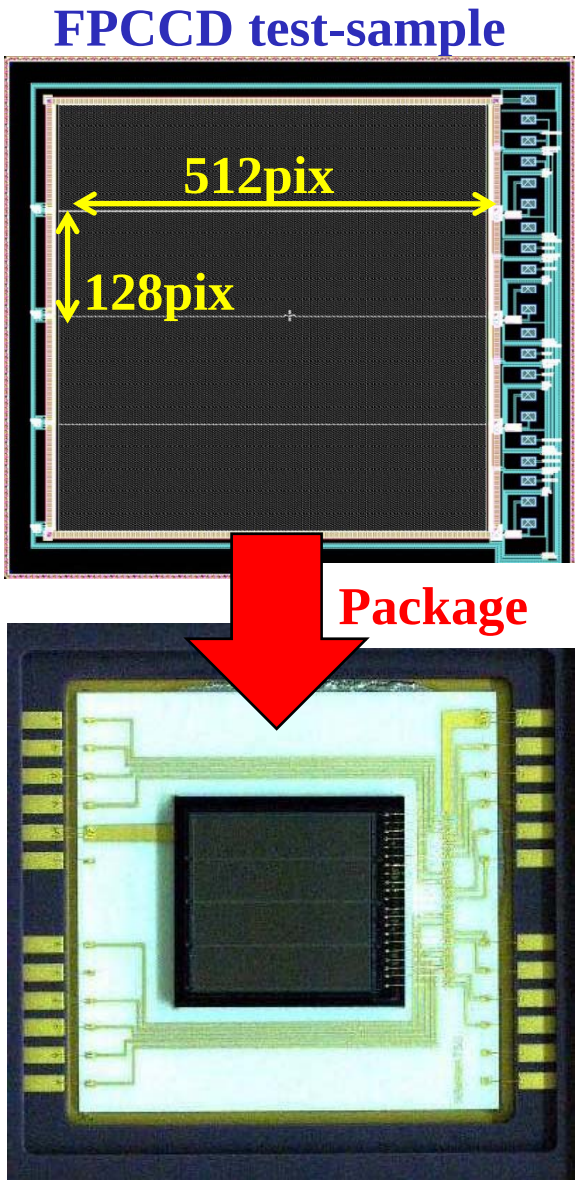
The 1st FPCCD test-sample is shown.

FPCCD test-sample

The test-sample of FPCCD was produced in Mar., 2008 by Hamamatsu.

FPCCD test-sample

- Chip-size : 8.2 x 7.5 mm^2
- Pixel size: 12 x 12 μm^2
- # of readout channels: 4
  - 512 x 128 pix/ch
- The several combinations of the wafer-thickness and amplifier-types were produced.
  - Wafer thickness (epi) : 15μm, 24μm
    - ✓ 24μm-ware has higher specific resistance for easy full-depletion.
  - Amplifier : 7 types

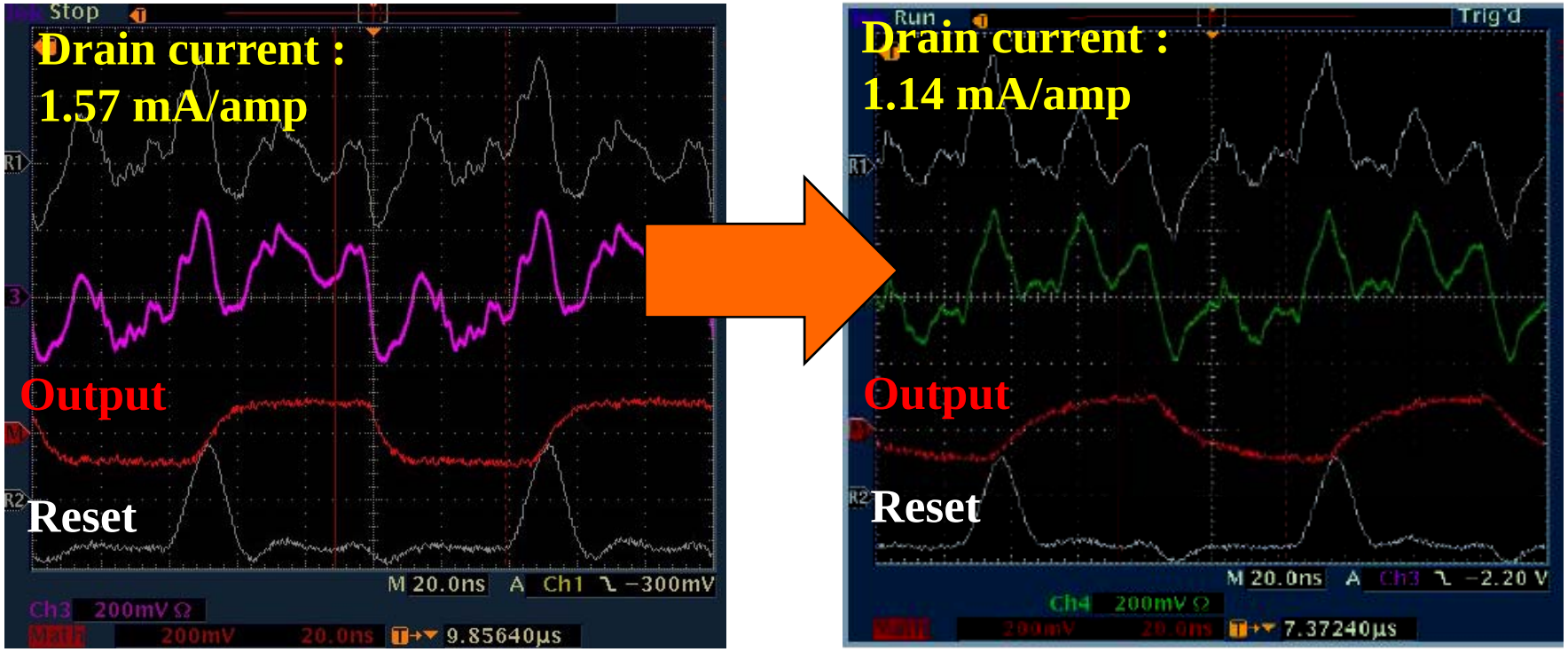


Test results by Hamamatsu

The output signals were checked at 10Mpix/s by Hamamatsu.

- The rectangle shape of the signal output can be observed.
- The signal shape becomes steep for low drain current in the amplifier.
  - The low drain current is important for the low power consumption.

  → The detail response-test will be performed soon.

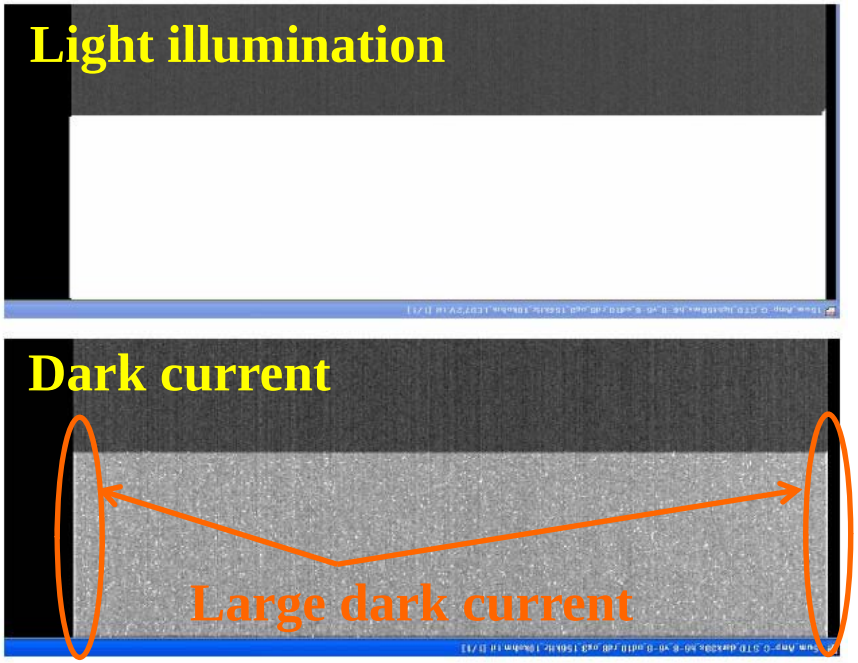


Improvement issues

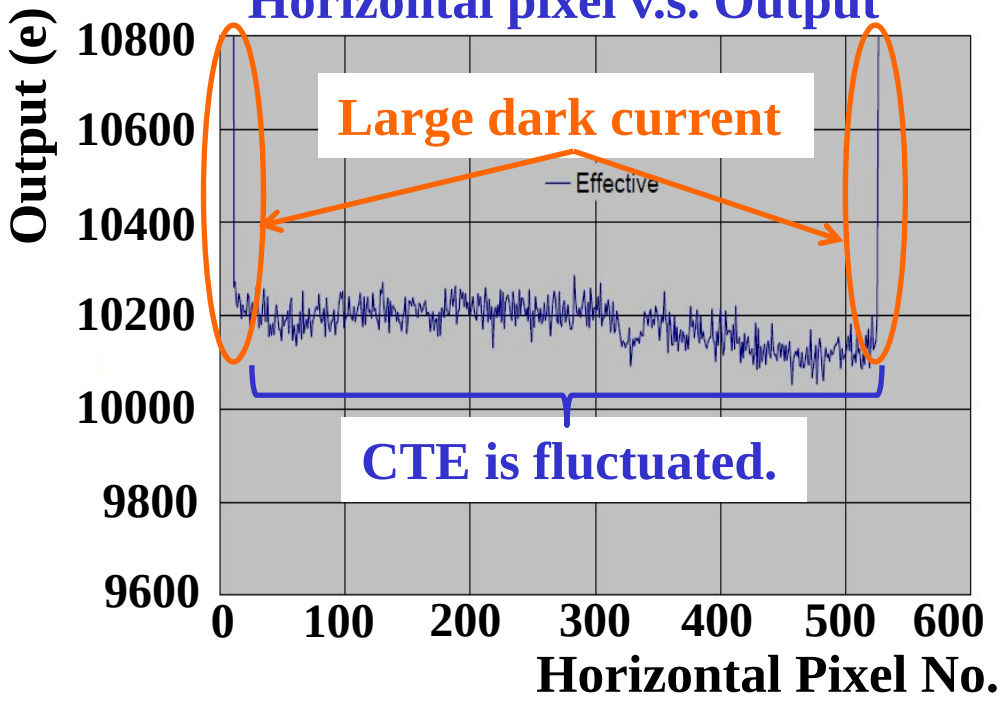
There are still some issues to be improved.

- The dark current becomes large at the horizontal edge.
  - The layout will be modified after 2008.
- The charge transfer efficiency (CTE) is fluctuated for each vertical line.
  - This problem will be recovered for the next production in 2008.

Output from the readout pixels



Horizontal pixel v.s. Output

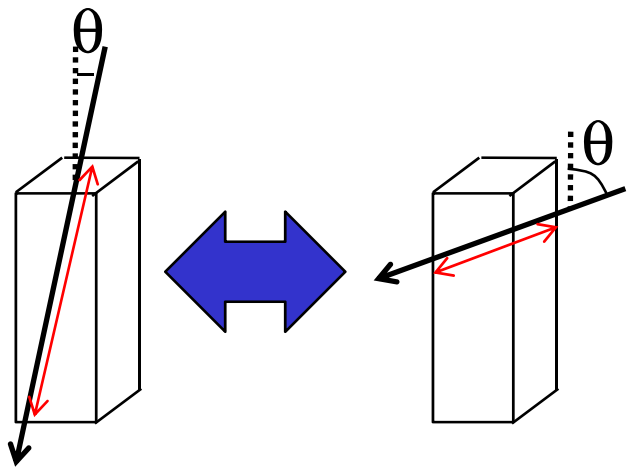


Development of Readout ASIC

Requirement to the readout ASIC

Requirement to the readout ASIC

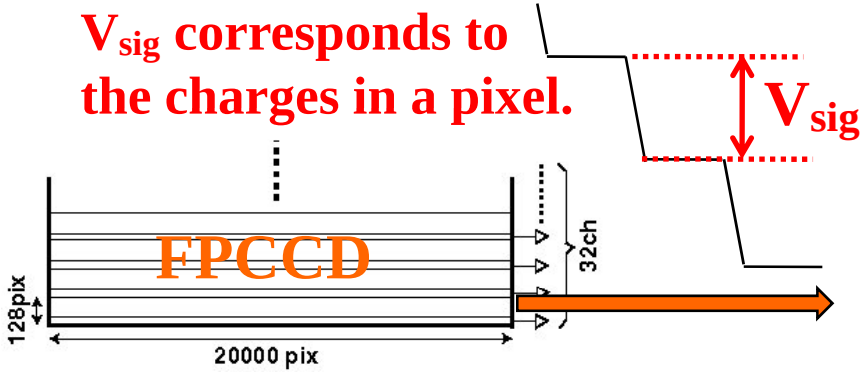
- Readout rate : >10 Mpix/sec
  - [20000 x 128 pix]/[0.2 s]
- Noise level : < 30 electrons
  - Signal level for large angle: ~500e
  - Total noise including CCD: <50e
- Power consumption : < 6 mW/ch
  - Required power consumption in a cryostat <100 W.
  - Total power consumption : <16 mW/ch (~100W/6000ch)
    - ✓ FPCCD : ~10mW/ch



To satisfy these requirements, the readout ASIC was designed.

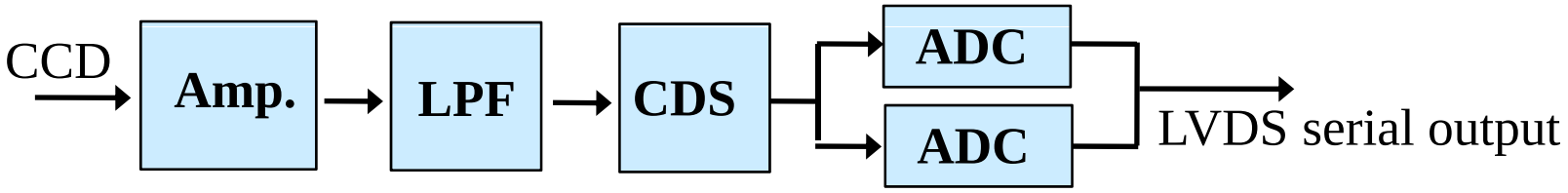
Design of the readout ASIC

Elements in readout ASIC



- Amplifier
- Low-pass filter (LPF)
- Correlated double sampling (CDS)
  - The voltage difference between each pixel is read.
- 7-bit charge sharing ADC
  - The readout with 10Mpix/sec is realized by using 2 ADCs alternatively.
  - Low power consumption: < ~10 μW

Based on this design concept, the prototype ASIC was developed.



Prototype ASIC

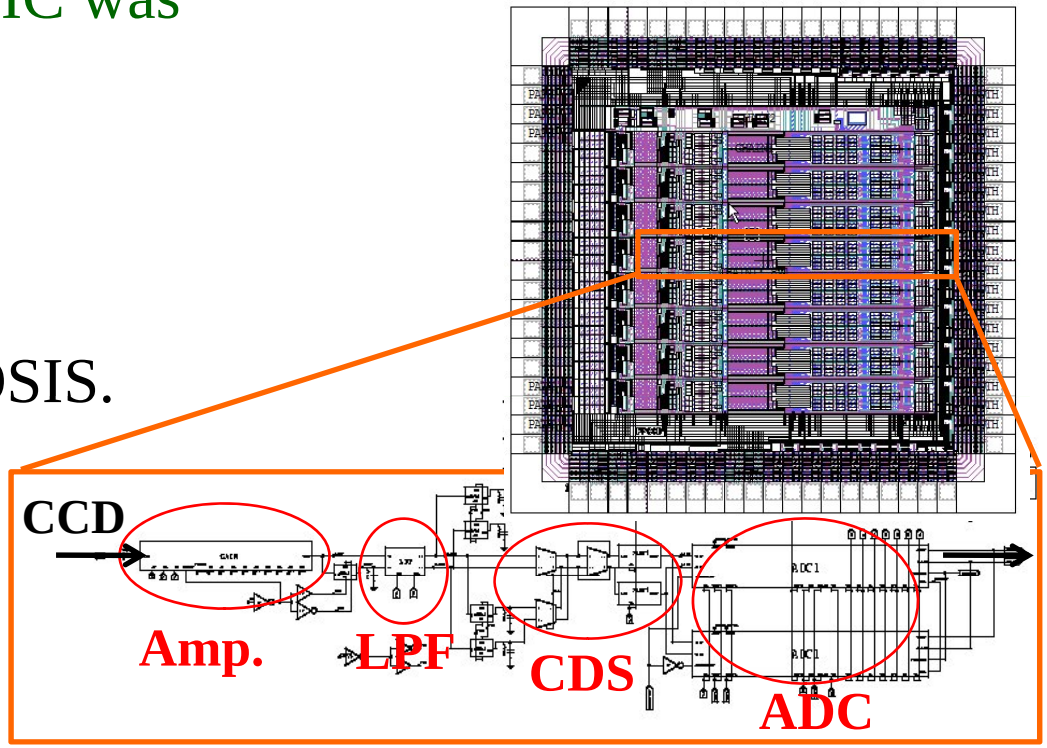
The prototype of the readout ASIC was produced in Jan., 2008.

ASIC prototype

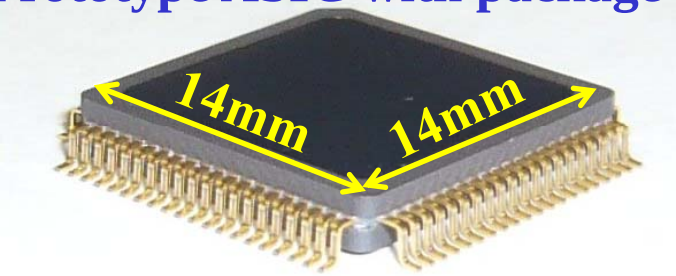
- 0.35μm TSMC process
- The chip was produced by MOSIS.
  - Size: 2.85 x 2.85 mm^2
  - # of pad: 80
  - # of readout channels: 8
- Package : QFP-80 pin

The response test was started.

Layout of prototype ASIC



Prototype ASIC with package



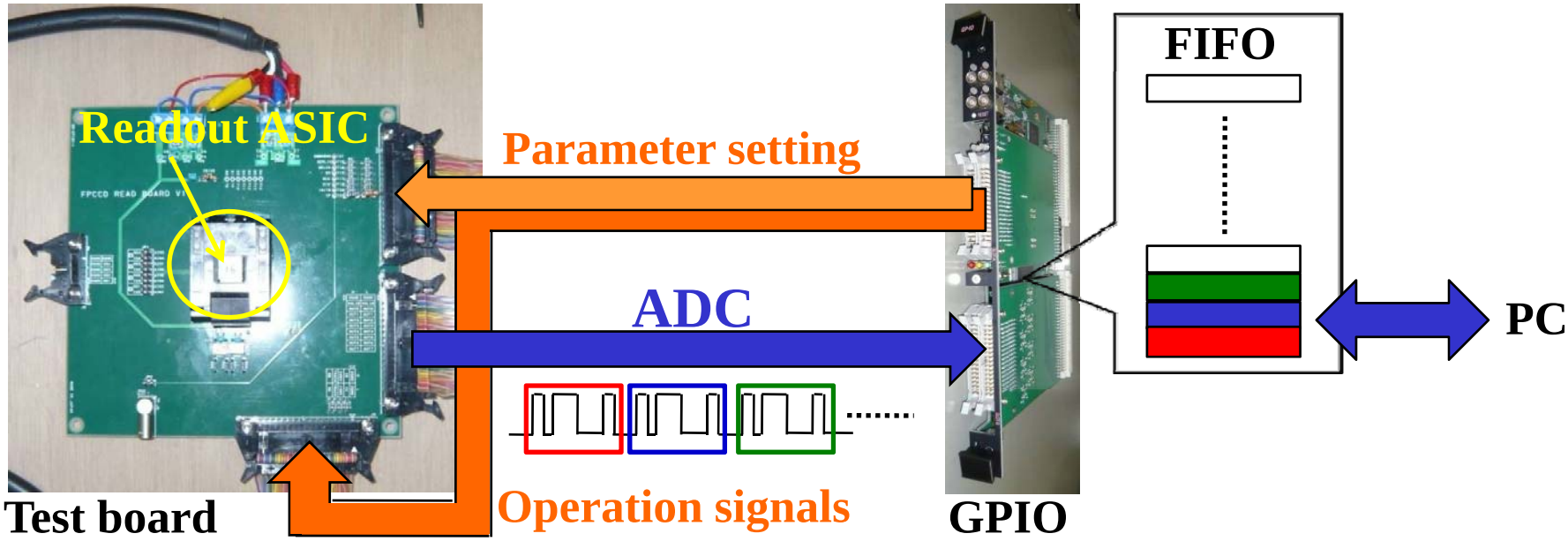
Readout system

The readout system was constructed to check the ASIC respose.

Readout system

- Operation and data-acquisition is done by VME-GPIO module.
- ADC serial pulse is analyzed by a FPGA on the GPIO module.
- The ADC information is sent to PC.

→ The response test was started with 10kHz readout operation.

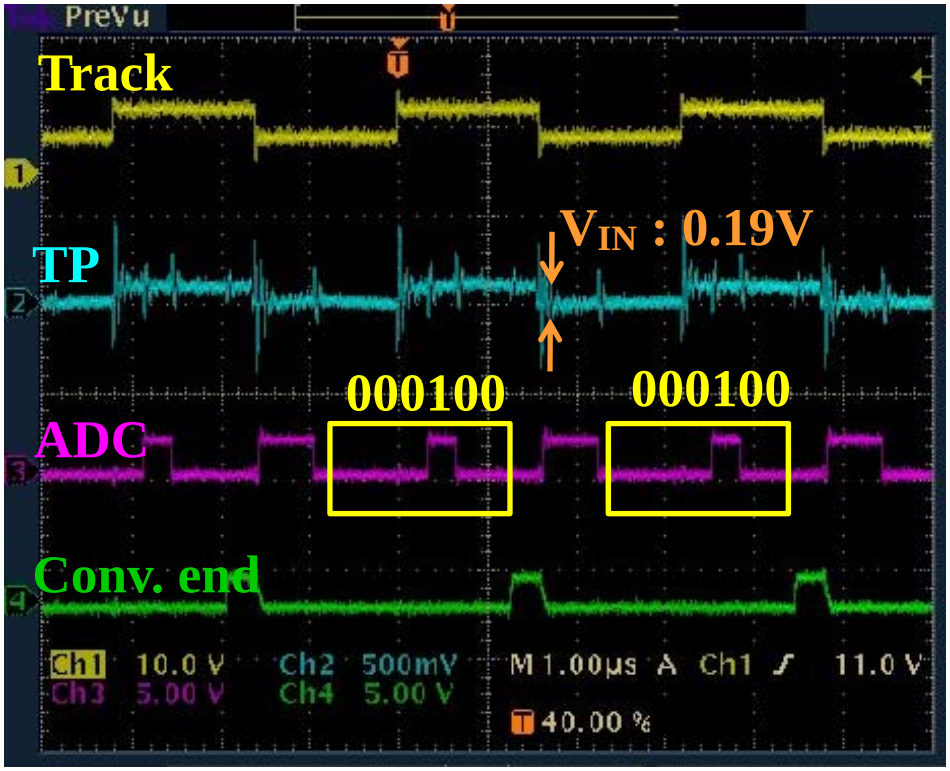


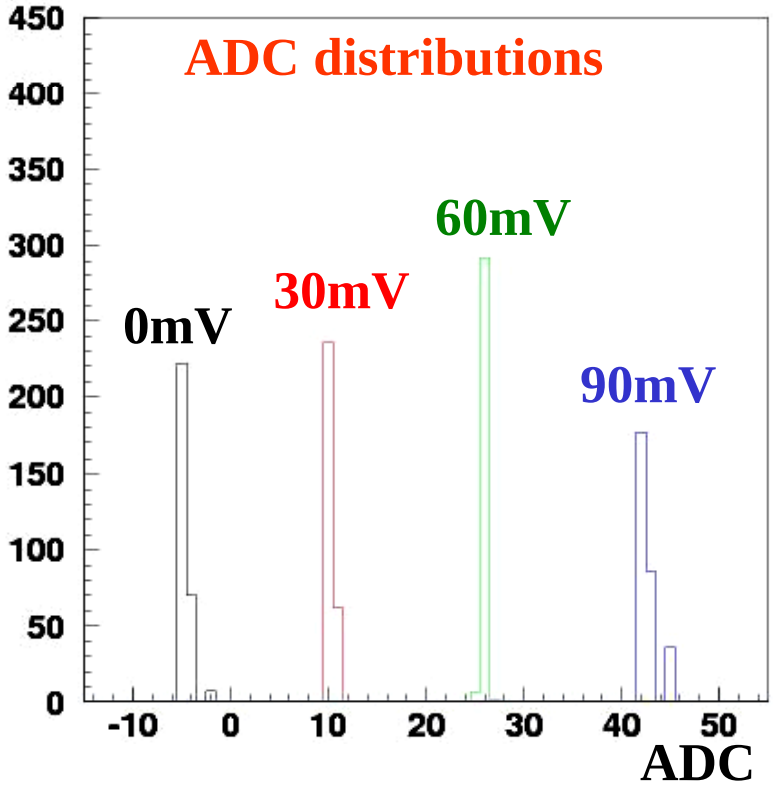
Response of prototype ASIC

The ASIC response was checked by using the test-pulse.

- The serial ADC signals were output from ASIC, correctly.
- The ADC distributions read by the readout system seems to be good.

→ The performance of the prototype ASIC was investigated.





Measurement of noise level

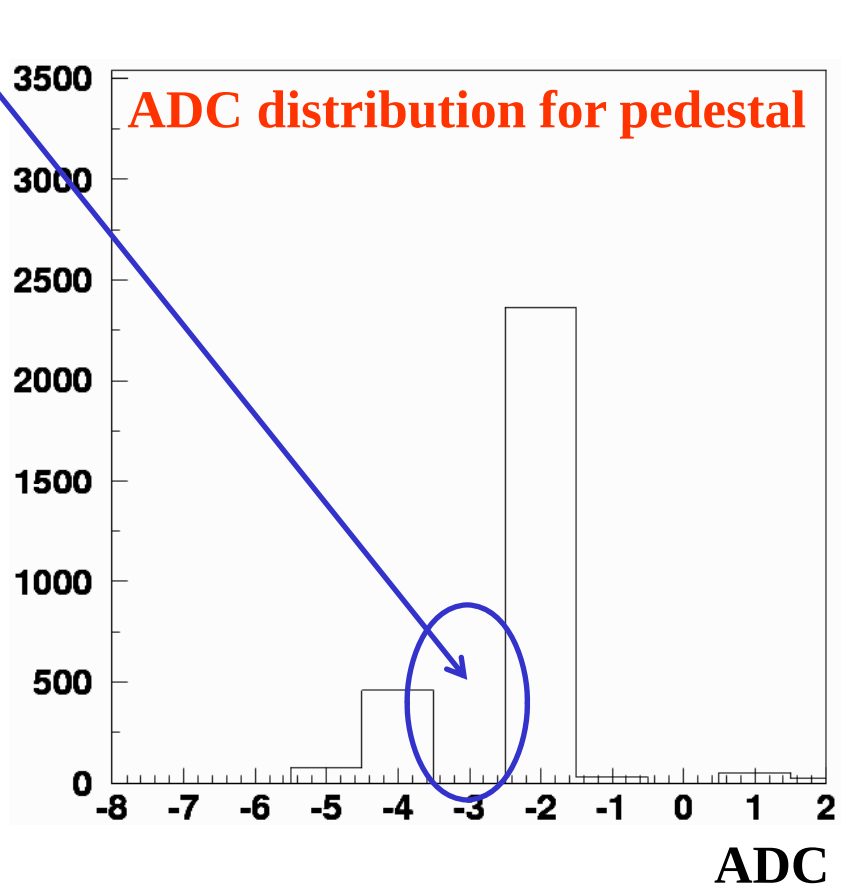
The noise level of the prototype ASIC was checked.

- Some ADC numbers are not output.

  → The reason will be checked.

The result was converted to the noise level in FPCCD:

- Requirement : <30e
- **Measurement : 40e**
  - RMS : 1.0ADC
  - 1 ADC = 0.2mV for sensor input
  - 5μV/e in FPCCD



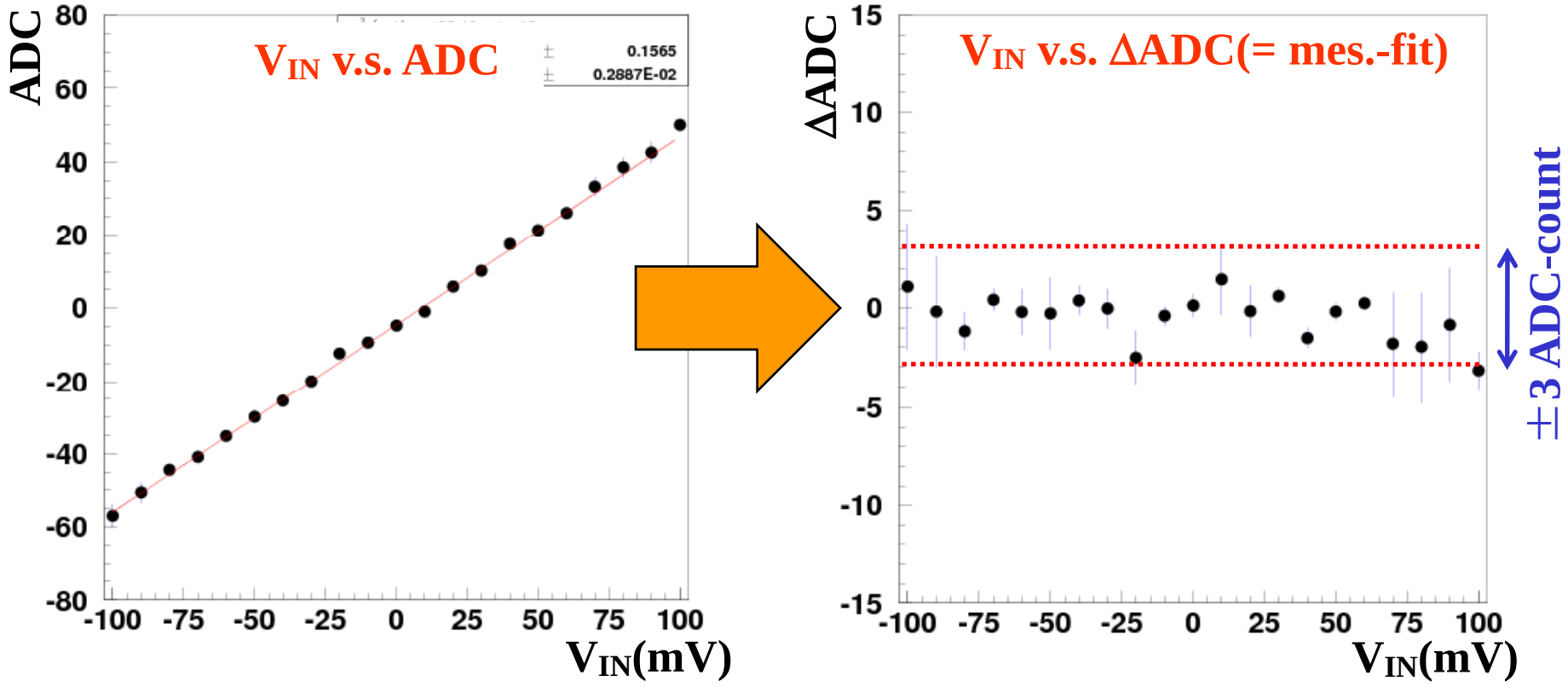
The noise level was almost acceptable.

ADC linearity

- The linearity was within ±3 ADC due to the lost ADC numbers.
  - 1 ADC = 0.05mV for sensor input

  → ±30e in FPCCD

- **The fluctuation in the linearity satisfies the requirement.**

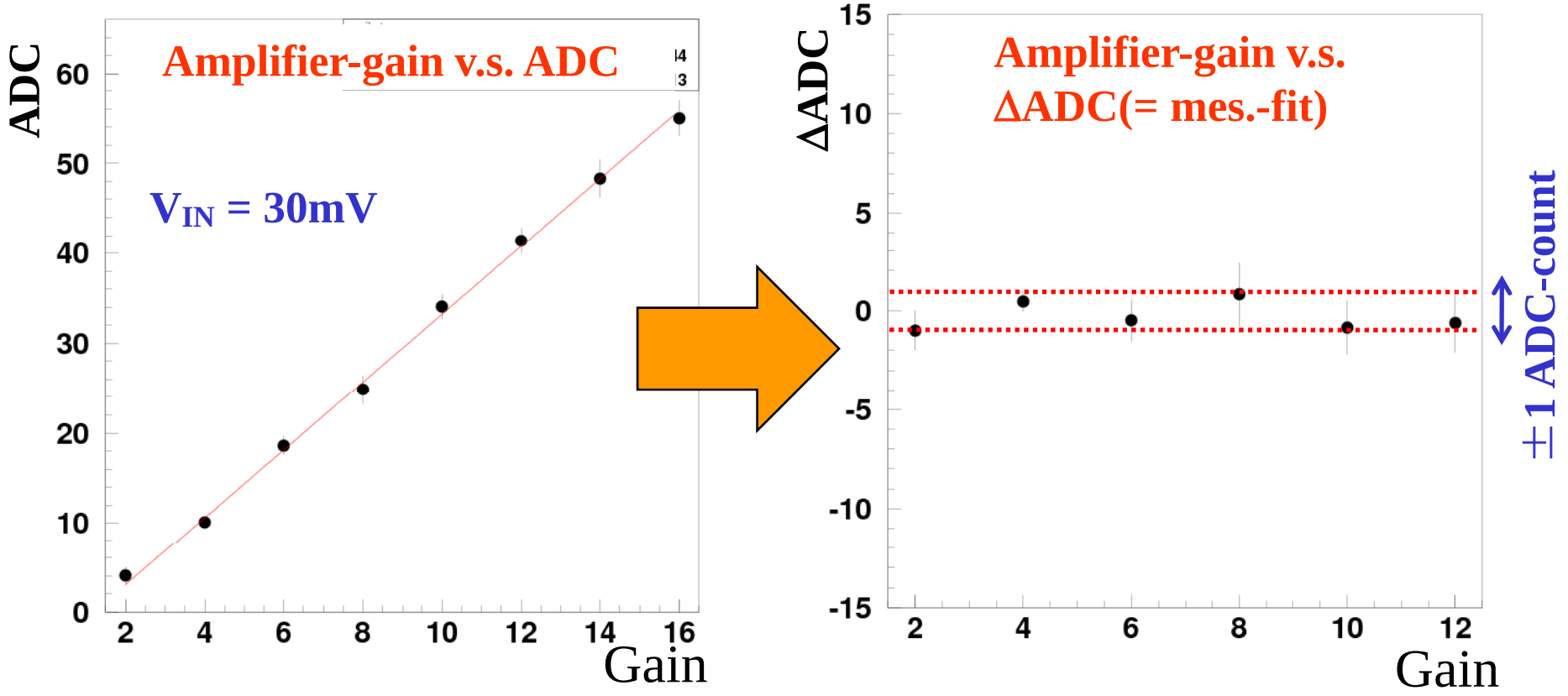


Amplifier-gain v.s. ADC

The ADC output was studied as a function of the amplifier-gain.

- The linear dependence on the amplifier-gain was obtained.
- The linearity was within ±1 ADC-count.

→ **This fluctuation is within the requirement for the noise level.**



Summary & Next step

- The FPCCD is developed for the ILC vertex detector.
- The test-sample of FPCCD sensor was produced in 2008.
  - The detail response-test will be started soon.
  - The quality will be improved for the next sample produced in this year.
- The readout ASIC was developed to read large amount of pixels in FPCCD.
  - The basic performance satisfies the requirement at the A/D conversion rate of 10kHz.
  - The readout at 10MHz is the next step.