



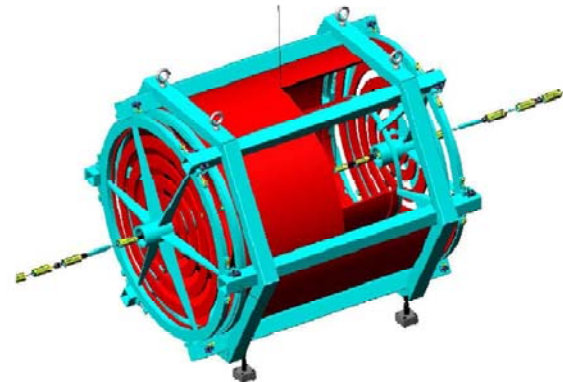
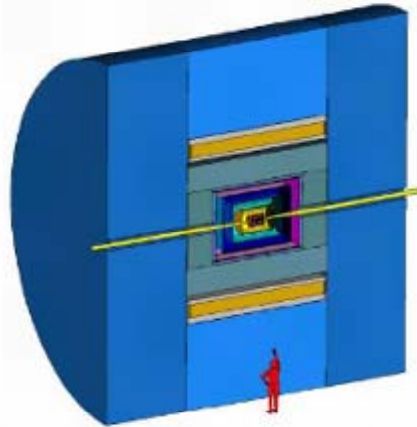
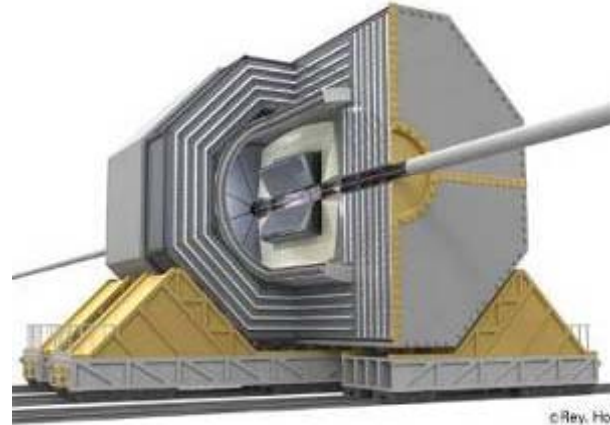
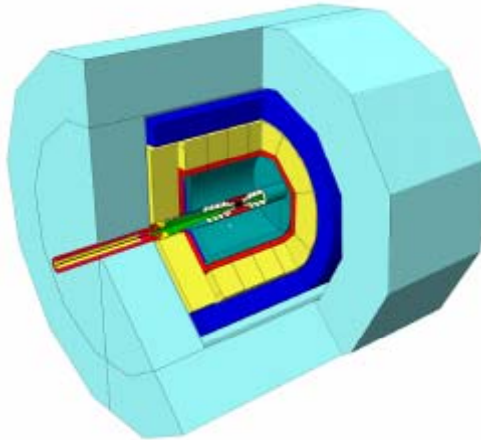
Pixel-based Vertex and Tracking Detectors for ILC

Further details in the reports of the ILC detector R&D Reviews (2007)
at http://www.linearcollider.org/wiki/doku.php?id=drdp:drdp_home

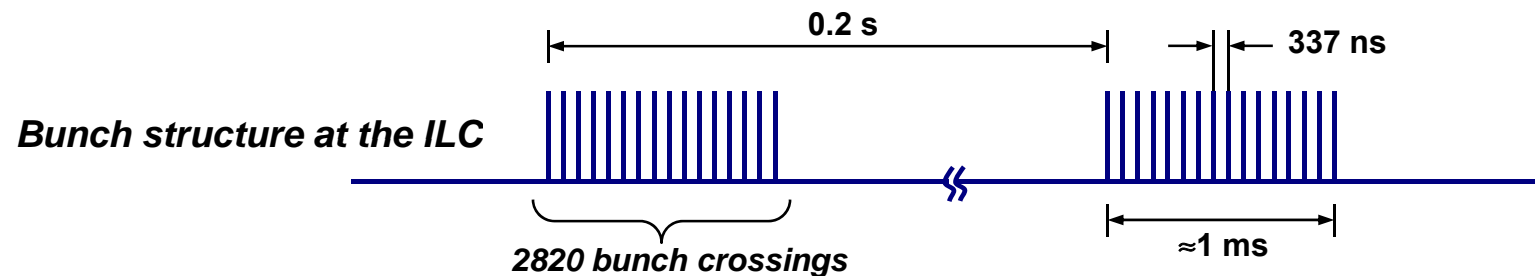
Chris Damerell
RAL



The three detector concepts

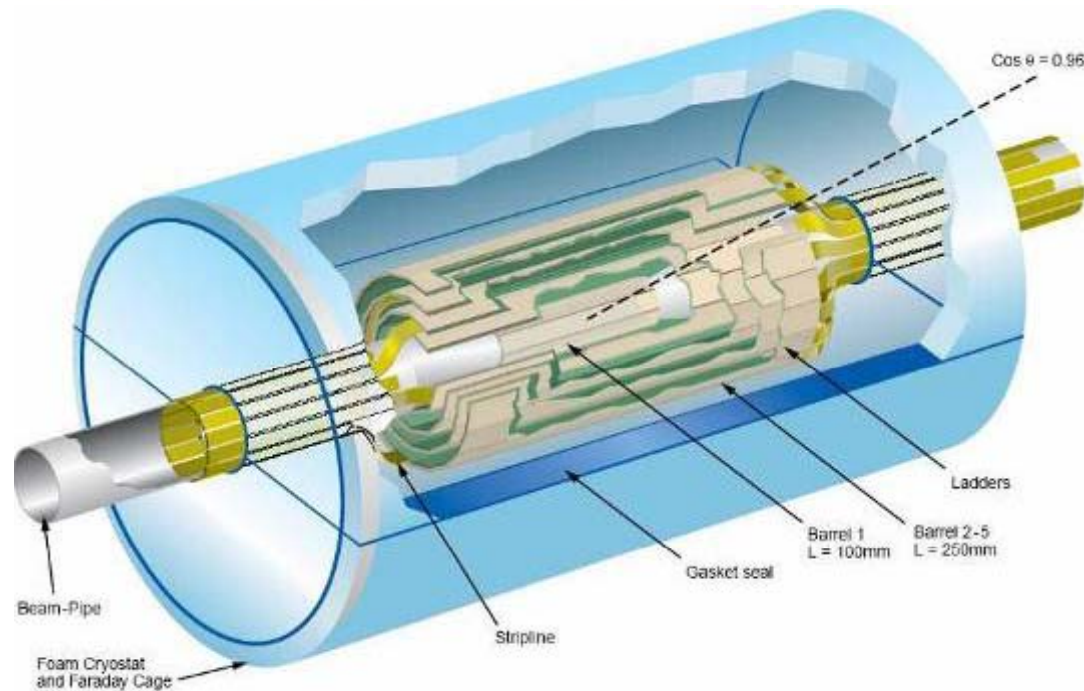


- LDC and GLD now merged into ILD for the LOI and TDR phase
- Work will lead to 'light' or 'demonstrator' or 'practice' TDRs in 2010-2012
- **Detectors to be built depend on R&D that cannot be completed before ~2012**
- Hermetic calorimetry with single bunch time-stamping is obligatory

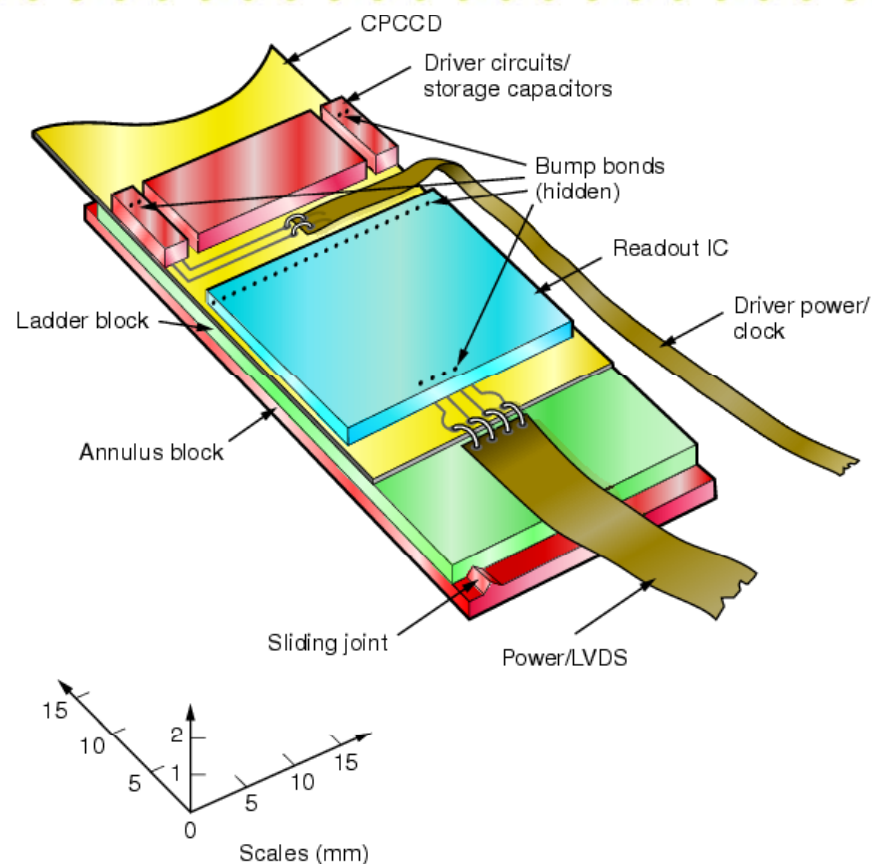


- **Detector options:**
 - Single bunch timing or time-stamping
 - Time-slicing of train (eg 10 slices at $100\ \mu\text{s}$ intervals)
 - Integrate signals through train, with relaxed readout during the inter-train period
- No 'right answer', despite statement that one should 'time-stamp everything'
- There's a power advantage in partial or complete time integration – fine sensor granularity can compensate for pileup from multiple bunch crossings
- Lower power enables reduced material budget – desirable for physics
- There's a successful history of exploiting tradeoffs between granularity and time resolution in ACCMOR and SLD collaborations
- Contrast LHC, where single bunch timing is mandatory for all subdetectors

ILC vertex detector



- Precision measurement of jet energies is not enough: which are b-jets, charm-jets or light quark jets? For the heavy quark jets, which are quarks and which anti-quarks? Latter is most cleanly established by measuring the ‘vertex charge’, pioneered with considerable success by SLD
- Achieving the required performance is the task of the most expensive ILC detector R&D topic – currently 9 options are being pursued



Optimal geometry (long barrels, or short barrels plus discs, will depend on ladder-end details that are not yet defined for *any* technology



VXD technologies

- All approaches aim for $\sim 3 \mu\text{m}$ precision and $< 40 \mu\text{m}$ 2-hit resolution
- Target material budget is $\sim 0.1\% X_0$ per layer
- They vary from single-bunch time stamping to time integrating with special compensating features
- List them in approximate order of adventurousness – one or two are more likely to be candidates for second generation upgrades

FPCCD – Yasuhiro Sugimoto (*Takubo-san, this wkshop*)

- CCD with 5 μm pixels, read out once per train; 20 times finer pixel granularity instead of 20 time slices
- Pair bgd rejected by mini-vectors indicating track direction
- Bgd rejection depends on closely spaced pairs of sensors through the barrel
- All signal processing is column parallel at ends of ladder, beyond active area
- **Possible showstopper^{**}:**
 - **real bgd rejection factor proves to be less than ~ 20 as simulated**

**** one example showstopper per project,
all agreed by the project leaders**

CPCCD – Andrei Nomerotski

- Fast readout of CCD aiming for 50 μ s frame rate
- Main novel features are column parallel readout, with bump-bond connections on 20 μ m pitch to readout chip including amp, analogue CDS, ADCs, sparsification and memory
- In addition, generating the high drive current necessitated the development of special driver chips
- **Possible showstoppers:**
 - **Unacceptable bulk of service electronics at ladder ends**
 - **Biggest threat is that full-scale ladders won't be made, due to lack of support from the UK funding agency (STFC)**

CMOS MAPS (MIMOSA) – Marc Winter

- 3T architecture, limited to NMOS transistors in pixel
- Rolling shutter – ‘row parallel’ to get the required readout rate
- Goal is 25 μ s (40 frames) on inner layer. Larger pixels on outer layers. Former may be too conservative, latter may be too optimistic. Detailed simulations needed
- Plan to use 10-20 sensors per ladder, due to yield considerations
- **Possible showstopper:**
 - **Frame-rate CDS, not robust against baseline drift and low fcy pickup**



DEEP n-well – Valerio Re (*Francesco Forti, this wkshop*)

- Full CMOS in pixel, collecting signal charge on the deep n-well that houses the NMOS transistors (triple-well process)
- In-pixel data sparsification and time-stamping with 30 μ s precision
- Goal is ~ 15 μ m pixels, so binary readout OK
- CDS achieved by in-pixel time-invariant signal processing
- **Possible showstopper:**
 - **Fall short of full min-I efficiency due to charge collection to competing in-pixel n-wells**

CAP – Gary Varner

- CMOS MAPS, with signal storage (after charge-to-voltage conversion) on in-pixel capacitors
- Aim for time slice $< 50 \mu\text{s}$ with >10 storage cells, but difficult to achieve performance with adequate noise performance
- Needs fast shaping time to accept signal from last BX before the sample. Signals are referenced to a baseline established at start of train, so there is exposure to baseline drift
- **Possible showstopper:**
 - **Insufficient pickup immunity due to charge-to-voltage conversion during the noisy bunch train**



DEPFET – Laci Andricek

- Signal charge stored on ‘internal gate’ – unique in-house technology
- Complex design – as well as sensors, need steering chips along edge of ladder, and readout chips bump-bonded at ladder ends
- **Possible showstopper:**
 - **Failure to reach required readout rate with full system**

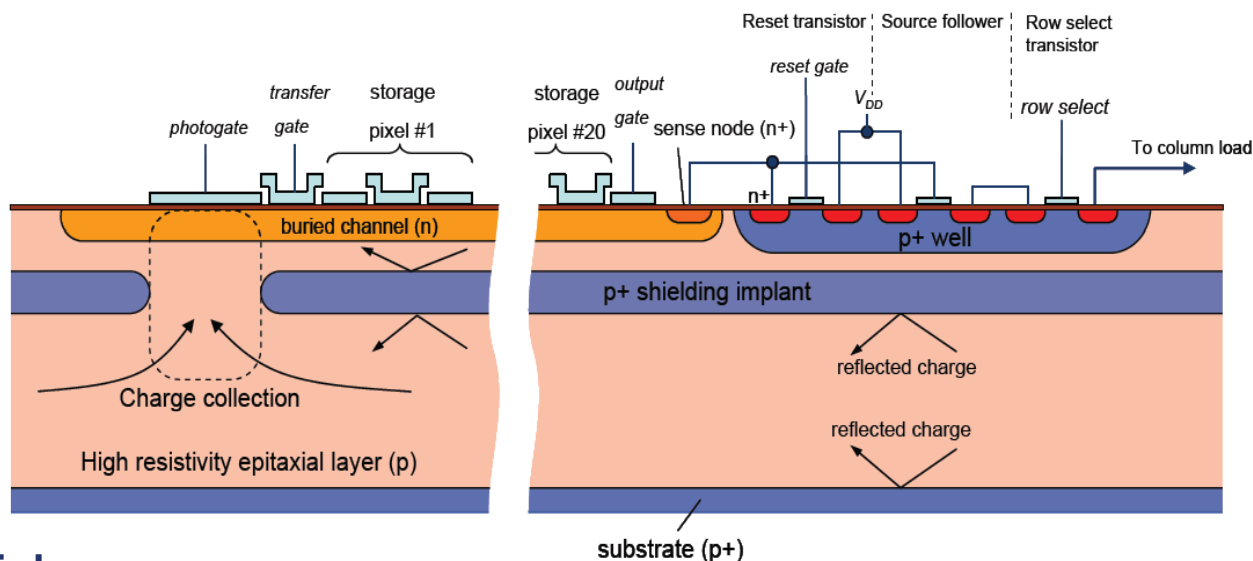


Chronopixels – Dave Strom

- Goal is to time-stamp (single bunch) by pixel functionality that can fit into a 10 μm pixel (full CMOS with 45 nm design rules)
- Deep p-well to shield the signal charge from the PMOS transistors
- Binary readout will give sufficient precision
- **Possible showstopper:**
 - **Unacceptably high power dissipation**

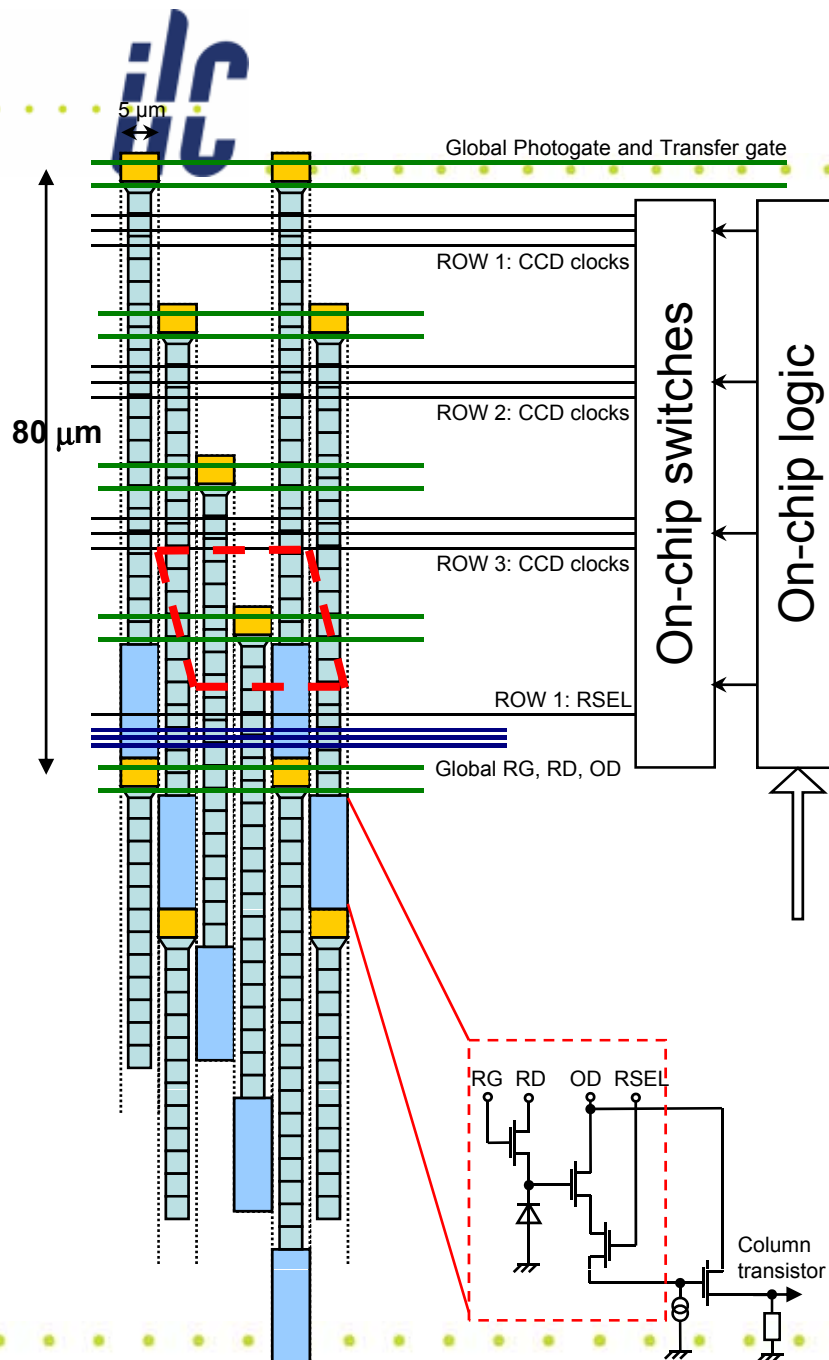
Vertically integrated pixel detectors (SOI & 3D) – Ray Yarema (Grzegorz Deptuch, this wkshop)

- An impressive strategy to be liberated from the constraints of CMOS by developing tiered systems
- Potential for data-driven systems with single-bunch time stamping, the ‘physicists dream’
- Plan is for very small pixels with binary readout, like the chronopixels
- Problems from back-gate effect with first manufacturers (Lincoln Labs) but a potentially clean solution with Tezzaron (wafer fab by Chartered Semiconductos in Singapore)
- Cu-Cu thermocompression bonding (also being developed by IBM, MIT, ...)
- Chartered currently process 1000 wafers/month
- **Possible showstopper:**
 - **4 Gpixels may exceed the power limits for gas cooling**



Operating principles:

1. Charge collected under a photogate
2. Charge is transferred to 20-cell storage CCD in situ, 20 times during the 1 ms-long train
3. Conversion to voltage and readout in the 200 ms-long quiet period after the train
(insensitive to beam-related RF pickup)
4. As in CCDs and pinned photodiode imaging pixels (aka 4 T pixels) the output gate decouples the charge collection from the charge sensing function, which can dramatically improve the noise performance
5. 1 MHz column-parallel readout is sufficient



- ISIS combines CCDs, in-pixel transistors and CMOS edge electronics in one device: **non-standard process**

- Proof-of-principle device (ISIS1) designed and manufactured by e2V Technologies – works fine

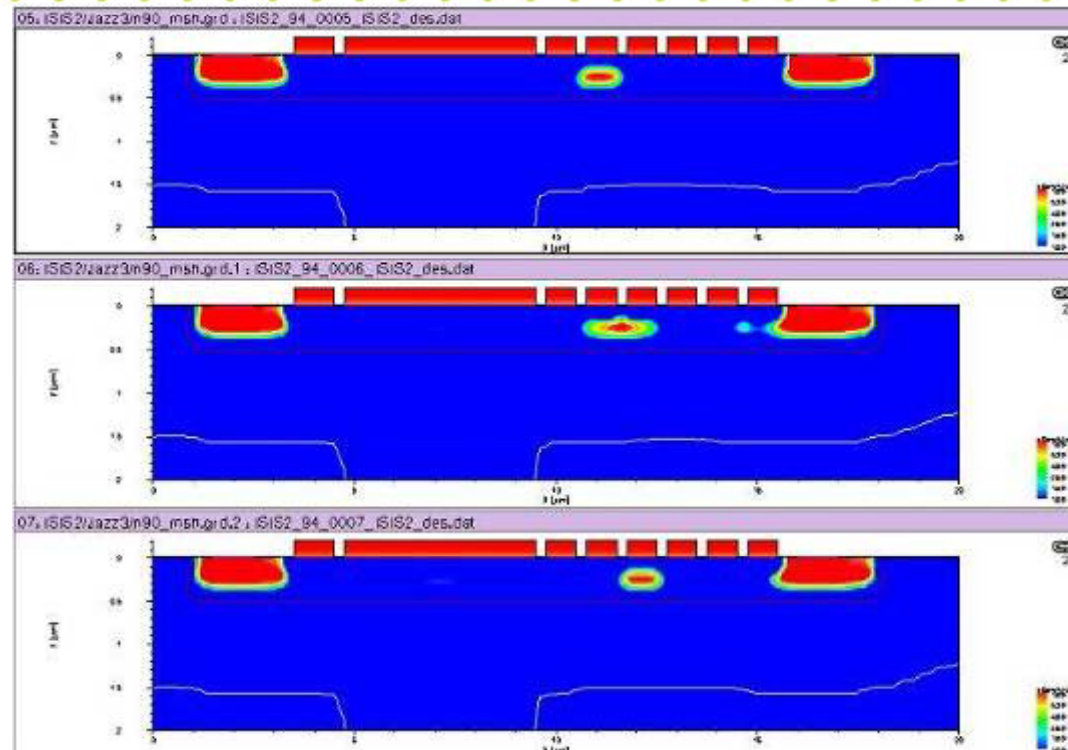
- ISIS2 (a prototype close to design goals) designed at RAL (Konstantin Stefanov and Pete Murray), due for delivery from Jazz Semiconductors next month:

- ❖ Modified 0.18 μm CMOS process with CCD-like buried channel and deep p+ implants. Single level (non-overlapping) poly for collection and transfer gates

- ❖ Jazz have had success with mixed CMOS-CCD pixel structures, for example with Jim Janesick, so we have some confidence ...

- ❖ Currently 80x10 μm storage pixel: goal is 80x5, leading to 20x20 imaging pixel as shown (slightly trapezoidal)

3-phase, pixels
~5x3 μm (WxL)



- The ISIS concept, a prior invention for optical imaging, has led to high speed frame-burst cameras for visible light – DALSA Corp. Initially 10^6 frames/s, now developing 10^8 frames/s
- These use a pure CCD process: a challenge as been to produce a CCD structure in a CMOS process. Explored since Jan 2004 with DALSA, Tower, Zfoundry and Jazz
- Jazz is restricted to a brief BC activation step (~30 s at high temperature) and to non-overlapping gates (effective gap ~0.25 μm) in their 0.18 μm opto process – see simulation above by Konstantin Stefanov



- Possible showstoppers:

- inefficient transfer from photogate to storage register (due to tails on deep p implant etc)
- poor c.t.e. within storage register (problems of buried channel and/or gaps between poly gates – *potential pockets*)
- problems scaling down to 20 μm imaging pixel
- problems stitching for full-scale devices ($\sim 12 \times 2 \text{ cm}^2$)

Most of these R&D groups plan to have full-scale ladders in test beams by 2012, as part of the demonstration of technical capability for an ILC facility able to satisfy all the performance goals set by the physics

In the vertex review, Su Dong pointed out that a mixed system, with a higher performance technology for layer-1, might be optimal for ILC

In the meantime, message to funding agencies: **don't be in a rush to down-select**

SLC Experiments Workshop 1982,
just 8 years before start of SLC

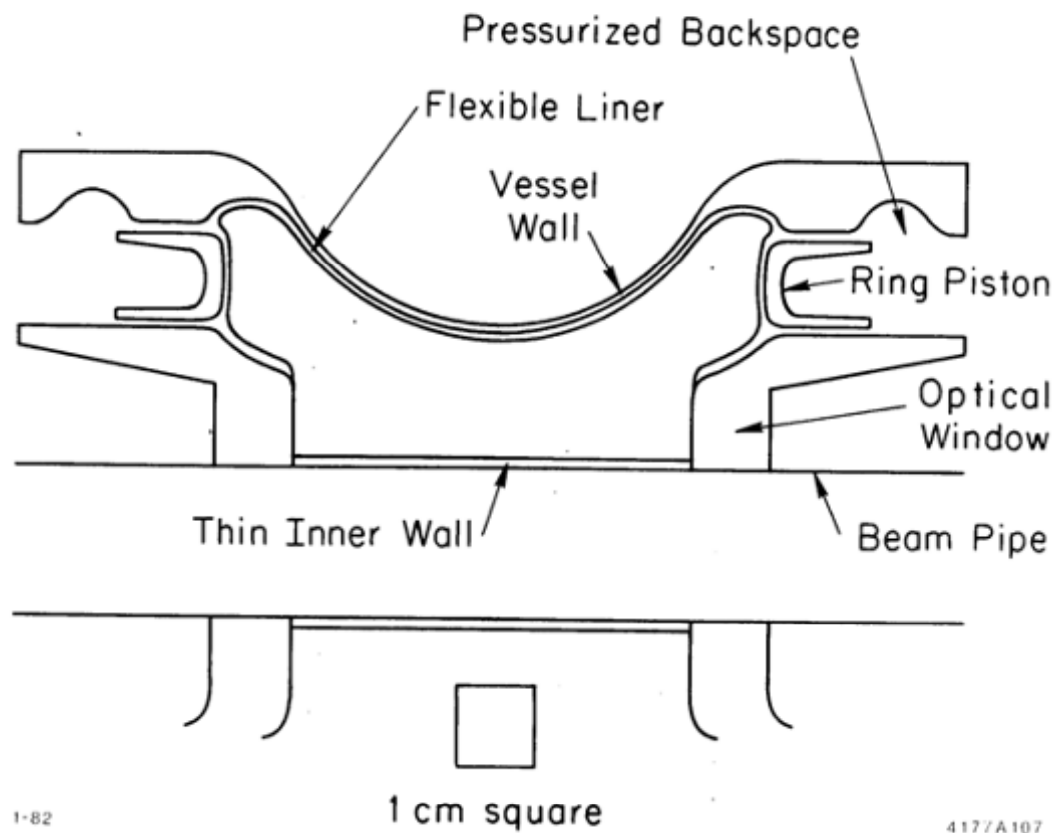


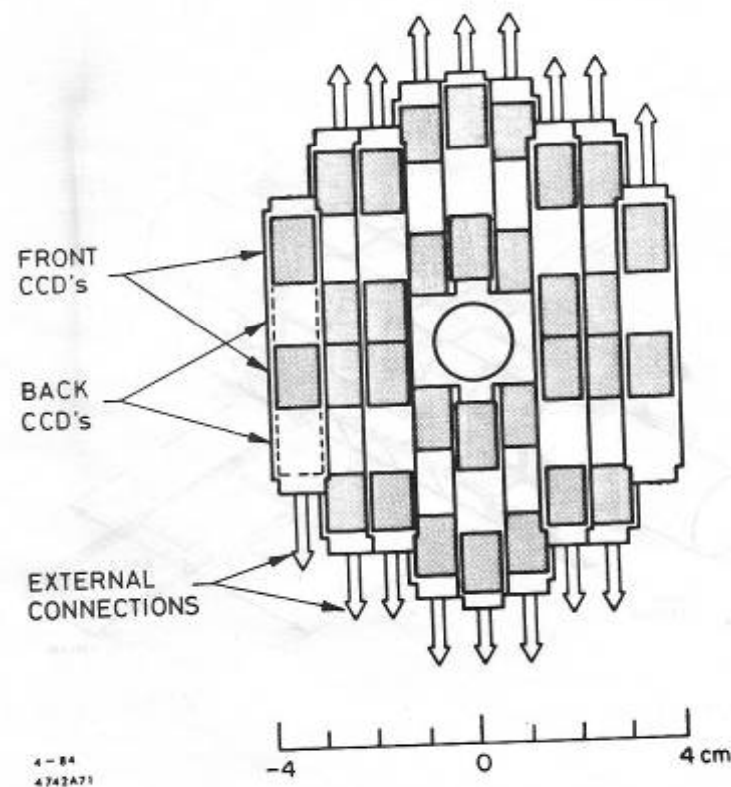
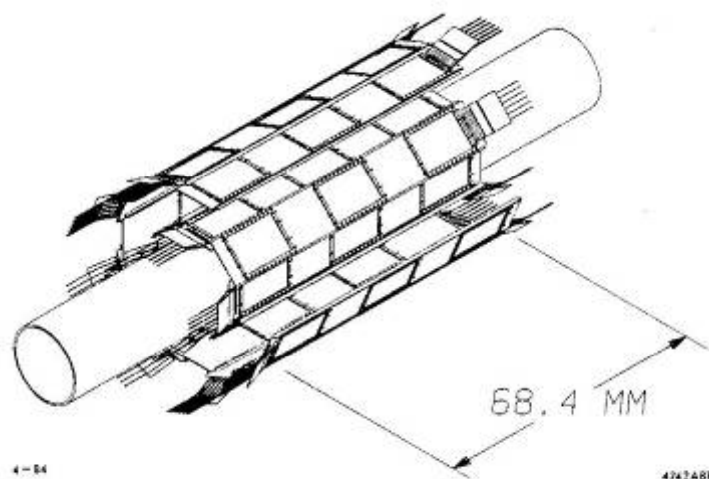
Fig. 7. Conceptual design of a propane bubble chamber vertex detector.



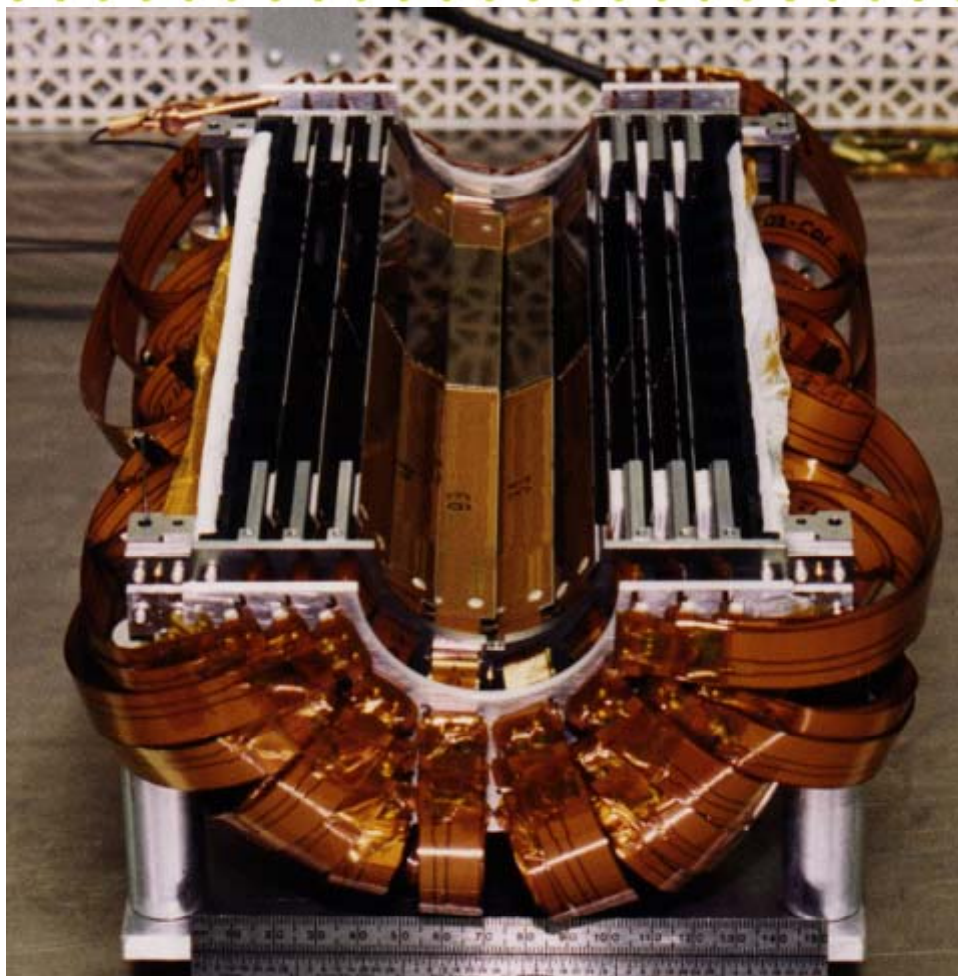
SLD's Vertex Detector Design in 1984

CCDs had demonstrated efficiency for min-I particles

R_{bp} was still 10 mm



What was installed in 1995:
307 Mpixel CCD system, with
 $R_{bp} = 25$ mm

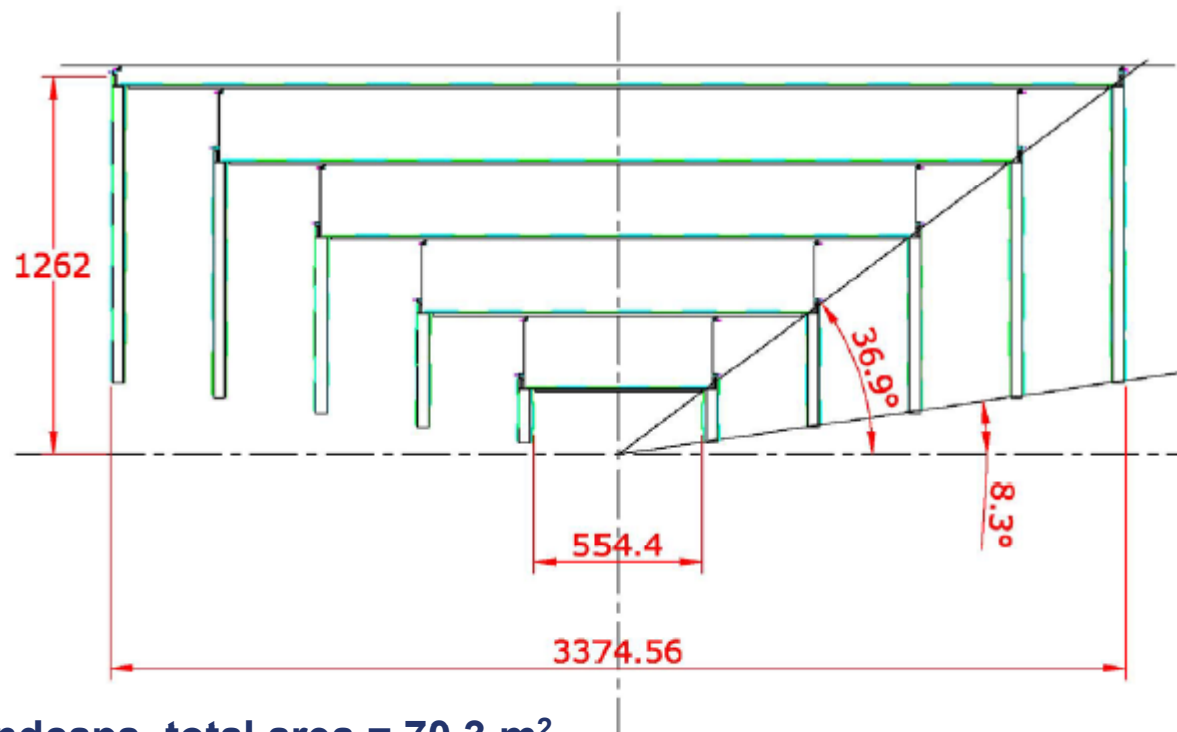




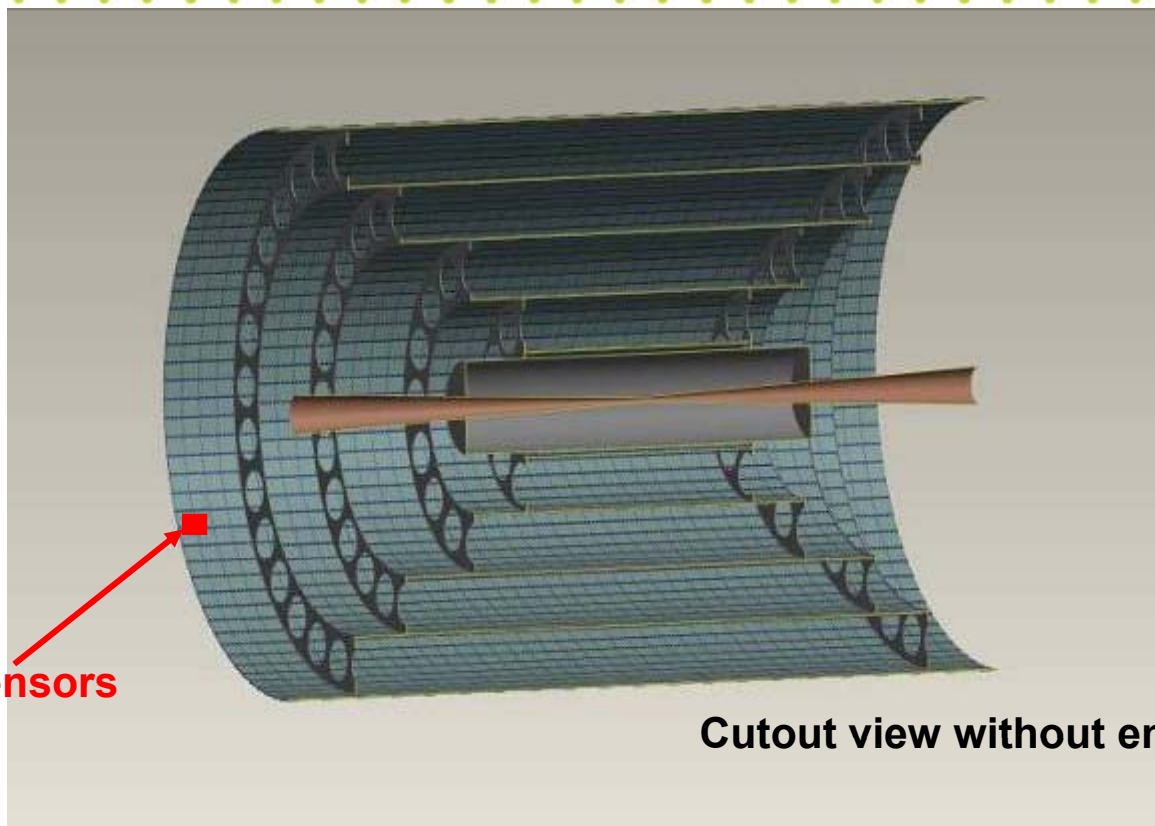
Silicon Pixel Tracker (SPT)

- The 3 concepts consider TPC, silicon microstrip tracker and a low mass drift chamber, so why even think about another option?
- **Tracking review raised concerns whether the target material budget ($\sim 0.1 X_0$ over all angles) could be realised for any of these options**
- A much higher material budget would seriously damage the ILC physics prospects
- A tracker made with *monolithic pixel sensors* could provide the thinnest layers ($\sim 50 \mu\text{m}$ Si plus support structure) and the maximum information per layer, hence require the smallest number of layers
- A major challenge could be to make such a detector with sufficiently low power to preserve gas cooling
- Suggestion to meet this challenge is to back off from time stamping and even time slicing, relying on the ECAL to label each track with its bunch number in the train

SiD tracker layout (silicon microstrips)



- 5 barrels and 4 endcaps, total area = 70.3 m²
- Everyone (?) now accepts need for standalone trk finding in this subsystem
- With 50 $\mu\text{m} \times 50 \mu\text{m}$ pixels – **28.1 Gpix system**
- Low mass support, gas cooling
- If each sensor is 8 cm \times 8 cm (2.6 Mpix): 11,000 sensors is total
- Note: forward disks will probably need time stamping, due to high bgd



one of 11,000 sensors
8x8 cm²

Cutout view without endcaps

- SiC foam support ladders, linked mechanically to one another along their length
- 5 **closed cylinders** (incl endcaps, not shown) will have excellent mechanical stability
- ~0.6% X_0 per layer, 3.0% X_0 total, over full polar angle range, plus <1% X_0 from VXD system (goal)
- 30 Gpixels is in line with trends in astronomical wide-field focal plane systems by 2020

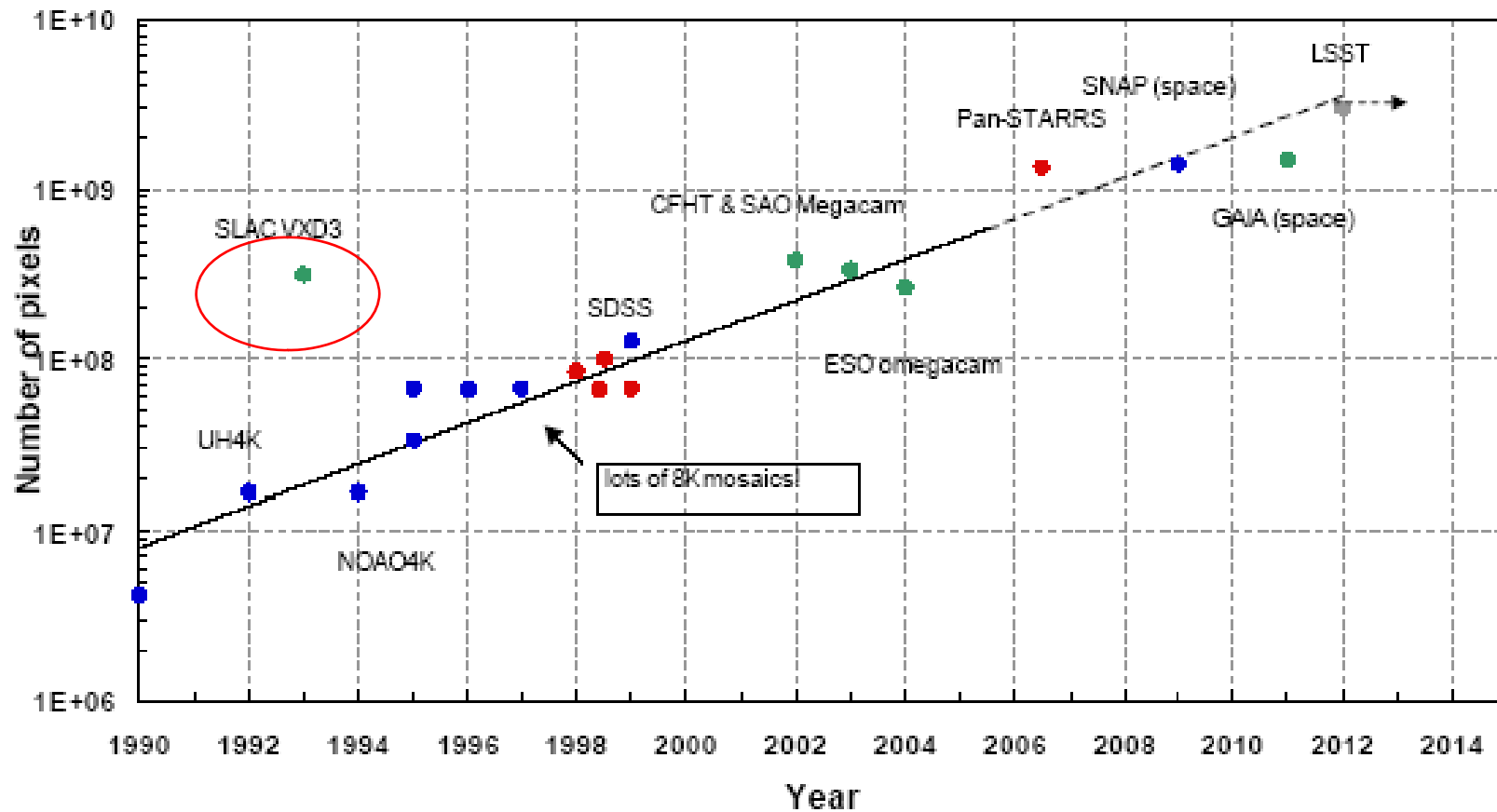


Illustration of focal plane sizes, from Luppino/Burke 'Moore's' law

Focal plane size doubles every 2.5 years

From: Burke, Jorden, Vu, SDW Taormina 2005



SPT technologies

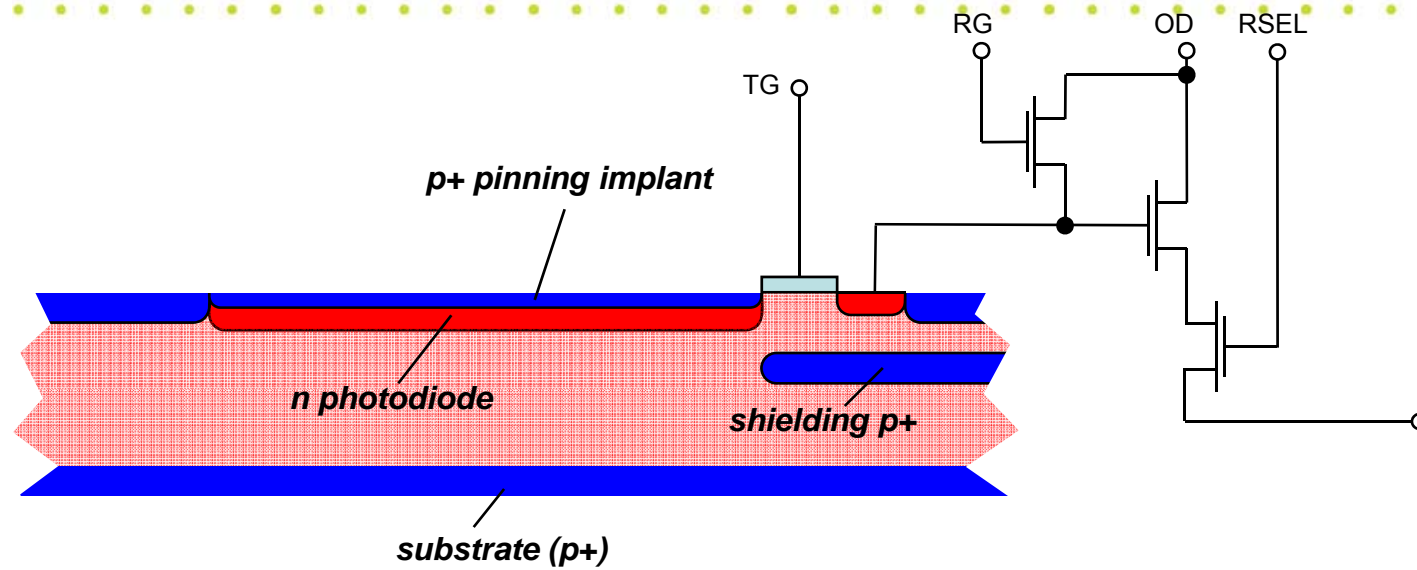
All options aim for $\sim 15 \mu\text{m}$ precision with binary readout of $50 \mu\text{m}$ pixels

Similar area coverage to ATLAS SPT, but 5000 times more channels, 30 times less power, 20 times less material. Is this feasible?

CCD – Konstantin Stefanov

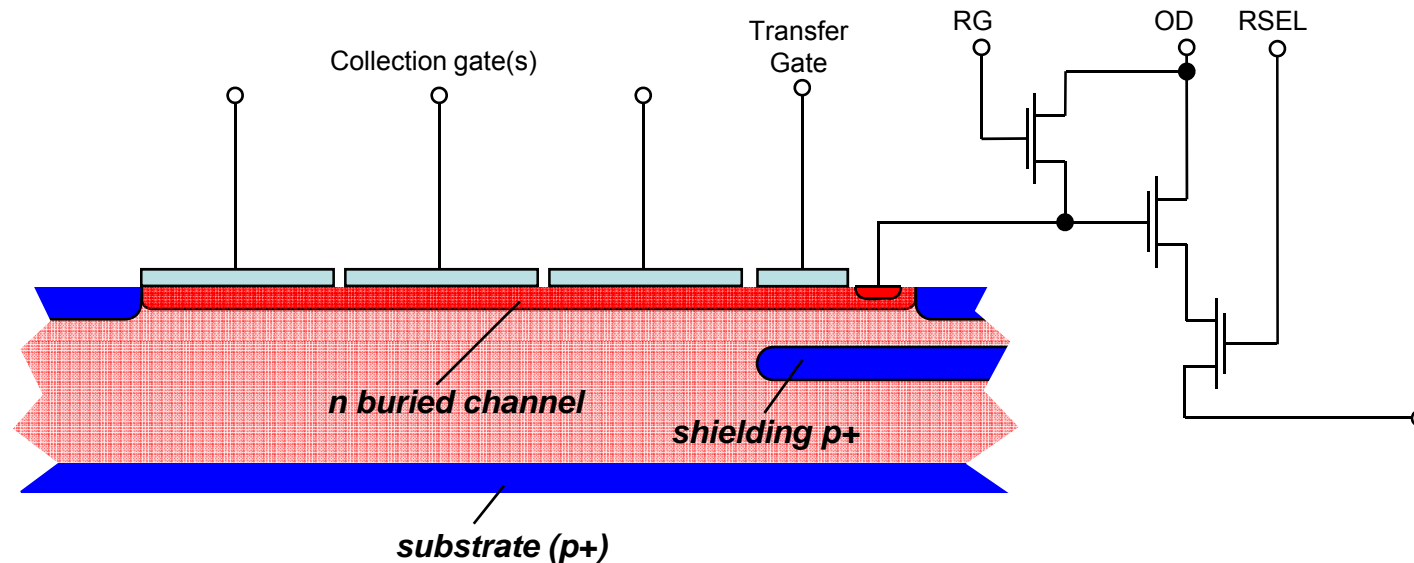
- Reasonably confident in 100% min-I efficiency, though it hasn't been demonstrated
- Total in-detector power dissipation $\sim 600 \text{ W}$ is fine for gas cooling
- LSST (3.2 Gpixels) being prototyped by e2V, will be a valuable 10% demonstrator

Pinned Photodiode (PPD or 4T) - Konstantin Stefanov



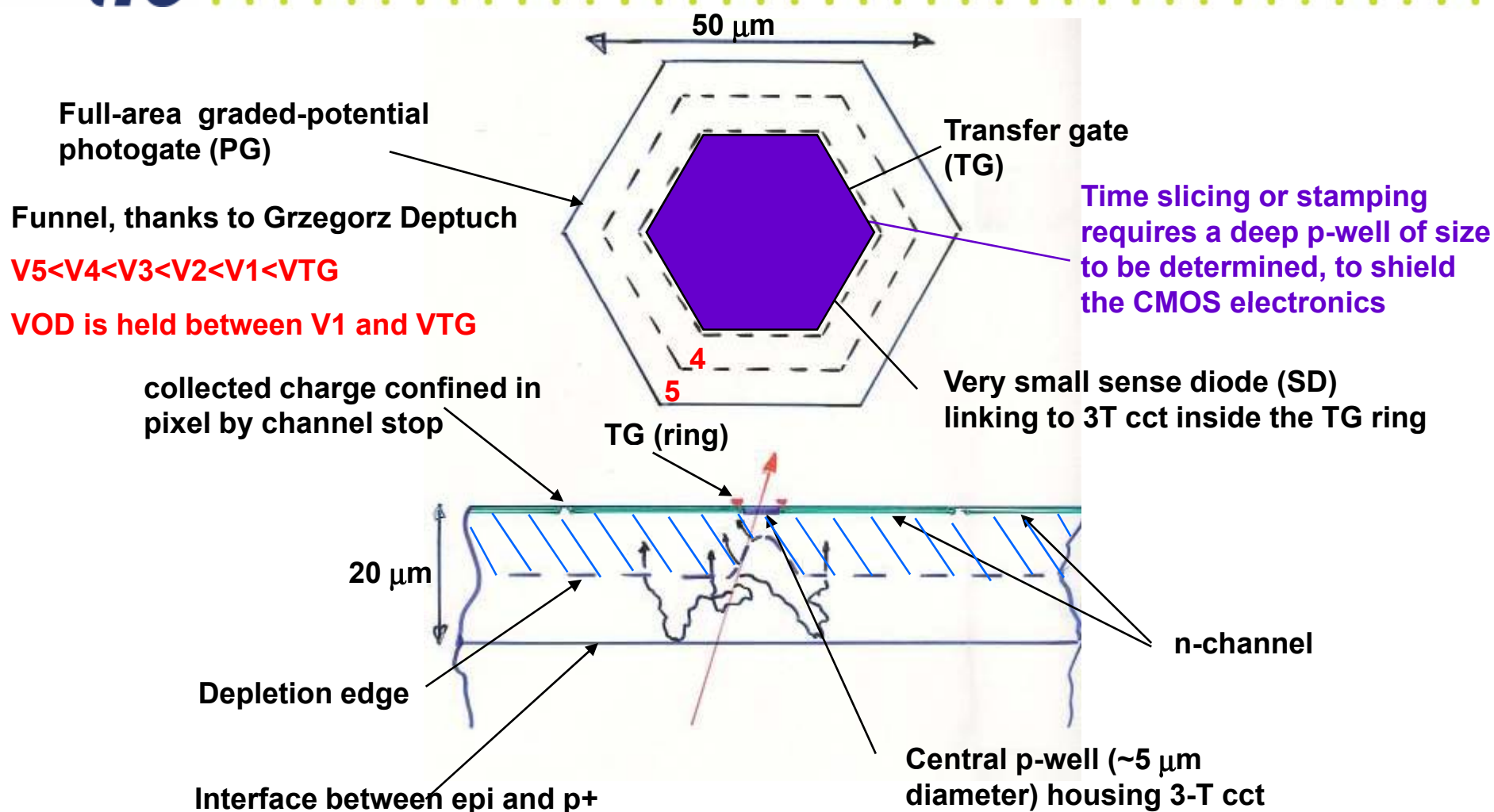
- PPD IP offered since ~5 years ago by numerous foundries for imaging
- Pinning implant results in fully depleted n layer
- Charge transfer gate TG decouples charge collection from sensing, permitting correlated double sampling and low noise (10 e- ENC quoted)
- Large area PPD pixels being developed at RAL
- Possible problems with *inefficient* transfer induced by small potential fluctuations in the photodiode area

Photogate (PG) - Konstantin Stefanov



- Charge transfer allows correlated double sampling and low noise (10 e- possible)
- **LCFI is developing the underpinning technology for the ISIS**
- Charge transfer is fast due to funnel action (next slide)
- Possible problems with inefficient transfer due to barely buried channel and inter-gate gaps (consequences of developing a combined CCD-CMOS process)
- Hope of success with Jazz Semiconductor – currently merging with Tower

PG pixel – possible layout



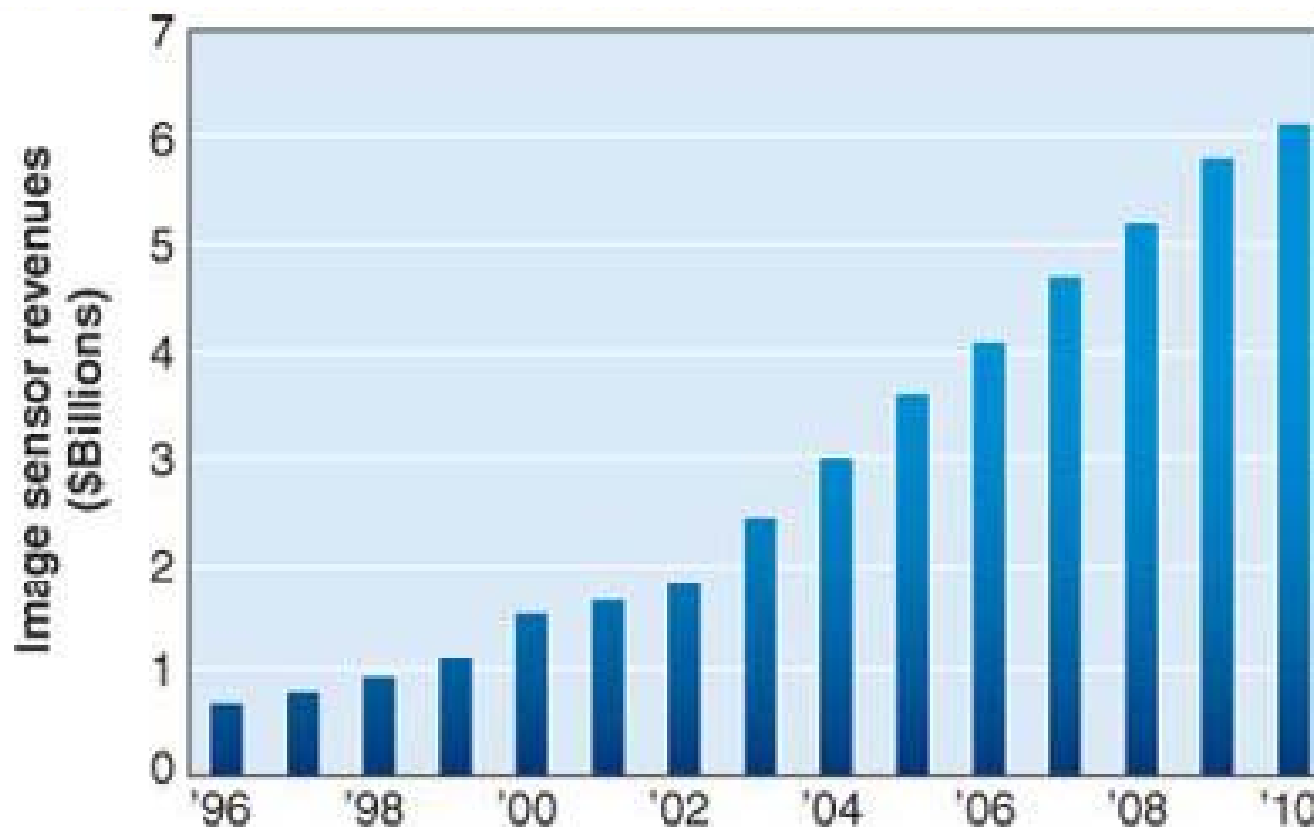
Note: Charge collection directly to TG contributes to the signal. Unwanted charge collection directly to the tiny sense diode may be negligible, so a *shielding deep p-implant may not be needed*



Conclusions

- As in optical imaging sensors, the increasing availability of **CCD structures in CMOS processes** is opening new windows for vertex detectors and particle tracking systems
- For an ILC tracker, such structures would permit the accumulation of one or more packets of signal charge, integrating or time-slicing the bunch train, followed by readout in which the charge sensing process is decoupled, both in terms of sense node capacitance and in time (allowing leisurely readout in the quiet period between bunch trains) – excellent noise performance
- Logically this is the opposite of ‘pulsed power’; the readout is inactive through the noisy bunch train, and proceeds steadily through the inter-train period.
Average power is probably easily compatible with gas cooling
- As well as unprecedented vertex detector capability, the requirement of excellent tracking performance, with a detector that is effectively **transparent to photons over the full polar angle range**, can probably be realised
- The ILC is a good candidate to benefit from these developments, which will be applicable elsewhere, for example **fast-burst imaging of X-rays**
- Maybe 3% of the tracker (fwd disks) will need time stamping, the break point to be determined by simulations

Additional material

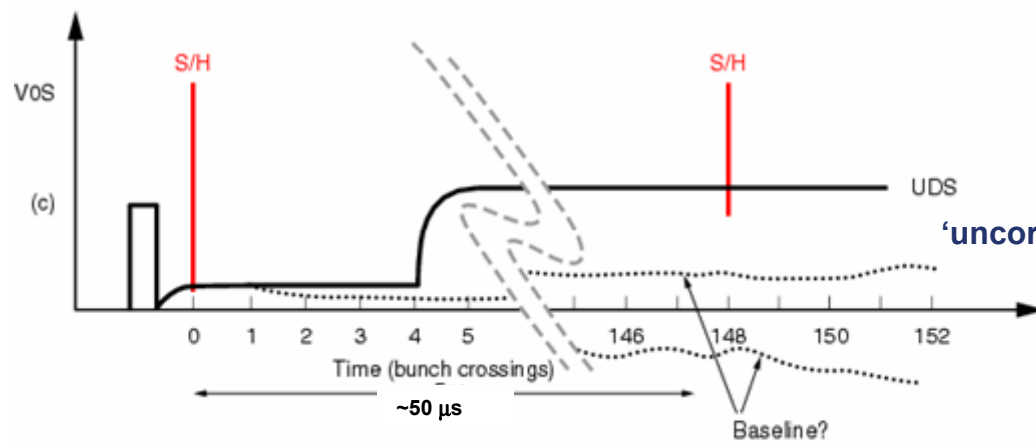
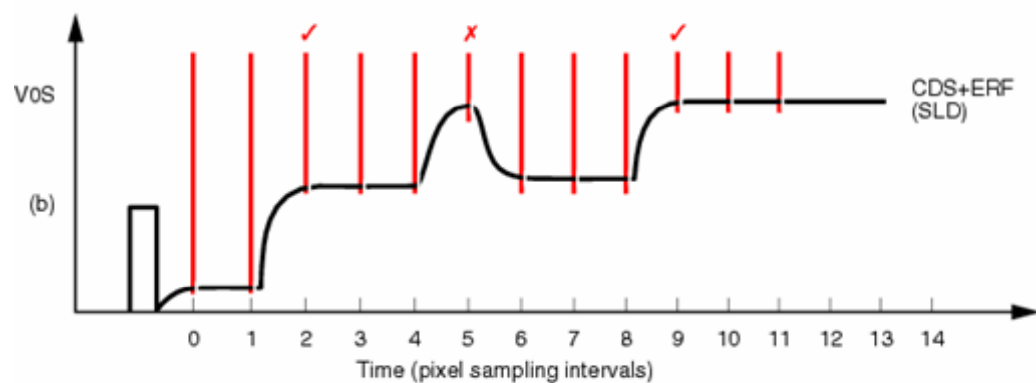
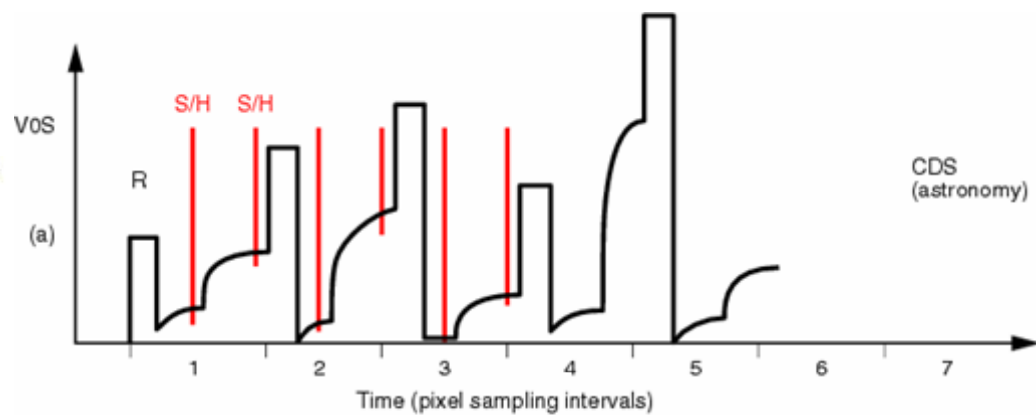


As with developments in microelectronics, we (the particle physics community) are now small fish in a very large pond.

In the '50s and 60s, fast electronics was synonymous with 'nuclear electronics'

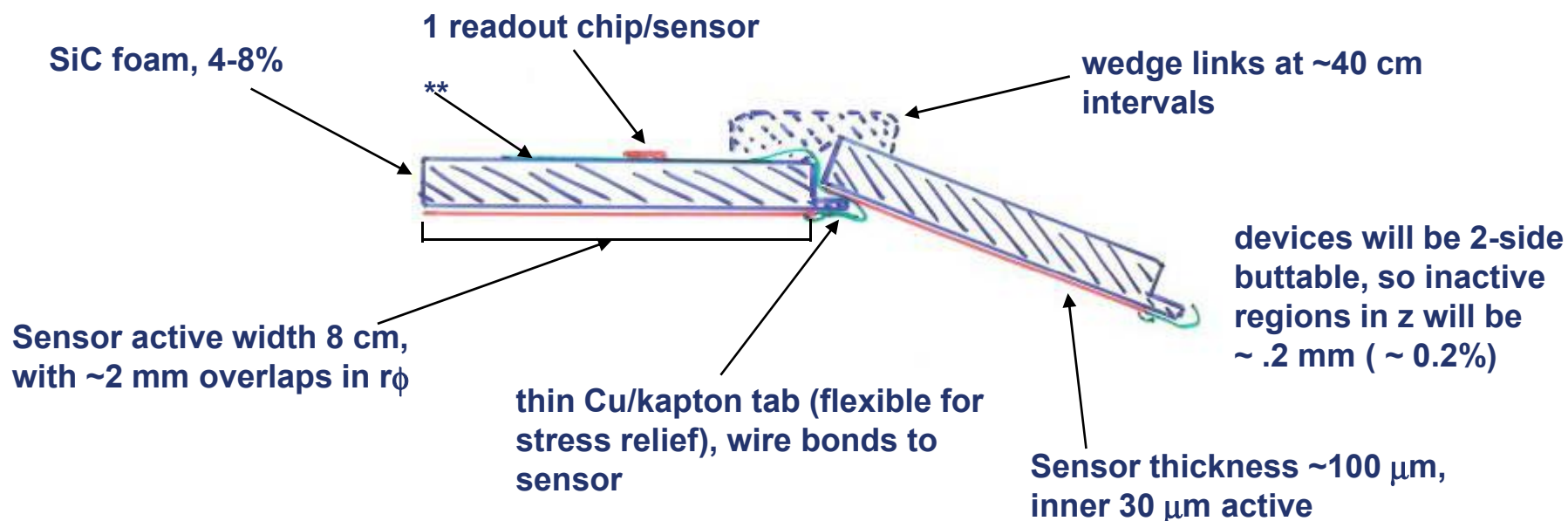
These days, progress driven by consumer markets is much faster.

We scientists can take advantage of this ...





End view of 2 barrel ladders ('spiral' geometry)



** single layer Cu/kapton stripline runs length of ladder, double layer in region of tabs (~5 mm wide) which contact each sensor. Single Cu/kapton stripline runs round the end of each barrel, servicing all ladders of that barrel

Bottom line: potential material budget $\sim 0.6\%$ X_0 per layer, but much design and R&D needed to establish mechanical stability, including shape stability wrt push-pull operations (taking advantage of stress-free 3-point kinematic mount)

