DHCAL

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R&D is in framework of the CALICE collaboration

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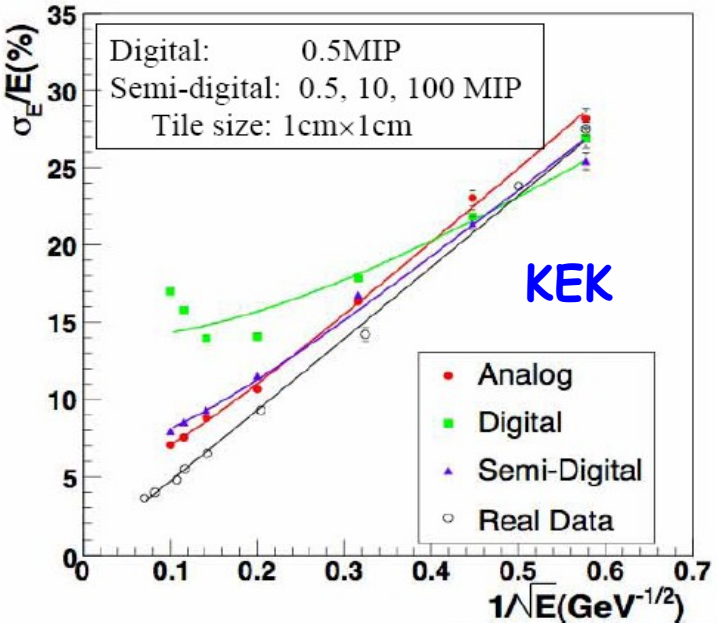
Contents of presentation

- DHCAL
- μMegas
- Readout electronics
- Test beam experiments
- M^2 prototype and M^3 simulation
- Conclusion

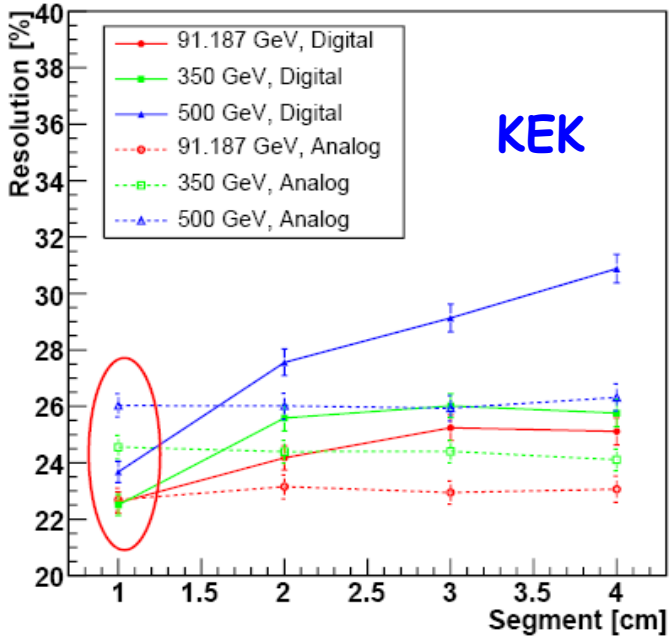
Digital hadronic calorimeter

DHCAL concept:

- Digital readout allows construction of high granular hadronic calorimeter
- This leads to better PFA performance (hadronic shower separation)
- Gaseous detectors are well suitable choice for DHCAL
- Cheap and robust detectors are under development:
  - Europe – *μMegas* and RPC
  - US – RPC and GEM
- DHCAL has energy resolution performance comparable with AHCAL



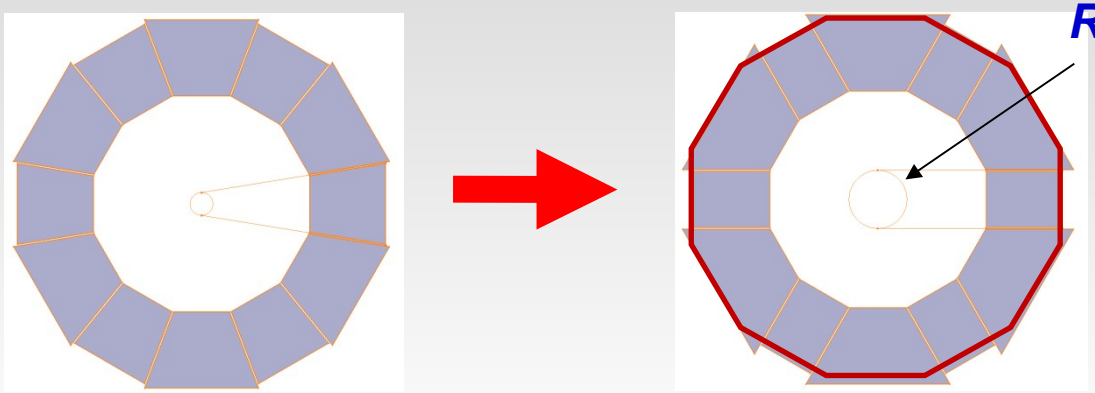
Hadron energy resolution



Jet energy resolution

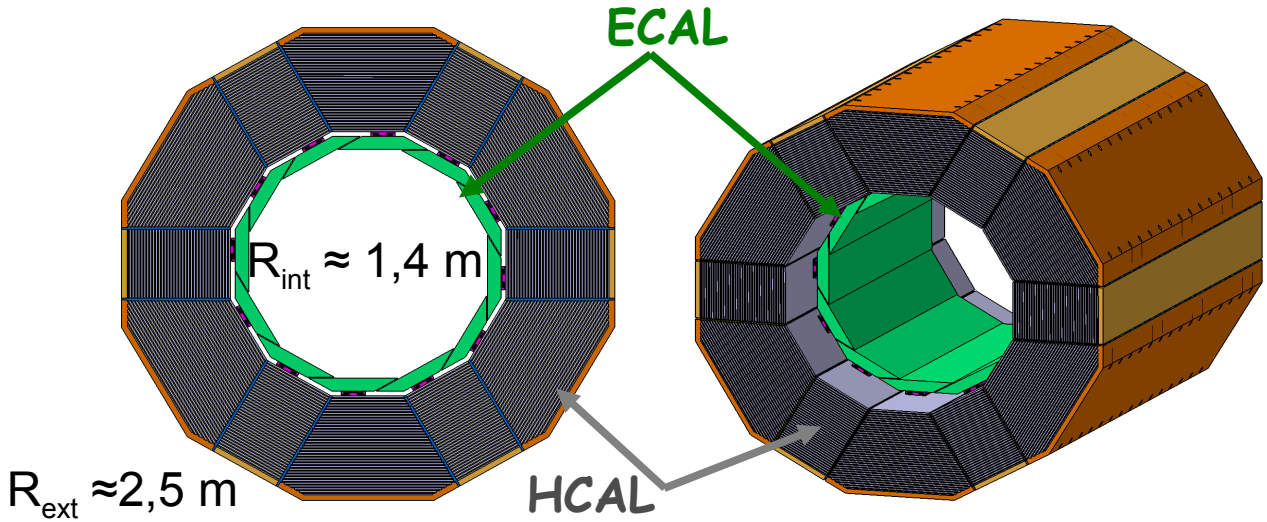
New SiD HCAL geometry

Symmetric geometry – optimization (LAPP)



Internal shell is identical with ECAL

Assembly proposition



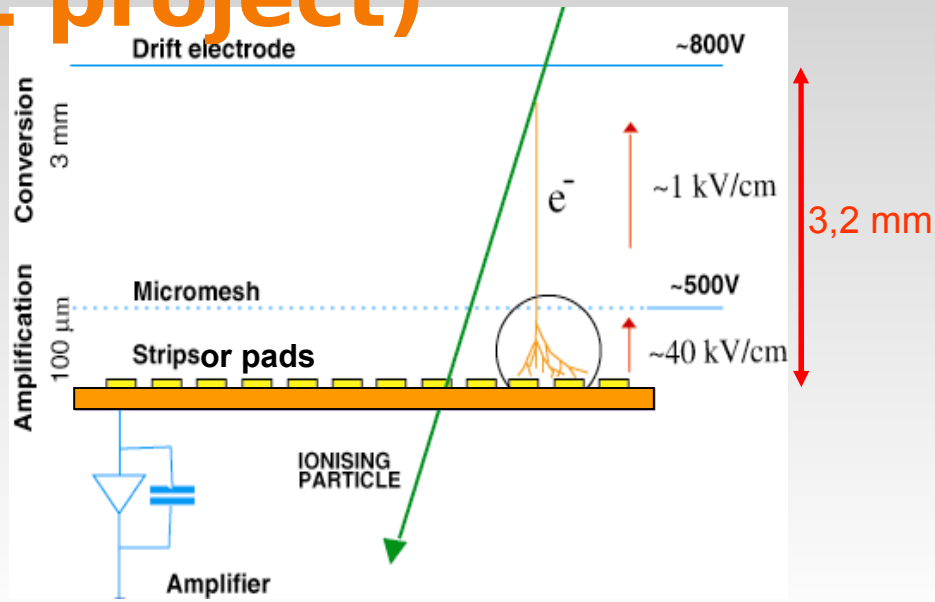
HCAL represent ~3000 m² of active area and ~30M channels of 1cm²

New off-pointing geometry of DHCAL has been approved by SiD collaboration

MicroMEsh GAseous Structure (EuDHCAL project)

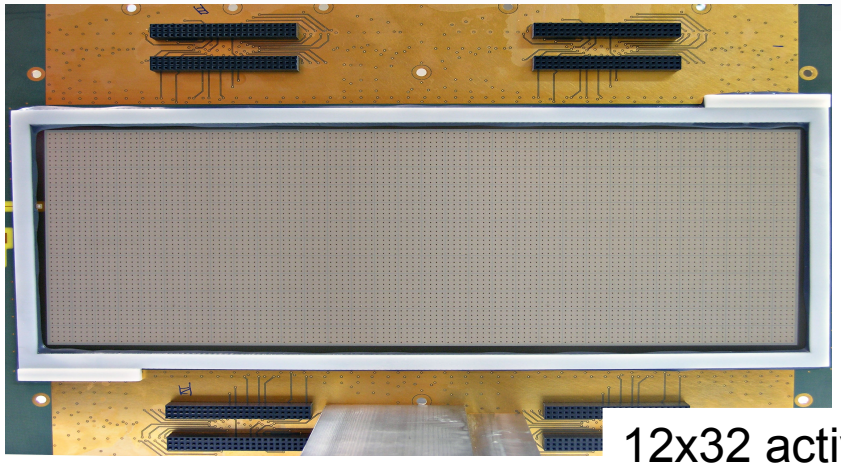
µMegas characteristics

- Gas (Argon + Isobutane)
- Hight voltage < 500 V
- High rates
- Robust, relatively low cost
- Thickness 3.2 mm



µMegas prototypes at LAPP

- Bulk technology
  - Mesh – 325 LPI
  - Spacers: 120 µm height
    300 µm diameter
  - Pads: 1x1 cm^2
- The chamber
  - Stainless steel with copper cathode
  - 95% Argon + 5% Isobutane
  - 3 mm conversion volume
- Read out: gassiplex, hardroc, dirac



12x32 active pads

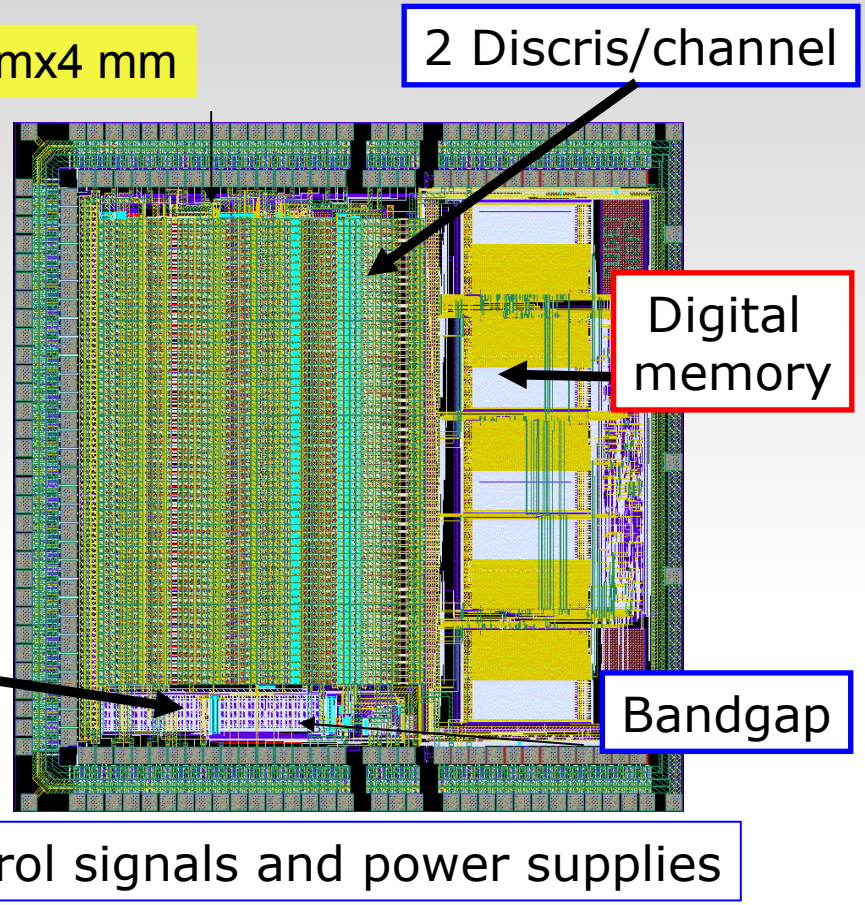
µMegas prototypes:

- Analog readout: - 3 chambers 6x12 pads
  - 1 chambers 12x32 pads
- Digital readout: - 4 chambers 8x32 pads
  - 1 chamber 8x8 pads

Readout electronics - HARDROC

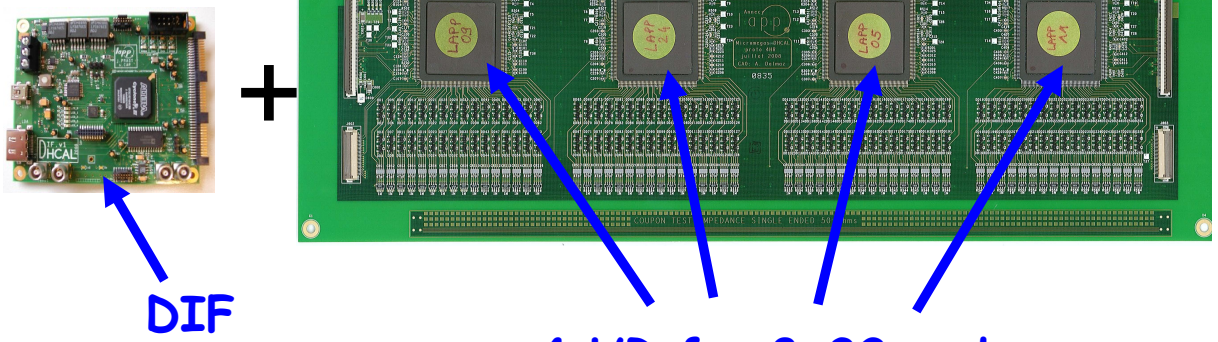
Hardroc 1 (2) (LAL)

- ASIC developed for RPC readout
- AMS SiGe 0.35 µm technology
- Analog and digital readout
- 1 chip (16 mm², 19 mm²) – 64 channels
- 2 (3) thresholds in 10 bit precision
- Digital memory for 128 events
- Gain 2^6 (2^8) – 10 fC to 1 pC (5 pC to 10 pC)
- Crosstalk < 2%
- Low consumption - < 10 µW/channel
- Power pulsing < 0.5%



DIF board (LAPP)

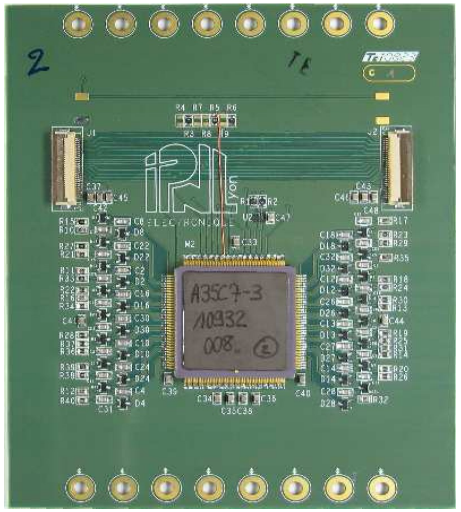
- Control data from up to 100 VFE (hardroc and dirac) chips
- Store and send data to DAQ
- Provide USB connection to PC

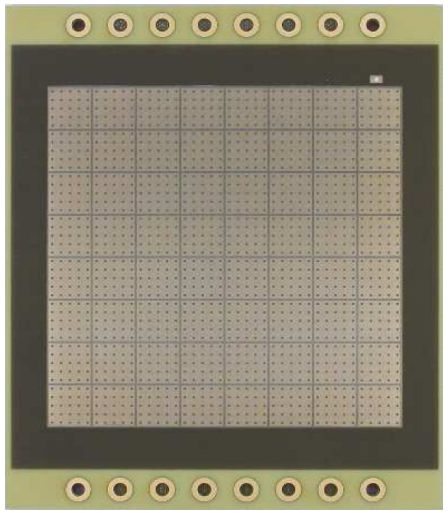


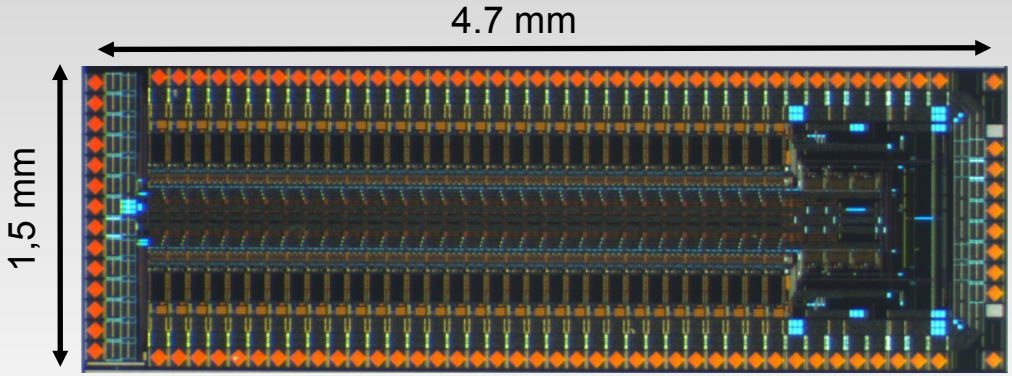
Readout electronics - DIRAC

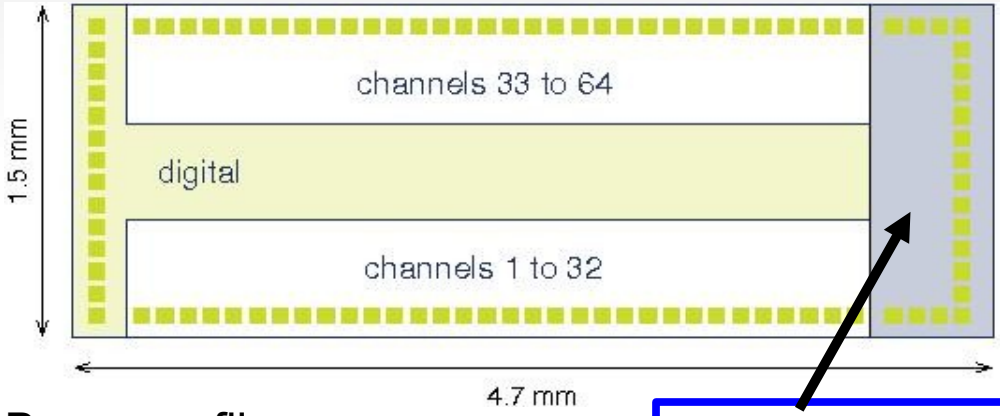
Dirac (IPNL)

- ASIC developed for μMegas readout
- AMS CMOS 0.35 μm technology
- Digital readout
- 1 chip (7 mm²) – 64 channels
- 3 thresholds in 8 bit precision
- Digital memory for 8 events
- 2 gains – 3 fC to 200 fC (100 fC to 10 pC)
- Low consumption - < 10 μW/channel
- Power pulsing < 1%



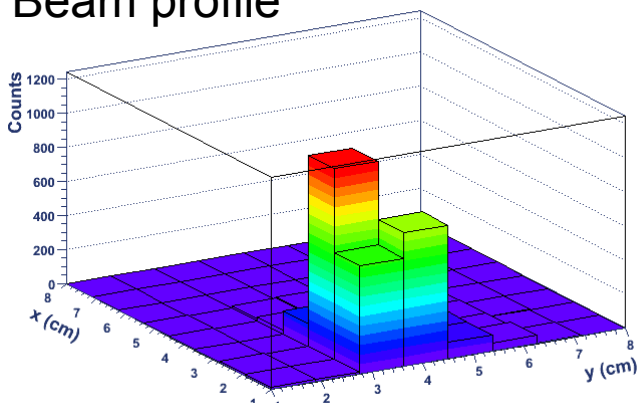






DACs
Power pulsing
Power supplies
Analogue control

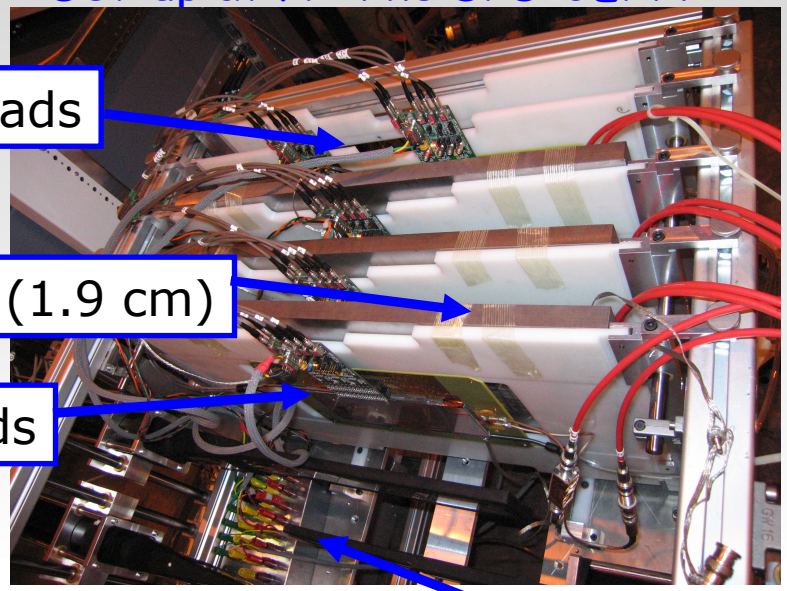
Beam profile



Dirac has been tested in test beam 2008 with 8x8 pads

Test beam

Set-up at H2 line SPS-CERN



Main objectives

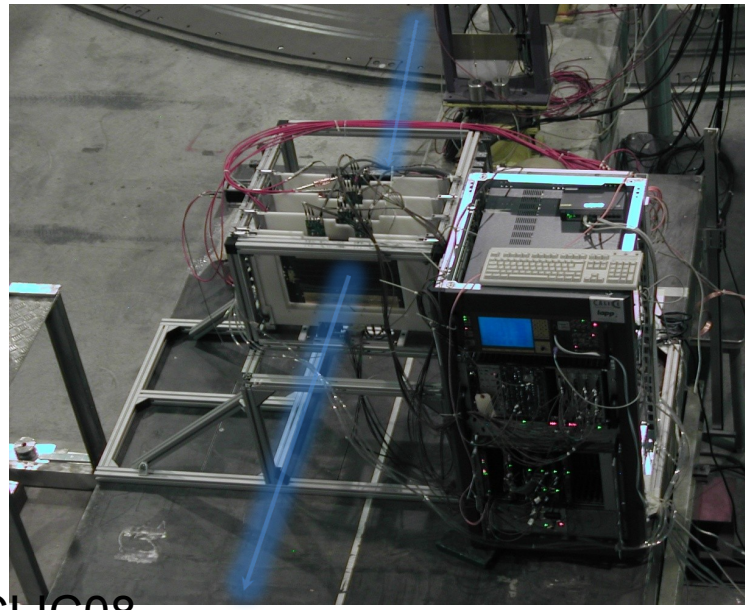
- Prototypes disparity
- Pad homogeneity
- Efficiency and multiplicity
- Crosstalk study
- Behavior in hadronic shower

Set-up

- 3 chambers 6x16 pads
- 1 chamber 12x32 pads
- Analog readout (gassiplex)
- DAQ: centaure (subatech, Nantes)
- Slow control
  (HV, gas distribution, temp.)

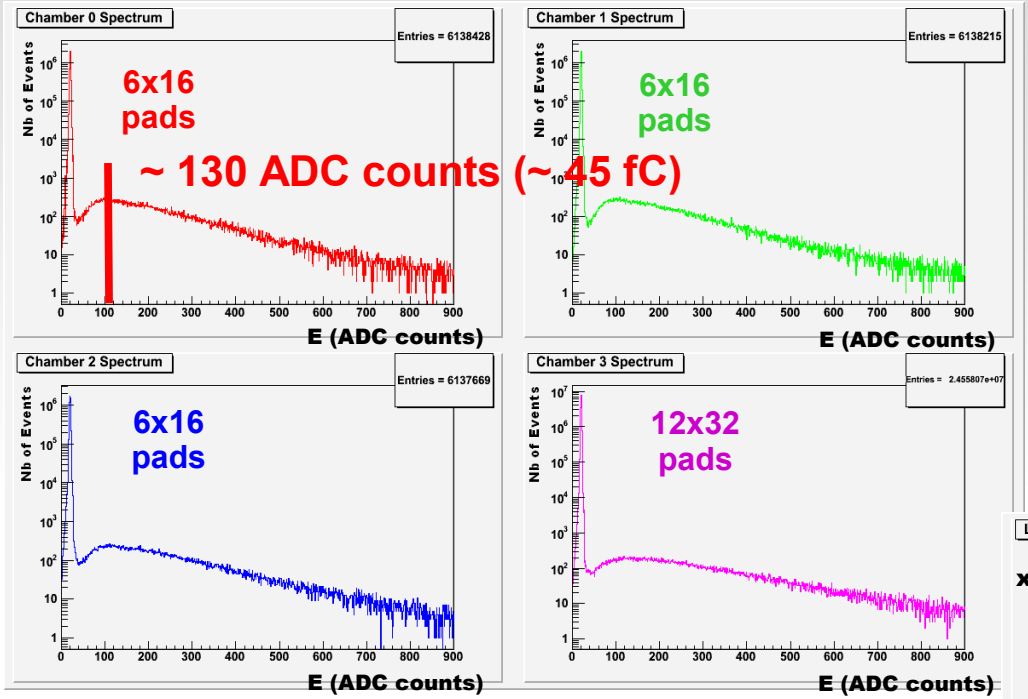
Test beam data

- 50 and 200 GeV pions
- 200 GeV muons
- 200 GeV pions with and without iron absorber in front of the system

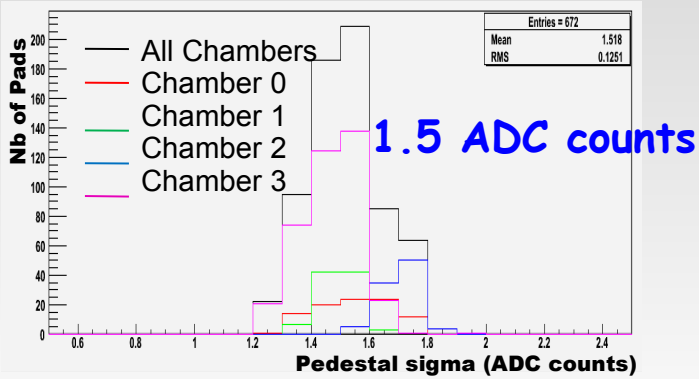


MIP signal and noise performance

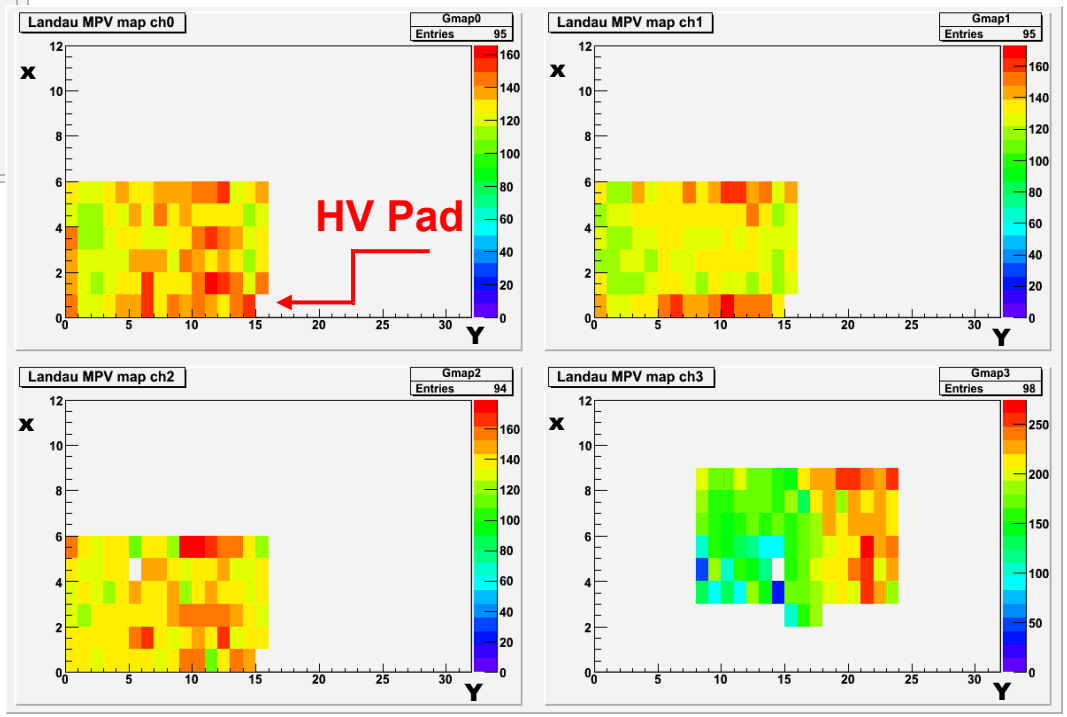
MIP signal in 4 chambers (for all pads)



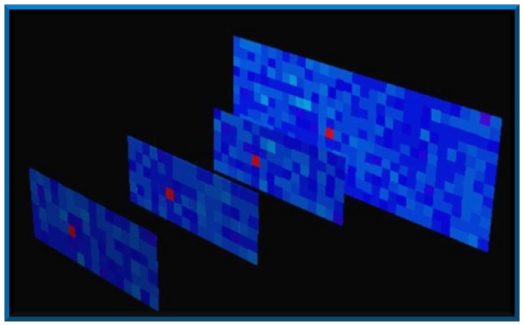
Electronic noise



Landau peak vs pad

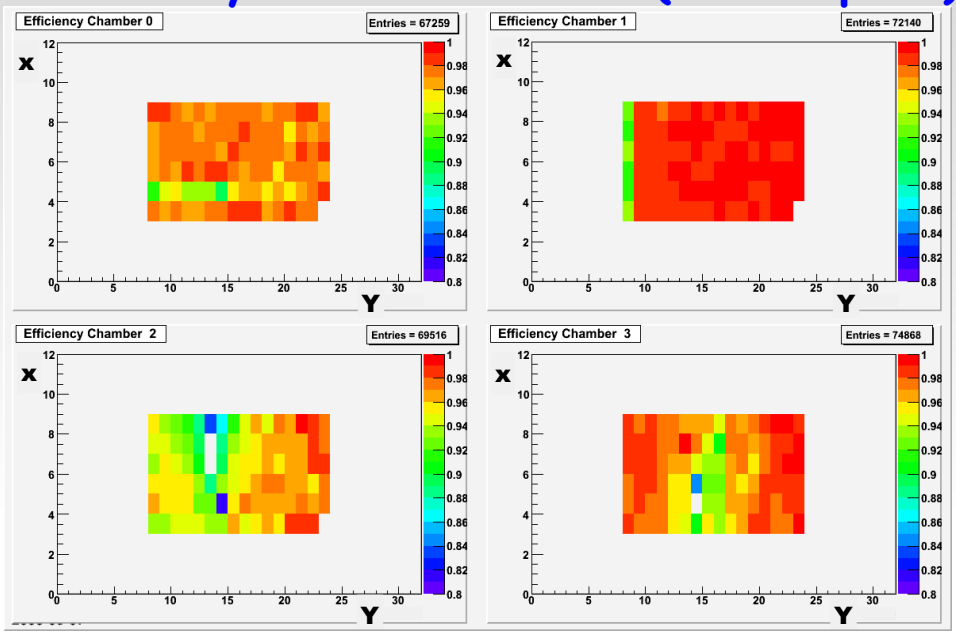


Only events with single hit in 4 chambers are considered (30 % of events)



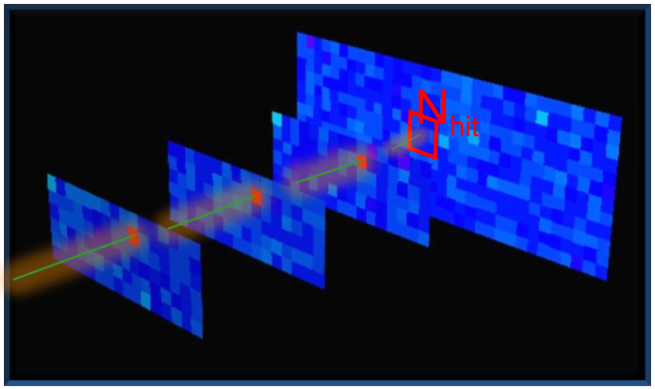
Efficiency and Multiplicity

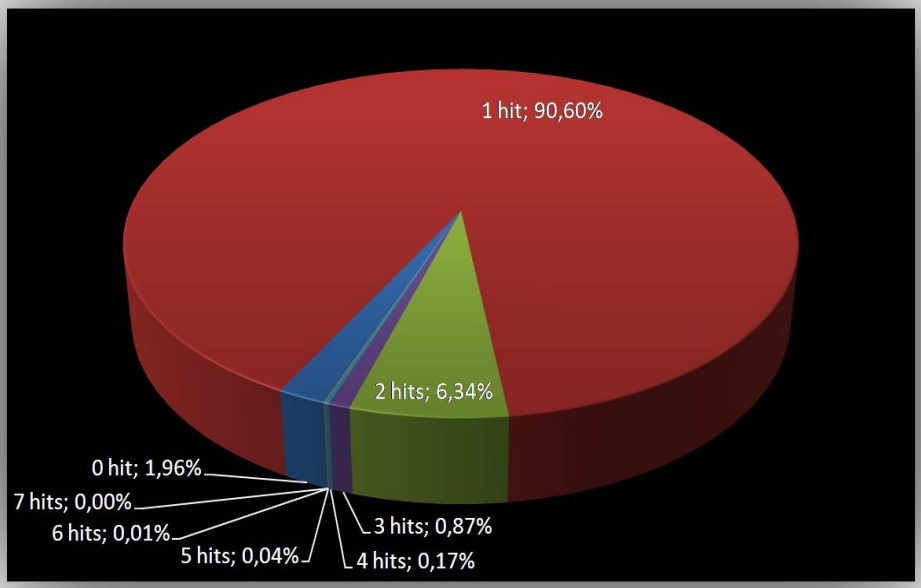
Efficiency for 4 chambers (for all pads)



	Efficiency
Chamber 0	97,05 ± 0,07%
Chamber 1	98,54 ± 0,05%
Chamber 2	92,99 ± 0,10%
Chamber 3	96,17 ± 0,07%

Pad multiplicity ~ 1.07 for 1 chamber (75 kevents)





Count the Number of hit(s) in a 3x3 array around the expected hit

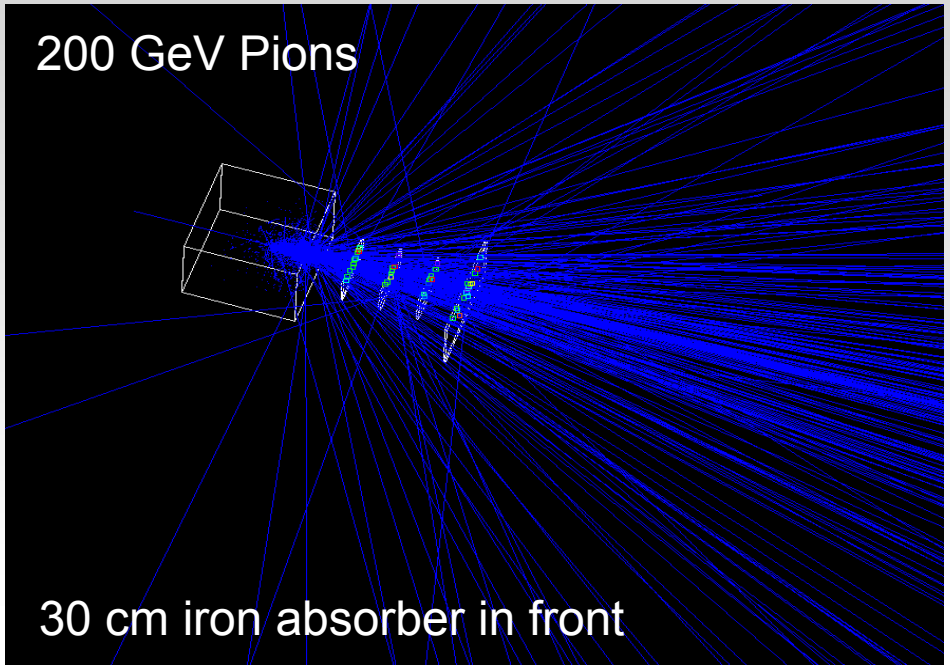
Test beam simulation

Test beam setup is being simulated

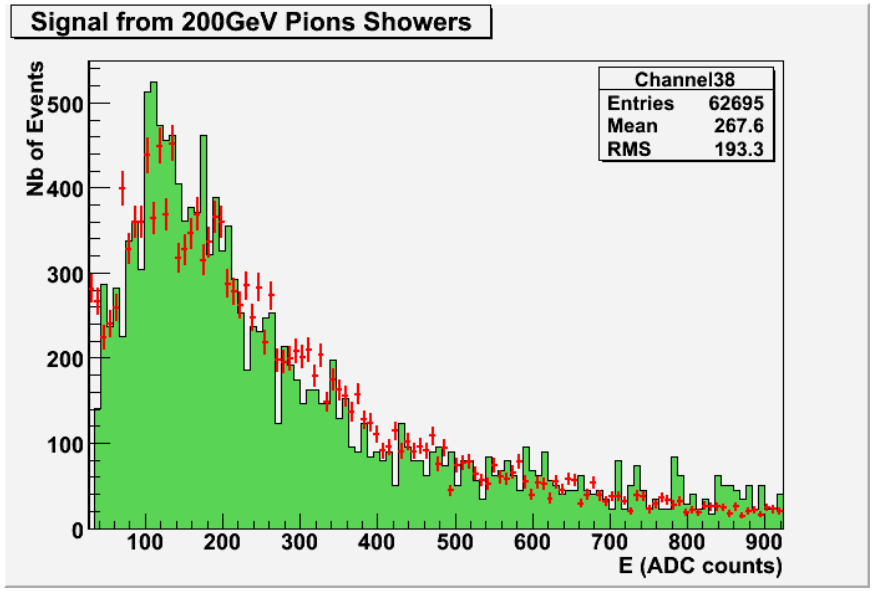
- Comparison with real data
- Better understanding of our detector
- Preparation for next test beam

Simulation tools

- SLIC full simulation (Geant 4)
- Analysis using JAS3



Single channel respond in shower



Simulation

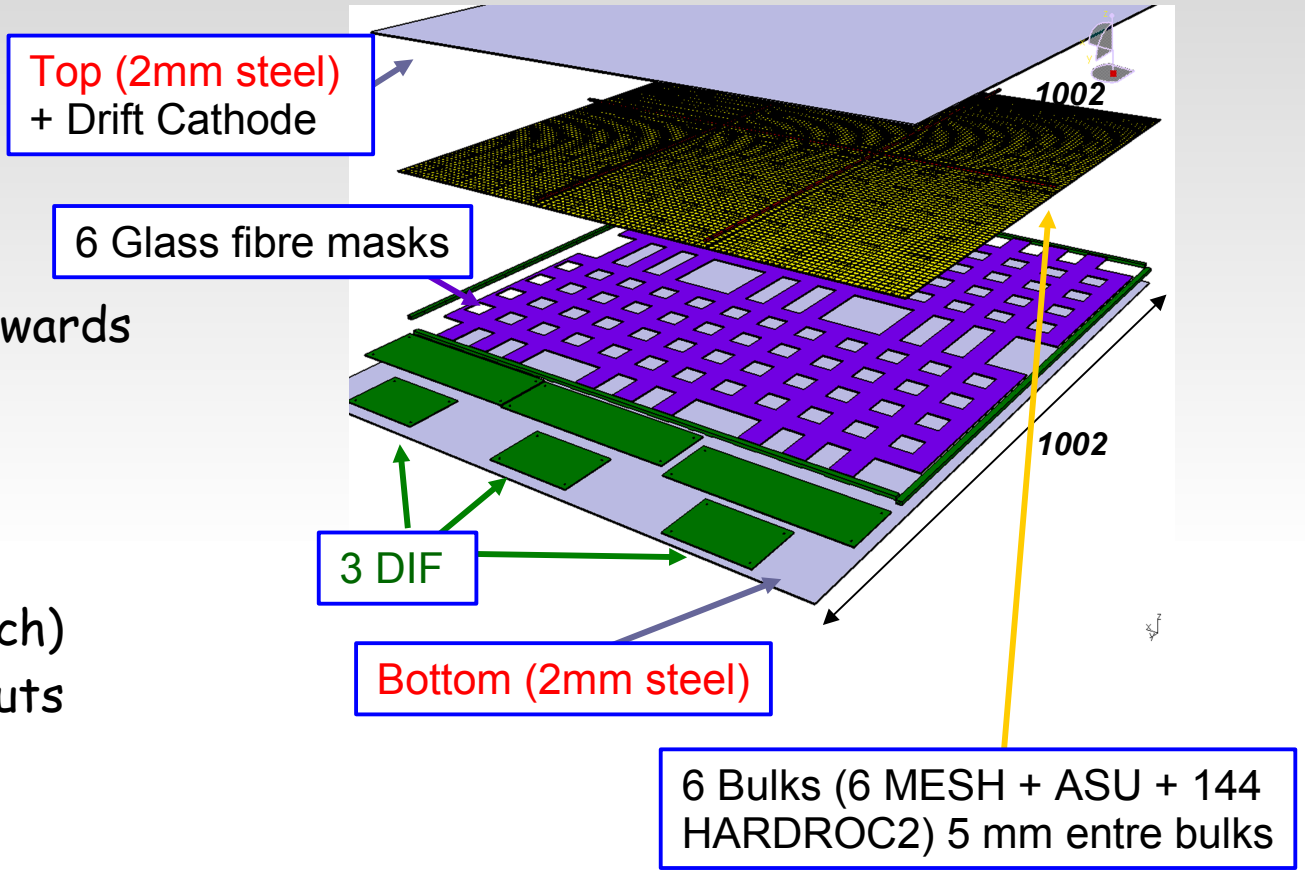
Real test beam data

ADC counts

M² µMegas prototype

M² prototypes:

- ~10 000 channels !
- Prototypes to be ready for test beam 2009!
- Performance studies towards the technology for m^3



M² µMegas design

- 6 bulks (50x32 pads each)
- Hardroc or dirac readouts
- DAQ
  - USB + PC
  - CALICE DAQ2

Next step: m^3 with ~ 400 000 readout channels

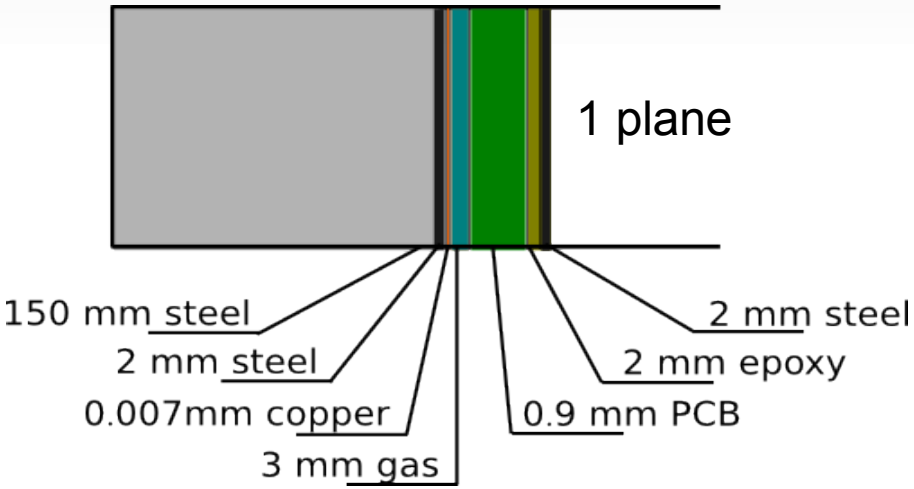
Similar work (m^2/m^3) is underway with RPC (US and EU)

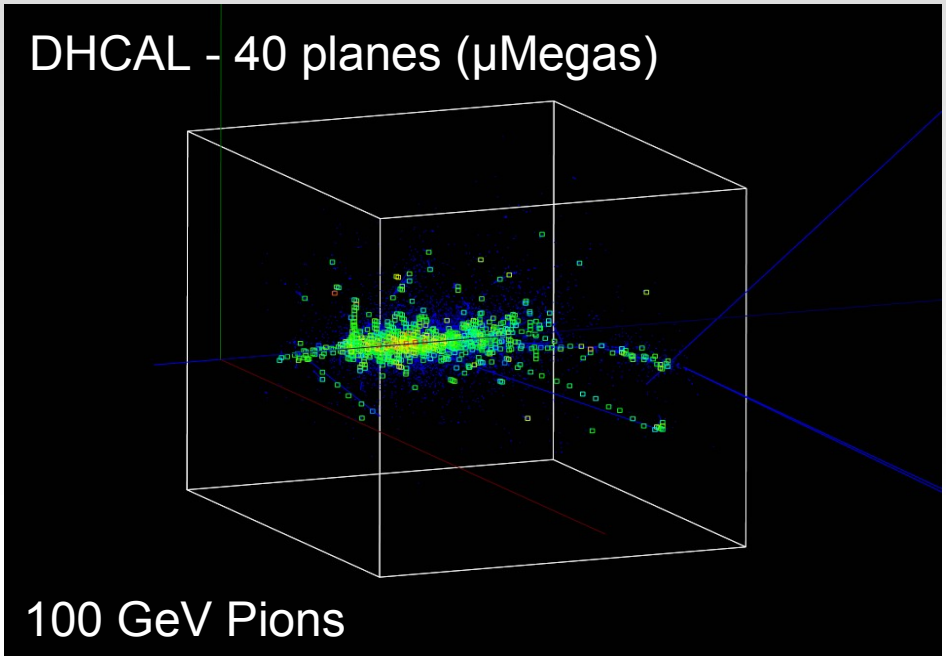
M³ µMegas Simulation

Simulation tools

- SLIC full simulation (Geant 4)
- Analysis using JAS3

Geometry - 40 planes with µMegas and 2 cm steel absorber

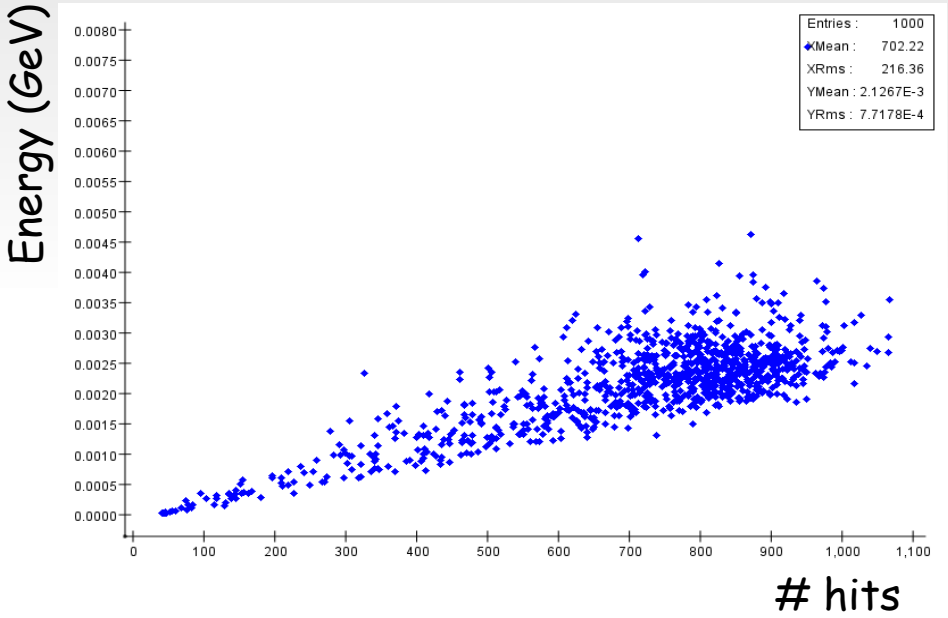




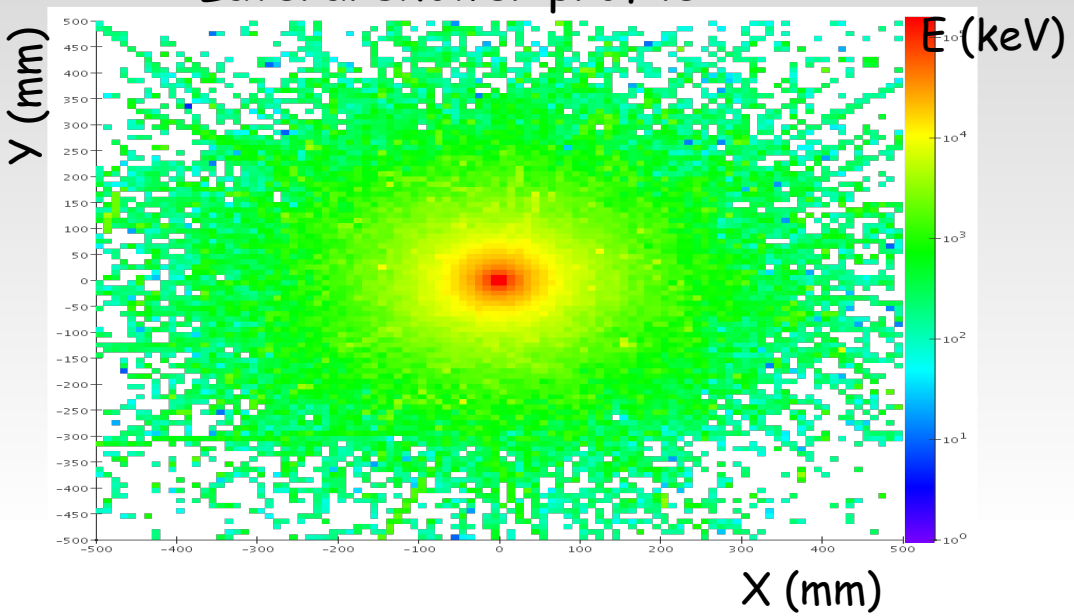
M³ µMegas Simulation

Example – 100 GeV Pions, 1000 events

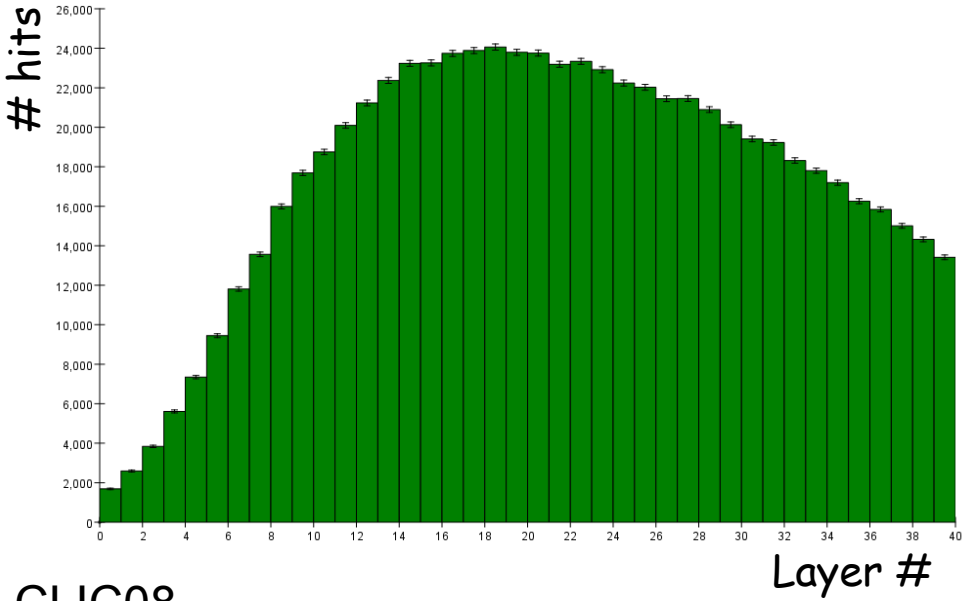
Energy vs hit for each event



Lateral shower profile



Longitudinal shower profile



Conclusions

- Several μMegas and RPC prototypes have been successfully built and extensively tested
- The first μMegas test beam results have showed very good performance complying with DHCAL needs
- Development of large scale prototypes is well underway and is going to be ready for a test beam 2009
- The simulations have started for TB and M^3 structures and will be extended to SiD/CLIC detectors studies
- Similar work on RPC (US and EU) and GEM (US)