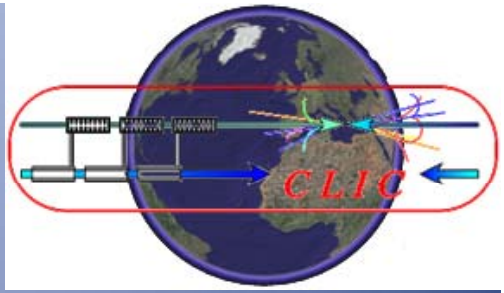
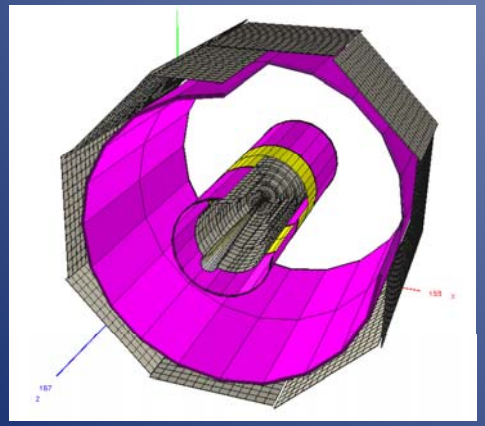
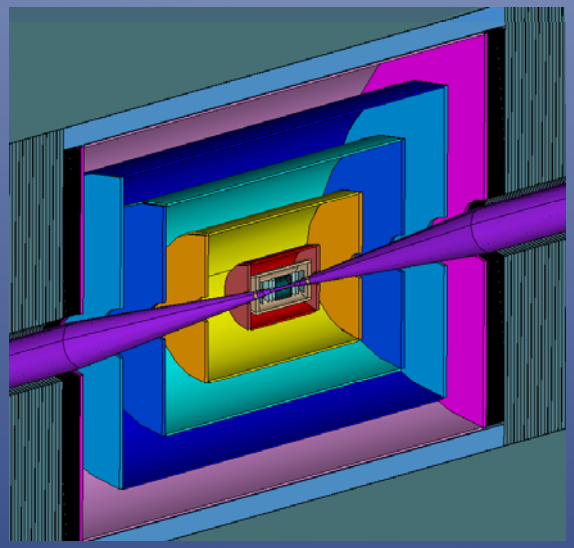
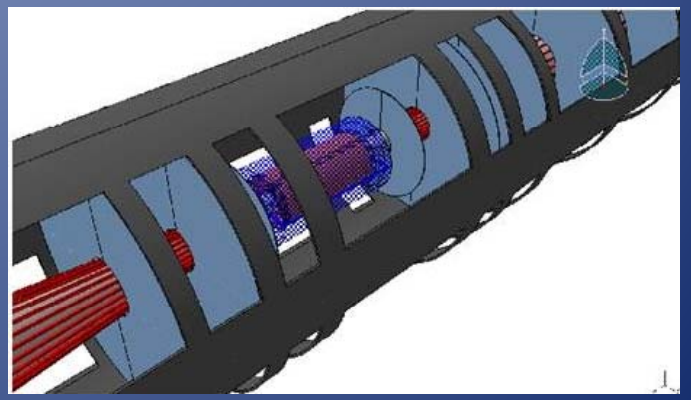


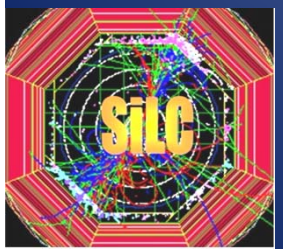
Silicon Tracking for CLIC experiments

Aurore Savoy-Navarro, LPNHE Université Pierre et Marie Curie/CNRS-IN2P3









CLIC08 WORKSHOP, 14-17 October 2008, CERN

SYNOPSIS

- The main goals for tracking at CLIC
- Main tracking parameters for operation at CLIC vs ILC
- Tracking scenarios with Silicon detectors at LC
- Silicon trackers: Roles and duties
- R&D roadmap
- Perspectives and concluding remarks

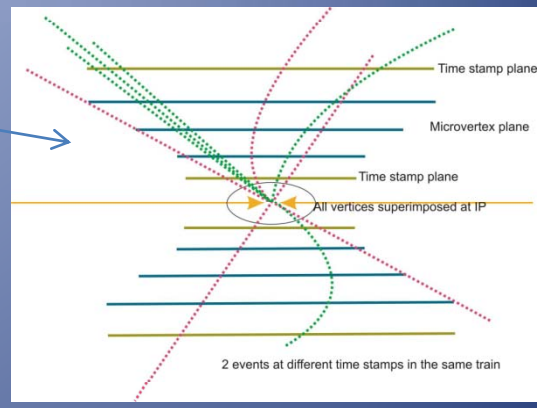
Most of the material discussed here comes from R&D work within: SiLC, SiD and EUDET

Main parameters for tracking

Need time stamping with high precision (xcrossing 0.67ns)

only at vertex detector level

what about the tracker?



Need double hit recognition for the tracking

New developments on TPC => TPC is back again in the game

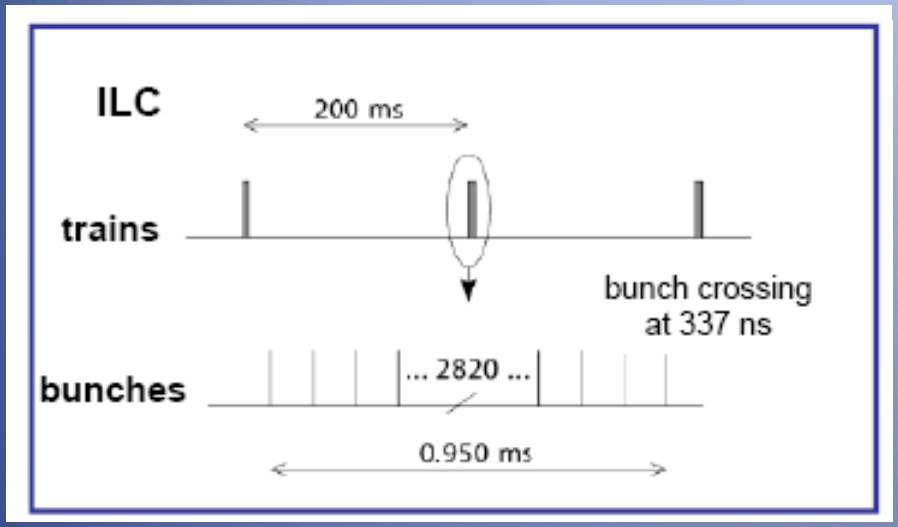
thus 2 scenarios:

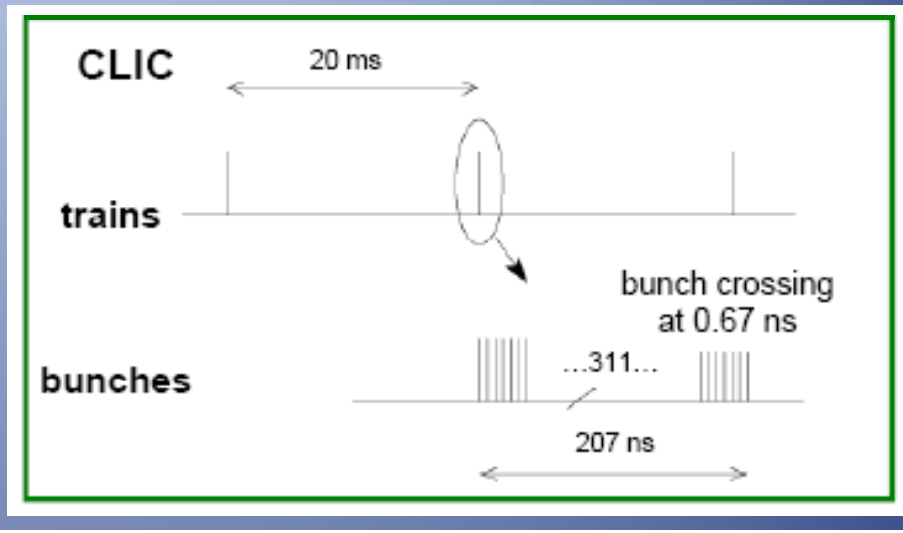
All Silicon tracker

Silicon +TPC tracker

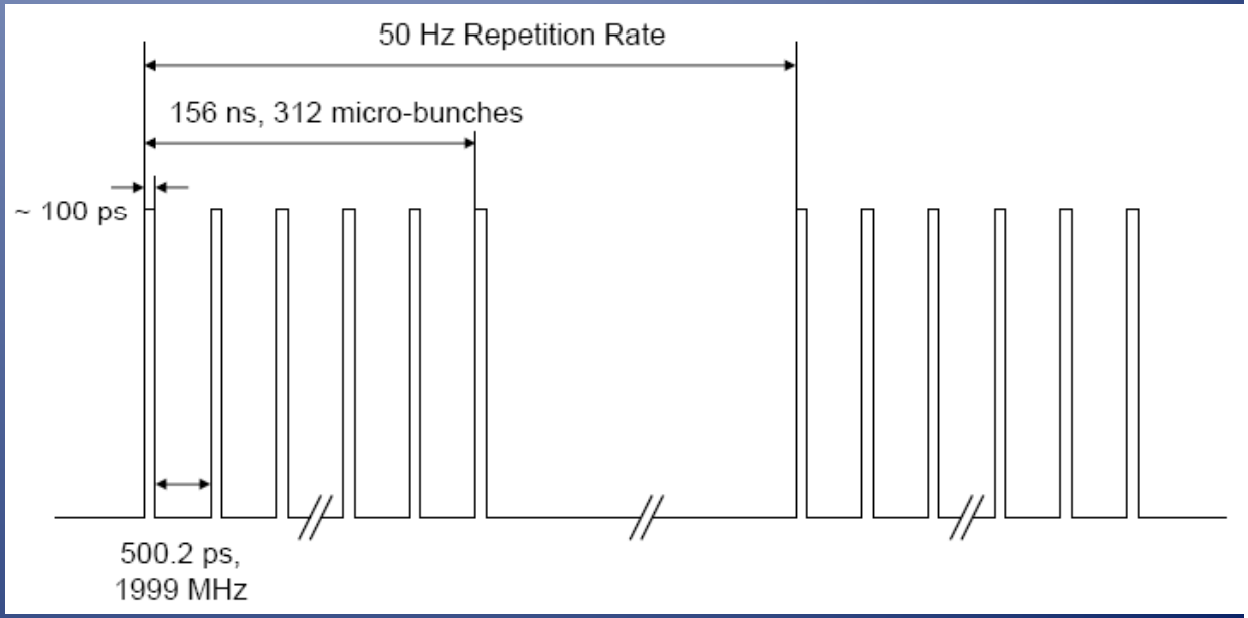
These 2 alternatives are studied also for ILC

Machine cycle: CLIC vs ILC





Imposes short shaping time restriction on pulseheight processing (see later)
Study for feasibility of power cycling
Possibility of time stamping with what Si sensor techno?



Some important parameters for trackers: CLIC vs ILC

parameters	ILC	CLIC
Time stamping	O(100 ns) (achievable by Si layers)	O(100-200ps) (special layers?)
Shaping time	LONG: 0.5 to 1.5 µs	SHORT: O (150ns)
Power cycling: Y/N? (inter bunch train /reduction factor	YES (OK) (200ms/~ 70)	YES? (20ms/to be studied)
Double track recognition	YES (OK)	YES-YES (OK)
$\sigma(\delta p_T/p^2_T)$	a few 10^{-5} (c/GeV)	idem
Spatial resolution	4 to 7 µm (OK)	idem
Material budget/layer	~ 0.7-0.8% X0 (OK)	idem

Main tracking scenarios

Currently considered for ILC:

Tracking with or without gaseous detector as central tracker

Thus:

- all-Silicon tracking (a la CMS), or:
- combined central gaseous tracker plus Silicon tracking

(as CDF, present ATLAS)

Thus nothing new under the SUN but the technologies and requested performances => active R&D going on…

For CLIC these tracking scenarios could be used as well (if no new bright idea):

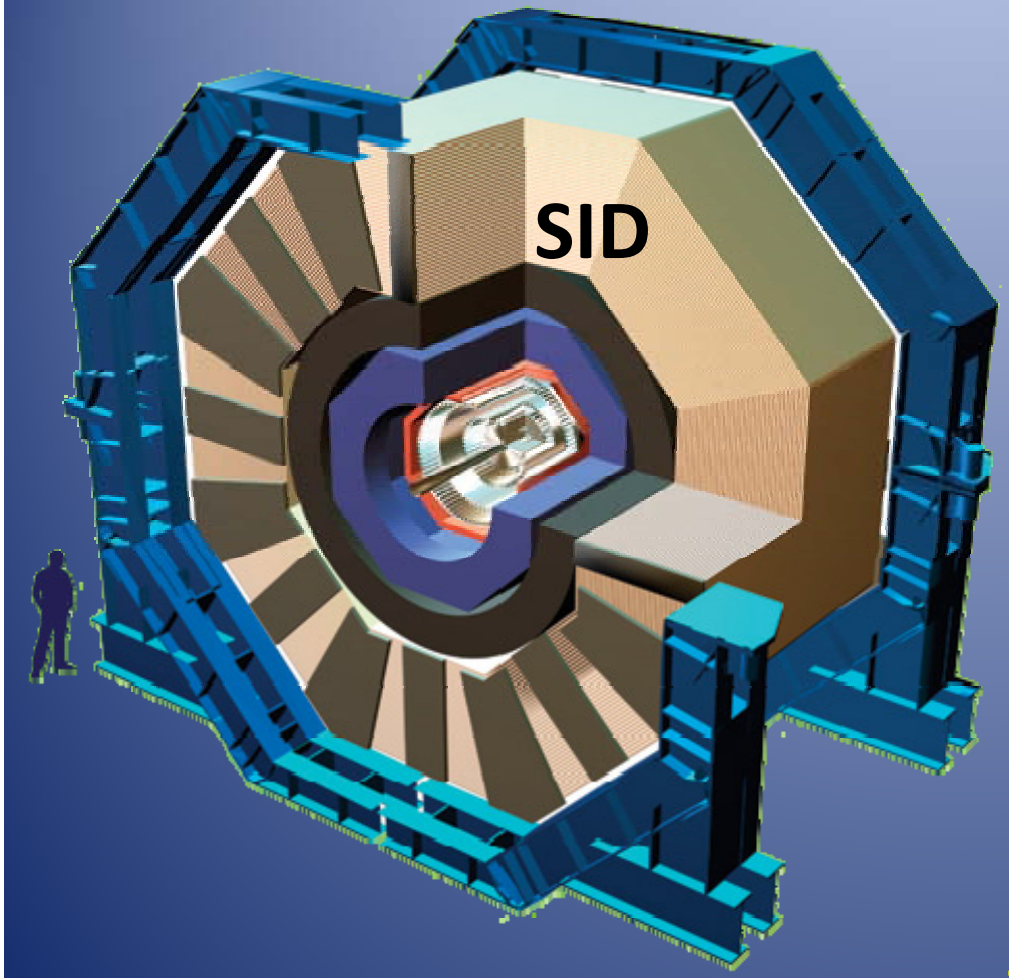
All Silicon tracking: OK

TPC new wave can work in CLIC environment

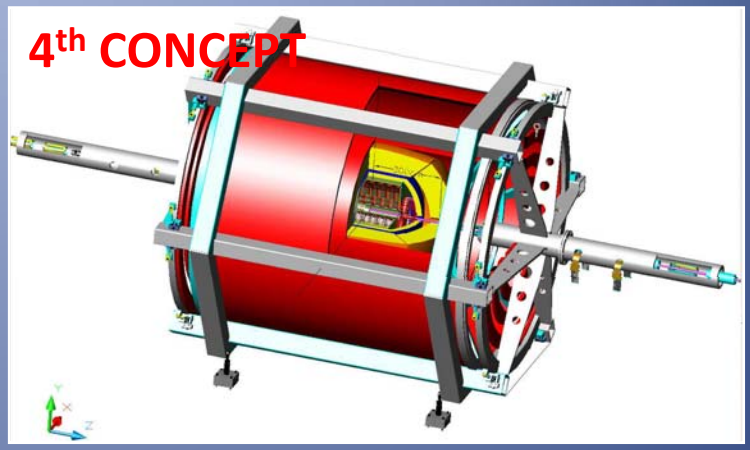
DCH a la 4th concept (still to be proven).

Silicon tracking: Roles and duties

ALL SILICON TRACKER



ALL Silicon tracker a la CMS is promoted by SiD



One of the tracking option studied by 4th concept includes an all-Silicon-tracking

(''Choose the best tracking...'' GPYeh)

Z!! An ALL-Si Tracking is a fully integrated tracking system Z!!

Main assets of Silicon tracking:

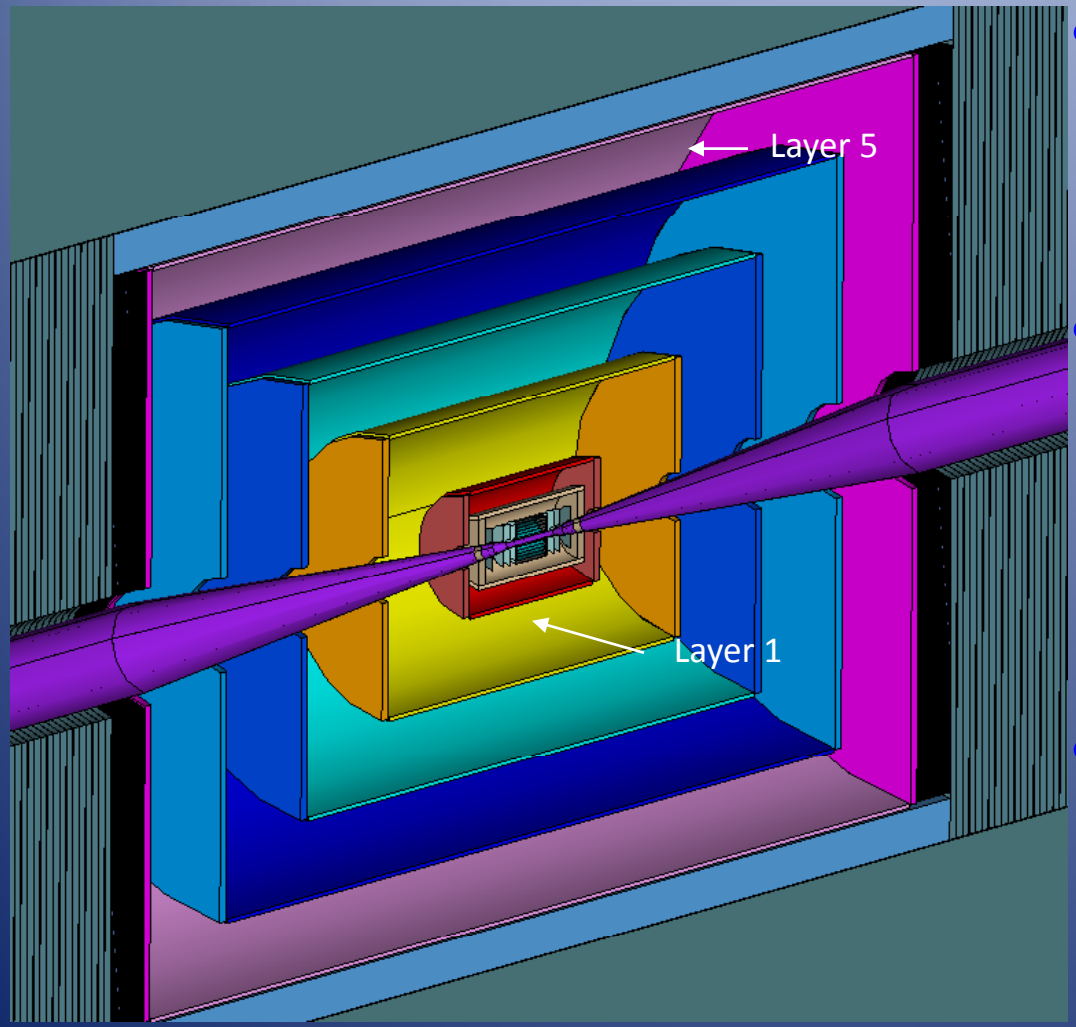
- Uniform and robust technology: excellent homogeneity
- No pb with high magnetic field
- High precision device (high momentum & excellent spatial – *few microns*-- resolutions)
- FE Electronics ‘’naturally’’ integrated on the detector
- Easy and very good angular coverage (homogeneity and fully integrated design)
- Easy to calibrate and align
- Close connection with Industry (lot of advances in the field)

Main caveat: minimizing material budget

(not only true for this device!!)

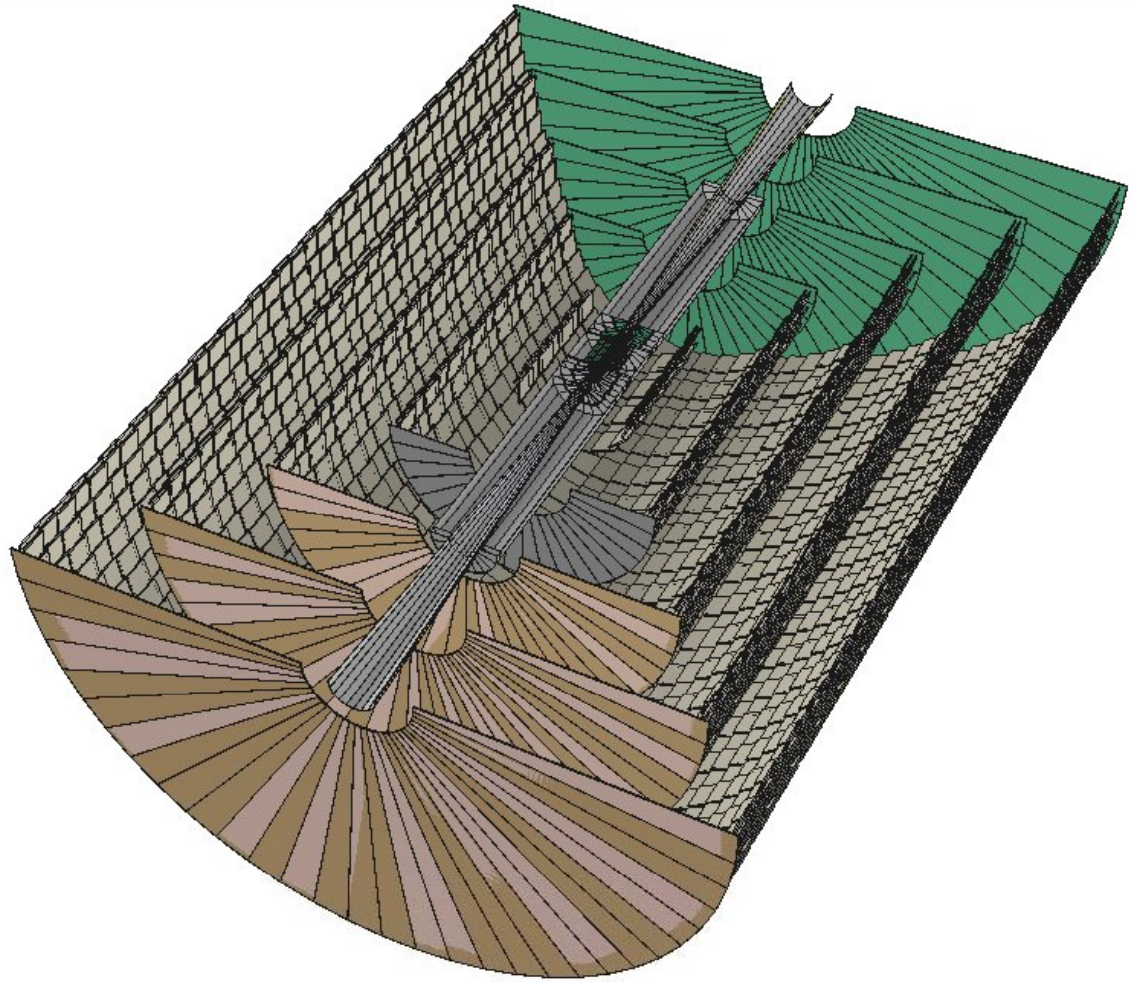
Ex: SiD Tracker

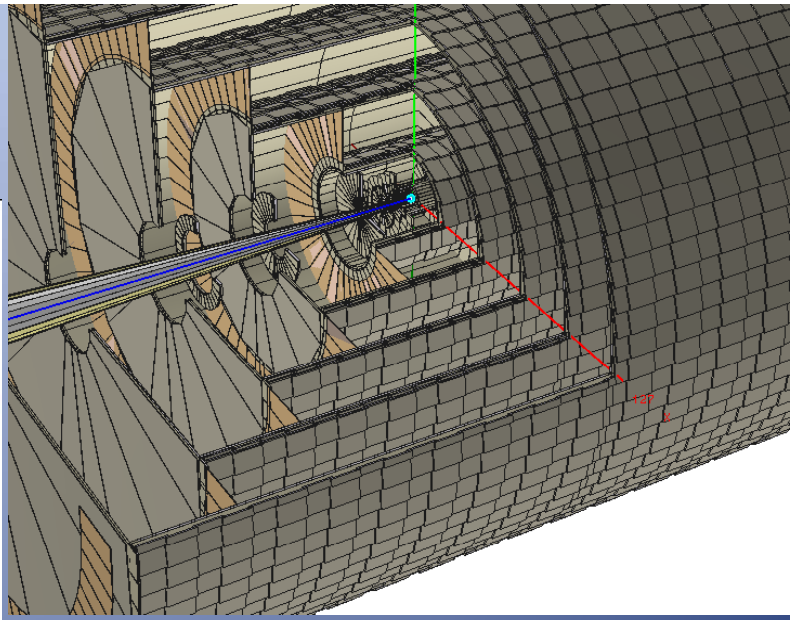
- 5-Layer silicon strip outer tracker, covering R_{in} = 20 cm to R_{out} = 125 cm, to accurately measure the momentum of charged particles



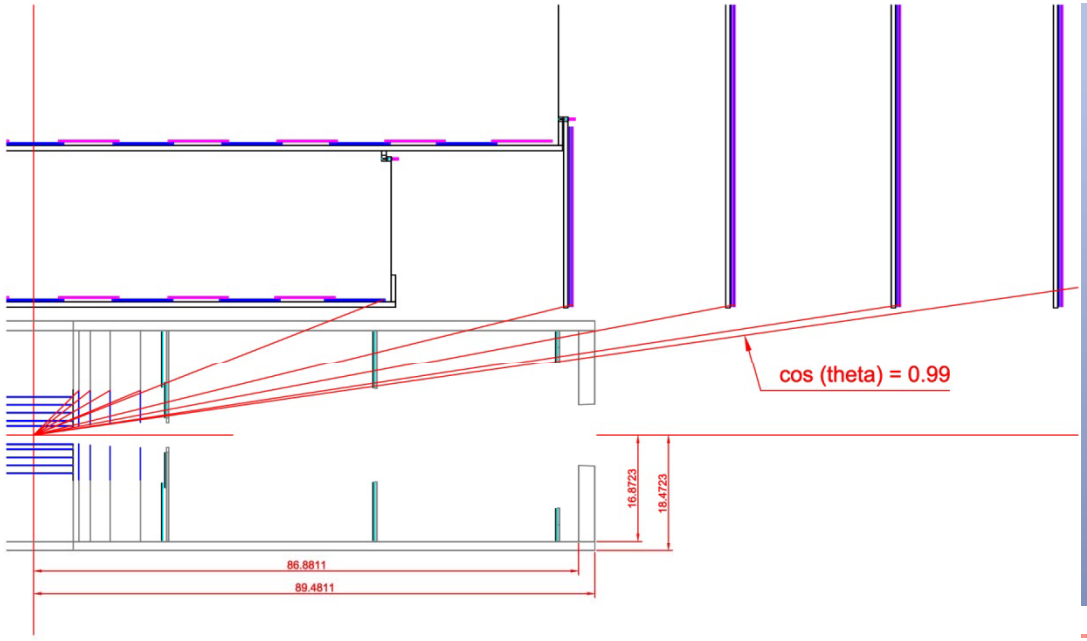
- Support
  - Double-walled CF cylinders
  - Allows full azimuthal and longitudinal coverage
- Barrels
  - Five barrels, measure Phi only
  - Eighty-fold phi segmentation
  - ~ 10 cm z segmentation
  - Barrel lengths increase with radius
- Disks
  - Four double-disks per end
  - Measure R and Phi
  - varying R segmentation
  - Disk radii increase with Z

SiD Tracker





- 5 layer Si-Tracker
- 5 barrel cylinders
  - ϕ readout only
  - 10 cm z segmentation
- 5 forward double disks
  - measure r and ϕ
  - Projective geometry

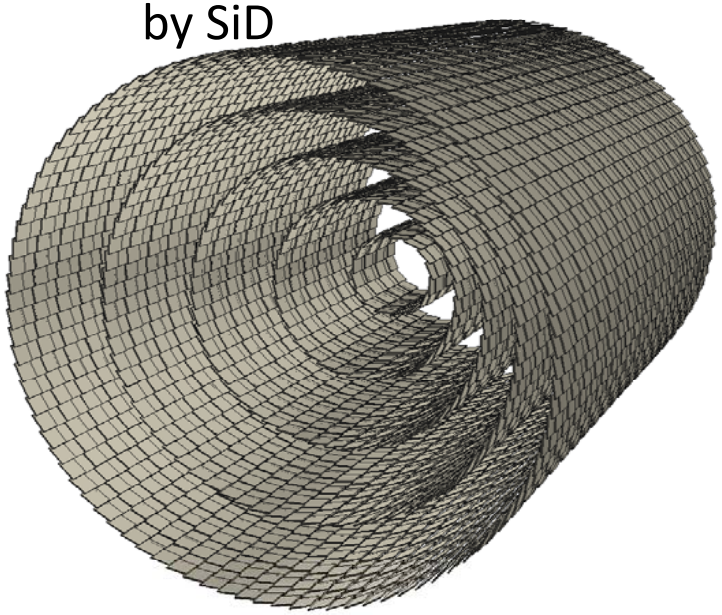


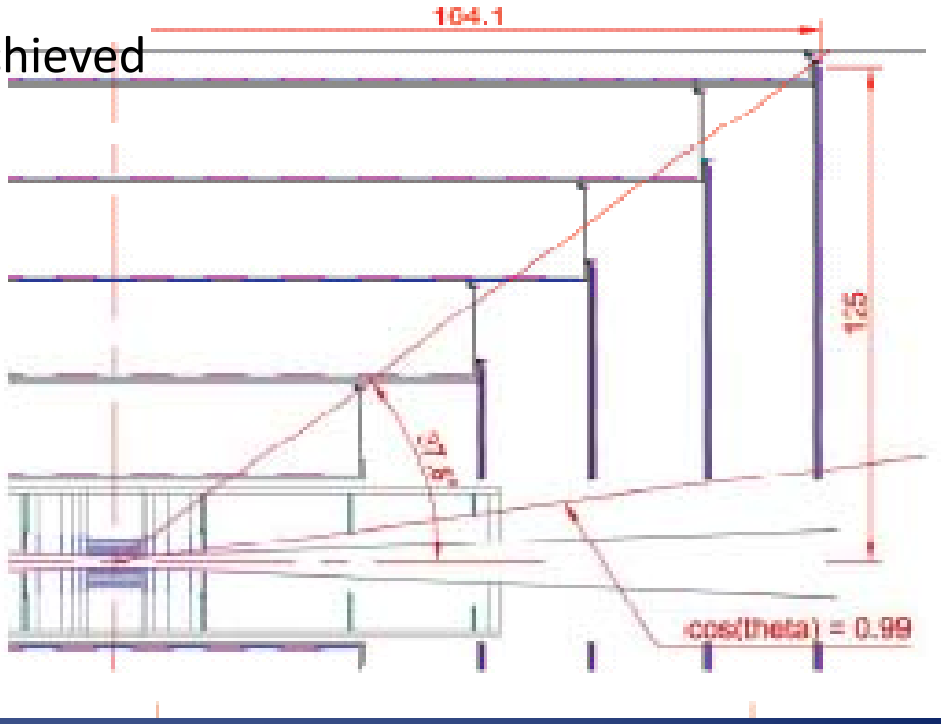
SiD Tracker

- Sensor Tiles for barrel
- Kapton cables for signal routing
- Lightweight space frame

  0.8% X0/layer

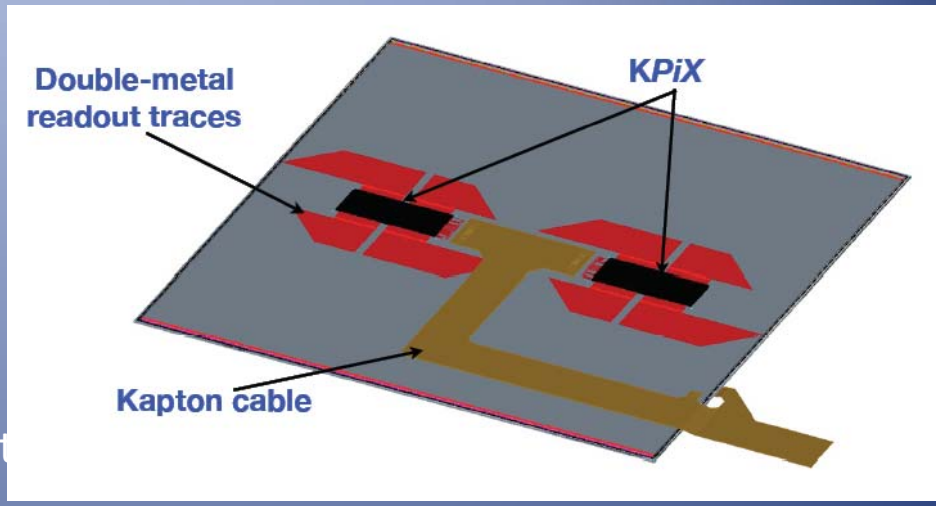
Already a detailed mechanical design is achieved by SiD

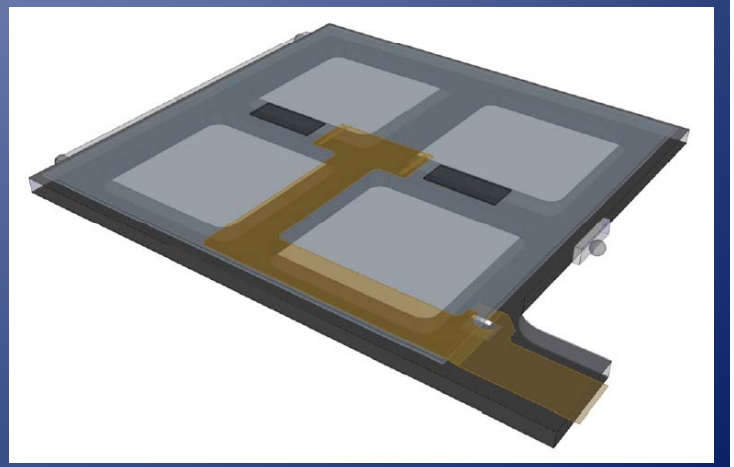




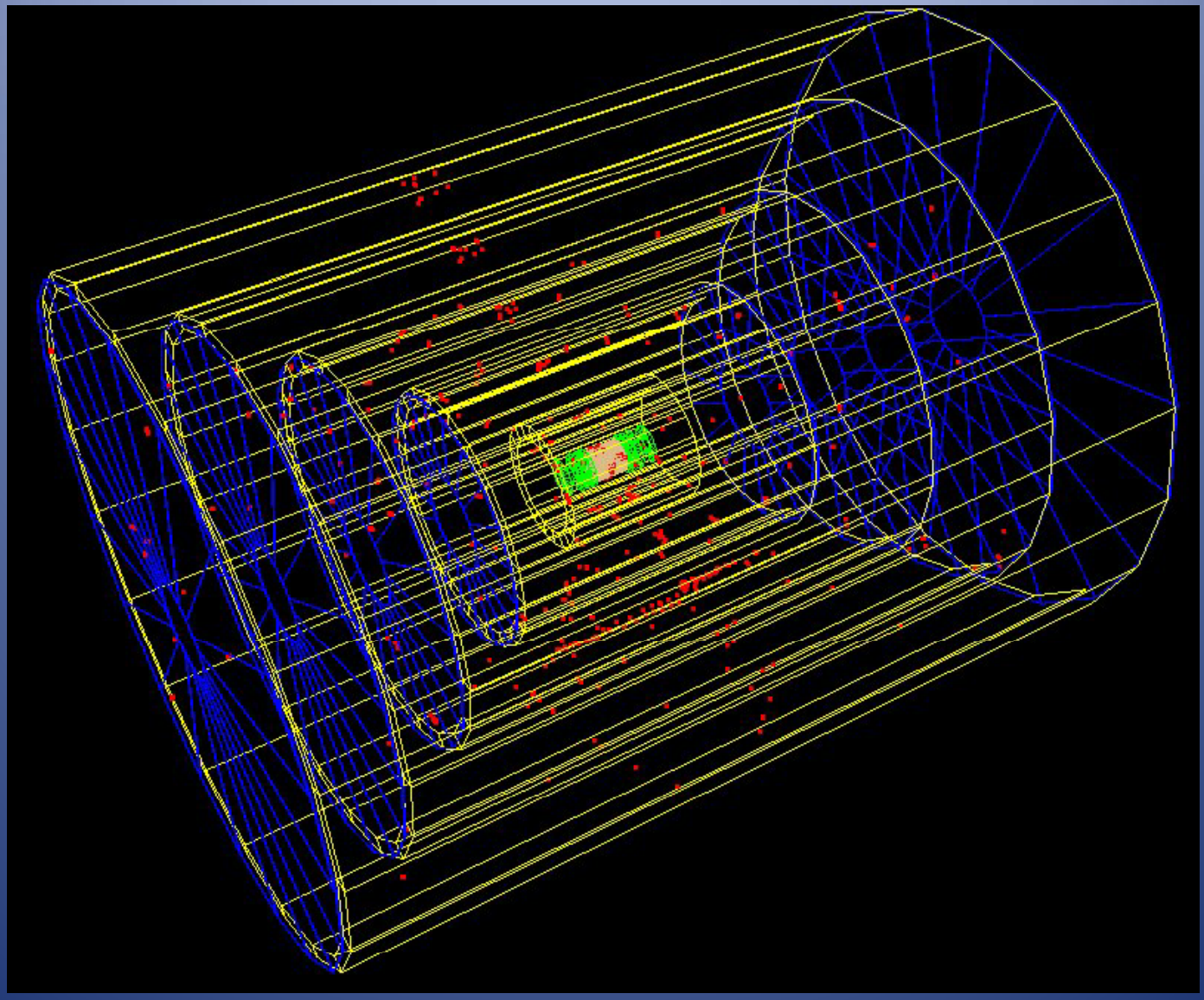
Sensor and Module Design

- Hybrid-less design
  - 93.5 x 93.5 mm^2 sensor from 6" wafer with 1840 (3679) readout (total) strips
  - Read out with two asics (kPix) bump-bonded to sensor
  - Routing of signals through 2nd metal layer, optimized for strip geometry
    - Minimize capacitance and balance wit trace resistance for S/N goal of 25
  - Power and clock signals also routed over the sensor
- Module support
  - Minimal frame to hold silicon flat and provide precision mounts
    - CF-Rohacell-Torlon frame w/ ceramic mounts
    - CF-Torlon clips glue to large-scale supports
  - Ease of large scale production, assembly and installation/replacement
- Power pulsing for tracker allows for air cooling
  - Factor of >80 in power reduction
  - But have to deal with enormous Lorentz forces





SiD in ILCROOT $e^+ e^- \rightarrow t^+ t^-$

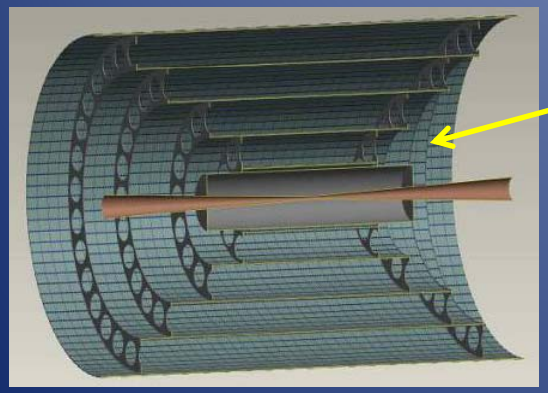


SiD present design is not the only possible all-Silicon tracking design!!

To be studied in such a case:

- **Design**: More layers combining single –sided with some double-sided?
  => not only a ''sagitter'' linking the vertex detector with the very-fine grained calorimeter-tracker, as in the present SiD design, but
  => a real autonomous tracking device.

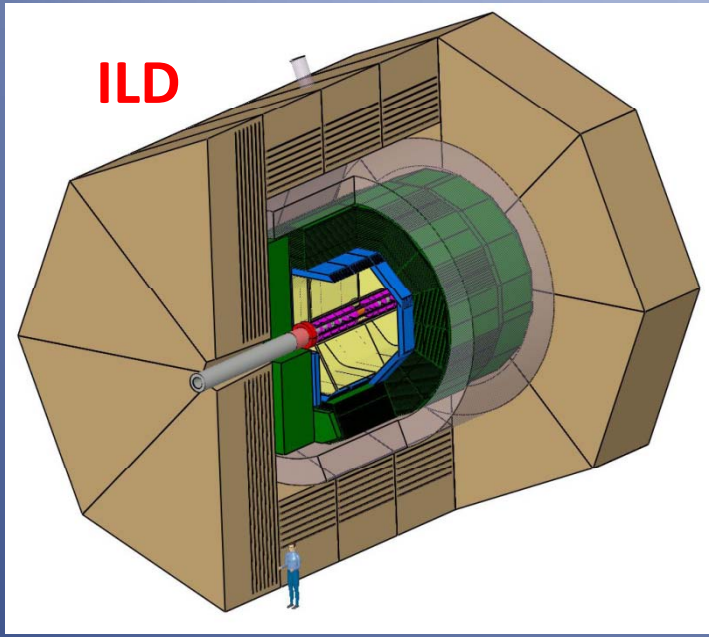
- **Sensor technology**: What strip sensors technology?
  some layers in pixels?
  All pixel tracker?
  1 or 2 layers for the time stamping?



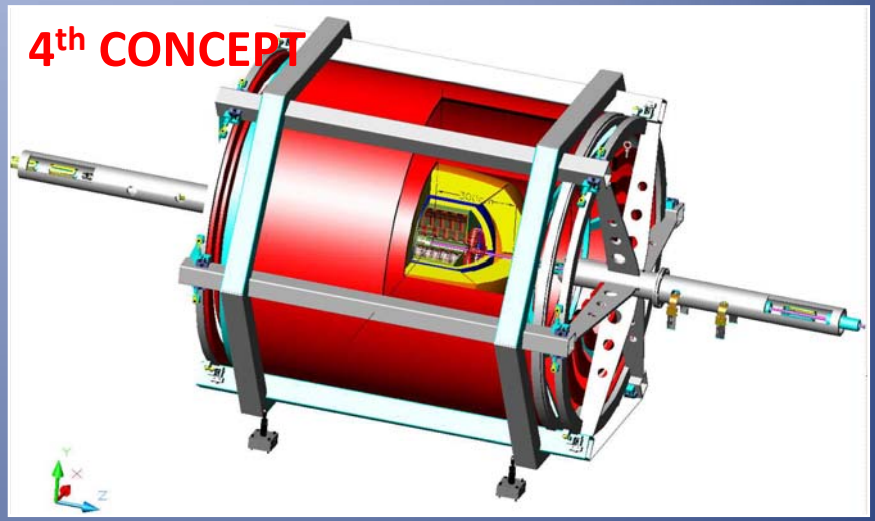
Subject of simulation and optimization studies to be actively pursued

SILICON TRACKING WITH CENTRAL GASEOUS TRACKER

(new technology developments on TPC=>OK at CLIC)



TPC central gaseous tracker combined with 4 Si tracking components
(ILD reference design: optimization and detailed simulation studies for LOI'2009)



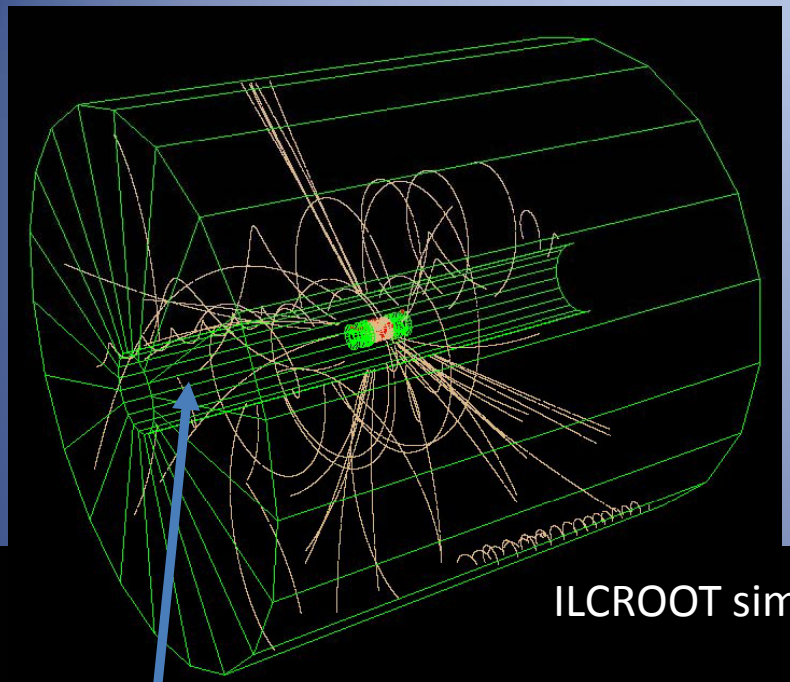
The tracking of 4th concept includes a case with a Drift Chamber as central tracker: is this exportable at CLIC ?
(Study is starting on this issue)
Envisaging to combine with Si tracking
(Study is starting on this issue)

Combines pros of the two tracking technologies but in counterpart some non homogeneity in the overall design not always easy to handle

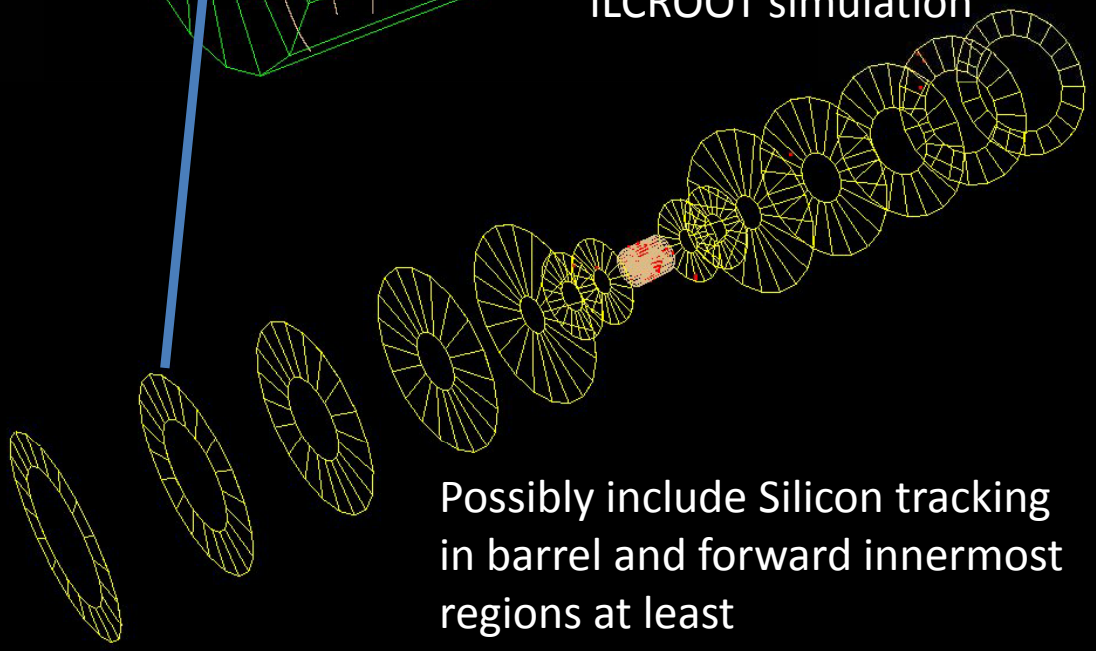
Si tracking role and duties in a combined (hybrid) tracking scenario

- Provides HERMETICITY – FULL ANGULAR COVERAGE
- Improves MOMENTUM and SPATIAL resolution
- Alignment
- Time stamping
- Monitoring of gaseous tracking distortions
- Redundancy (robustness)
- Entry point (or entry vector) to calorimetry

SILICON TRACKING WITH CENTRAL GASEOUS TRACKER

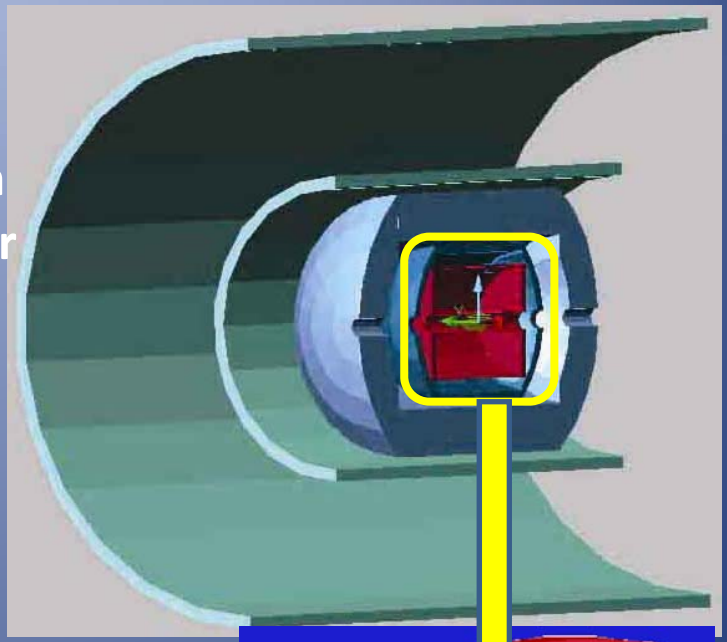


ILCROOT simulation

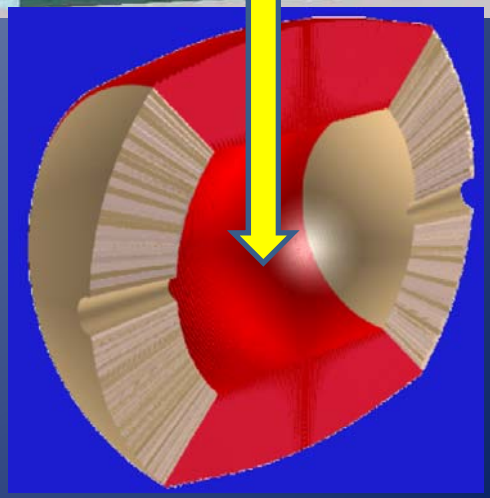


Possibly include Silicon tracking in barrel and forward innermost regions at least

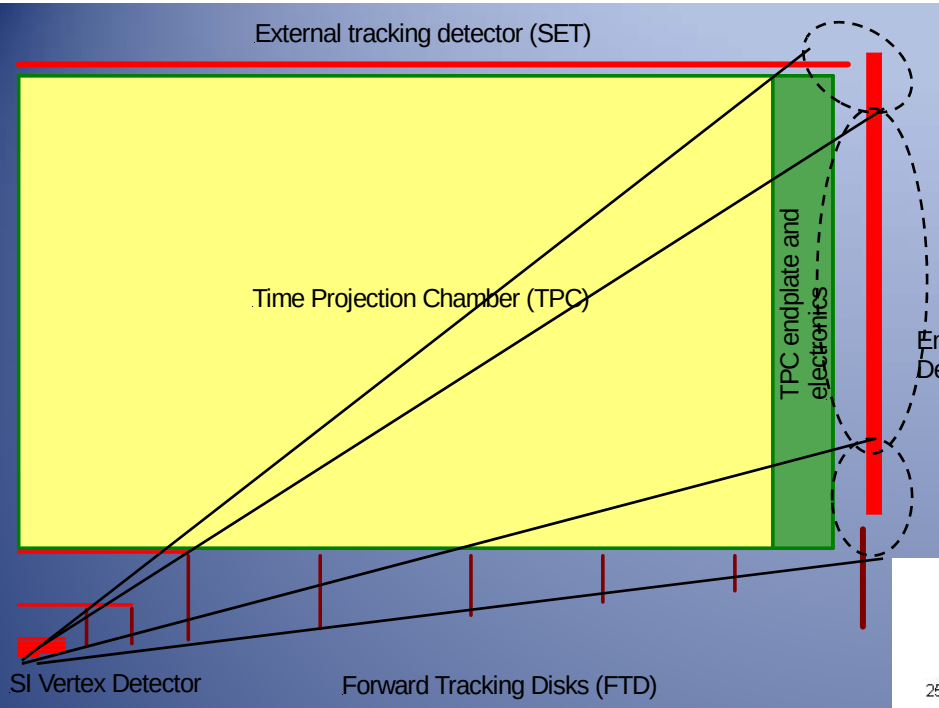
4th Concept: Scenario with Drift Chamber

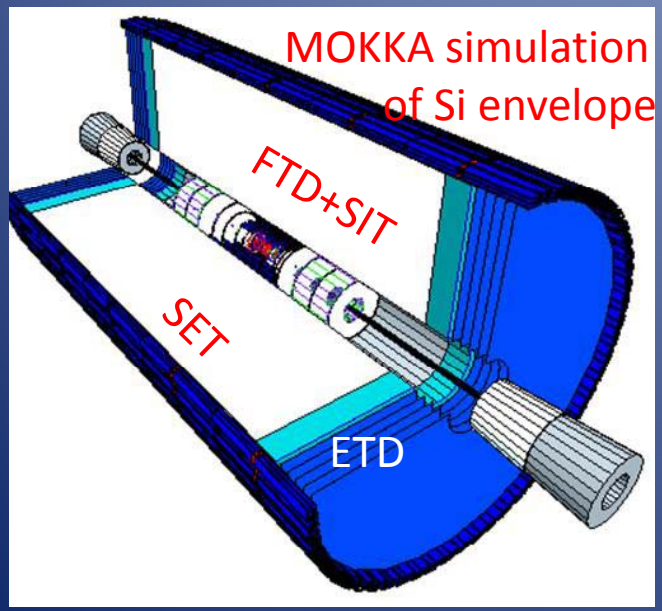


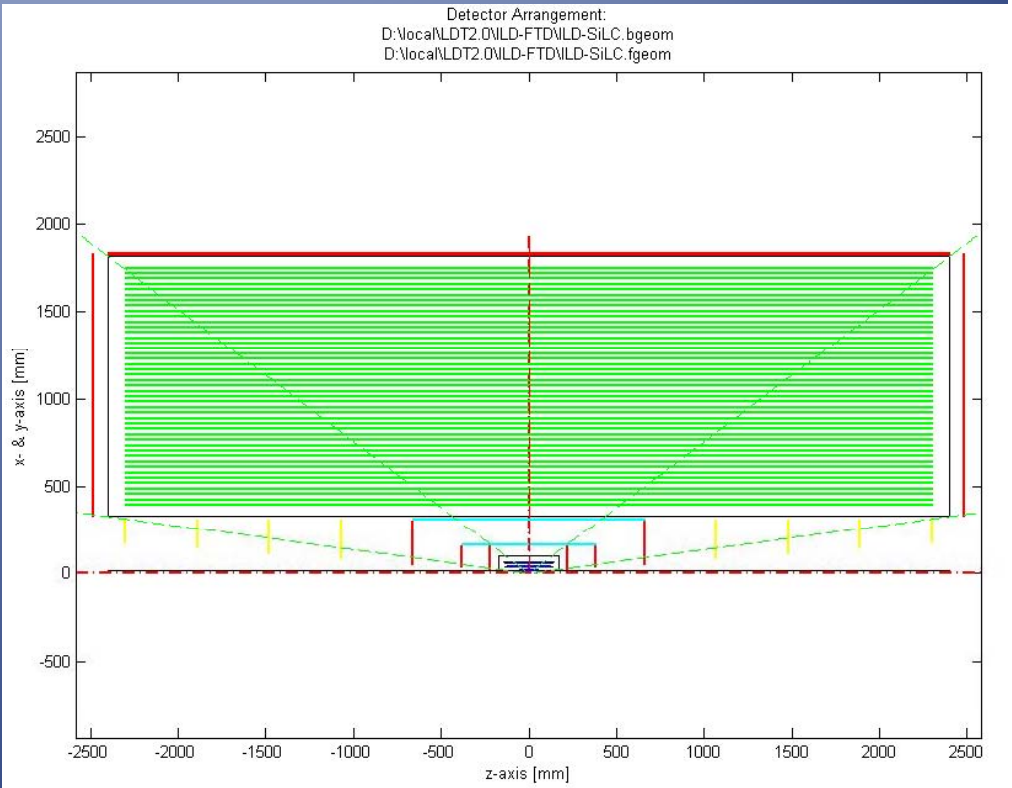
MAIN ISSUE: DOES DCH WORKS at CLIC ?(yet to be proven)



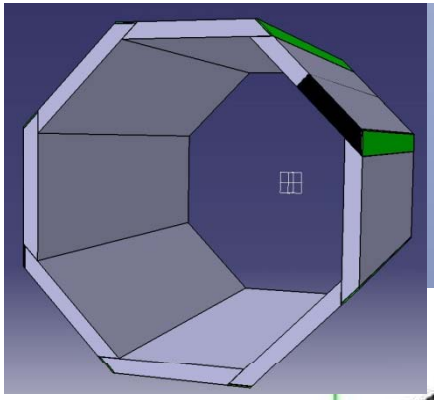
The silicon envelope or tracking hermeticity



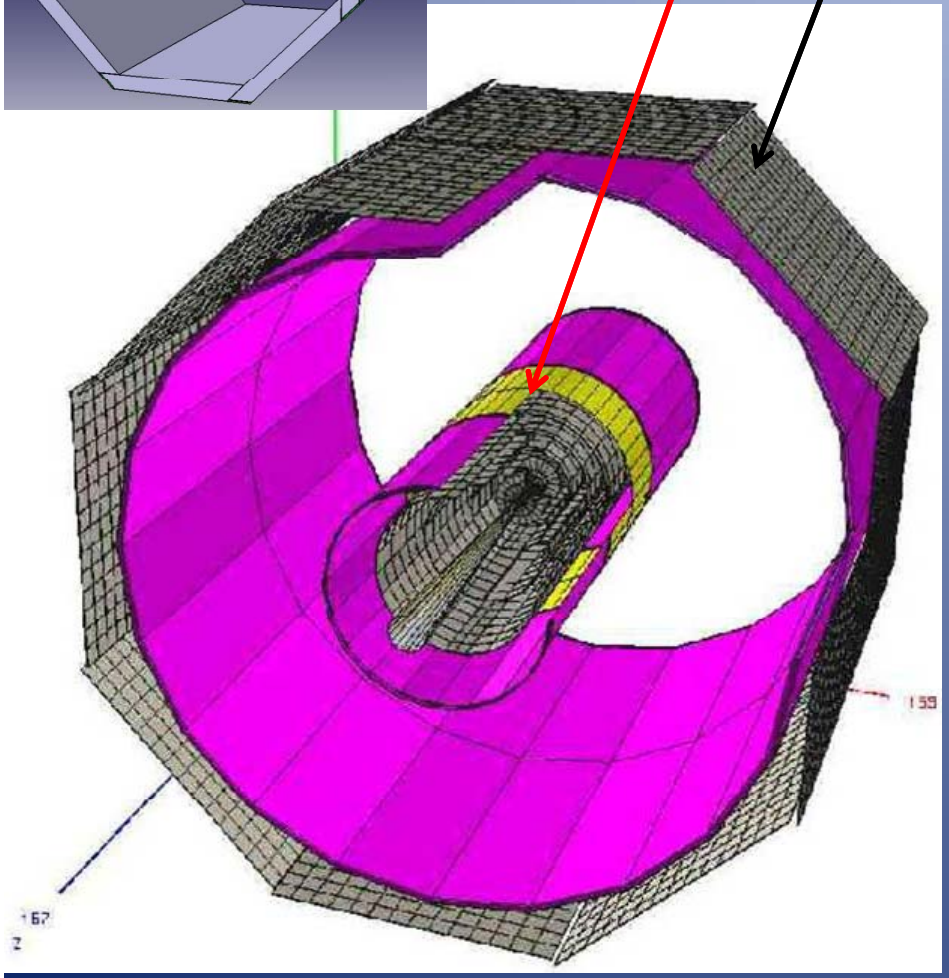




ILD Silicon tracking: Set-up

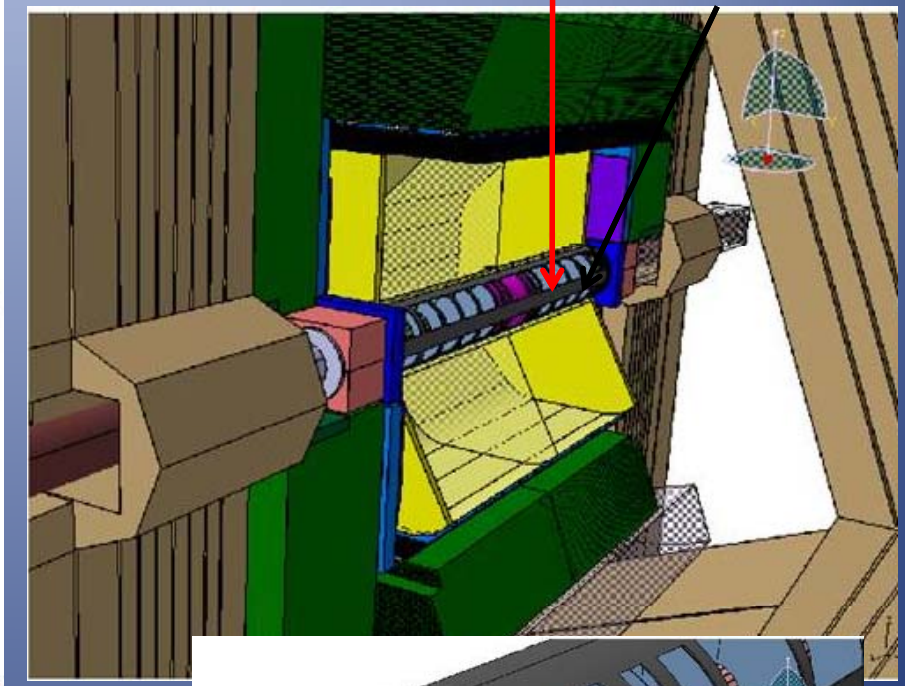


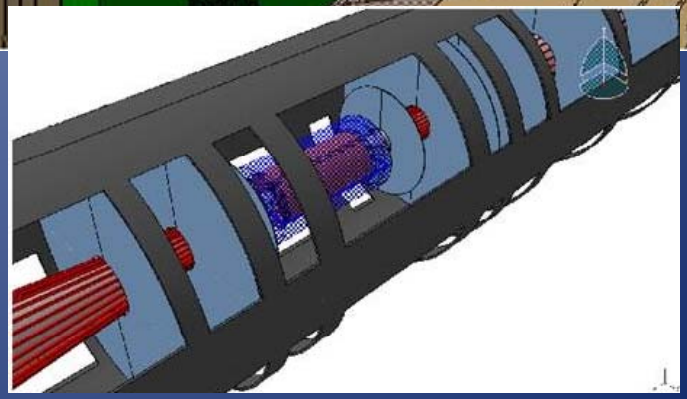
Barrel: SIT &SET



Simulation ILCRoot

Very preliminarymechanical design

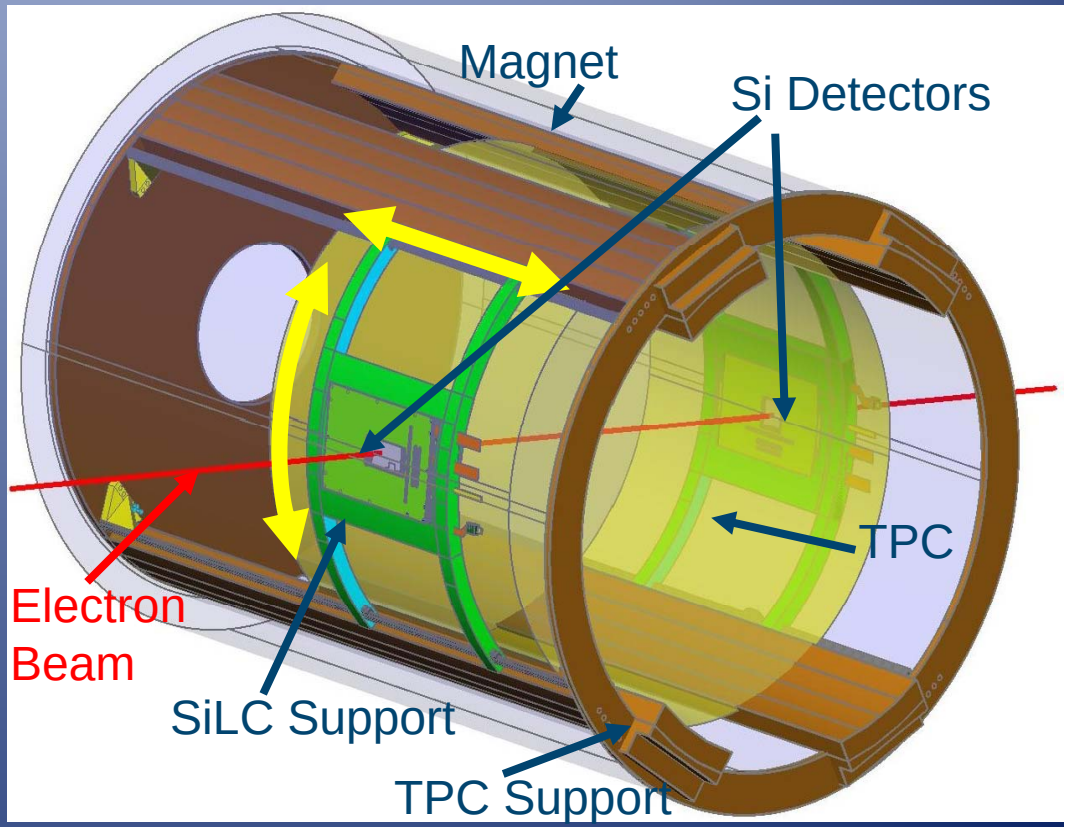




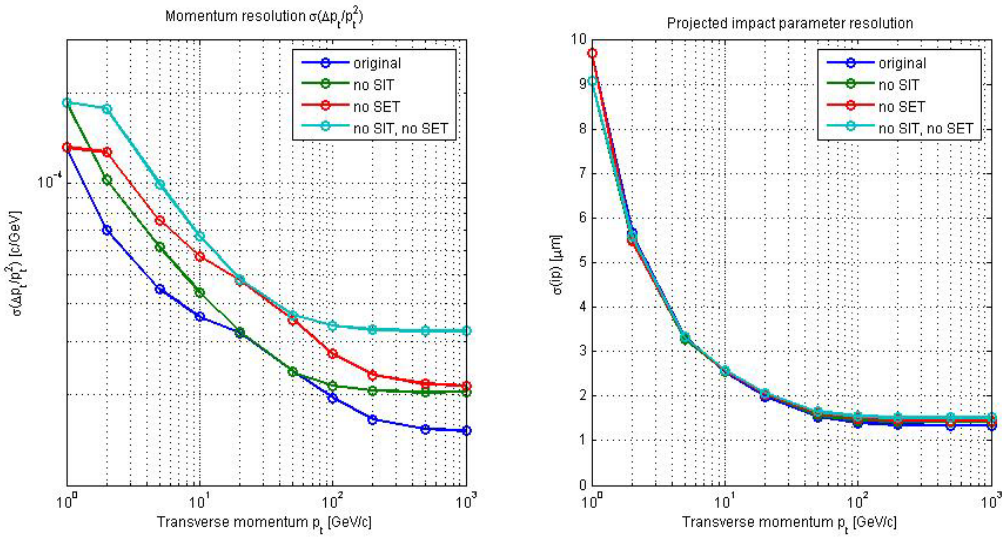
LP-TPC: Silicon Envelope

(HEPHY, IEKP Karlsruhe, LPNHE)

- **four silicon modules** will be installed:
  - two in front and two behind the TPC, with respect to the e^--beam
    - ➢ two independent support structures are needed
  - on each side:
    - ➢ one horizontal module consisting of two daisy-chained sensors
    - ➢ and one vertical module consisting of one sensor
- **movable support system** is needed because it must be possible to scan the TPC
  - the TPC and the magnet will move relative to the beam
  - the sensors have to stay inside the beam line

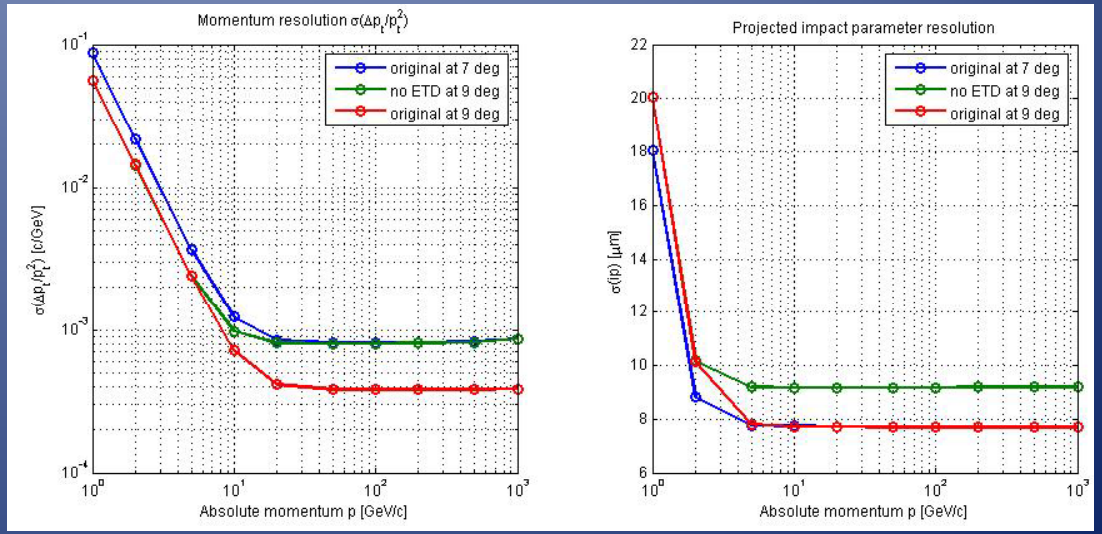


Improvements of momentum and impact parameters if TPC combined with Si trackers

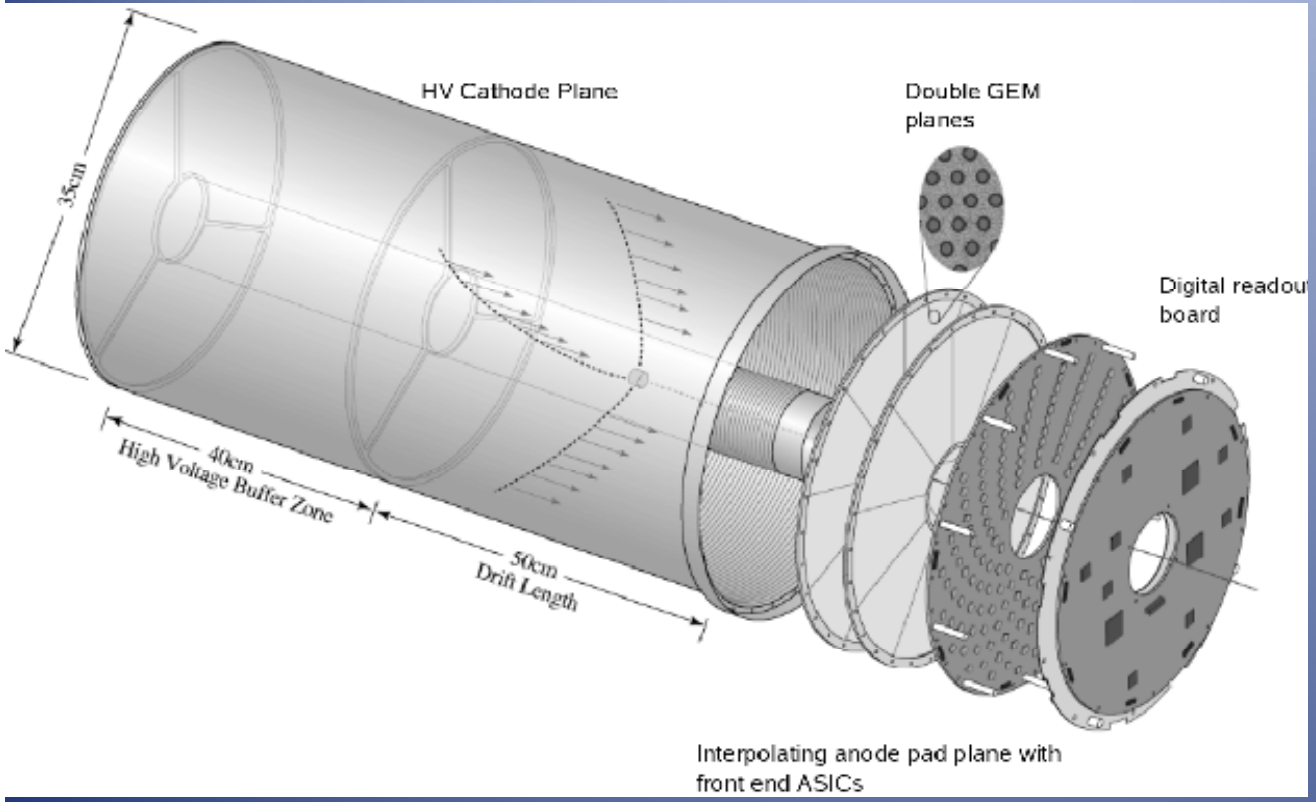


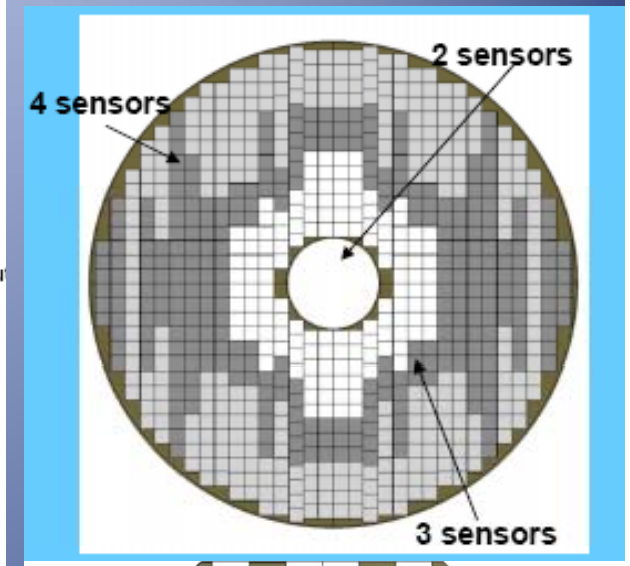
•Barrel region:
Achieving an asymptotic value of $\sigma(\Delta p_t/p_t) < 2\cdot10^{-5}$ [c/GeV], the present detector setup succeeds in complying with the demanded value of $\sigma(\Delta p_t/p_t^2) = 5\cdot10^{-5}$ [c/GeV] for reduced relative momentum resolution.
The projected impact parameter resolution reaches an asymptotic value of 1.5 [μm].

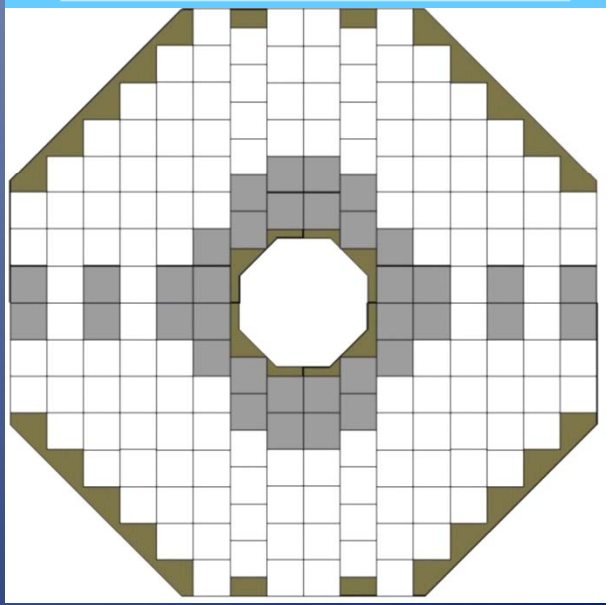
In the forward ILD region reduced relative momentum resolution reaches an asymptotic value of
$\sigma(\Delta p_t/p_t^2) < 10^{-3}$ [c/GeV]
and the impact parameter resolution levels off at 8-10 [μm].



The TPC: The endcap issue







After the TPC end cap: include one XUV point (instead of projective geometry: much simpler design, similar to barrel SET)

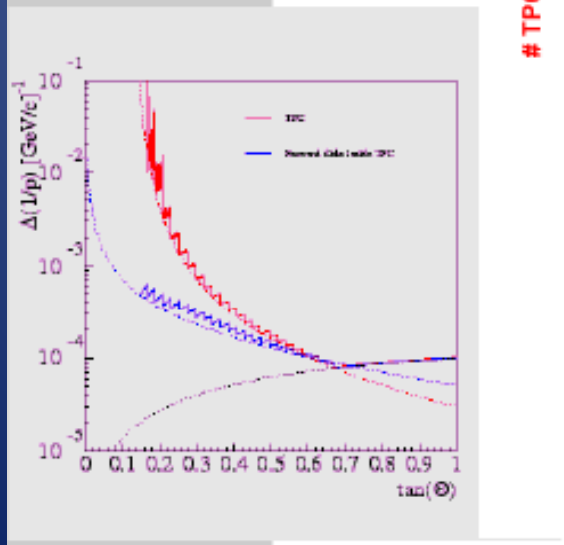
This serves as ‘’entry point’’ for ECAL.

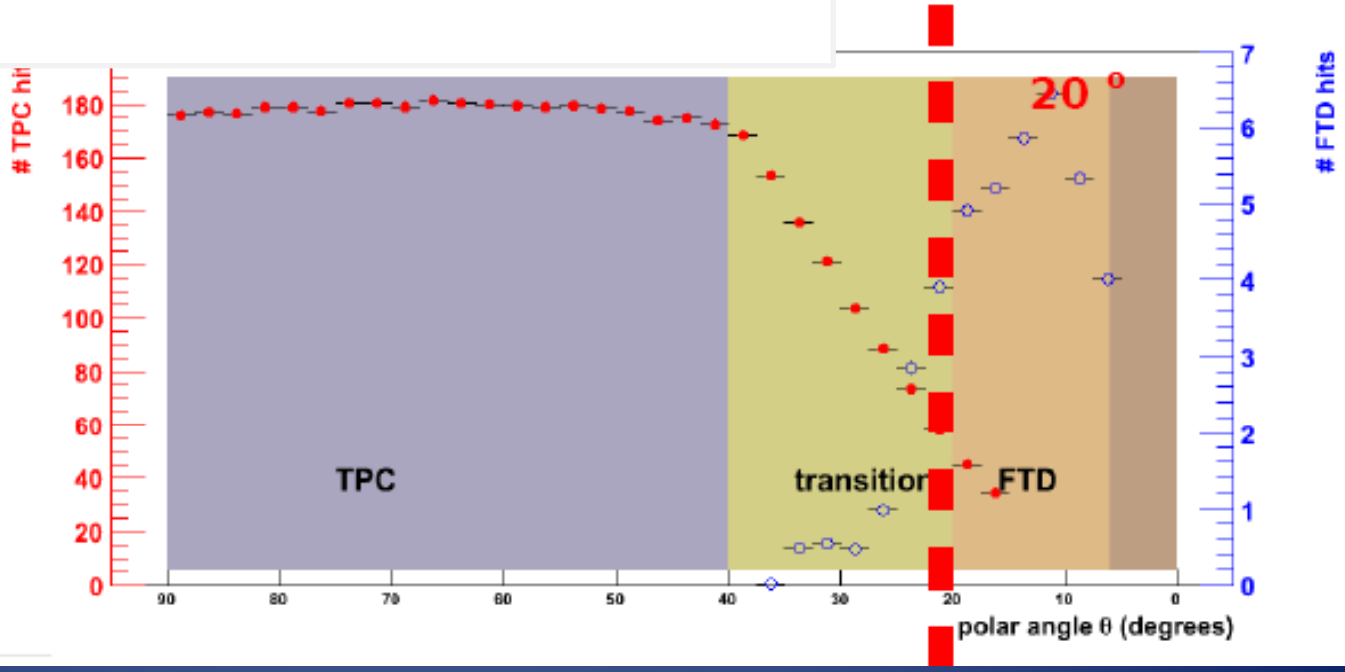
Forward tracking: interplay with central tracker

(Very) forward tracker in a gaseous + silicon tracker concept is "all-silicon"

For track polar angles below 40° reduced TPC coverage
Below ~ 30° FTD starts to contribute
Below ~ 20° FTD dominates the measurements

TPC/FTD hits vs. polar angle Large

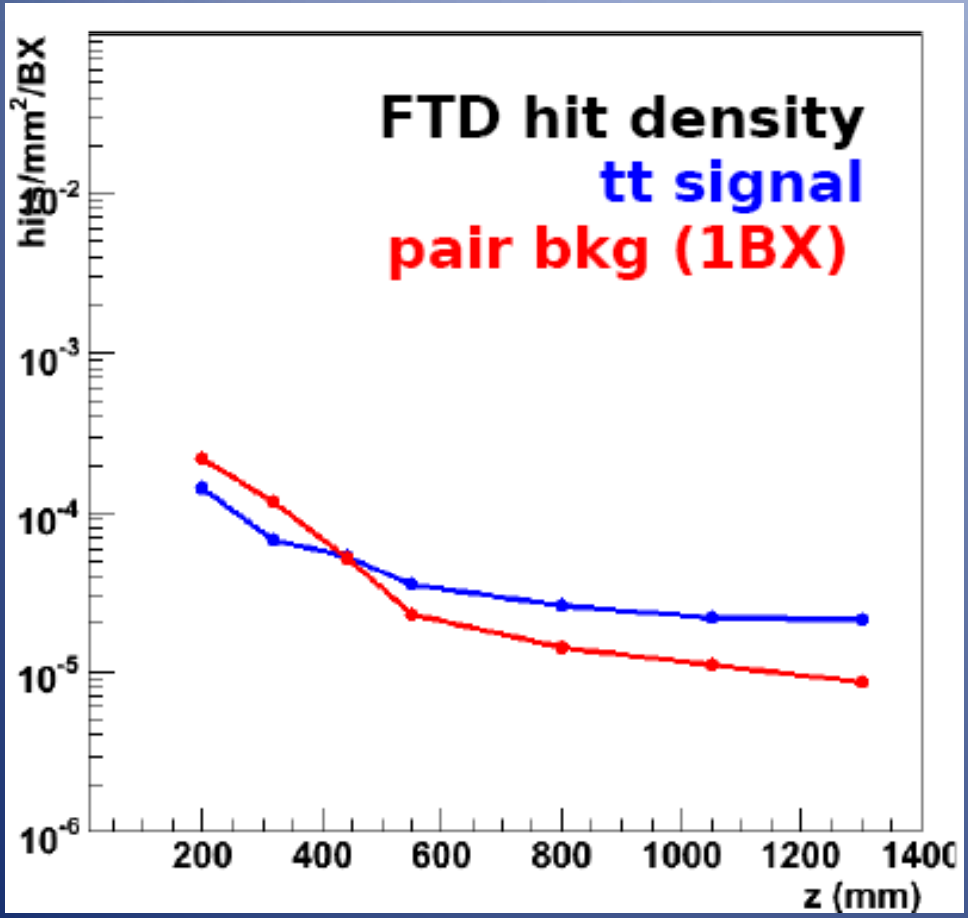




For very forward tracks (θ<20 ^{o}) FTD has to be capable of **standalone pattern recognition with 7 space points over nearly 2 m**, compared to:

Central track in ILD: 6 VXD + 2 S IT + O(200) TPC + 1 SET

Forward SiD: 4 VXD + 5µstrips



Significant background: hit Density due to a single BX comparable to that of tt-events

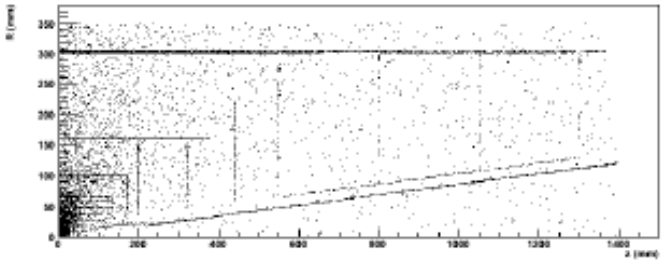
Forward tracking: challenges

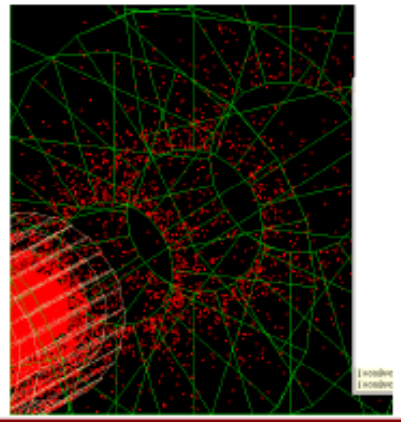
momentum resolution with unfavourable field orientation
lever arm, R-f resolution

impact parameter measurement for very forward tracks
material and resolution disk0 + VXD services

standalone pattern recognition in presence of background and low momentum tracks
R-segmentation, material, read-out speed

minimal distortion of particles/global performance
material





Baseline and Roadmap

Two timescales are foreseen:

- Be ready to build in 2012 (baseline & R&D)
- Be ready to build ≥ 2015 (R&D)

Baseline: based on microstrips and DSM FE bump bonded onto the detector (as proposed by SiLC in collaboration with Industry = HPK)

R&D: pursue on technological developments and use/keep an eye on more modern available solutions

R&D: Technological choices and issues

Sensors: edgeless, higher granularity, thinner

- Si-strip
- Pixel technologies
- New Sensors technologies (mainly driven by 3D on strips and pixels or ??)

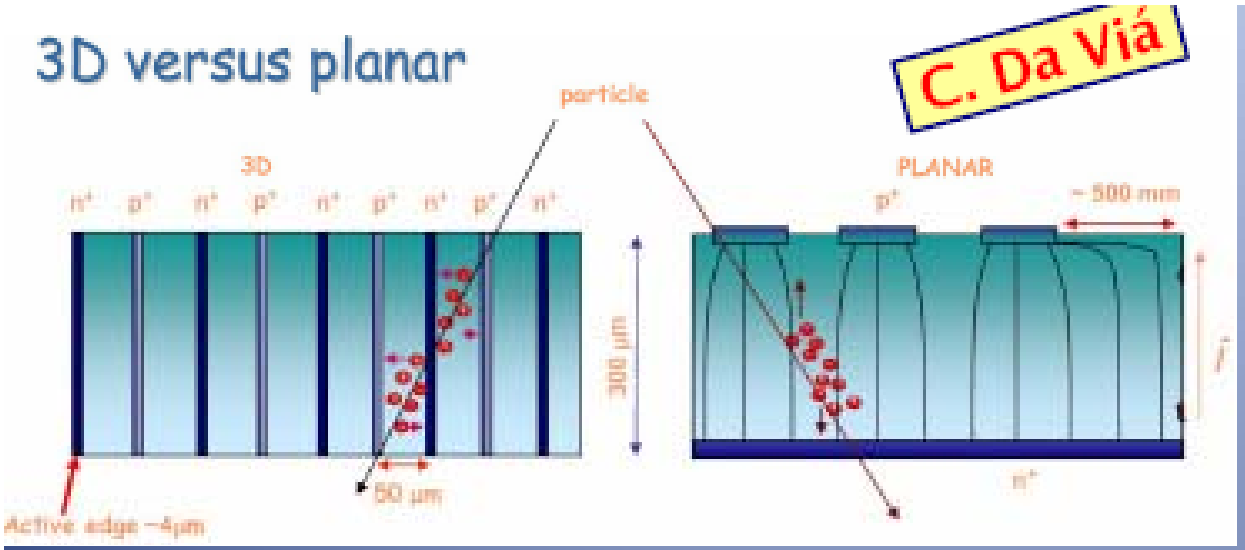
Electronics: low noise, low power consumption, power cycling, high processing level, high multiplexing, fault tolerant

- DSM FEE
- direct connection to the Silicon sensor (strip or pixel), 3D vertical interconnect
- integration to the overall readout and DAQ

Integration Technologies:

mechanical support and construction of elementary module (tile), cooling, connection of electronics to detector, cabling, alignment, mechanical integration of these components within the overall detector

Hand in hand with LHC upgrades or other facilities R&D and in collaboration with Industrial firms



Basic elements of the Silicon tracker:
Sensors
FEE readout system
Direct connection between them
- Bump bonding (HPK)
- 3D interconnect (starting within global effort)

NEW: 3D Planar strip detector by VTT

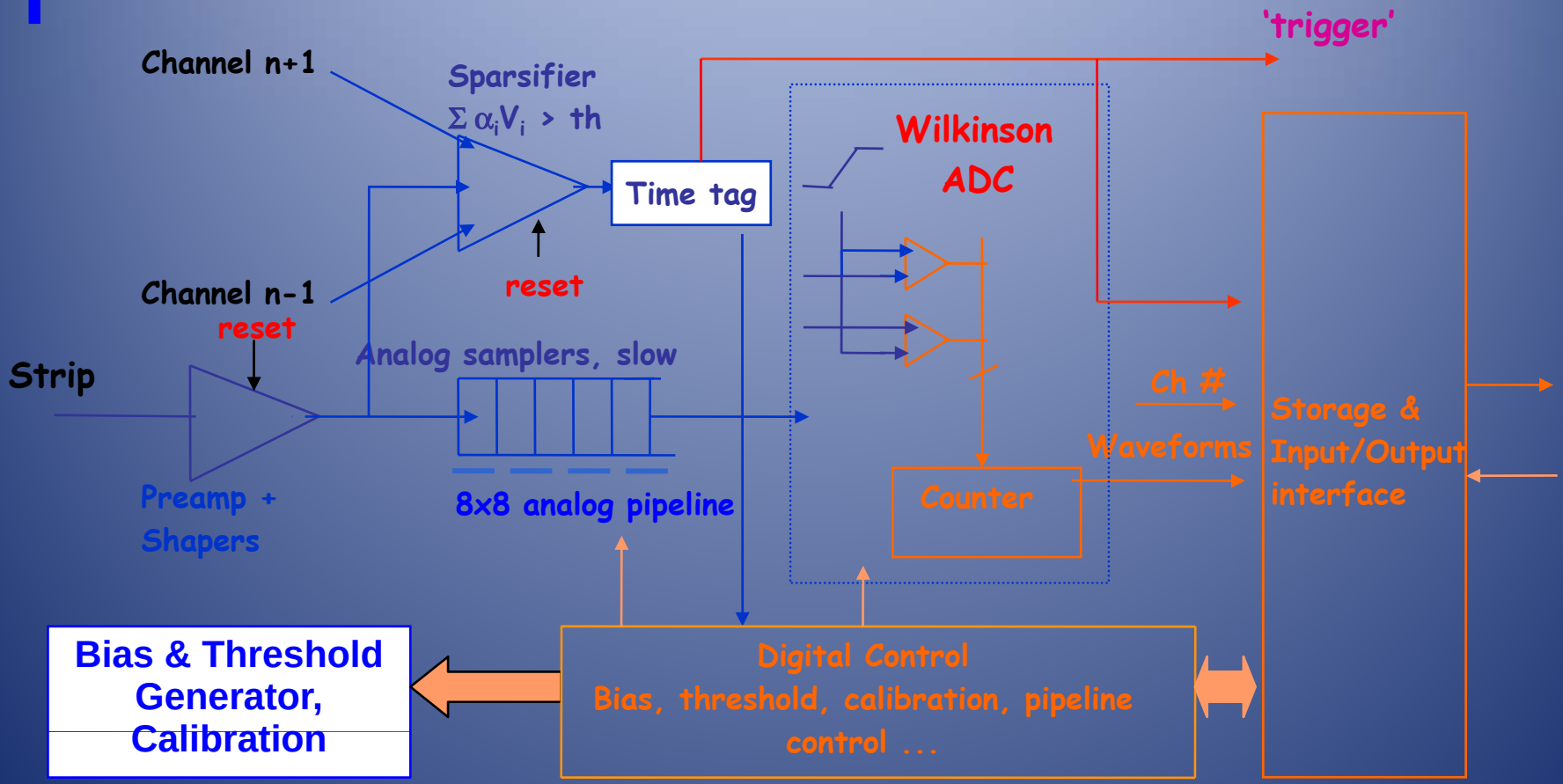
EDGELESS, THINNER

FE Electronics for Si trackers

- Analogue and digital processing of Si micro-strips
- Low noise
- Low power consumption
- High multiplexing factor
- Direct connection to the sensors
- Low material budget
- Easy to calibrate, high fault tolerance & performance

For many of these reasons choose CMOS DSM techno

General view of the circuit



Main features of new circuit

88 channels (1 test channel): Preamplifier, shaper, sparsifier, analogue pipeline (8x8 cells), 12 bits ADC
Can be revisited to cope with CLIC machine constraints
2D memory structure: 8x8/channels

Fully digital control:

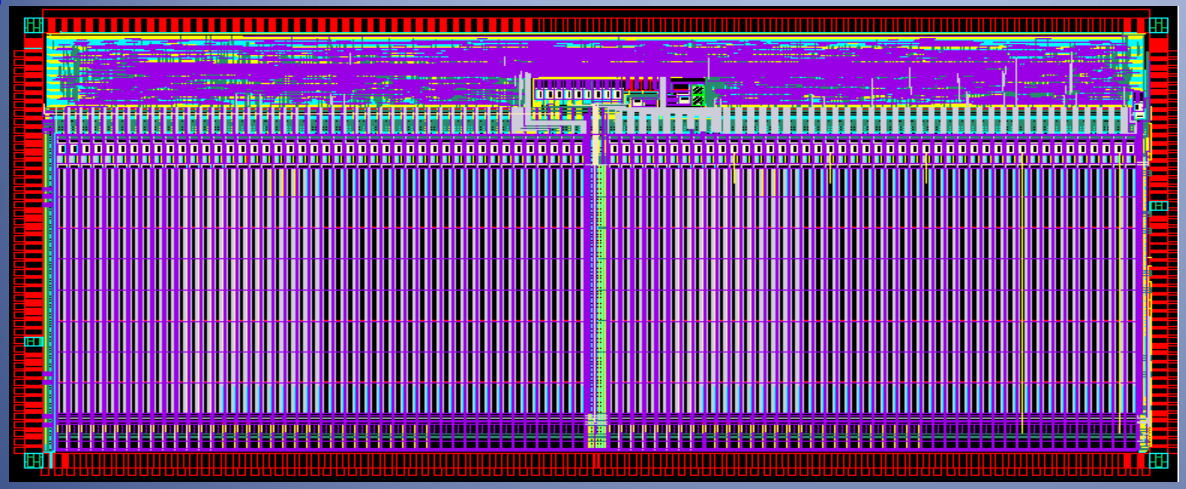
- Bias voltage(10 bits) and current (8 bits)
- Power cycling (can be switched on and off)
- Shaping time programmable
- Sampling frequency programmable
- Internal calibration (fully programmable 10 bits DAC)
- Sparsifier's threshold programmable per channel
- Event tag and time tag generation

=> High fault tolerance
=> High flexibility, robustness

.....

2 Trigger modes: Internal (Sparsification integrated)
External (LVTTL) for beam test

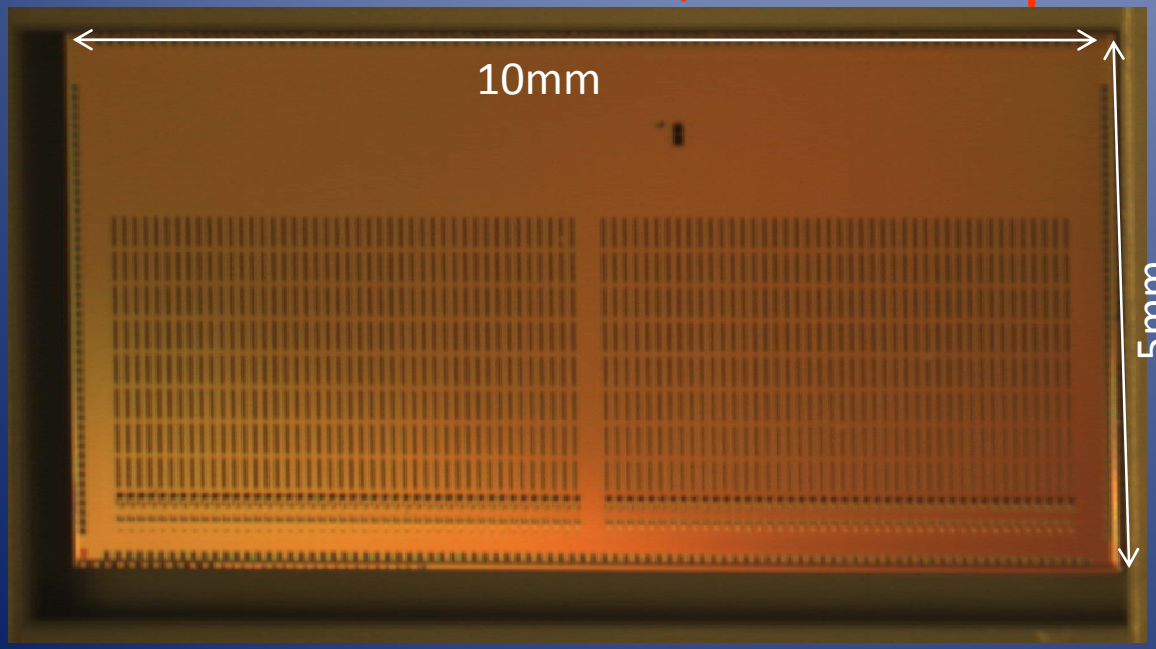
LAYOUT VIEW and PHOTOGRAPH



Size: 5mmx10mm
88 channels (105um pitch)
105umx3.5mm/channel

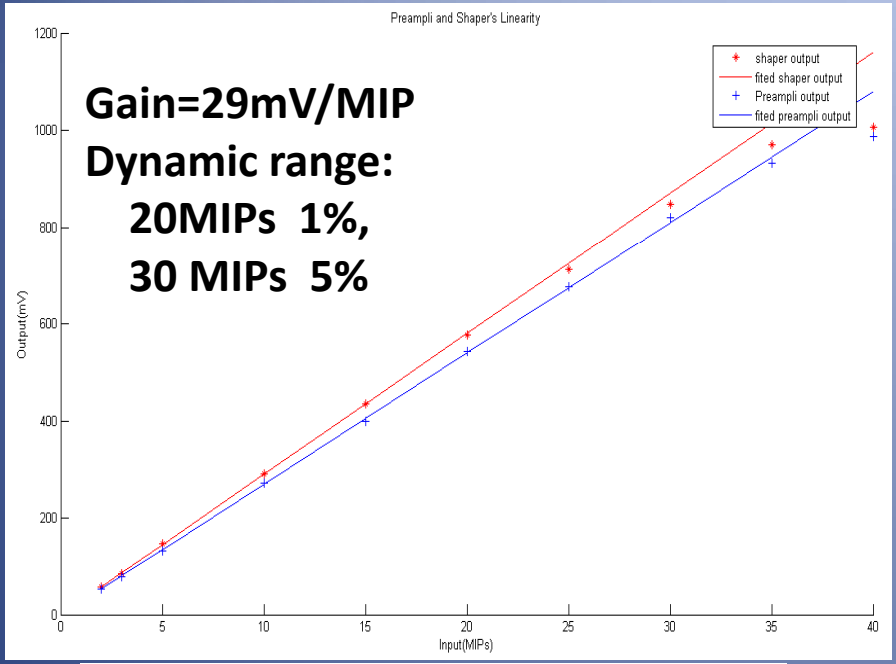
Analog: 9.5mmx3.5mm
Digital : 9.5mmx700um

Submitted June 24th '08, received September 12, 08, 20 packaged for functionality tests; received end last week.

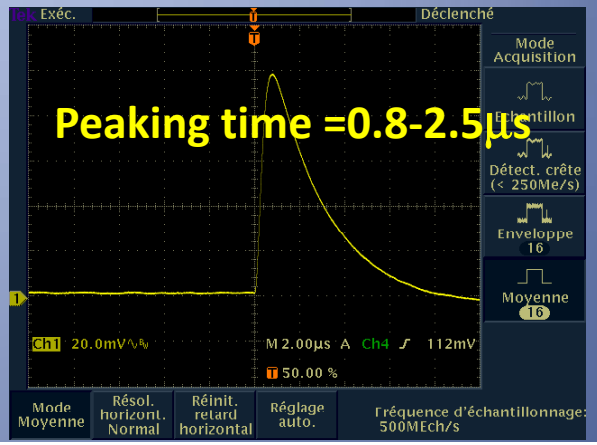


Photograph of the new chip SiTR_130-88

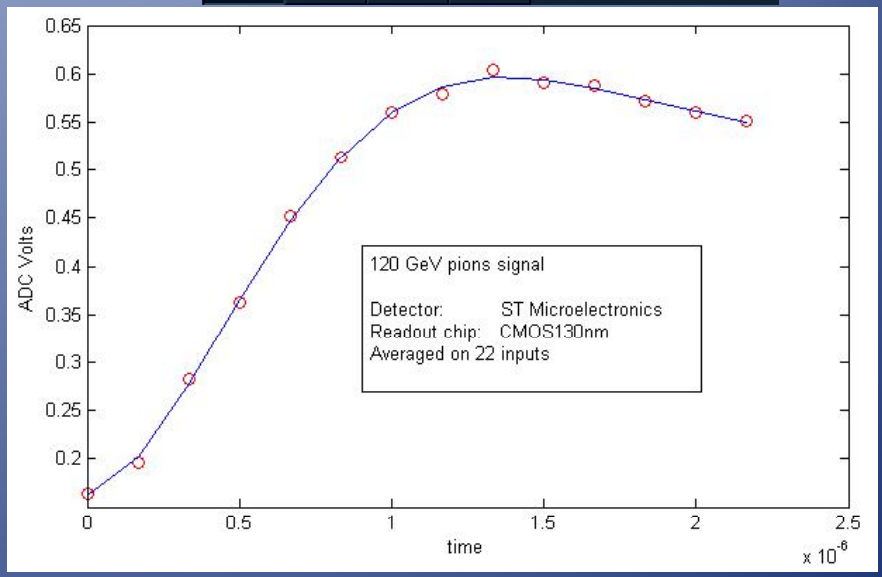
Performances of previous 130nm chip version

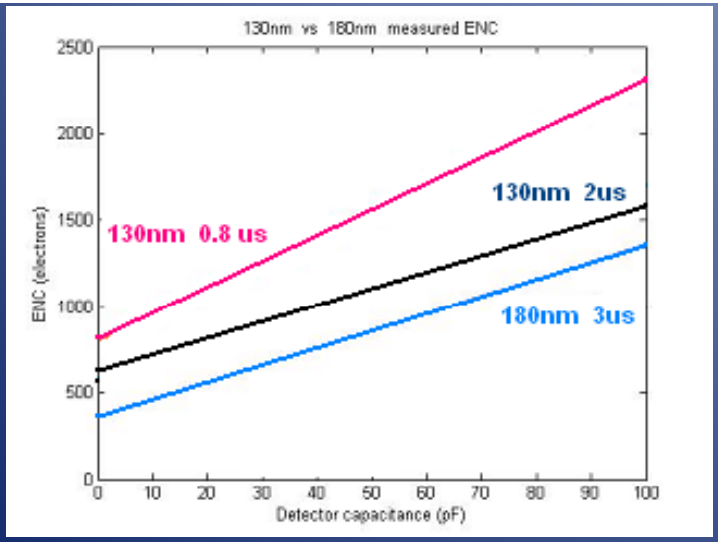


Gain=29mV/MIP
Dynamic range:
20MIPs 1%,
30 MIPs 5%

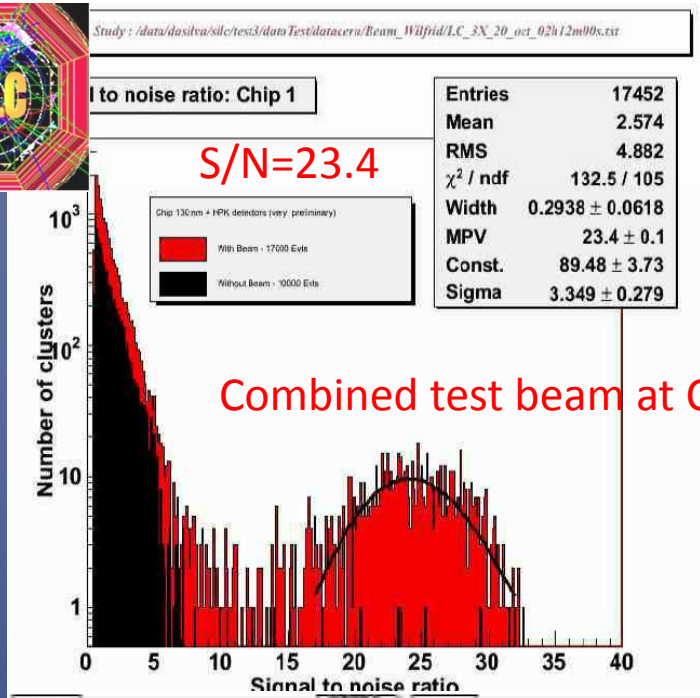


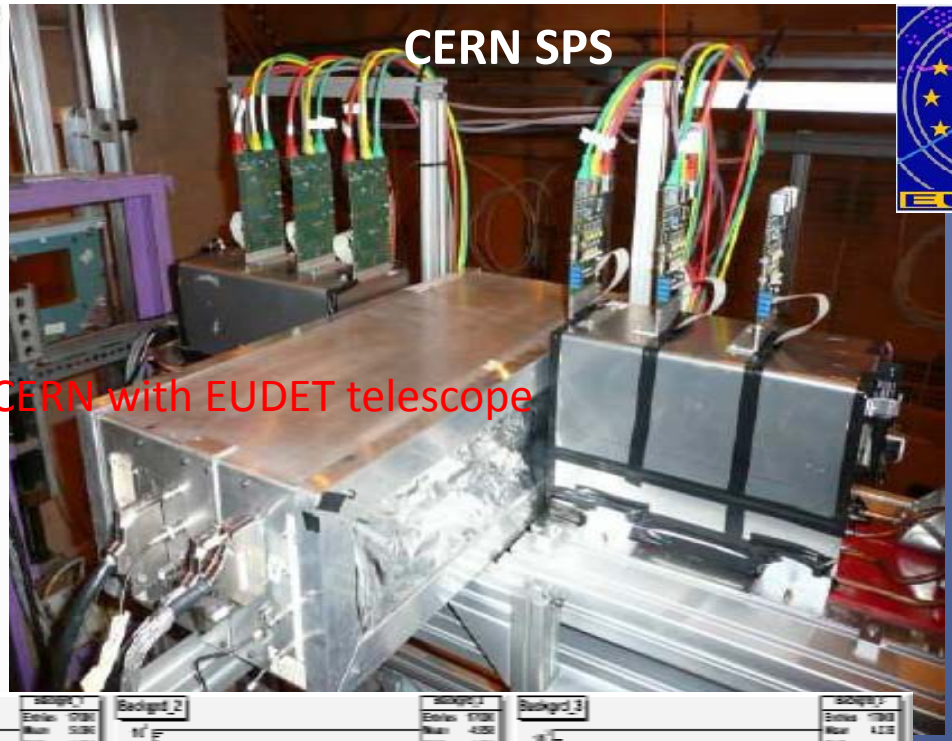
Peaking time =0.8-2.5µs



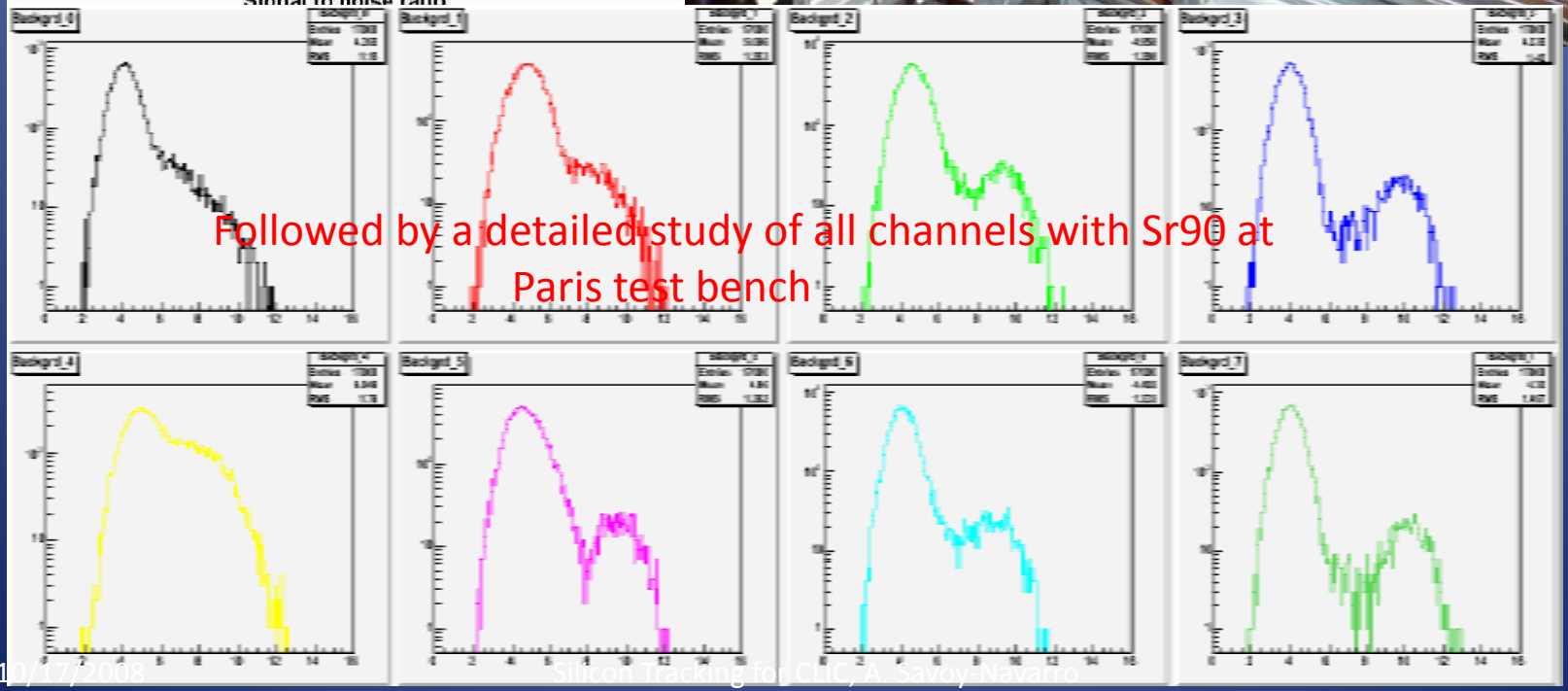


130nm @ 0.8 µs : 850 + 14 e-/pF
130nm @ 2 µs :625 + 9 e-/pF
180nm @ 3 µs : 375 +10.5 e-/pF





Combined test beam at CERN with EUDET telescope



Followed by a detailed study of all channels with Sr90 at Paris test bench

CLIC vs ILC: COOLING ???

In the Silicon tracking scenario for ILC: there is NO cooling

Because of:

⇒Low power dissipation per channel (1mWatt)

⇒To be added to the power cycling (factor 70)

⇒ No major radiation hardness issues

⇒ External layer strips length relatively long (up to 30cm)

This is certainly a major element in being able to reduce the Material budget.

A careful study need to be made in the CLIC case revisiting the FEE power dissipation (especially VFE), the power cycling issue etc...

Perspectives & concluding remarks

- Silicon based tracking technology is certainly suited to build the large area trackers for the future LC(‘s)
- A all Silicon-tracking system is a well integrated system that offers a lot of advantages especially in the large angle and very forward region that are becoming more & more crucial for Physics at these energies. It works both at ILC and CLIC.
- Combined with a central gaseous tracker the Si tracking components help in overall angular coverage, improvements in spatial and momentum resolution, time stamping, alignment and handling of distortions. It provides in addition redundancy.
- These two scenarios are feasible both at ILC and CLIC
- But important R&D activities must be pursued on sensors, FEE, mechanical issues, with a certain number of common goals but also some differences.

The SiLC R&D collaboration is one of the sub-detector ''transversal'' R&D collaboration that tackles all these issues for the ILC proposed detectors,
with strong synergy with the LHC Si tracking builders (legacy) and future LHC upgrades.
The requests of the CLIC tracking are indeed starting to be also taken into account by this collaboration.

With many thanks to all SiLC and EUDET collaborators (special to V. Saveliev, M. Valentan, M. Vos) and also C. Gatto, H. Weerts, G.P. Yeh ....apologies for not listing all contributors.