# CLIC: Timing in Tracking

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# OUTLINE

- Specification from the CLIC machine
- Use of timing information in CLIC tracking
- ASICs Current developments with timing capability
- Long term strategy for fast timing tracking R&D
- Conclusion

# LHC, ILC, CLIC, NA62

| | LHC | | | |
|---|---|---|---|---|
| | **ATLAS VX** | ILC | CLIC | NA62 [1)] |
| **BX spacing [ns]** | 25 | 300 | **0.5** | avg 1ns |
| **Nb of BX/train** | 2808 | 2820 | **312** | $2*10^9$ |
| **Bunch train length** | 70μs | 1ms | **156 ns*2 s** | |
| **Repetition rate [Hz]** | 40M | 5 | 50 | 0.07 |
| **Nb of Bunch/s** | 36M | 11400 | 15600 | $10^9$ |
| **Hit/mm$^2$/Bunch max** | 0.05 | 0.05 | **0.1-1[2)]** | $6*10^{-4}$ |
| **Radiation level fluence** | **~$10^{15}$/10 y** | **~$10^{13}$** | **~$10^{14}$** | **~$2•10^{14}$/y** |

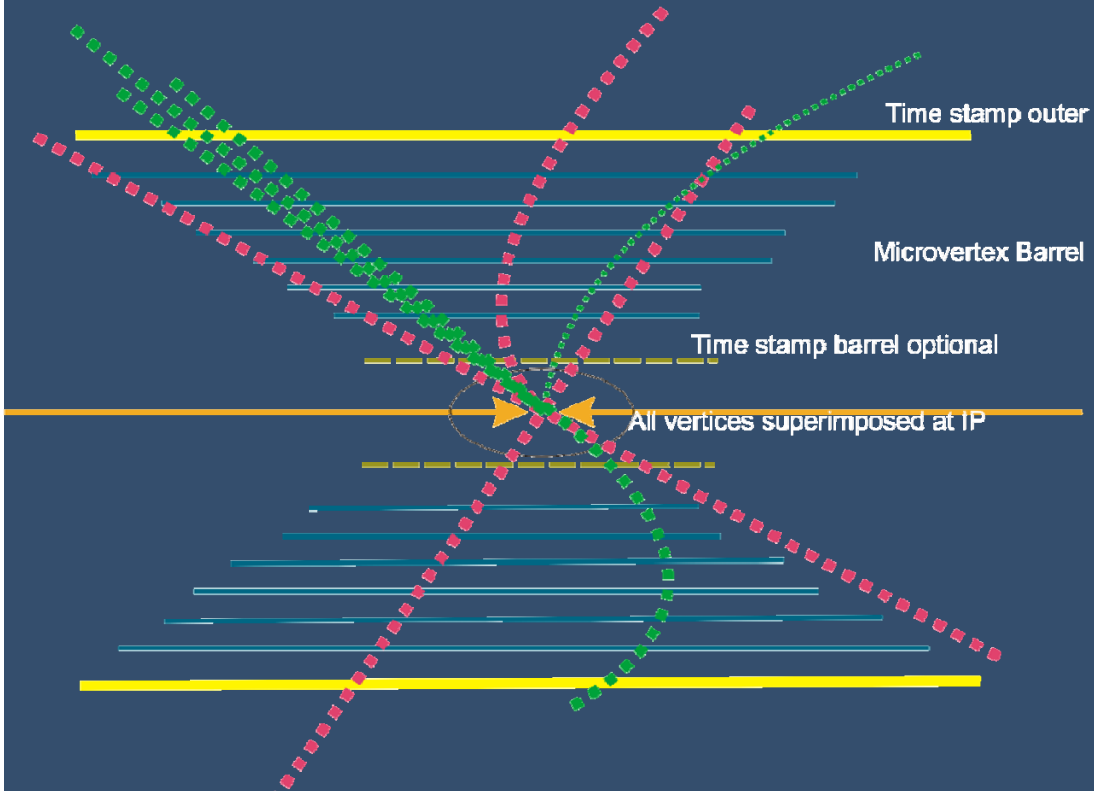
bx = particles train = spill

Daniel's talk: background pairs and muons at r=3 cm @ 5T and r=1 cm @ 3T

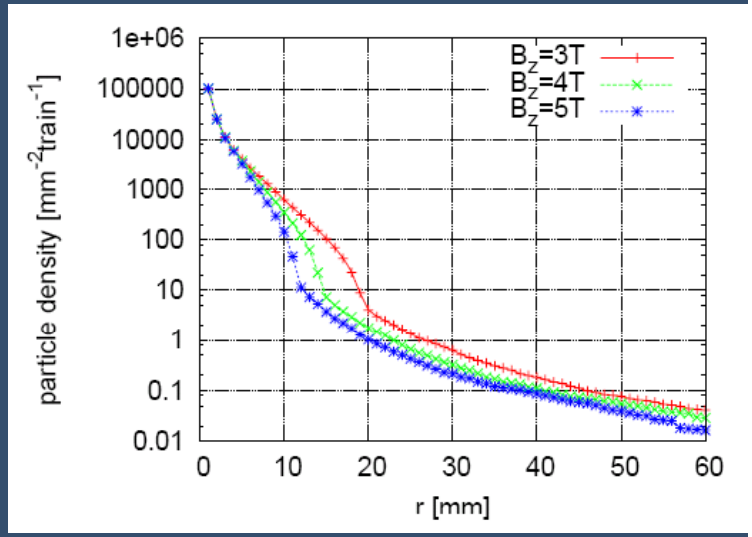
http://tecker.web.cern.ch/tecker/par2007.pdf, http://clic-meeting.web.cern.ch/clic-meeting/clictable2007.html

# Why timing in tracking in CLIC

- Eliminate tracking ambiguities within a train
  - Caused by superimposed vertices, track topology cannot be use anymore for vertex identification
  - Stamping tracks helps to identify vertices with bunches
- Would timing in tracking help to reject background



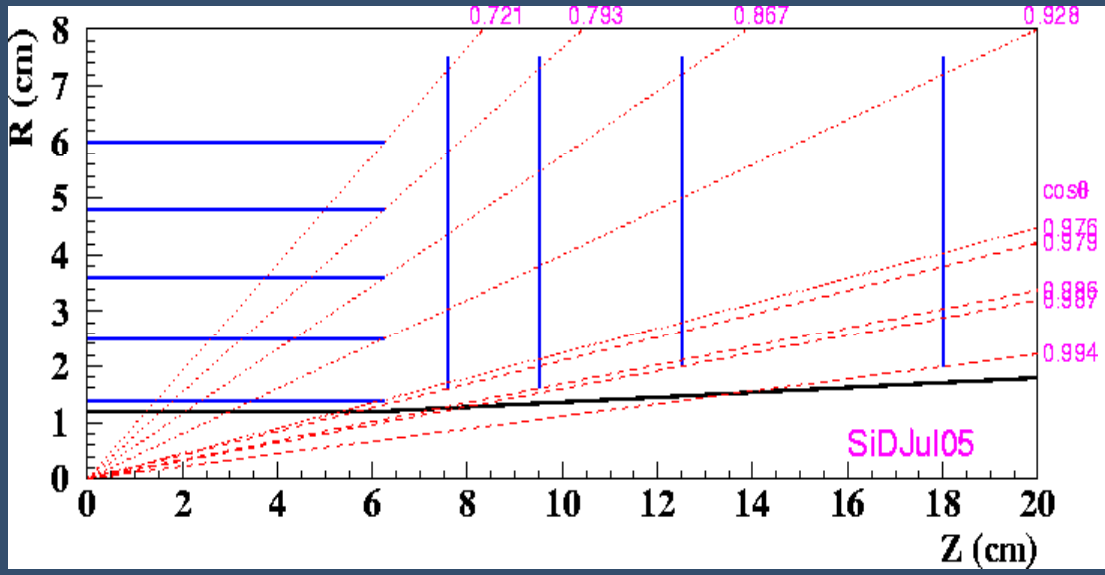

D.Schultze, pairs production at 3 TeV



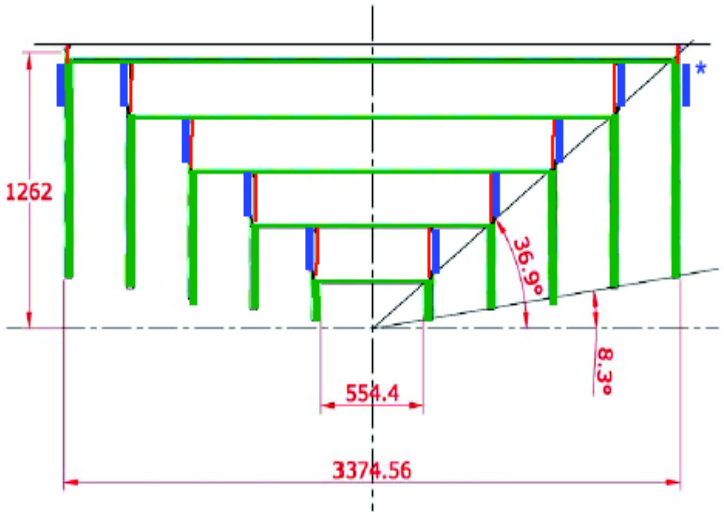
# CLIC tracking Layout ? SiD example

- Choice of the timing implementation in the tracking system
  - Radius, number of timing-tracking planes
  - Outer tracker barrels look more attractive if background rejection needed
    - Tracking geometry might be strip or macropixel
  - Timing in vertex possible if coherent pairs rate affordable
    - What is the benefit in terms of tracks reconstruction?

ILC SiD vertex layout




ILC SiD tracking layout



# Objectives of the time stamping

- Identify tracks with bunches within a train: 3D + t tracking
  1. Associate hits to bunch numbers
  2. Associate tracks to time stamped hits
  3. Associate vertex to time stamped tracks
  4. Produce vertex and track candidates associated to bunches
- Correlate time stamped tracking with calorimeter and muons
  - Timing capability of calorimeters and muon system?
- Pair, background rejection: more ambitious objective
  - Removing non-pointing vertex tracks and hits
    - In tracking barrels
    - In vertex

# Chip data rate

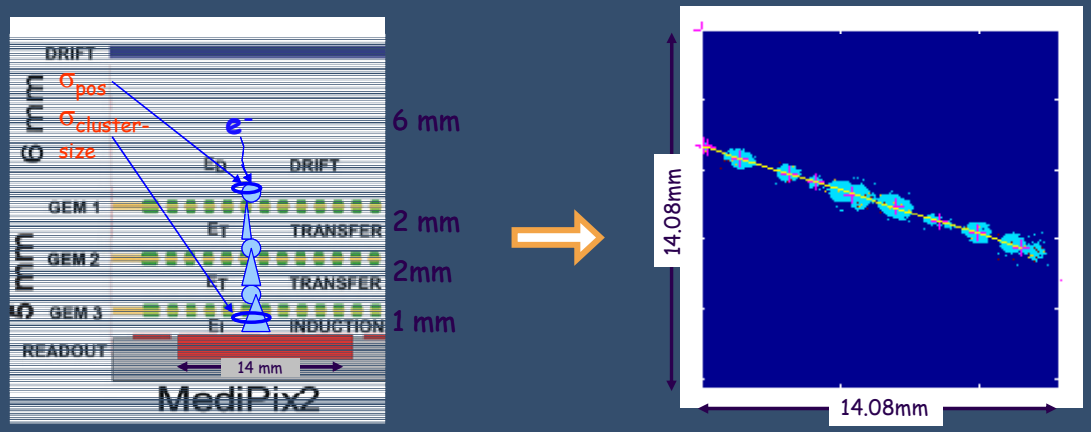
- 1 hit/mm²/bx
  - Assume chip of 15 x 15 mm = 225 mm²
  - Assume 32 bit data per hit
    - (16 bit address + 11 bit time + …)
  - Instantaneous train Hit rate per chip 225/bx or 450 Ghits/s
  - Hits accumulated per chip during train: 70200
  - Data accumulated per chip during train: 70200* 32 = 2.2 Mbit
- Data stored during train and read-out afterwards (off-time is ~20 ms)
  - Otherwise data rate is high
- Preliminary conclusion
  - local 2 Mbit local memory is needed

# Present ASIC with timing

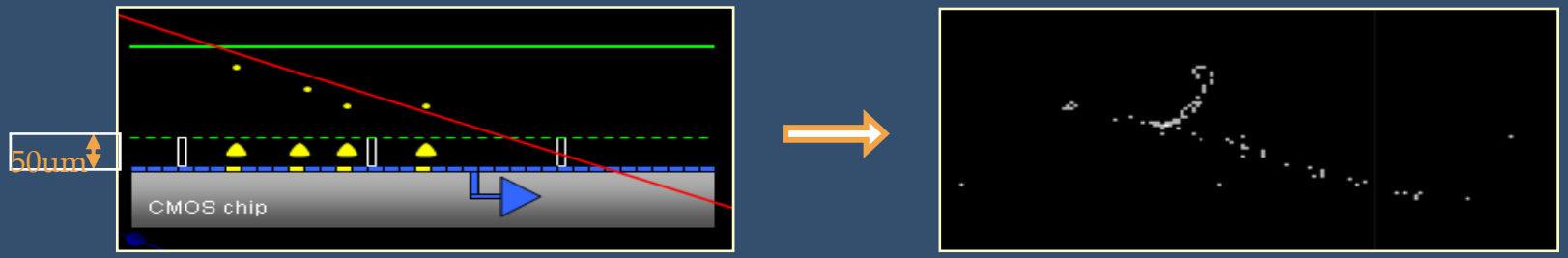
- Specification and architecture
  - Timepix
  - Gossipo
  - NA62 Gigatracker
    - Processing in pixel cell
    - Processing outside pixel cell

# From Medipix to Timepix

- A novel approach for the readout of a TPC at the future linear collider is to use a CMOS pixel detector combined with some kind of gas gain grid
- Using a *naked* photon counting chip Medipix2 coupled to GEMs or Micromegas demonstrated the feasibility of such approach




GEM



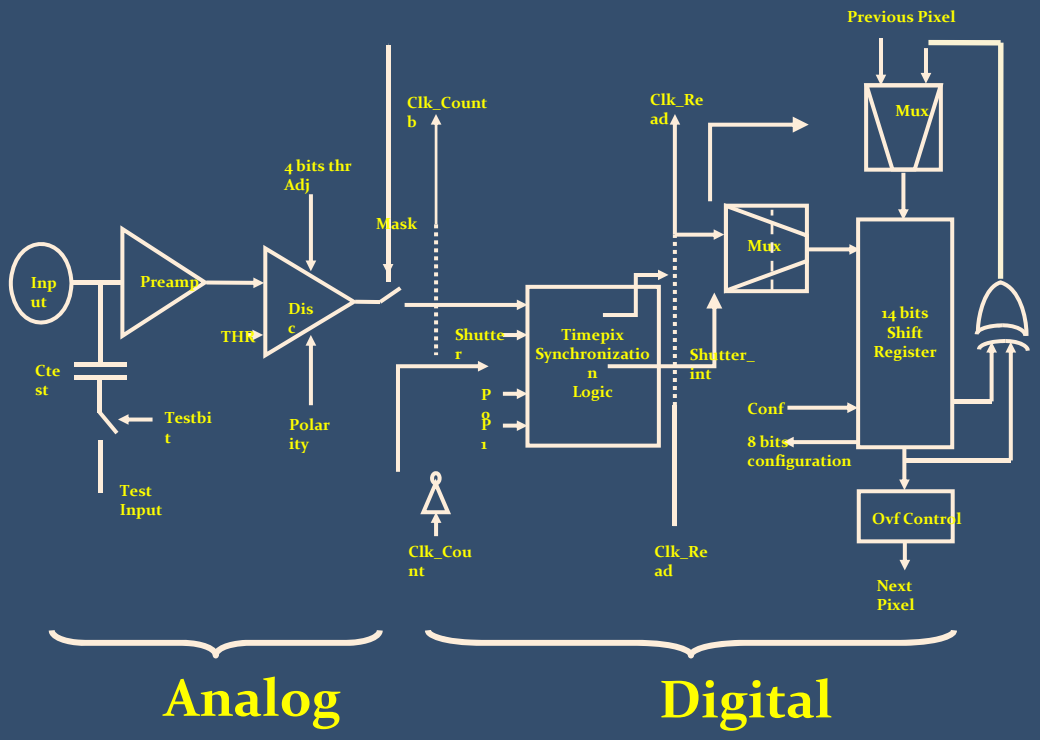

Micromegas

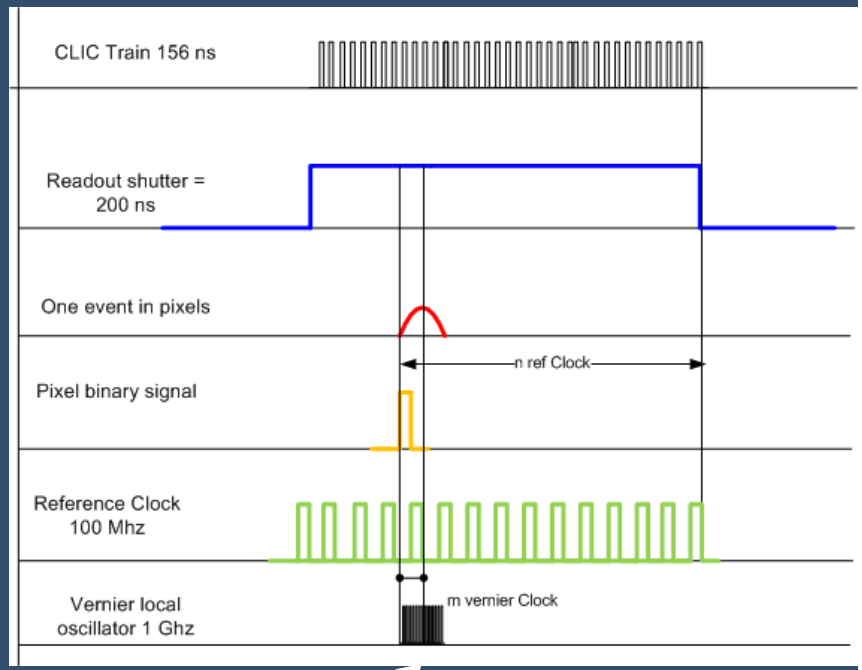
# From Medipix2 to Timepix …

- NIKHEF/Saclay, Freiburg experiments in 2004/2005
  - Demonstrated 2-D reconstruction of single electrons feasible with *naked* Medipix2 chip
- To further exploit Medipix2 has been redesigned to incorporate a time stamp with a tunable resolution of 100 to 10ns.
  - ⇒ 3-D position + time
- Timepix Requirements
  - Keep as similar as possible to Medipix2
  - Eliminate 2nd threshold
  - Add possibility of programming pixel by pixel arrival time or TOT information
- This modification was supported by the JRA2/EUDET Collaboration (www.eudet.org)

# Timepix schematic

- Block diagram, possible implementation for CLIC track timing

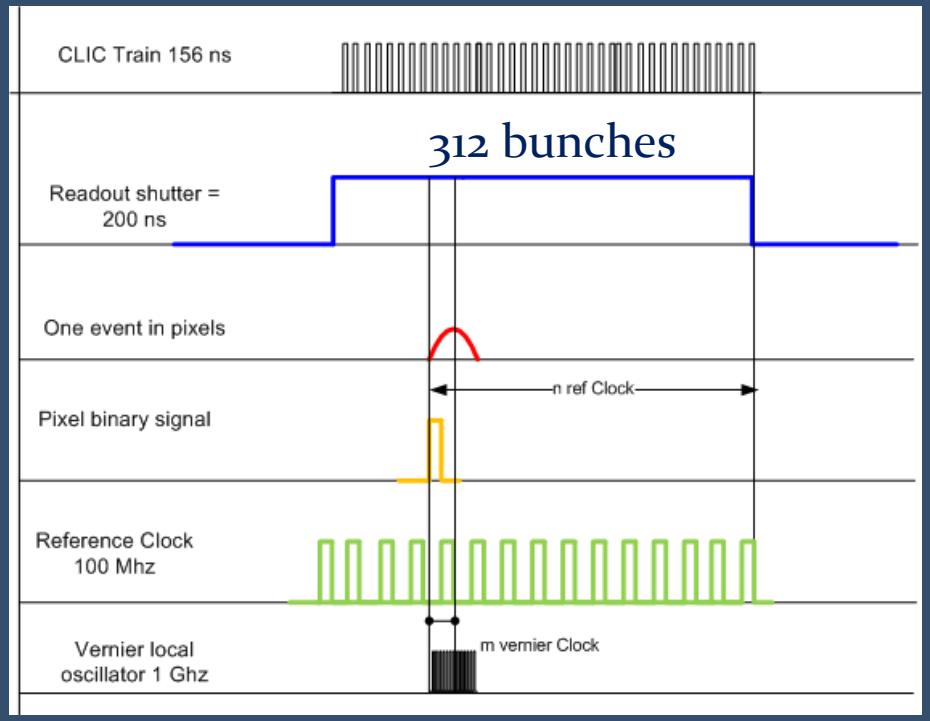


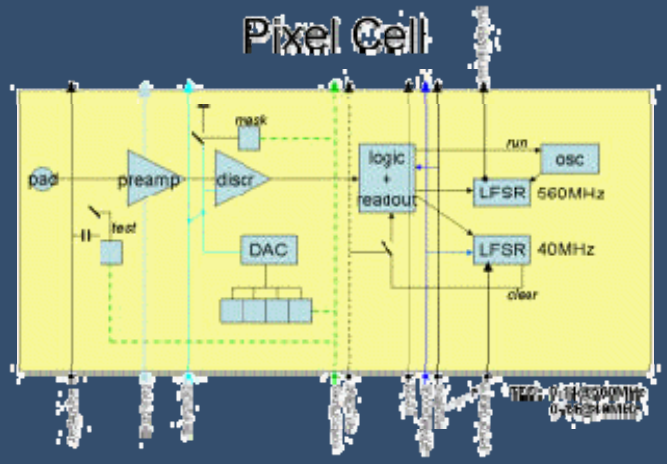




Gossipo Nikhef
vernier is 560 Mhz
Reference clock is 40 Mhz

# Gossipo chip

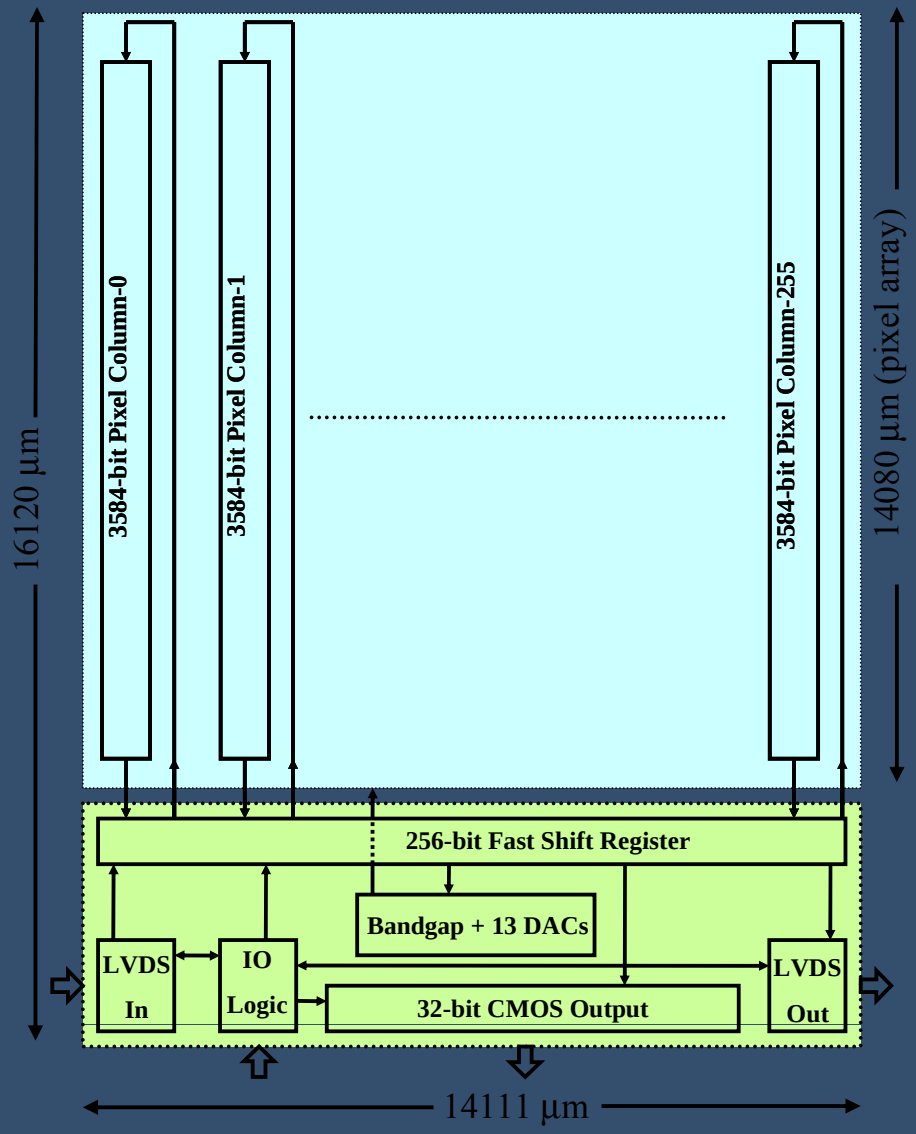
- It is a timing improvement of the TimePix scheme
  - Scheme developed at Nikhef
  - TimePix pixel cell has an additional vernier counter driven by a 560 MHz local oscillator (ring counter)



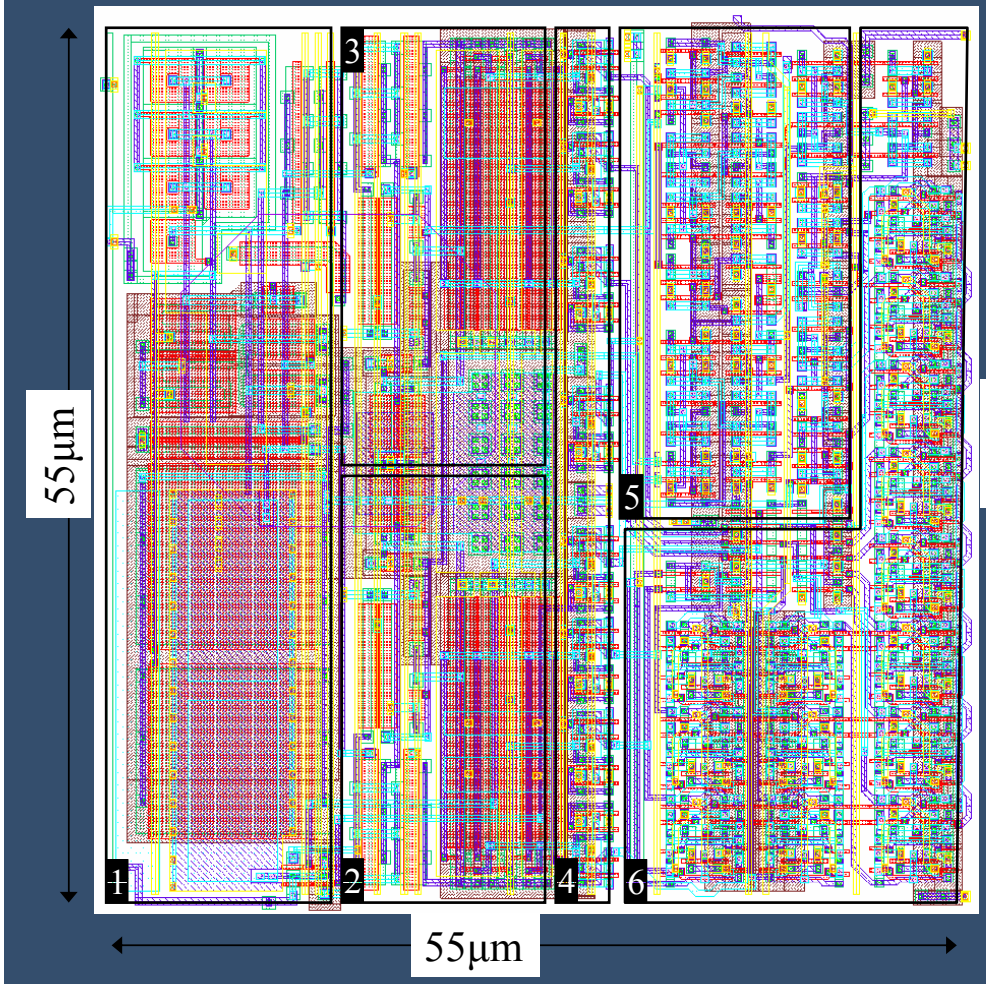
# Timepix Architecture

- Chip architecture almost identical to Mpix2 MXR20
  - M0=M1=1 and Shutter ON FClock used as Ref_Clk
- 256x256 55µm square pixels
- Analog Power
  - 440mW
- Digital Power Clk =50MHz
  - 220mW, Clk distribution
- Serial readout at100MHz
  - 9.17 ms
- Parallel readout (@100MHz)
  - 287 µs
- > 36M transistors

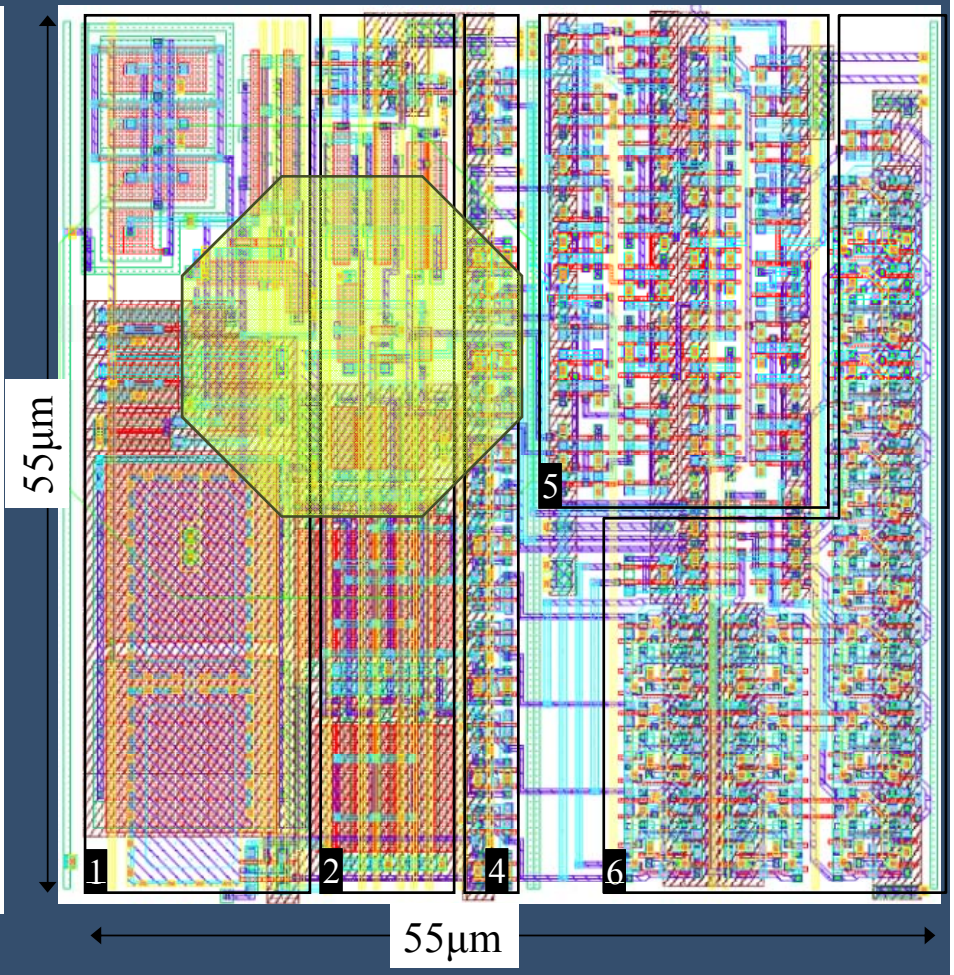


# Medipix2 to Timepix2 layout

- Mpix2MXR20 layout

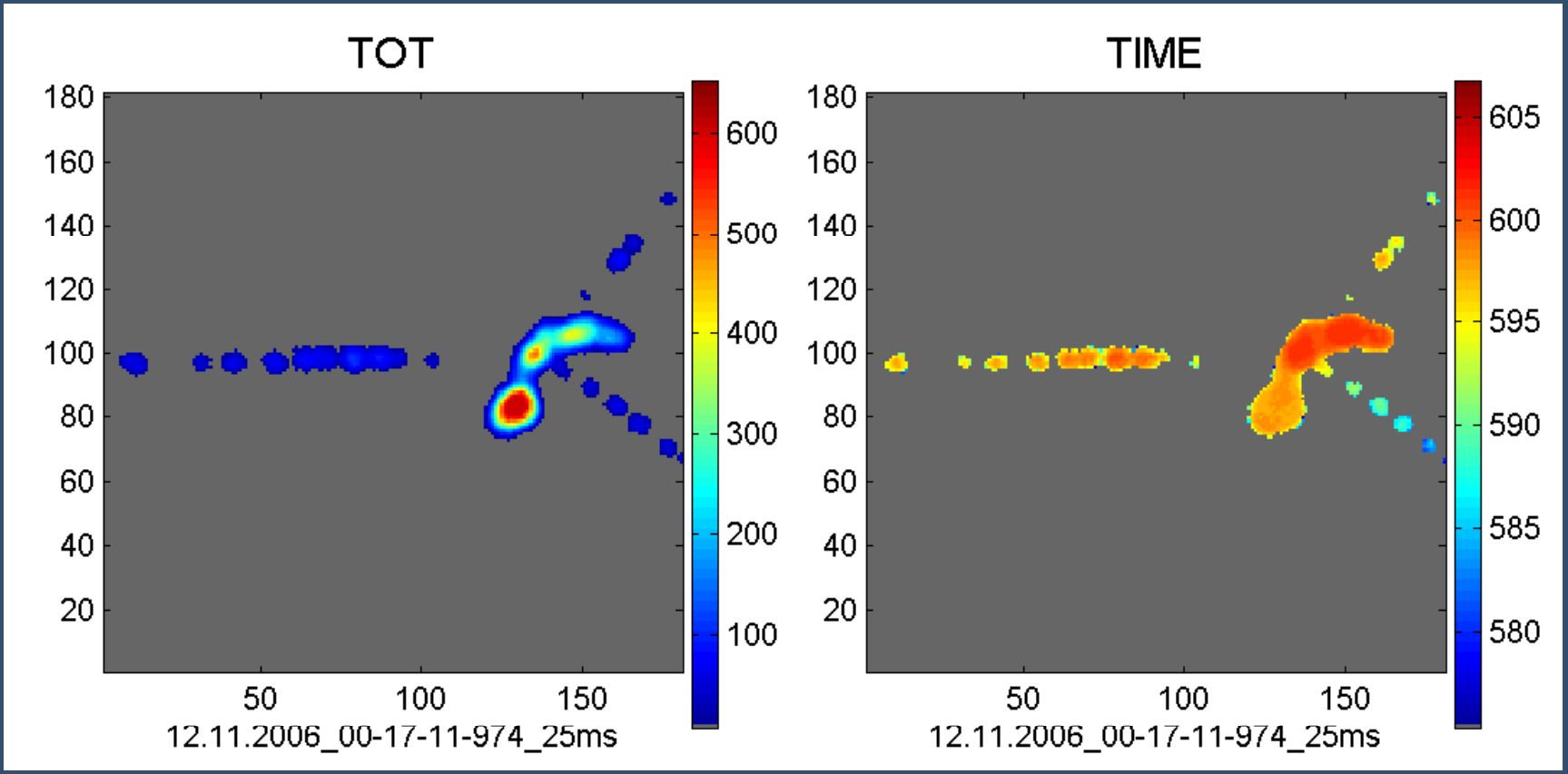



Timepix layout



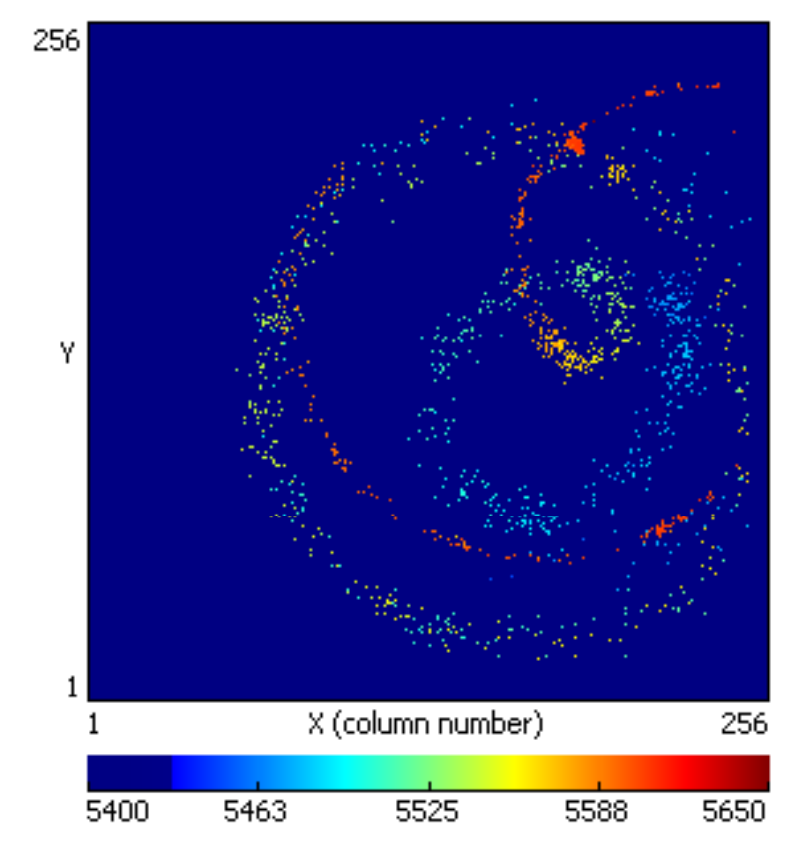
# Timepix with 3x GEM detector

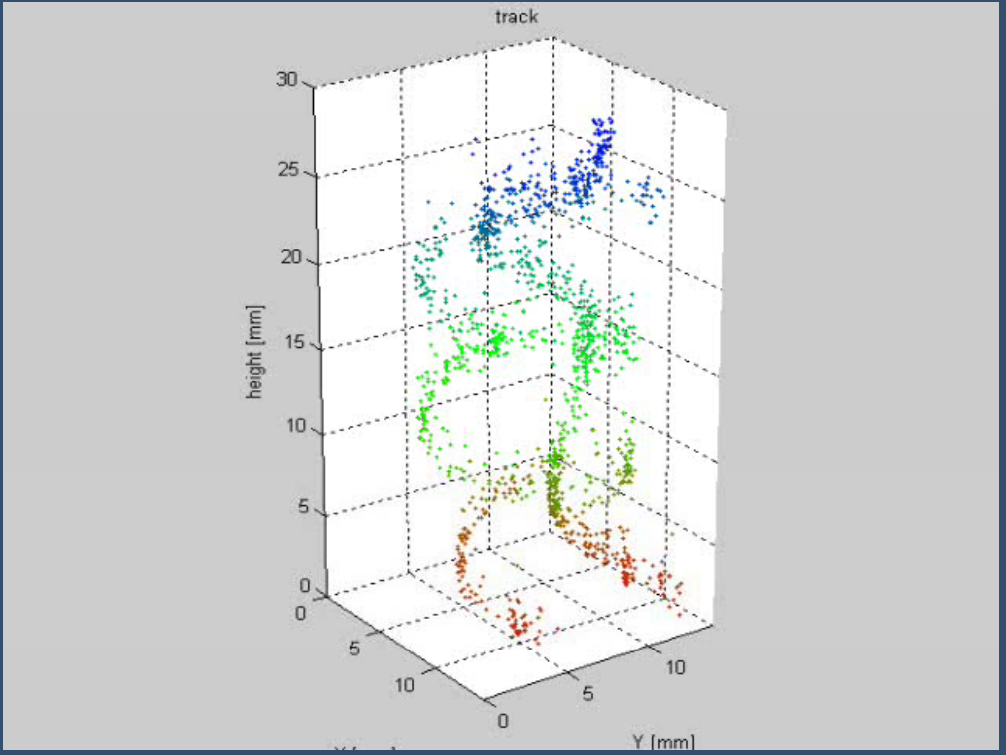
- DESY test beam in November 2006



# TimePix with Micromegas

- A 5 cm³ TPC (two electron tracks from $^{90}$Sr source)



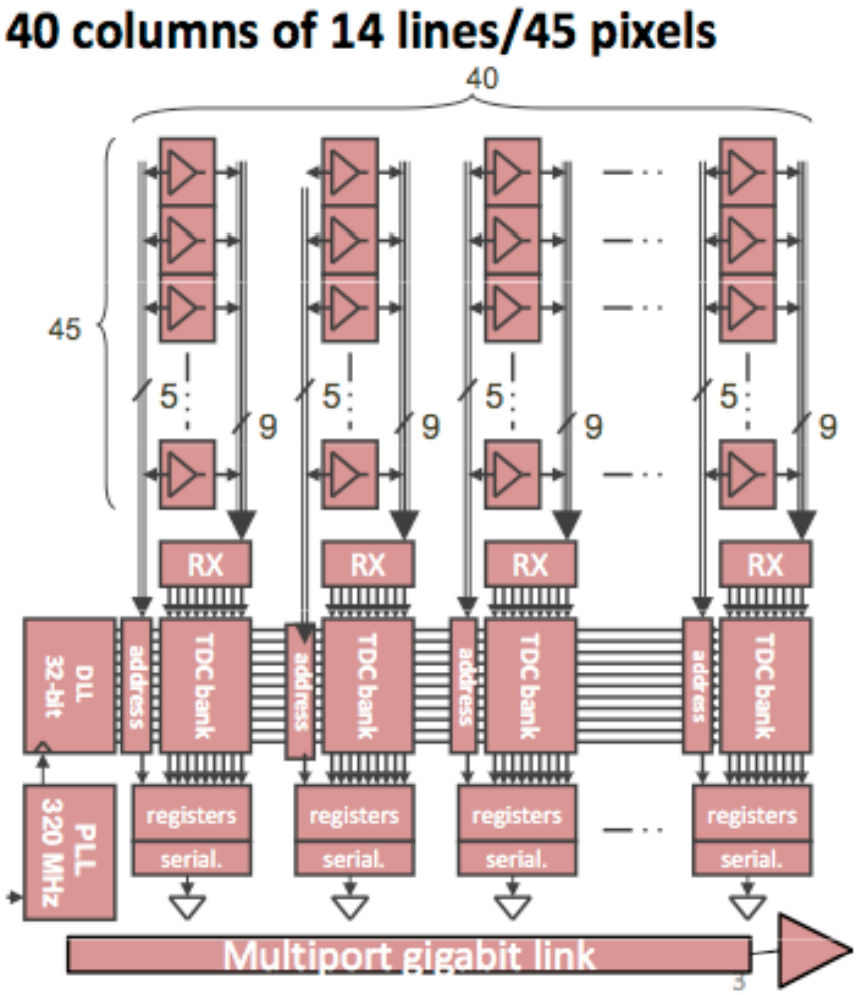




Nikhef thanks to J.Timmermans

# NA62 EOC Architecture

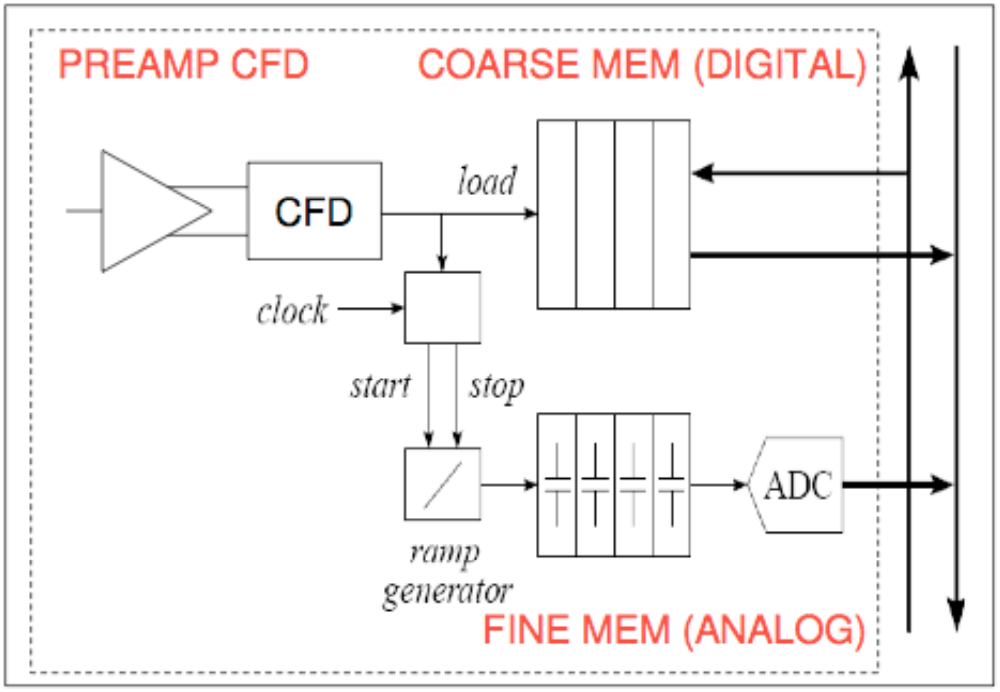
## EOC architecture

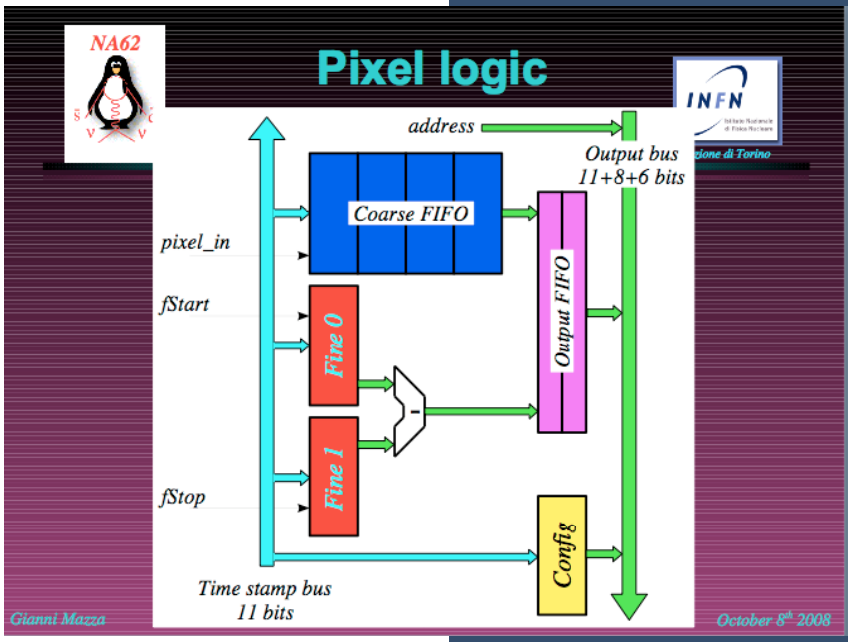
- No digital processing in pixel
- TDC, Time stamping and data pipelining in end of column
- DLL based digital TDC
- Time walk correction by a time over threshold discriminator
- Column pixel addresses encoded with a 5 x 9 matrix
- Bus system using cross coupled transmission lines, low current swing signal , with pre-emphasis for dispersive loss compensation



# NA62 on-pixel TDC architecture

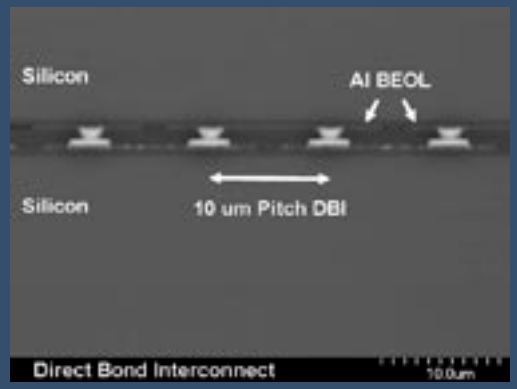
Efficient local derandomization
Efficient use of pixel area
Reduce end of column complexity

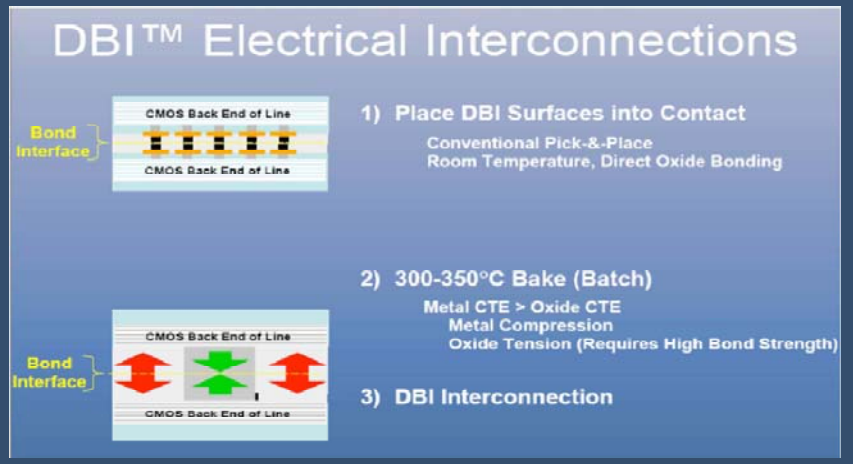


# The future of Hybrid design

- The detector/electronics can be optimized
  - Si, thin EPI , 3D Si etc.., any advanced CMOS process can be used
  - Detector speed is essential for CLIC timing performance
  - Not possible for monolithic device
- Optimal signal to noise at high rates
  - Essential for clean pattern recognition in complicated high CLIC events with background
  - Single pixel hit
- Advance in sensor electronics hybridation
  - Assembly without bumps
  - Thinning electronics and sensor wafers
- Direct bond interconnect (DBI) technology developed by Ziptronix, followed by FNAL
  - 10 µm pitch, 1.5 M interconnects/cm², thinning wafer down to 20 µm




http://www.ziptronix.com/techno/

# The future of cooling

- On chip cooling integration: Microchannel cooling system
- Compatible with 3 D integration
  - Jae-Mo Koo, Integrated Microchannel Cooling for Three-Dimensional Electronic Circuit Architectures
  - With microchannel evaporators engineered in silicon, microfluidics
    - Long term development… like CLIC

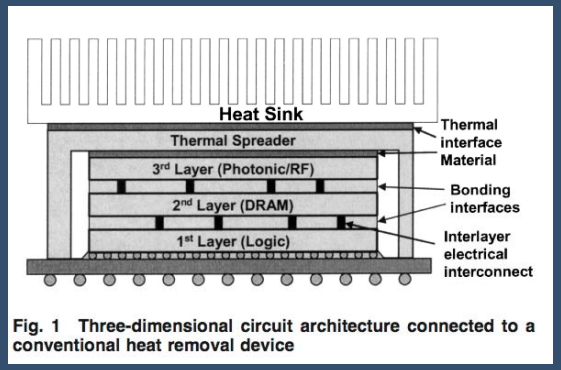
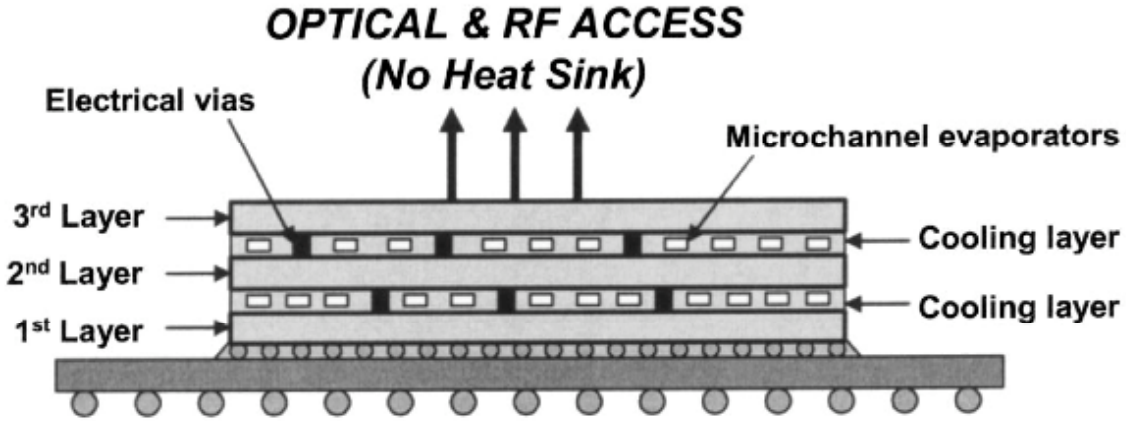



Fig. 1 Three-dimensional circuit architecture connected to a conventional heat removal device

http://www.stanford.edu/group/microheat/




(a) 3D circuit with a microchannel cooling system

# Summary on readout architectures

- Timing in vertex
  - Timepix architecture fits well to pixel vertex geometry
    - Is power consumption affordable?
      - Power cycling strategy, low power circuit design
      - Further design study should be done to validate this approach
    - Is timing in vertex needed?
      - Answer should come from study of track reconstruction and background
- Timing in tracking Barrels
  - NA62 Gigatracker is well adapted to macropixel or strip
    - power consumption?
    - Cabling and cooling looks easier than in vertex
- Typical power/cm$^2$
  - Timepix, 600mW, 50µm pixel time resolution of 10 ns
  - NA62 GTK, 500mW, 300µm pixel, time resolution of 100 ps
    - Cycling clock and bias might decrease those numbers by a factor 50
- Data rate
  - Estimate of 2 Mbit/chip/ train for 1 hit/mm2/bunch
    - Data stream O.K with a local memory and readout between train (20 ms)

# Conclusions

- Goals of time tagging in tracking
  - Isolate individual vertices by timing analysis
    - Correlate time stamped hits with tracker hits
  - Generates multiple vertex candidates occurring in one train by associating hits to bunches
  - Correlate timing tracking information with calorimeter/muon
- Implementation of the timing layer
  - On a dedicated tracking barrel,
  - Integrated in the tracking layers
  - Integrated in the vertex
- Geometry , resolution
  - Pixel, Strip segmentation?
- Layout, size
  - Stave or module ?
- Timing performance
  - Do we need 0.5 ns time bunch identification, or a coarse timing information, 1 ns , 2ns
    - If the pixel/train occupation is low
    - Trade off with analogue power consumption and sensor speed
- Issues
  - Material budget
  - Power consumption
  - Sensor speed
- Parameters from CLIC machine
  - CLIC event versus CLIC background
    - Pixel/strip event occupancy producing tracks pointing vertices
    - Pairs producing noise hits or non pointing vertex tracks
- Do we want to ask to track timing a background rejection capability?