BPM Amplifier for CTF3 TBL: Status and Future Work

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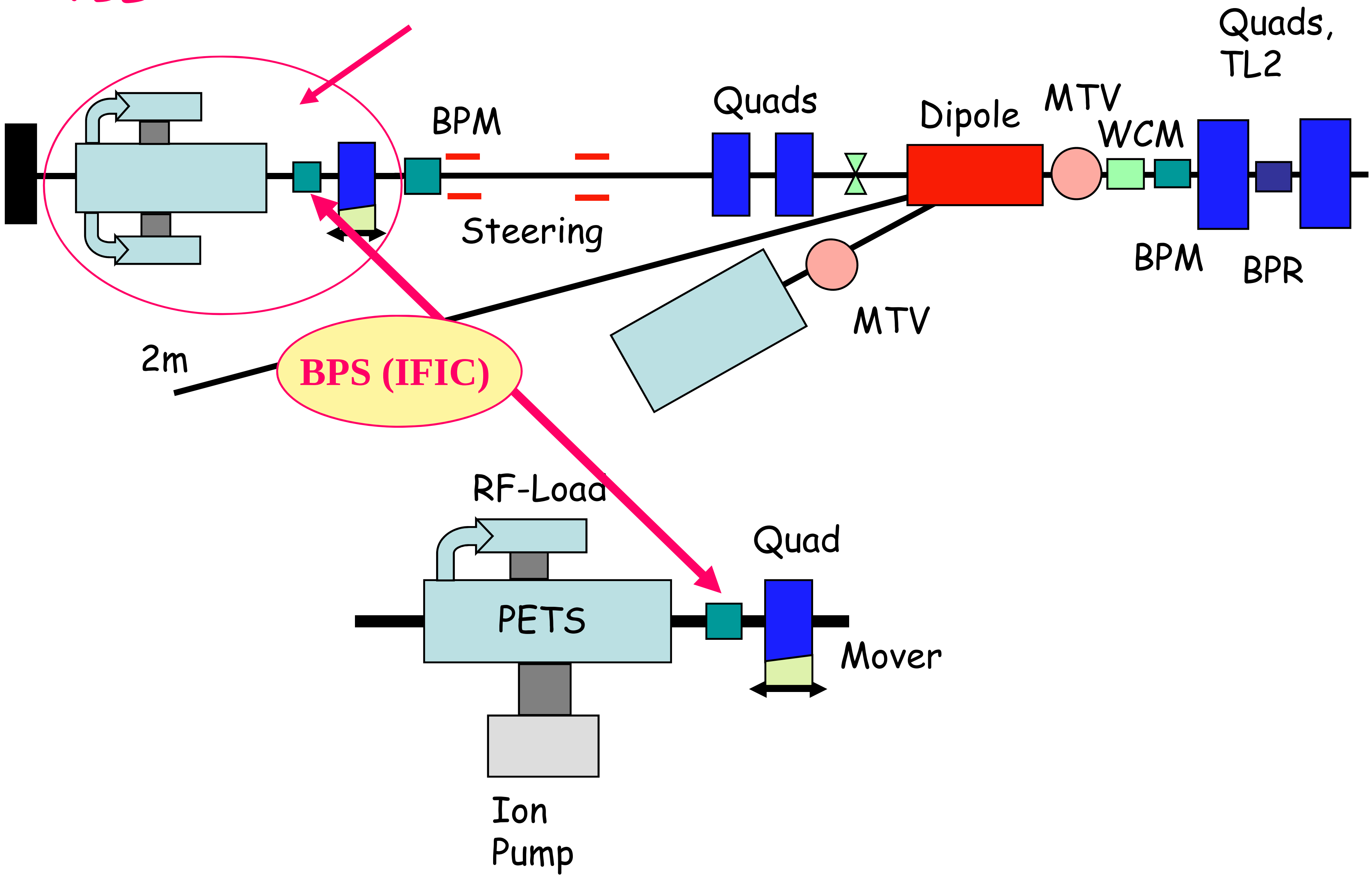
- CLIC WORKSHOP, 14-17 October 2008 -

TBL



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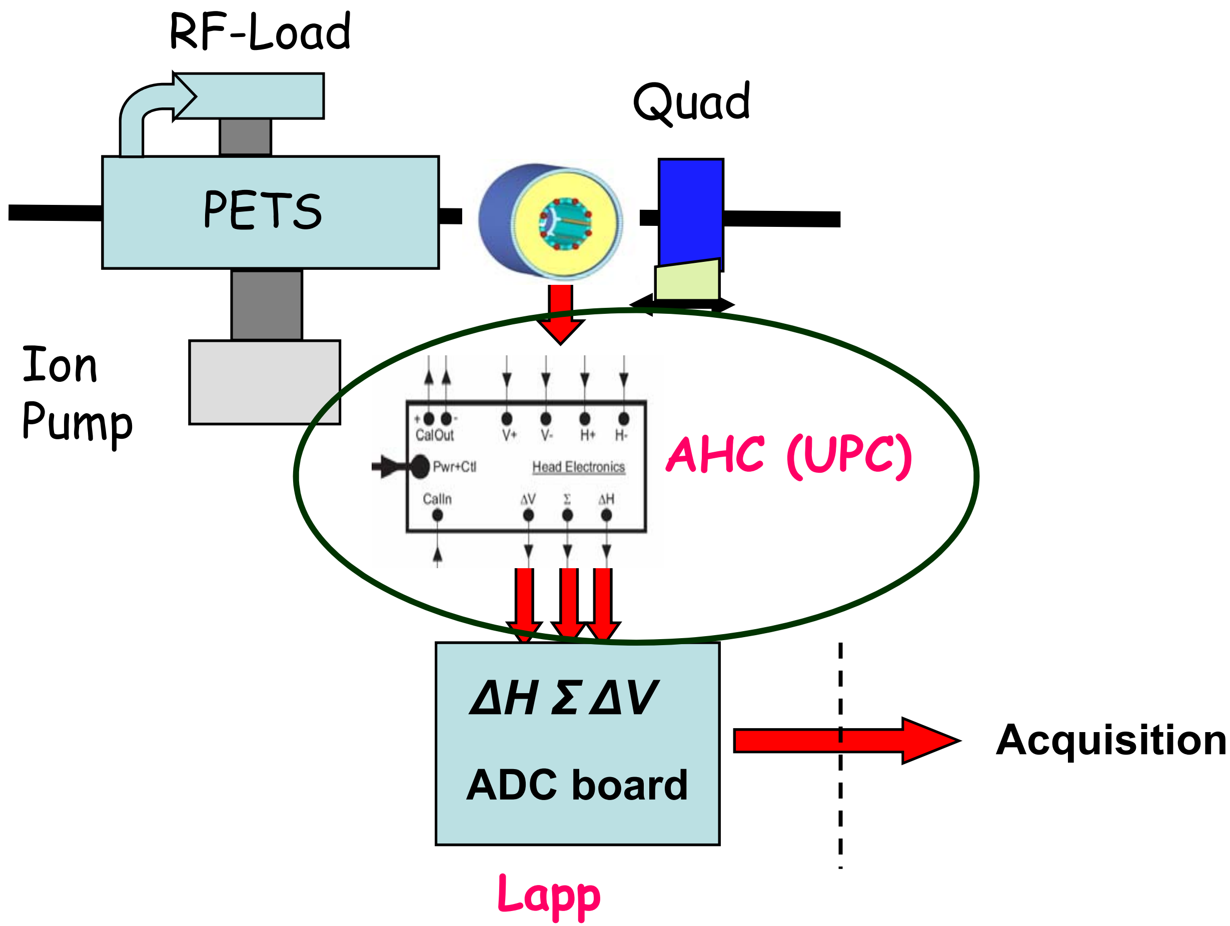

RF-Load
Quad
PETS
Ion
Pump
CalOut
V+
V-
H+
H-
Pwr+Ctl
Head Electronics
CalIn
ΔV
Σ
ΔH
AHC (UPC)
ΔH Σ ΔV
ADC board
Acquisition
Lapp

BPM+Amplifier specifications

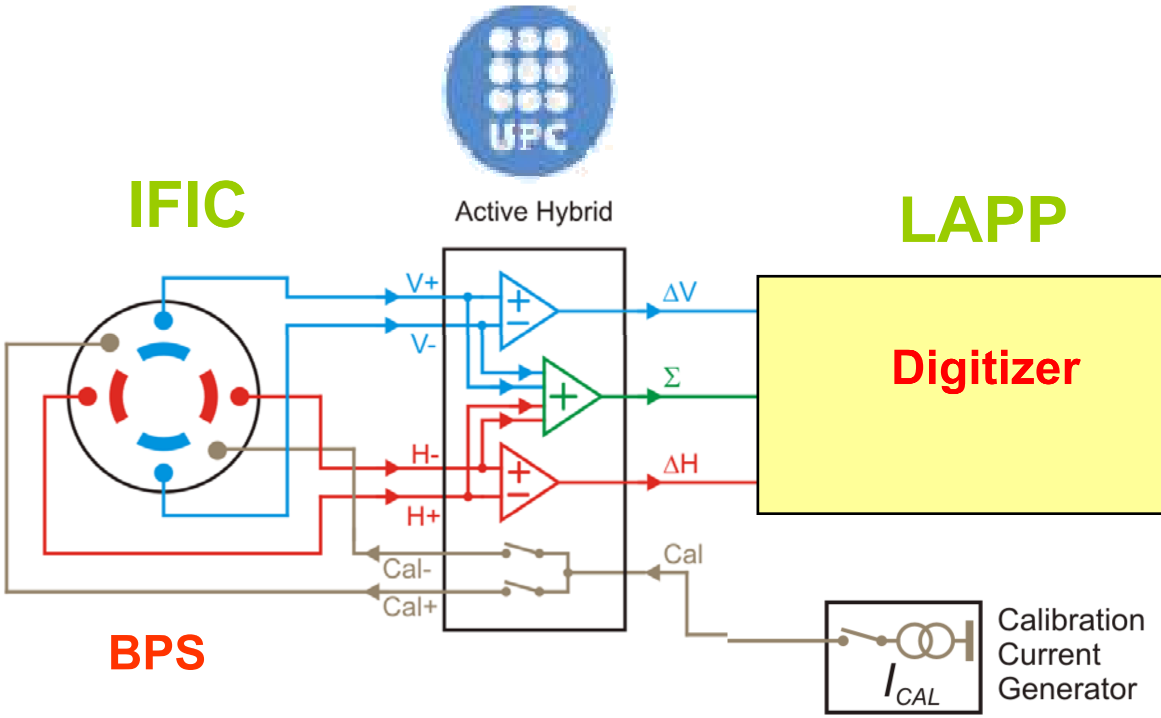
BPMs for the TBL: parameters	
BPM analog bandwidth (BPM with associated electronics)	10 kHz -100 MHz (200 MHz is highly desirable)
Beam position range of interest	+/-5 mm horizontal and vertical
Beam aperture diameter	24 mm
Overall mechanical length	< 100 mm
Number of BPM's in TBL	16
Resolution at maximum current	<5 mm
Overall precision	<50 mm

Typical radiation levels	<1000 Gray/year (or 100 Krads)

General scheme of the analog amplifier

- The signals (V+,V-, H+ and H-) captured by the BPM IPU are amplified and processed to the difference and sum signals which are then digitized.

- The amplifier is a part of head (front-end) electronics.



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Specifications of the interface between the analog amplifier and the BPM (developed by IFIC)

- 4 BPM outputs, one from each electrode: H+, H-, V+, V-
- 2 BPM calibration inputs
- Input and output impedances: 50 ohms
- Because of high signal levels from the BPM (due to the high current beam, around 30 A) the amplifier must include an input attenuator

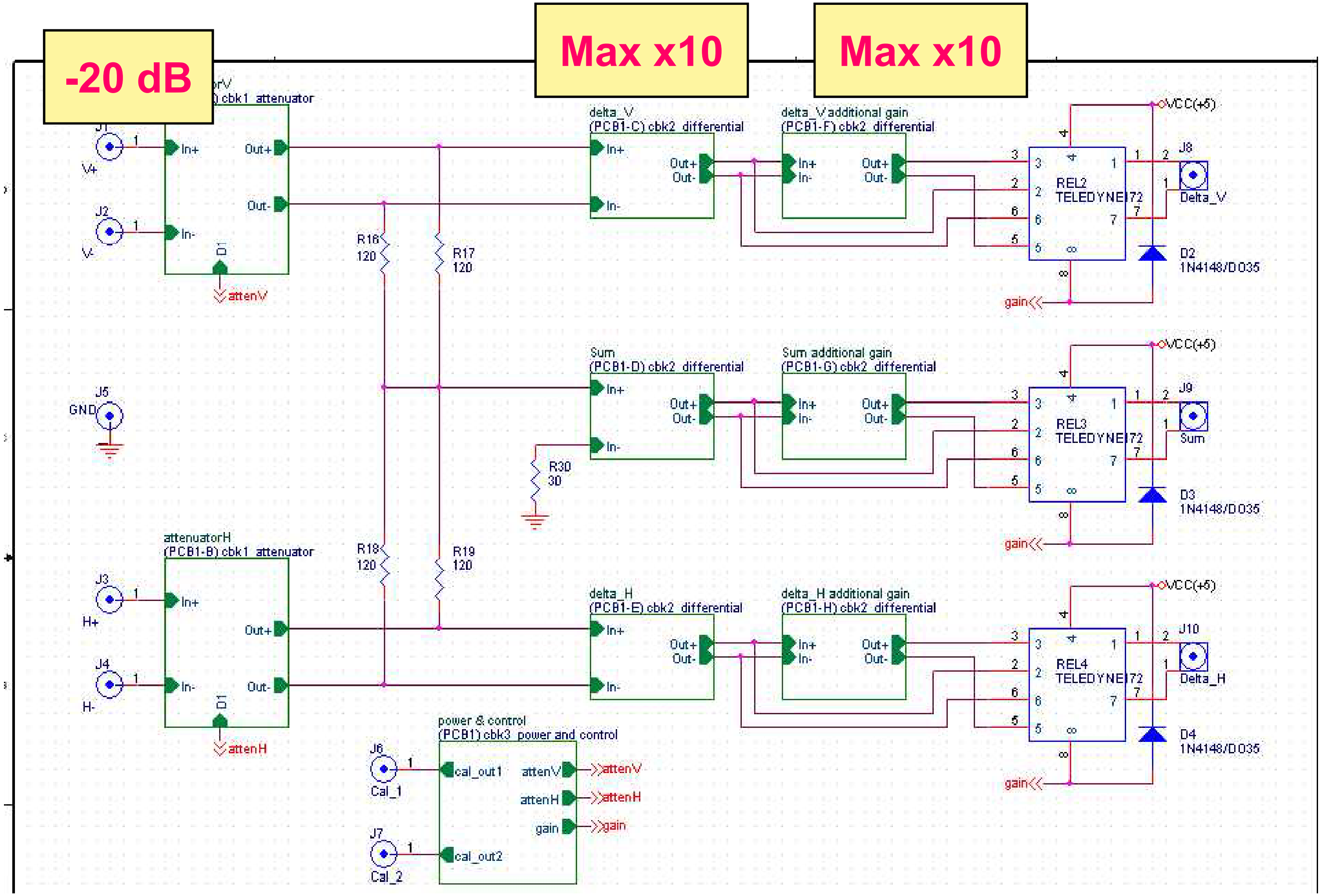
Specifications of the interface between the analog amplifier and the digitizer (developed by LAPP)

- The amplifier analog outputs must be differential and bipolars.
- Voltage levels: +-0,7V max
- Input and output impedances: 50 ohms
- As an output the amplifier provides 3 double (balanced) signals:
  - 1 sum signal (∑)
  - 2 difference signals (ΔH and ΔV, corresponding to the horizontal and vertical pair of electrodes).

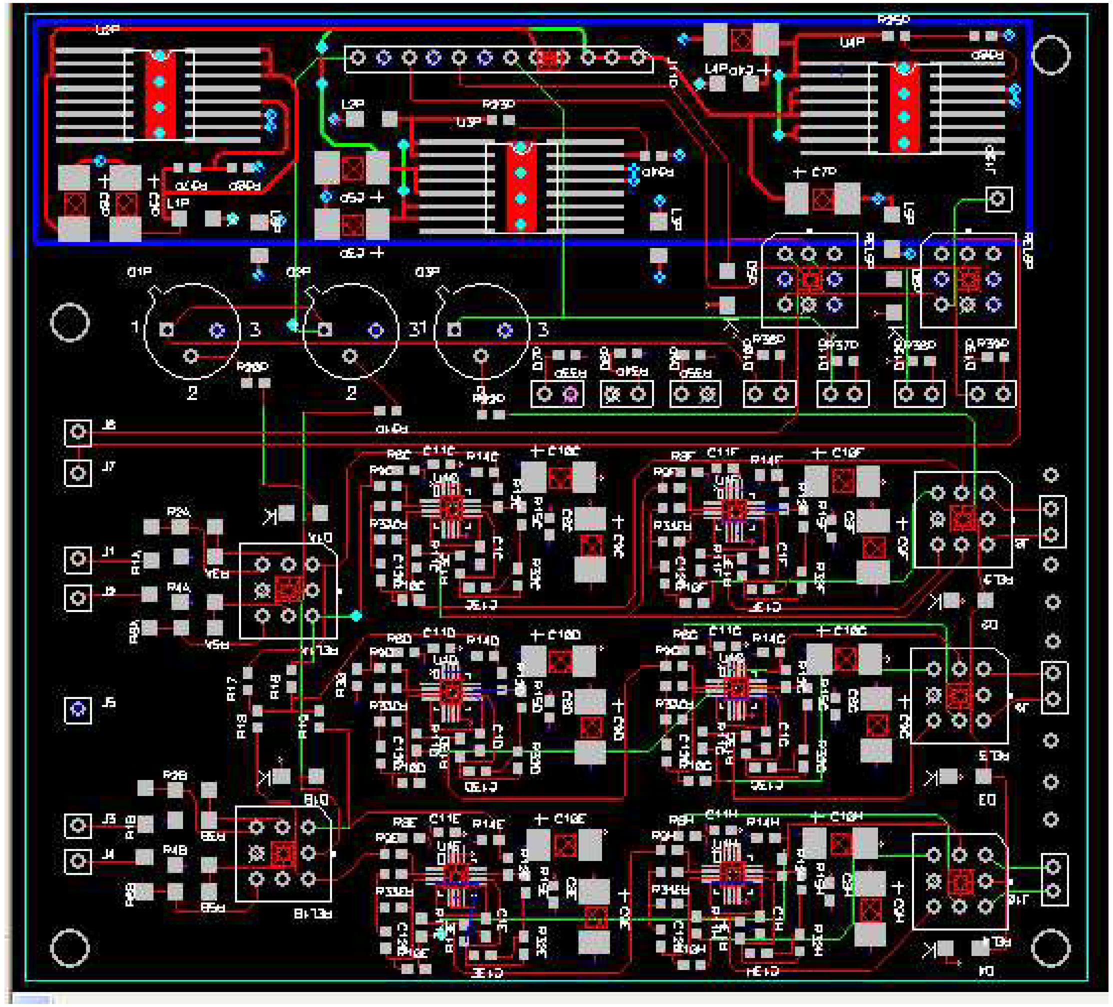
Amplifier design: the most critical components

- **Rad-hard** wideband IC amplifier: THS4508 (manufactured by TI and tested by up to 100 Krads)
- RHFL4913 (**rad-hard** positive regulator) (tested up to 100 Krads by the manufacturer, ST
- RHFL7913A (**rad-hard** negative regulator) (tested up to 100 Krads by the manufacturer, ST)

Schematics done according to the previous specifications (first prototype)



CAD design of the PCB (first prototype)



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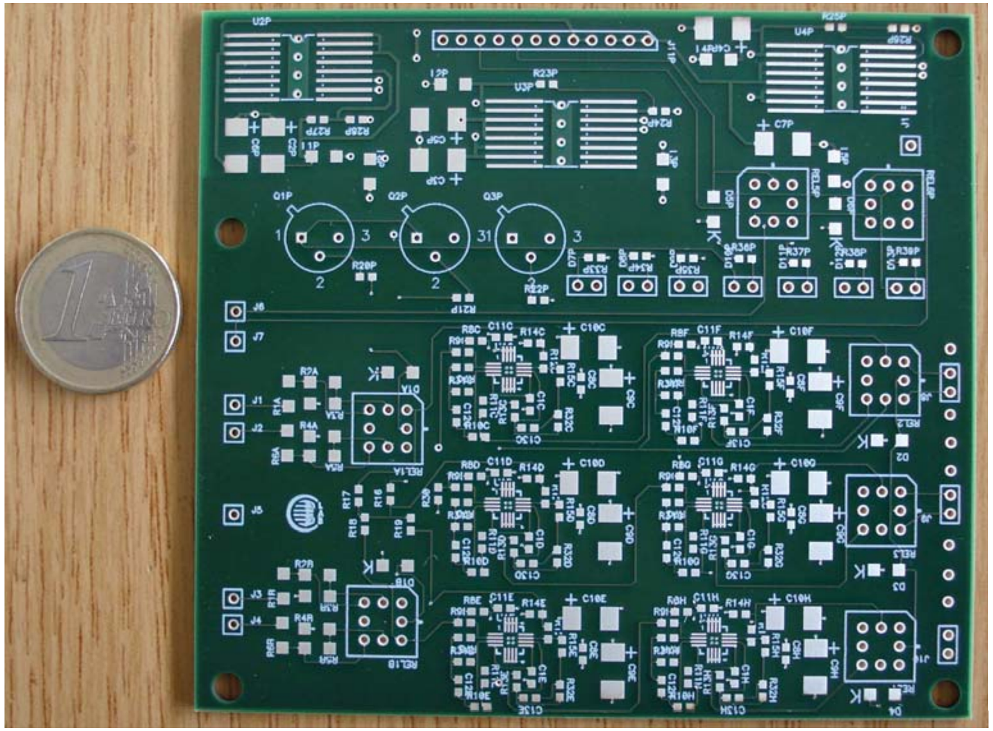
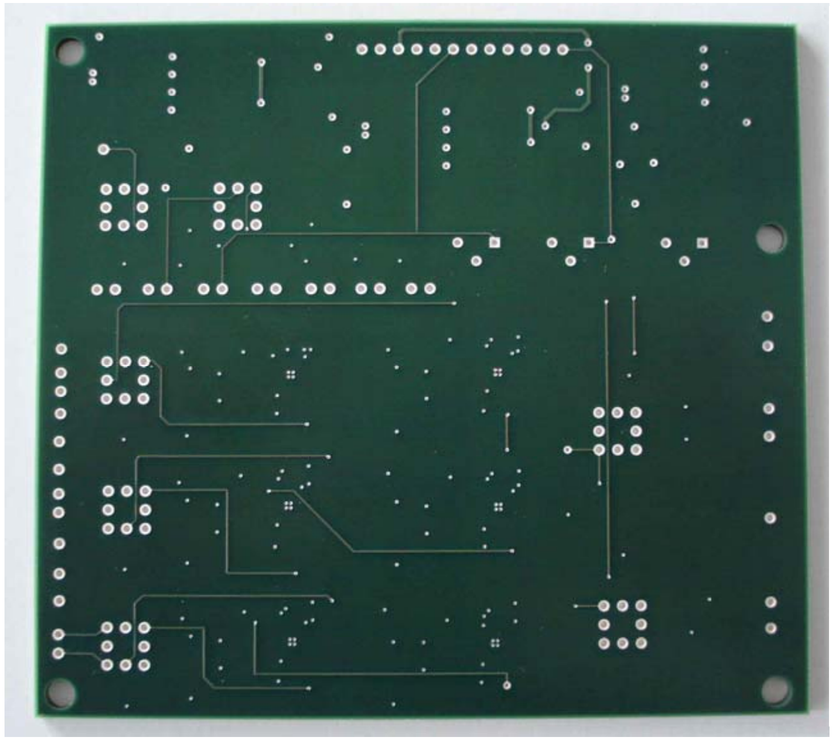
The 6-layers manufactured PCB (first prototype)



TOP



BOTTOM

First version of the amplifier completed

Power supply, control (gain, attenuation, calibration)

ΔH, ΔH, ∑

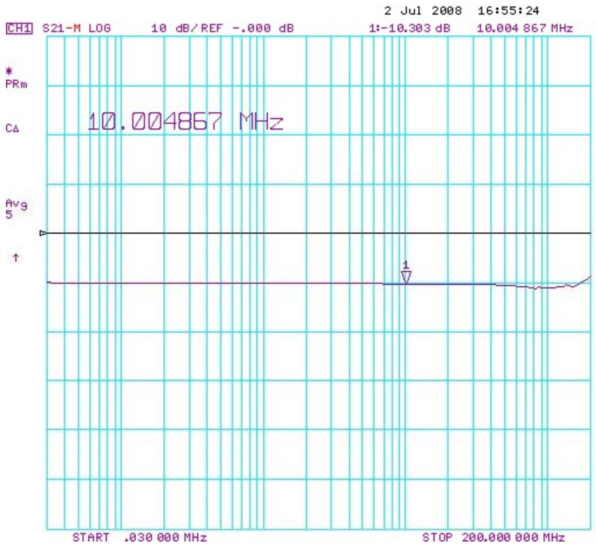
Cal

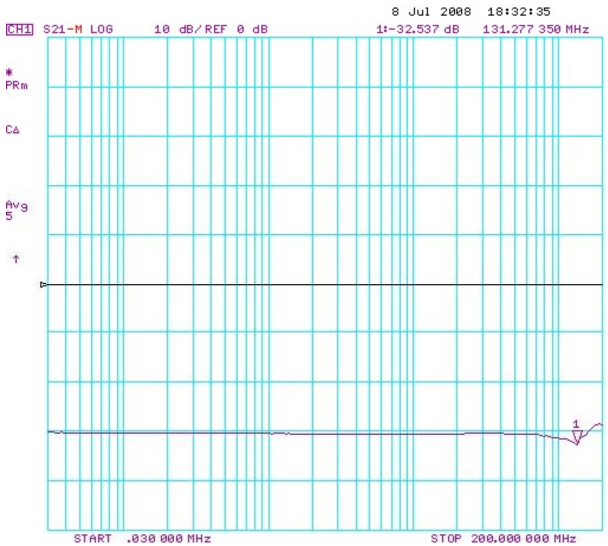
Cal ±

H+,H-,V+,V-

- It was necessary to modify the input attenuators to reduce the high level signals transmitted from the BPM:
  - At the center position and in a high beam current case (30 A) each electrode output is around 4 V (at 50 ohms input impedance)

Amplifier frequency response (test done at the UPC lab., June 2008)





- ΔV (differential) frequency response without 'droop' compensation (from 30 KHz to 200 MHz). The curve is quite flat: OK

- The correct Δ-channel response from 10 KHz to 30 KHz was verified by using an oscilloscope

Δ H results are similar

-∑-channel frequency response (from 30 KHz to 200 MHz). The curve is quit flat: OK

- The correct ∑ channel response from 10 KHz to 30 KHz was verified by using an oscilloscope

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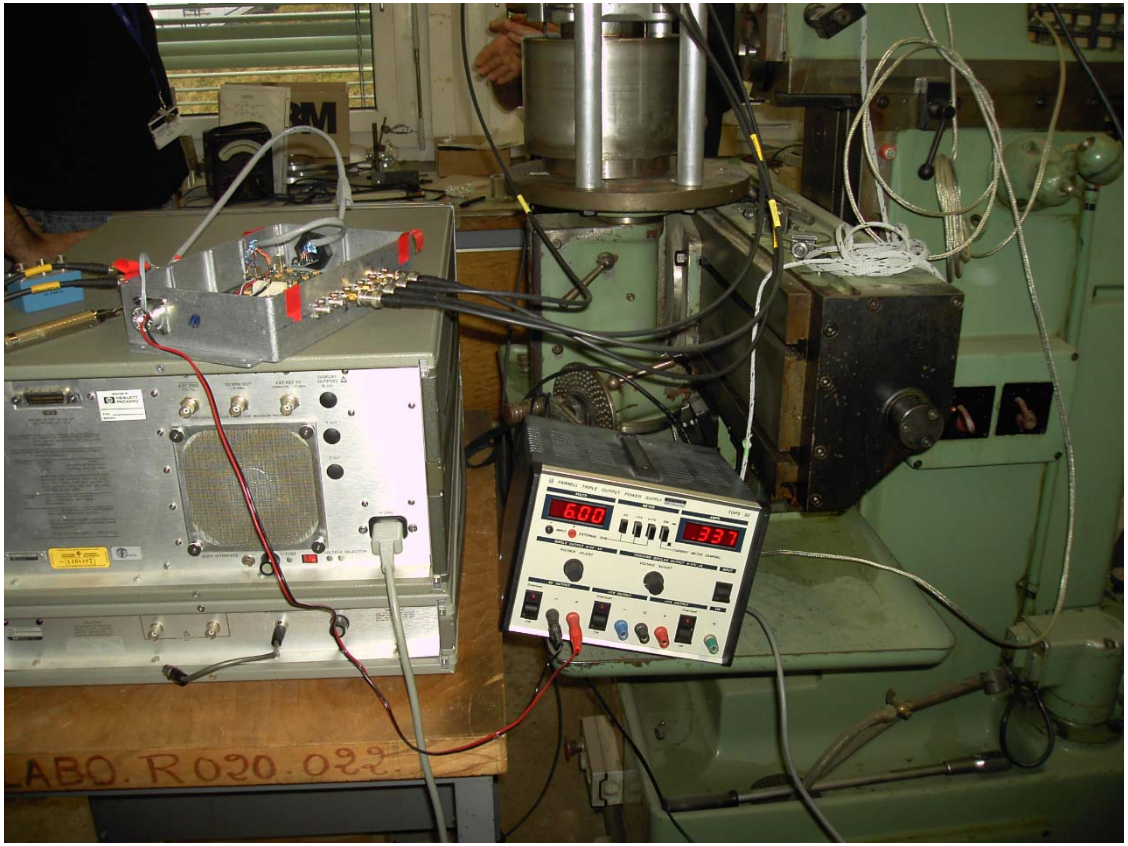
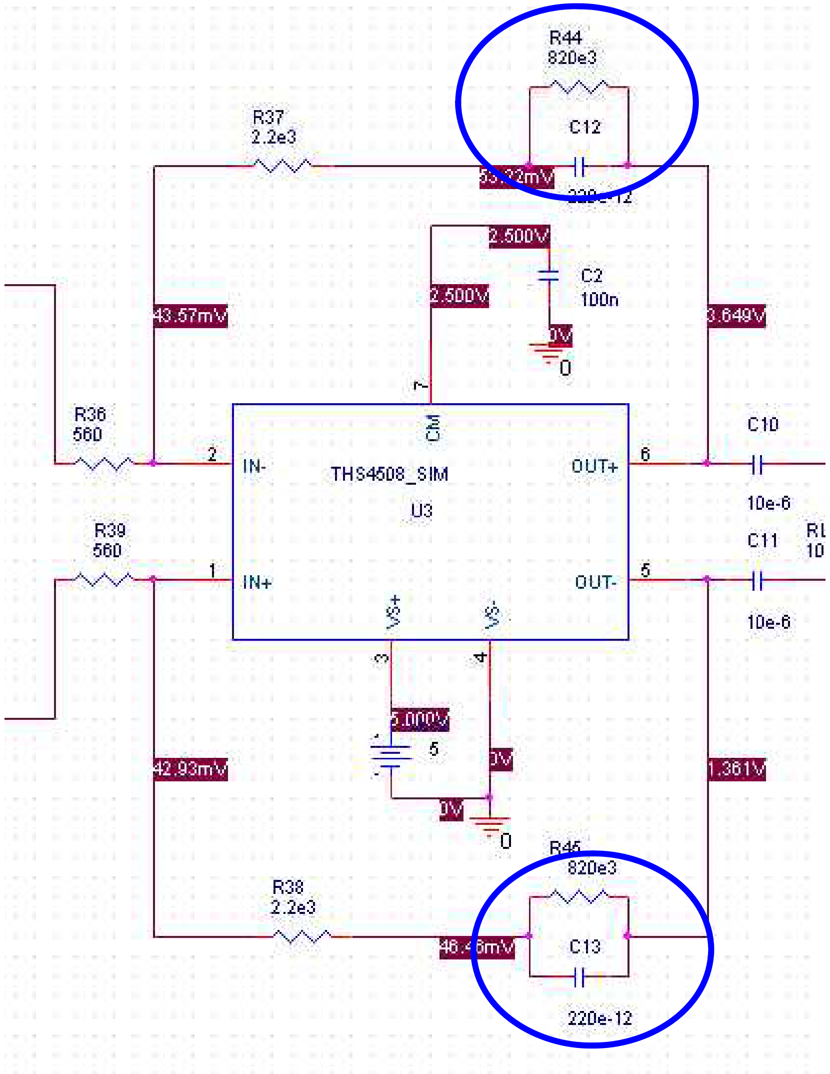


Wire test at the laboratory of Lars Soby (December, 2007)

A 'droop' compensation has been done



- **R-C network compensation:**

$$f_c = 74kHz$$

$$f_c = 10kHz$$

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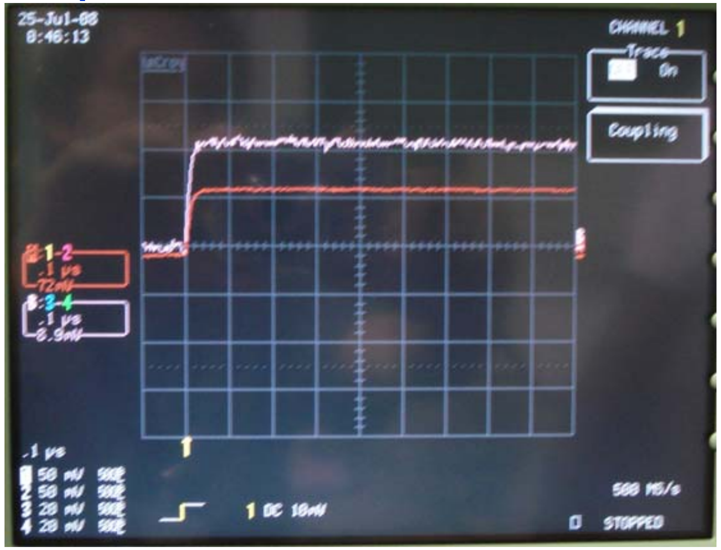
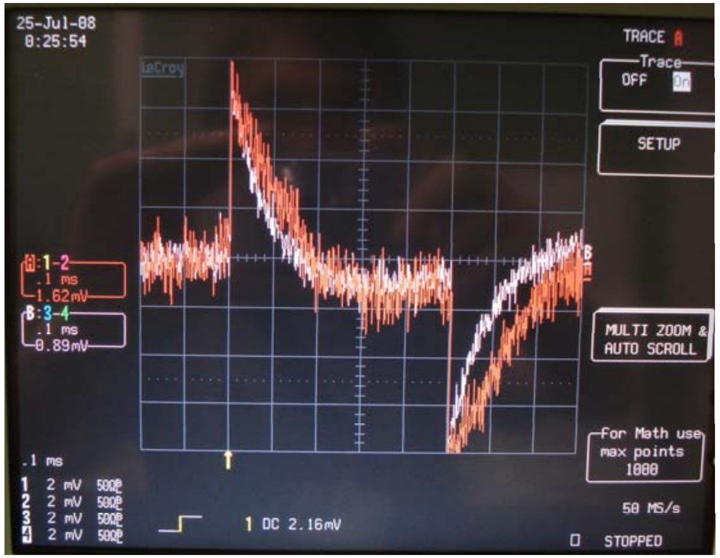
IFIC BPM + Amplifier: time responses after ‘droop’ compensation (wire and calibration tests done at the lab of Lars Soby, July 2008)



Δ and ∑ responses to a calibration excitation signal (the oscilloscope scale is of 100 ns/div)



Δ and ∑ responses to a ‘wire test’ excitation signal (the oscilloscope scale is of 10.000 ns/div)

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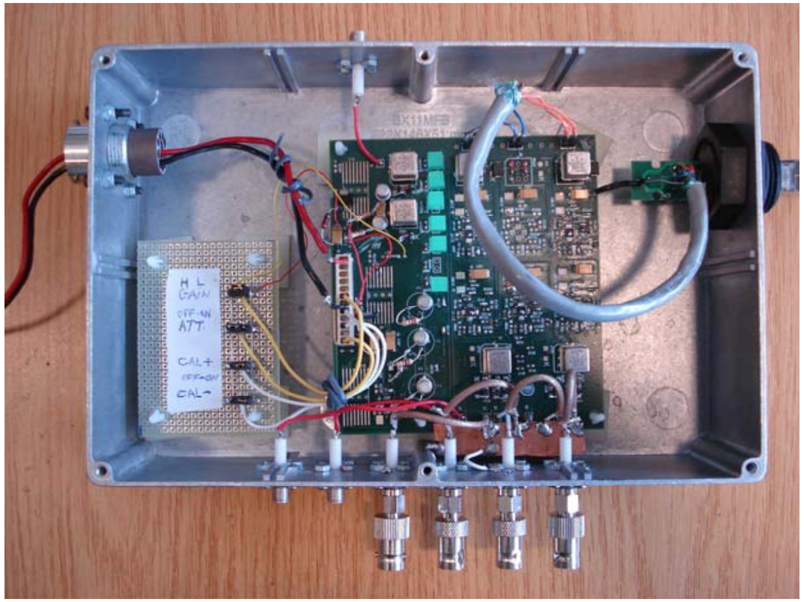
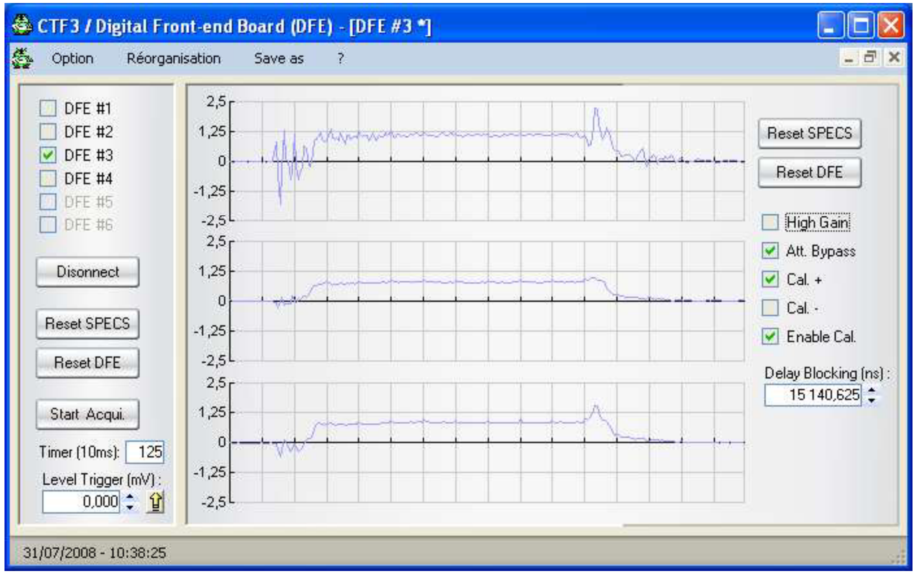
The first prototype of the BPS +amplifier has been installed at the TBL (July 2008)

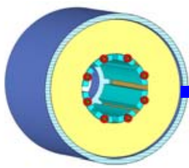


First amplifier prototype (July 2008)



First BPS + amplifier + digitizer test: time response to the calibration signal

(Courtesy V. Sebastien)

Calibration signal →  →  → Digitizer →

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UPC

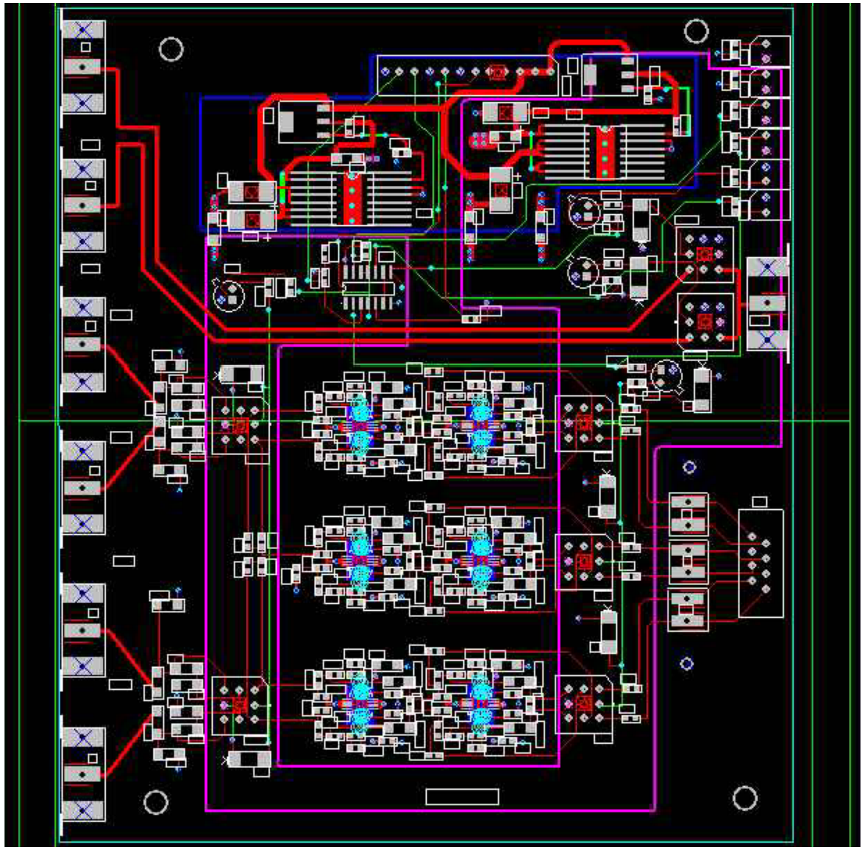
Conclusions after the tests of the 1st amplifier prototype

The results of the tests at the UPC lab and CERN show that the amplifier fulfills the main requirements:

- Each amplifier stage can achieve a gain up to 10.
- A bandwidth up to 170 MHz (above 100 MHz for sure) is achieved for each channel.
- The required voltage output levels are accomplished
- The amplifier electronic components are 100 Krad radiation tolerant.

Recent work:

- The schematic and PCB routing of the second prototype of the amplifier are completed
- The following improvements are incorporated:



✓The position of the connectors has been changed with the aim to eliminate the need of internal connecting cables

✓ The width of some tracks has been changed for a better 50 Ω matching

✓ Some delay differences between the channels has been compensated

✓Some imperfections and drawbacks of the first prototype design have been improved

Summary of the work done:

• First amplifier prototype designed and manufactured	2007
• First laboratory tests at the UPC	
• Wire test at CERN	December 2007
• Improvements and tests (wire and calibration signal) at CERN with BPS	June-July 2008
• Installation at TBL and calibration test at the TBL	July 2008

Ongoing and future work:

• First contact with the manufacturer of the PCB of the second amplifier prototype	October 2008
• Manufacturing and testing of the second amplifier prototype	November 2008
• Building and testing the total required series of the TBL amplifiers (16 units)	Starting from December 2008

Acknowledgements: Thanks to our collaborators from CERN: L. Soby, F. Guillot, S. Döbert et al., IFIC and Lapp groups.