LAPP BPM Read-out electronics in CTF3

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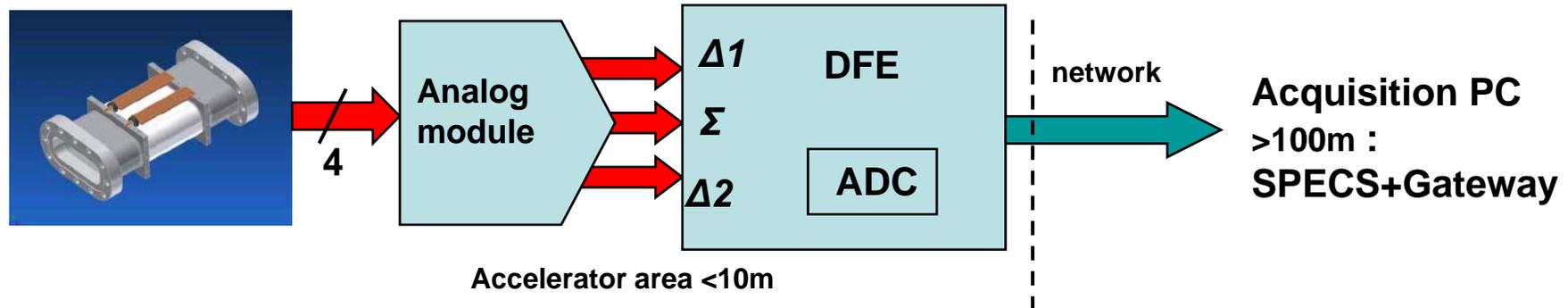
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WS CLIC 14-17/10/2008

BPM Acquisition architecture

Aim: *reduction of costs of long analog cables/ADC*
→ **Rad-hard acquisition electronics close to beam**.

Accelerator area <10m

Analog module: *Intensity & deviations processing BPI or BPM.*
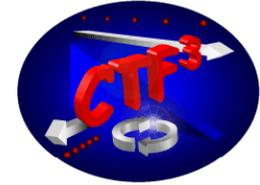
DFE board: - *digitalization* **3channels, 12 bits / 200MSps**.
   - *Feed-back for analog modules: gains, calibration and attenuations.*
   - *Daisy chain acquisition: 1 network cable per crate.*

Acquisition PC : *FESA-OASIS soft and specialist requirements feed-back.*

→ **Cost divided by a factor 3 comparing to a « far » acquisition.**

LAPP in CTF3

September 2005: creation of the CTF3 group in LAPP → R&D.

February 2006: analog + digital front-end solution proposed (Annecy bpm WS).

From November 2006 to summer 2008: production and installation of
47 analog modules and 31 DFE boards in 8 crates in TL2 and CLEX.

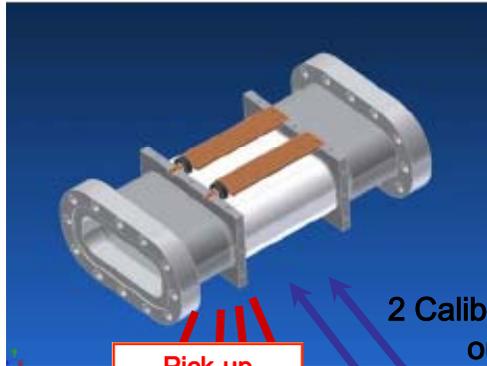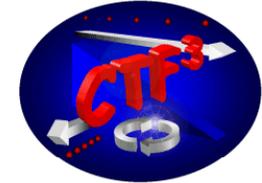→ All combination BPM&BPI pick-ups – Lapp&CERN analog modules
for the local acquisition.

Man power: ~2,5men/year full time since september 2005

→ analog, digital electronics and software,
one of whom funded by « Conseil général Haute Savoie ».

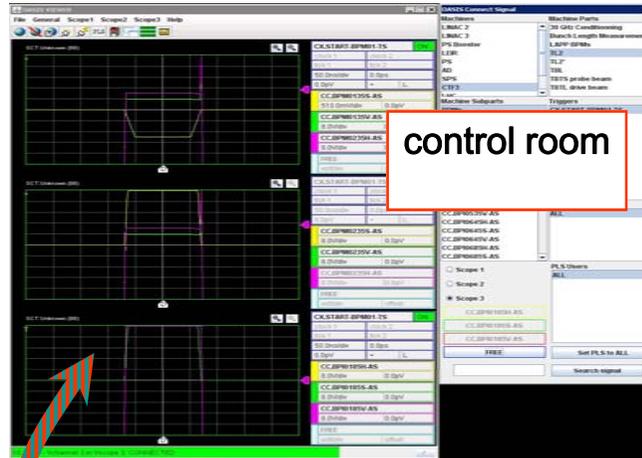**IN2P3 funding: ~100k€ from Sept. 2005 to end 2007.**

Still ~15 DFE to install for the BPS acquisition (2009): details to be discussed.
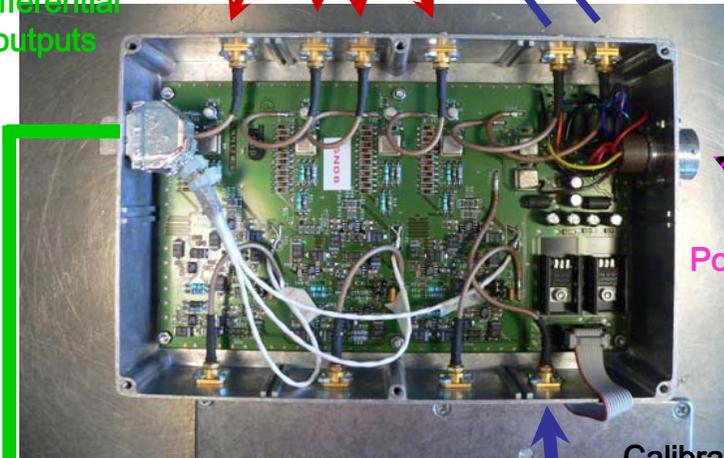
Read-out
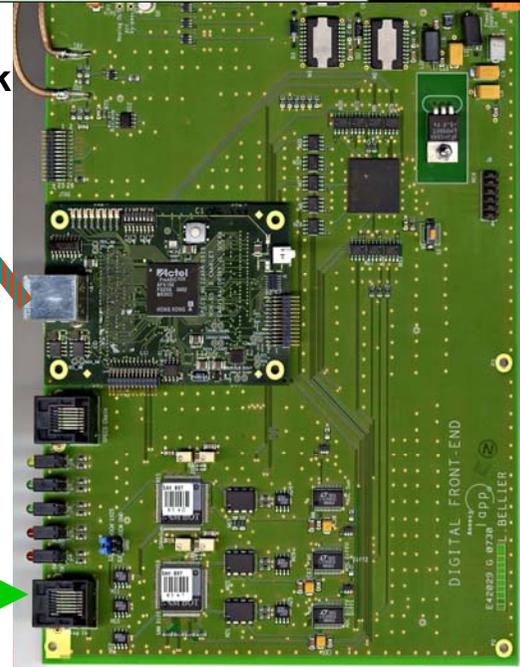

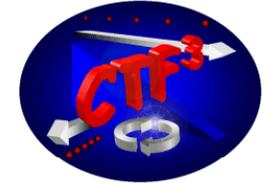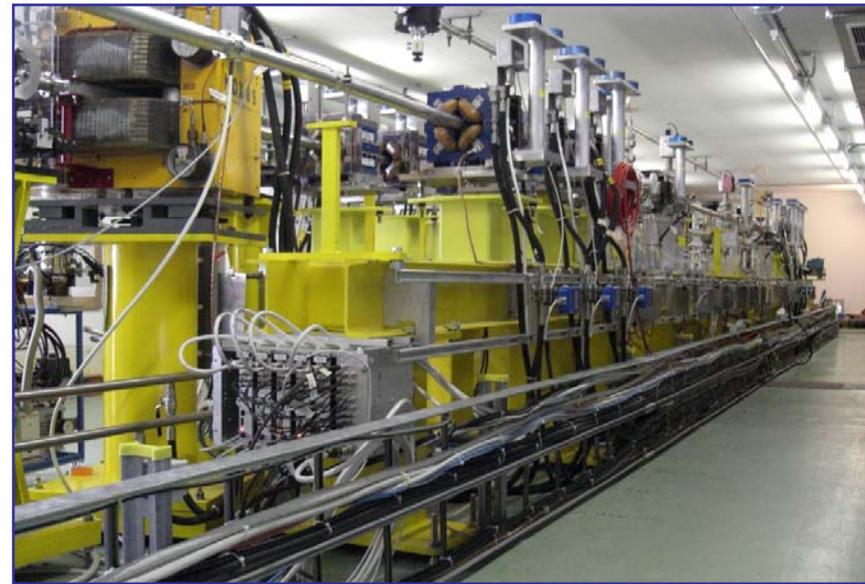Pick-up electrodes

2 Calibration pulse outputs

Differential outputs

control room

Network

Power supplies Controls
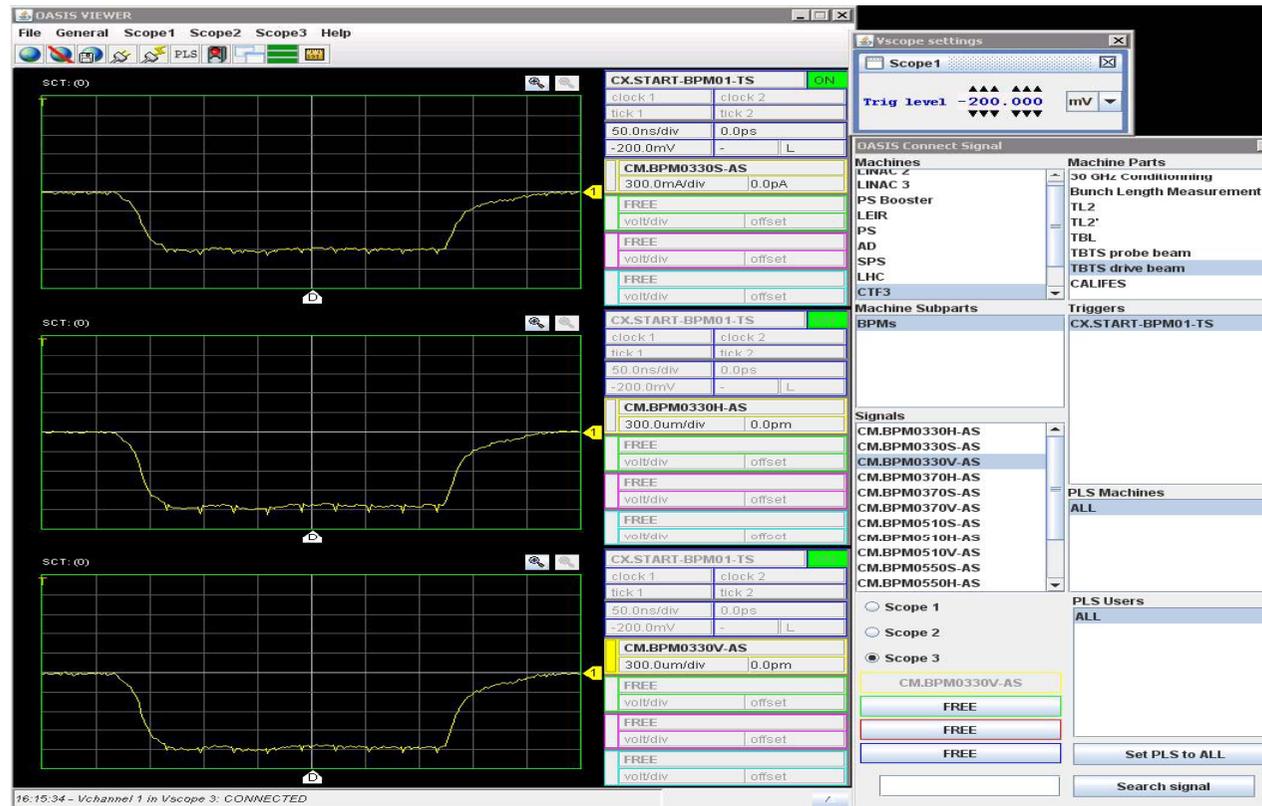
Calibration pulse input

DIGITAL FRONT-END

Uranus

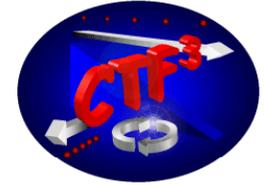# *Results*
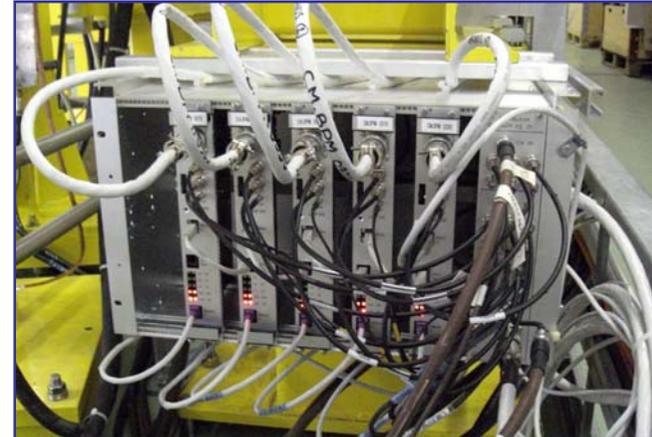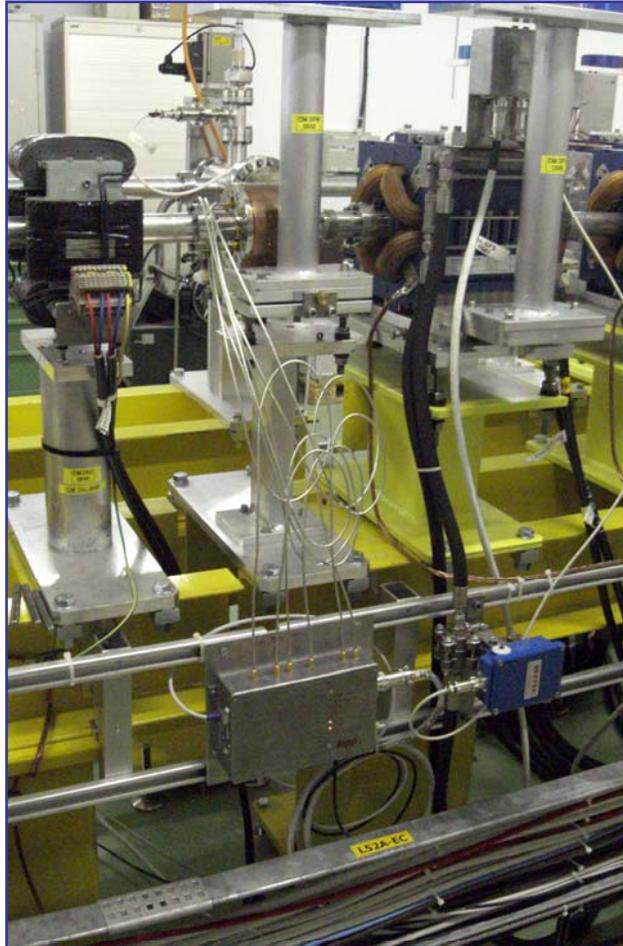
Debug during summer 2008:

several problems on sampling electronics and transmissions currently solved by soft.

Jitter solved by a trigger, sampling memory still to be calibrated.

Thanks to operation team feedback and patience!

16/10/2008   Sébastien VILALTE   6

Future : acquisition for CLIC

The logical evolution of this system is to be dedicated to a larger accelerator as CLIC:

Rare acces from surface, high number of channels, rad-hard, low-cost, low consumption…

Most important points to develop: **elimination of cables**

- **Power supplies:** *autonomous (220V sector, DC-DC converters…).*
- **Local calibration***.*
- **Network :** *flexible data collection, repetition crates…*
- **Acquisition architecture:** *faster ADC, direct bpm read-out, continuous sampling…*
- **FPGA processing:** *raw data, processed data…*
- **Radiations.**

Future : acquisition for CLIC

→ <u>**All-around accelerator standard acquisition**</u>.

A lot of specifications to be discussed with the collaboration:

- Input stages and input dynamic ranges.

- Informations to collect: definition of transfer rates.
    → possible switching between FPGA local process of position/intensity
    and raw data for precision.

- Definition of a standard crate for a module (n channels)

- Infrastructure possibilities to study (see Lars concrete shielded crate…)

- ETC…

Future : R&D in LAPP
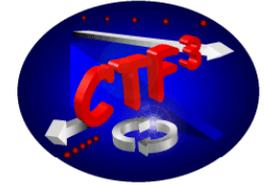
LAPP decided to get involved for a 2 years development:

~3 men/year and IN2P3 funding ~50k€/year.

New acquisition board:

    - 4 analog inputs with several input dynamic ranges, continuous 500Msps-12bits sampling.

    - 6GHz optical link for data, timing: no more cables, no EMC problems…

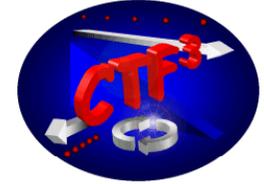   *- A Clock-management architecture to get free from timing problems.*

Board for local power supplies/calibrations facility:

study of a 220V sector power supplied crate & local calibration.

    → Problem of radiations!

Future : R&D in LAPP

- *Development about 1 year from September 2008: architecture and critical components chosen (ADC, timing, transmission) .*

- *The two boards will be compatible with the existing crates to be tested and debugged in the CTF3 (6 months more) with no interference with the actual system.*

- *The optical reception board (PCI) already existing.*

- *Radiation tests foreseen.*

- *Remarks and ideas are welcome...*

With the development of a multiplexer collection board, it could replace the current CTF3 acquisition …