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Evaluating the power efficiency and performance of multi-core platforms using HEP workloads

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As Moore's Law drives the silicon industry towards higher transistor counts, processor designs are becoming more and more complex. The area of development includes core count, execution ports, vector units, uncore architecture and finally instruction sets. This increasing complexity leads us to a place where access to the shared memory is the major limiting factor, making feeding the cores with data a real challenge. On the other hand, the significant focus on power efficiency paves the way for power-aware computing and less complex architectures to data centers. In this paper we try to examine these trends and present results of our experiments with "Haswell-EP" processor family and highly scalable HEP workloads.

Primary author: Mr SZOSTEK, Pawel (CERN)

Co-author: Dr INNOCENTE, Vincenzo (CERN)

Presenter: Mr SZOSTEK, Pawel (CERN)

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