

# 21st International Conference on Computing in High Energy and Nuclear Physics (CHEP2015)



Contribution ID: 247

Type: **oral presentation**

## Performance benchmark of LHCb code on state-of-the-art x86 architectures

*Tuesday, 14 April 2015 16:30 (15 minutes)*

For Run 2 of the LHC, LHCb is exchanging a significant part of its event filter farm with new compute nodes. For the evaluation of the best performing solution, we have developed a method to convert our high level trigger application into a stand-alone, bootable benchmark image. With additional instrumentation we turned it into a self-optimising benchmark which explores techniques such as late forking, NUMA balancing and optimal number of threads, i.e. it automatically optimises box-level performance. We have run this procedure on a wide range of Haswell-E CPUs and numerous other architectures from both Intel and AMD, including also the latest Intel micro-blade servers. We present results in terms of performance, power consumption, overheads and relative cost.

**Primary author:** SCHWEMMER, Rainer (CERN)

**Co-authors:** CAMPORA PEREZ, Daniel Hugo (CERN); NEUFELD, Niko (CERN)

**Presenter:** SCHWEMMER, Rainer (CERN)

**Session Classification:** Track 8 Session

**Track Classification:** Track8: Performance increase and optimization exploiting hardware features