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Investigation of High-Level Synthesis tools' applicability to data acquisition systems design based on the CMS ECAL Data Concentrator Card example

High-Level Synthesis (HLS) for Field-Programmable Logic Array (FPGA) programming is becoming a practical alternative to well-established VHDL and Verilog languages. This paper describes a case study in the use of HLS tools to design an FPGA-based data acquisition systems (DAQ). We will present the implementation of the CERN CMS detector ECAL Data Concentrator Card (DCC) functionality in HLS and lessons learned from using HLS design flow.

The DCC functionality and a definition of the initial system-level performance requirements (latency, bandwidth, and throughput) will be presented . We will describe how its packet processing control-centric algorithm was implemented with VHDL and Verilog languages. We will then show how the HLS flow could speed up design-space exploration by providing loose coupling between function's interface design and function's algorithm implementation.

We conclude with results of real-life hardware tests performed with the HLS flow-generated design with a DCC Tester system.

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