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# Development and test of the DAQ system for a Micromegas prototype installed in the ATLAS experiment

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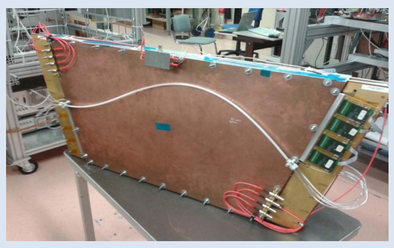
A Micromegas (MM) quadruplet prototype with an active area of 0.5 m² has been built at CERN and is going to be tested in the ATLAS cavern environment during the LHC RUN-II period 2015-2017. It adopts the general design foreseen for the upgrade of the innermost forward muon tracking systems (Small Wheels) of the ATLAS detector in 2018-2019. The integration of this prototype into the ATLAS data acquisition system using custom Scalable Readout System (SRS) ATCA equipment is presented.

## The Micromegas Small Wheel (MMSW) prototype

A Micromegas prototype detector with an active area of 0.5m² per layer has been built, which follows the general design foreseen for the upgrade of the ATLAS Small Wheels (New Small Wheel (NSW) project). It consists of a quadruplet structure with four active layers of 1024 readout strips each, and a strip pitch of 415 µm.
The chosen detector technology is the so called resistive strip Micromegas, that uses an additional layer of high-resistivity carbon strips on top of the copper readout strips to improve spark-tolerance. These two layers of strips are separated by one 50 µm layer of Kapton® Foil.
Two of these detector layers provide horizontal strips for a position resolution better than 100 µm in the precision coordinate of the spectrometer. The other two detector layers carry stereo-strips that are rotated by +- 1.5°, providing a resolution better than 2.5 mm in the second coordinate.

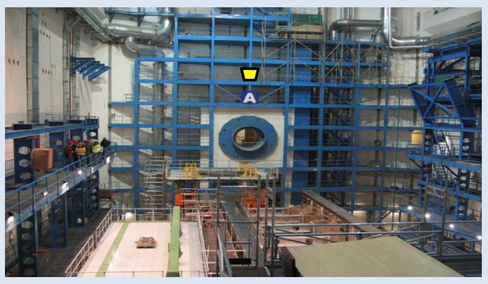


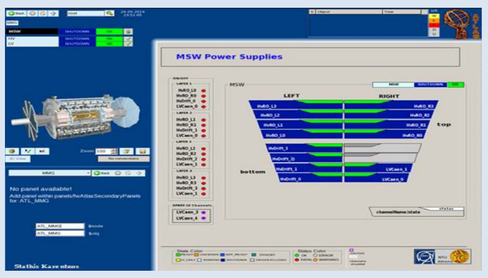
The Micromegas can not only deliver precision tracking information, but also serve as triggering system.
High Voltage distributors for the resistive strips and drift cathode are located on the side of the chamber.
For the moment APV25[a] chips on hybrid boards are used to read out the detector. These are connected by means of mezzanine cards, allowing the later replacement with front-end boards based on the VMM readout chip development for the NSW detectors.

## MMSW installation in ATLAS

The MMSW prototype chamber will be installed within the ATLAS environment, close to the cavern wall. Its purpose is to study the behavior of a NSW Micromegas quadruplet in the real ATLAS environment. This contains the recording of muon tracks, to directly compare these with the measurements of the current ATLAS muon detector system on an event-by-event basis. Another goal is the verification of the new VMM frontend triggering capability, and the support of the development of simulations and reconstruction algorithms.

It‘s location is foreseen within the scaffolding structure at the ATLAS cavern wall, recording particles from the interaction point at 20° with respect to the chamber surface. This is a good angle for Micro-TPC[b] angular tracking studies.
During the next Christmas Shutdown, the chamber is foreseen to be relocated on to the present small wheels.

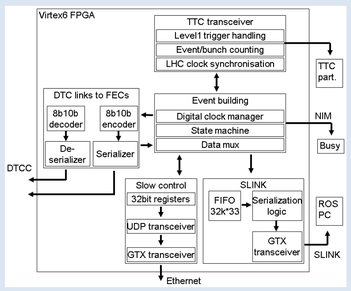


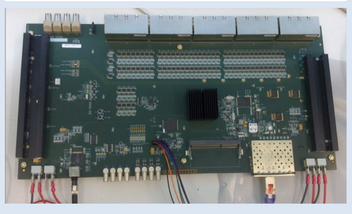



## Scalable Readout Unit (SRU) as ATLAS Read Out Driver (ROD)

The Scalable Readout Unit (SRU) is a custom FPGA board from the Scalable Readout System (SRS) electronics series developed within the RD51 Collaboration. The board hosts a Xilinx Virtex6 FPGA, as well as all necessary circuitry to interface it to the ATLAS Trigger and Data Acquisition (TDAQ) infrastructure. These include:

- The TTCrx ASIC, used to receive triggers and asynchronous data from the ATLAS trigger network, as well as the LHC bunch crossing clock for synchronous operation
- LEMO00 plugs for miscellaneous purposes like connection to the ATLAS BUSY tree structure
- SFP+ plugs for network connectivity and data connection to the ATLAS Read Out System (ROS) via emulated SLINK
- 40 RJ45 plugs with LVDS signal pairs for communication and readout of the frontend electronics



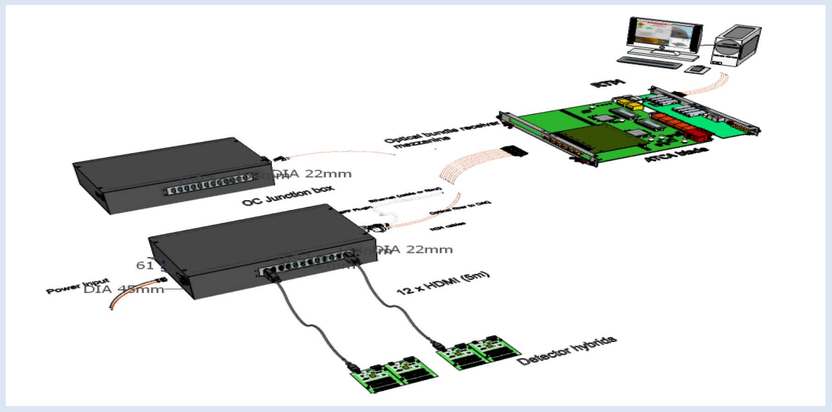



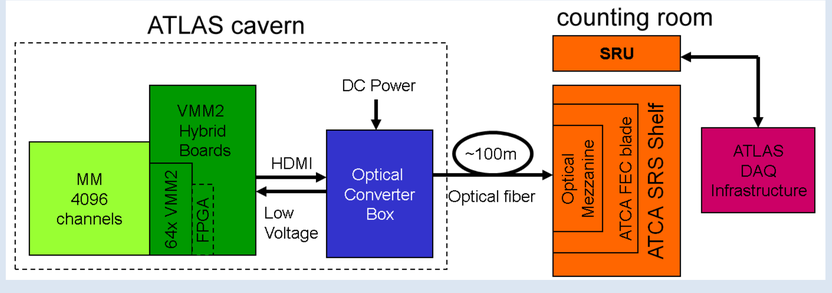
## Micromegas Prototype readout concept

Since the final and dedicated NSW electronics is currently under development, the Scalable Readout System (SRS) successfully provides the readout of the prototype detectors. The SRS system foresees several custom modules, that can be utilized to integrate the MMSW Micromegas prototype into the ATLAS Trigger and Data Acquisition (TDAQ) infrastructure.
Apart from the Scalable Readout Unit (SRU) and the ATCA FEC blades these include an Optical Converter (OC) box, communicating with the FEC blades via fiber optics. An OC box itself is able to represent the functionality of a FEC card, allowing the installation of different mezzanine boards, depending on the frontend electronics in use.
This allows to place the back-end electronics in a remote area (counting room), while the detector operates in a harsh environment (ATLAS cavern). The OC box contains several mechanisms to make it tolerant to Single Event Upsets (SEU) and other radiation-induced errors. It also contains radiation-hard DC/DC converters to power the frontend chips from an unregulated DC source. The OC box is currently in development stage.

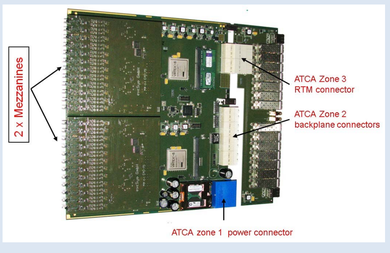
The modular concept of the SRS system allows to utilize different frontend electronics and readout chips with the same backend hardware.

For Micromegas detectors the APV25 frontend chip has been used successfully in the past, but the NSW detectors will be equipped with VMM frontend electronics, custom designed for this purpose. The SRS system has already been operated together with preliminary pre-series versions of these chips, that are also the natural choice for the MMSW chamber.




## SRS ATCA modules



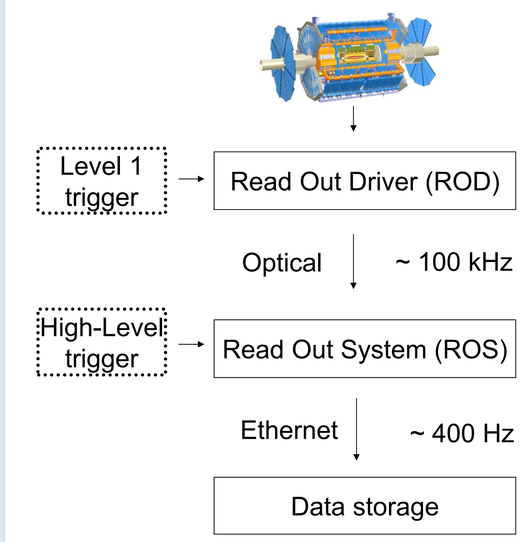

The ATCA Front End Concentrator (FEC) blades are used to distribute triggers and clock to up to 48 readout chips, as well as to gather their respective data, and perform additional computing like zero-suppression, etc.
FEC cards in non-ATCA standard are well established and widely used – the newly developed ATCA variant is currently in the test stage.

The ATCA FEC blade mother board houses two mezzanine boards, that offer A/D conversion circuitry, wired or optical connectivity and more – depending on the choice of mezzanine card and frontend chip. For example when using APV25 chips, one FEC blade with 24 HDMI connectors is able to read out more than 6000 detector channels.

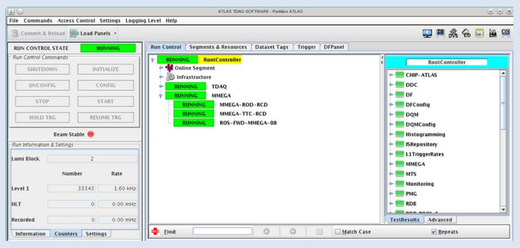
## Results of Micromegas integration into the ATLAS DAQ chain

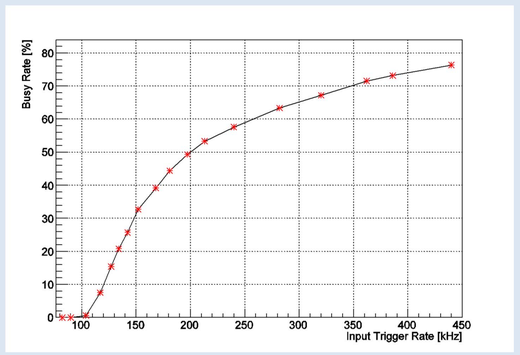
The ATLAS data acquisition system in RUN II (2015 – 2018) uses a two-staged triggering mechanism, to reduce the initial collision rate of 40 MHz down to around 400 Hz for final storage and analysis.
This first level trigger is performed in hardware with fixed latency, selecting events for further consideration at up to 100 kHz.
The Read Out Drivers (ROD) of the subsystems provide these events to the Read Out System (ROS) via optical SLINK.
The High level trigger algorithms in the next step are implemented in software and running on computer farms, selecting events based on regions of interest and partial event reconstruction.

The ATLAS events at the different stages are organized in 32bit words, including headers and trailers for unique identification.




Although the complete readout chain for the MMSW chamber is not yet available, the Scalable Readout Unit as Read Out Driver has already been included in the ATLAS infrastructure.
The configuration of the system is driven directly from the ATLAS Run Control System. By using the ATLAS TDAQ Software, a dedicated Micromegas segment has been implemented within the main ATLAS TDAQ partition, including the busy handling system.
It fully complies with the demands on data format, processing rate and software compatibility.
During several weeks of ATLAS cosmics data taking the system was successfully included in the infrastructure without errors.
Especially in its current configuration the modern FPGA architecture allows operation at very high event rates.
The average busy fraction of the Micromegas ROD is below 1% at 100 kHz level 1 trigger rate, being limited only by the following processing stages in the data acquisition chain.



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[a] M. Raymond et al, *The CMS Tracker APV5µm CMOS Readout Chip, Nuclear Science Symposium Conference Record 2 (2999) 9/113 – 9/118*
[b] *ATLAS New Small Wheel Technical Design Report: CERN-LHCC-2013-006*