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The Electronics, Online Trigger System and Data Acquisition System of the J-PARC E16 Experiment

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1. Introduction

The J-PARC E16 experiment aims to investigate the chiral symmetry restoration in cold nuclear matter and the origin of the hadron mass through the systematic study of the mass modification of vector mesons.
In the experiment,
e^+e^- decay of slowly-moving ϕ mesons in the normal nuclear matter density are intensively studied using several nuclear targets (H, C, Cu and Pb).
The dependence of the modification on the nuclear size and the meson momentum will be measured for the first time.

2. Experiment

The experiment will be performed in 2016 at the high-momentum beam line of the J-PARC hadron experimental facility,
where a 30-GeV proton beam with a high intensity of 1×10^{10} per pulse (2-second spill per 6-second cycle) is delivered to experimental targets.
Since the material budget around the targets is sensitive to the e^+e^- measurement,
thin detector systems are under construction.
The targets are surrounded by GEM Trackers (GTR) with three tracking planes to achieve the good resolution of 100 μm in the high rate environment of 5 kHz/mm^2.
The electrons (positrons) are identified by two types of counters.
One is the Hadron Blind Detector (HBD), which is a threshold type gas Cherenkov detector using GEM,
and the other is the Lead-glass EM calorimeter (LG).

3. Trigger electronics

The first level trigger is decided by the three fold coincidence of ∼620-ch from the GTR, ∼940-ch from the HBD and ∼1000-ch from the LG.
Cathode foils which face to the read out strips of the most outside GTR and pads of the HBD are divided into trigger segments.
A pulse fired on the GEM cathode foils are fed into an amplifier-shaper-discriminator (ASD) ASIC, which has been developed by our group in cooperation with
Open-It[1].
The LG signals are discriminated by a commercial fast comparator.
In order to gather the trigger primitives, which are sent from the GTR, HBD and LG in parallel LVDS signals, a trigger merger board (TRG-MRG) has been developed.
The TRG-MRG produces time stamps of the trigger primitives with a resolution of less than 4 nsec by using a Xilinx Kintex-7 FPGA.
The time stamps are serialized by the FPGA and transmitted to a global trigger decision module via optical fibers at each link rate of 5 Gbps or more.
The global trigger module utilizes a Belle-II Universal Trigger Board 3.
The first level trigger as well as a global clock of ∼125 MHz is distributed by Belle-II FTSW boards via Category-7 LAN cables to the front-end-modules described bellow.

4. Readout electronics

The numbers of readout channels amount to ∼56k, ∼36k and ∼1k for the GTR, HBD and LG, respectively.
In the current design, waveforms from all of the readout channels will be recorded by using analog memory ASICs to obtain timing and charge deposit information and to distinguish pulse pile-up in the high rate environment for the offline analysis.
The waveform from the GTR and HBD are stored with a 25 nsec cycle in APV25s1[2] chips and then transferred to the Scalable Readout System, which has been developed by the CERN RD51 Collaboration[3] (an R&D collaboration for MGPDs).
The LGs are read out by custom made boards, which employ DRS4[4] chips to record the pulses at 1 GHz.
Those modules digitize the waveforms and perform the zero suppression at online.
The data are collected by the DAQ-Middleware[5] using gigabit Ethernet and 10G Ethernet links.
The expected data rate is 660 MB/spill with the event rate of 2k/spill after zero suppression.

5. Summary

This is an overview talk on the electronics and trigger system
for the J-PARC E16 experiment.
Other contributions for the detail of the DAQ software, trigger ASIC,
and so on are also prepared and submitted by coauthors.

References

[1] http://openit.kek.jp/ (in Japanese)

[2] M. Raymond *et al.*, IEEE NSS Conf. Rec. 2 (2000) 9/113.

[3] http://rd51-public.web.cern.ch/RD51-Public/

[4] http://www.psi.ch/drs/

[5] http://daqmw.kek.jp/ (in Japanese)

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