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Online-Analysis of Hits in the Belle-II Pixeldetector for Separation of Slow Pions from Background

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The impending Upgrade of the Belle experiment is expected to increase the generated data set by a factor of 50.
This means that for the planned pixeldetector, which is the closest to the interaction point, the data rates are going to increase to over 20 GB/s.
Combined with data generated by the other detectors, this rate is too big to be efficiently send out to offline processing.
This is makes the employment of online data reduction schemes necessary, in which background is detected and rejected in order to reduce the data rates.
In this paper an approach for efficient online data reduction for the planned pixeldetector of Belle-II is presented.
The approach centers around the usage of an algorithm, the NeuroBayes, that is based on multivariate analysis, allowing the identification of signal and background by analysing clusters of hits in the pixeldetector on FPGAs.
The algorithm is leveraging the fact that hits of signal particles can have very different characteristics, compared to background, when passing through the pixeldetector.
The applicability and advantages in performance are shown through the D* decay.
In Belle-II these decays produce pions with such a small transversal momentum, that they barley escape the pixel detector itself.
In a common approach like extrapolation of tracks from outer detectors to RoIs, these pions are simply lost, since they do not reach all necessary layers of a detector.
Meanwhile usage of the cluster analysis succeeds in separating those pions from background, allowing to retain the data.
For that characteristics of corresponding hits, like the total amount of charge deposited in the pixels, are used for separation.
The capability for effective data reduction is underlined by a background reduction of at least 90% and signal efficiency of 95 %, for slow pions.
An implementation of the algorithm for usage on Virtex-6 FPGAs, that are used at the pixeldetector, was performed.
It is shown that the resulting implementation succeeds in replicating the efficiency of the algorithm, implemented in software, while throughputs that suffice hard realtime constraints, set by the read out system of Belle-II, are achieved and efficient use of the resources present on the FPGA is made.

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