gFEX
the ATLAS Calorimeter Trigger Global Feature Extractor

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The ATLAS Experiment

Phase I Upgrade
Luminosity $\sim 2 \times 10^{34}$ cm$^{-2}$s$^{-1}$
25 ns bunch crossing
Pile up of $<\mu>\sim 60$
Level 1 rate $= 100$ kHz
HLT rate $= 1$ kHz
Motivation

Increase trigger efficiency for *Fat-jets* in ATLAS

- High $p_T$ bosons and fermions are a key component of ATLAS physics.
  - $W, Z$ and $H$ bosons, top quarks and exotic particles.
  - Many analyses with boosted objects.

- Analyses that addresses this kind of physics use large $R$ jets with $R > 1$.

- The ATLAS Level 1 trigger is designed for narrow jets, with limited acceptance for large objects.
Simulation Studies

Larger trigger acceptance

boosted top

\[ H \rightarrow b\bar{b}^- \]

Simulations performed for 14 TeV, and for a \( <\mu> = 80 \).
Simulation Studies

Jet energy pile up subtraction

Correlation between the event energy density (x) and estimated by gFEX (y). The correlation is better than 90%.
gFEX is a component of the ATLAS L1 Calo system in **Phase I upgrade**. It complements the electron and jet feature extractors. It is a single board system. Both eFEX and jFEX are multi-board systems.

See **Reiner Hauser**'s talk on ATLAS data flow in Track 1, tomorrow.
gFEX Concept

- Coarse granularity data ($\Delta \eta \times \Delta \phi = 0.2 \times 0.2$) from calorimeters are received by high speed optical links and processed by four large FPGAs.

- The processing FPGAs are monitored and programmed by a Hybrid FPGA (SoC).

- Results are transferred to the next level in L1 trigger.
Finding Large Radius Jets

STEP 1 - Find seeds. Seeds are towers with energy above a set threshold.

STEP 2 - Sum energy from neighboring towers. Concurrently, estimate pileup energy.

STEP 3 - Subtract pileup energy and “join” results. The final result is stored on processing FPGAs.

325 ns latency.
The gFEX is an ATCA module conforming to the PICMG 3.0 Revision 3.0 specification [14]. The gFEX module will likely be placed in a sparsely populated ATCA shelf so it occupies two slots if needed: one for the board and one for cooling (e.g., large heat sinks), fiber routing, etc.

2.2 Input Data
The gFEX receives data from the electromagnetic and hadron calorimeter via optical fibers. For most of the detector, the towers — called gTowers — correspond to a range of $\Delta \eta \times \Delta \phi = 0.2 \times 0.2$. Calorimeter locations with towers different from this standard size are detailed in Sec. 3.3.

Calorimeter data are transmitted as continuous serial streams. The gFEX logic must be aligned with the word boundaries in this serial data for conversion into parallel data. The scheme for achieving this is not yet specified, however, possible mechanisms are being explored.

The calorimeter data are accompanied by a CRC code. This is checked in the Processor FPGA immediately following conversion from serial streams into parallel data. All data with a detected error are sent to the readout path without modification but are zeroed on the real-time trigger path. In addition, information about errors is collected as follows:

- **Input Error Count**: Incremented for any clock cycle with at least one error in any input channel.
- **Input Error Latch**: Active for any channel with at least one error. These bits remain set until cleared via an external signal.
- **Error Check Result**: Formed from an OR of all error checks for the current BC.
- **Global Input Error**: Formed from the OR of all bits in the Input Error Latch.

The Input Error Count, Input Error Latch, Error Check Result, and Input Error bits can be read via an IPbus command [15] and will be reported via the Hybrid FPGA. An IPbus command will be able to clear any or all of these registers. The Error Check Result and Input Error Count are included in the readout data for the current BC. Additionally, the quality of the input data is assessed:

See Jorn Schumacher's presentation in Track 1 tomorrow.
1. The baseline FPGA is the **XC7VX690T-FFG1927** speed grade -3 @ 320 MHz.

2. The SoC is the ZYNQ **XC7Z045-FFG900**, with dual ARM core and Linux OS (PetaLinux).

3. Input/Output
   - 4x 72-fold MPO* connectors (IN)
   - 2x 48 MPO* connectors (OUT)
   - miniPODs for Rx and Tx
   - JTAG, UART, RJ45 (Front)
   - ATCA Zone 1 & J23 ADF+ (Back)

4. The number of **input fibers** is 264 (at 6.4 Gb/s) or 232 (at 11.2 Gb/s).

\(^*\)MPO - Multiple-Fiber Push-On/Pull-off
Development Plans

1. gFEX is being developed in stages. The first phase (*ongoing*) is to prototype a board to assure full integration with L1 Calo. In a second stage a board with four FPGAs will be produced.

2. High speed optical links will be tested. Supported I/O speeds are 6.4, 9.6, 11.2 and 12.8 Gb/s.

3. Integration and link speed tests will take place at the end of 2015.

4. Firmware for data processing is being developed in parallel using commercial boards.
Prototype Schematic and Layout are complete! It is implemented in an ATCA board form factor.
Challenges

1. gFEX will be a 26 layer board, with a total thickness of ~2.6 mm.

2. The choice of material is critical for the high speed traces within the board. Selected Megtron 6.
Summary

The global feature extractor, gFEX, will add to ATLAS the capability to trigger on large radius jets at Level 1.

It is based on FPGA processing. Four large FPGAs will receive coarse data (0.2x0.2) from the EM and HAD calorimeters and select events of interest.

Prototype is now being built. Initial prototype addresses the interfaces with ATLAS L1. After this phase a full processor will be built.

gFEX is processor board that has a large number of high speed I/O lines and could be used in other applications.
Extra Slides
gFEX: number of optical fiber connections

<table>
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<tr>
<th>Partition</th>
<th>Coverage</th>
<th>6.4 Gb/s</th>
<th>9.6 Gb/s</th>
<th>11.2 Gb/s</th>
<th>12.8 Gb/s</th>
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<tr>
<td></td>
<td>gTowers/Fiber</td>
<td>bits/gTower</td>
<td>Fibers</td>
<td>gTowers/Fiber</td>
<td>bits/gTower</td>
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<tr>
<td>Barrel EM</td>
<td>8 15 64</td>
<td></td>
<td></td>
<td>8 22 64</td>
<td></td>
</tr>
<tr>
<td>Tile (Phase I opt.2)</td>
<td>16 ? 32</td>
<td></td>
<td></td>
<td>16 ? 32</td>
<td></td>
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<tr>
<td>Tile (Phase I opt.3)</td>
<td>12 10 48</td>
<td></td>
<td></td>
<td>12 ? 48</td>
<td></td>
</tr>
<tr>
<td>Tile (Phase II)</td>
<td>8 15 64</td>
<td></td>
<td></td>
<td>8 22 64</td>
<td></td>
</tr>
<tr>
<td>Standard EMEC</td>
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<td>7 26 32</td>
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<tr>
<td>Special EMEC</td>
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<td>14 12 24</td>
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<tr>
<td>HEC</td>
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<td>18 10 32</td>
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<tr>
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<td>16 11 8</td>
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<tr>
<td>FCAL 2&amp;3</td>
<td>12 11 12</td>
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<td></td>
<td>16 11 8</td>
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<td>Total (Phase II)</td>
<td></td>
<td>264</td>
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<td>232</td>
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</table>

Note: The TOBs are transmitted to L1Topo on optical fibers assuming that each Processor FPGA will have one or more independent gFEX. It is foreseen that the bandwidth could be increased up to 12.8 Gb/s. The TOB format and payload for transmission to L1Topo is the same as described in Sec. 3.1.
gFEX References

Performance Plots (Simulation)

https://twiki.cern.ch/twiki/bin/view/AtlasPublic/JetTriggerPublicResults#Global_Feature_Extraction_gFEX_P

gFEX Prototype Technical Specification

https://edms.cern.ch/file/1425502/1/gFEX.pdf