Evaluation of 'OpenCL for FPGA' for DAQ and Acceleration in HEP applications

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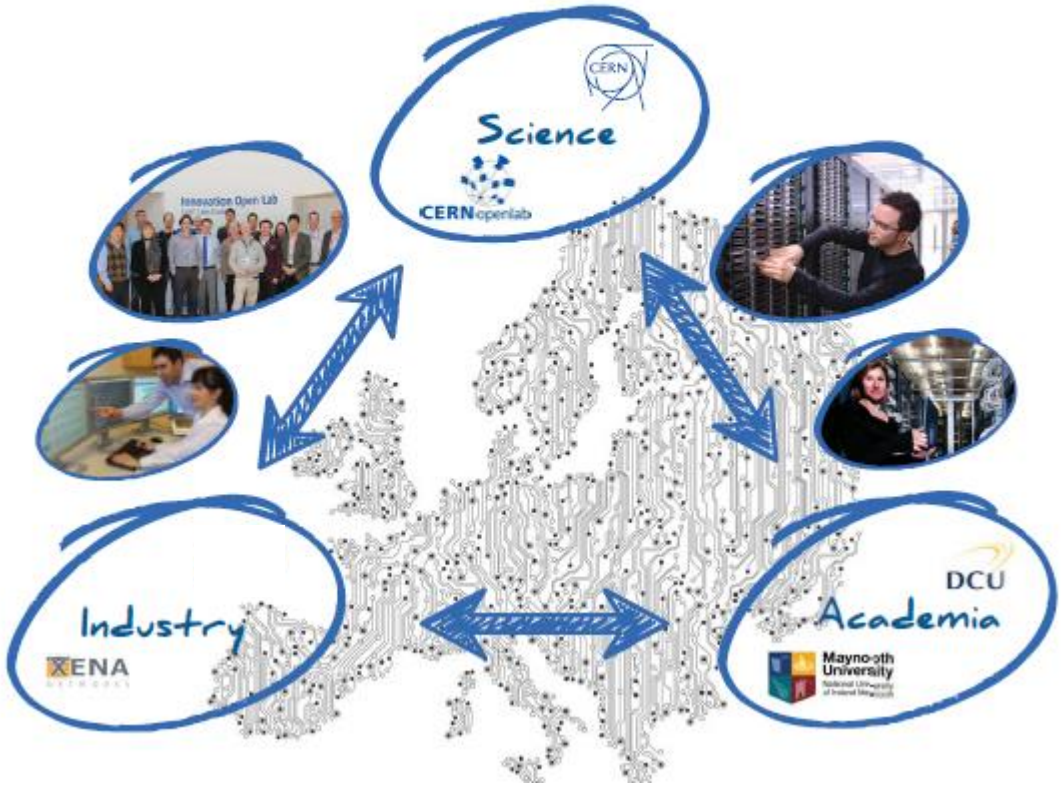
ICE-DIP 2013-2017:
The Intel-CERN European Doctorate Industrial Program

A public-private partnership to research solutions for next generation data acquisition networks, offering research training to five Early Stage Researchers in ICT

Research topics:

- Silicon photonics systems
- Next generation data
- High speed configurable logic
- Computing solutions for high performance data filtering



Background image: Shutterstock

The Grand Challenge for proposed upgrade of LHCb experiment

- **500 Data sources each generating data at 100 Gbps**
- **Requires FPGAs for**
  - **DAQ modules**
    - Adaptive, high performance
  - **Low Level Trigger decisions**
    - Algorithm acceleration
- **FPGAs are great**
  - High Performance
  - Flexibility - Build anything
  - **But…**

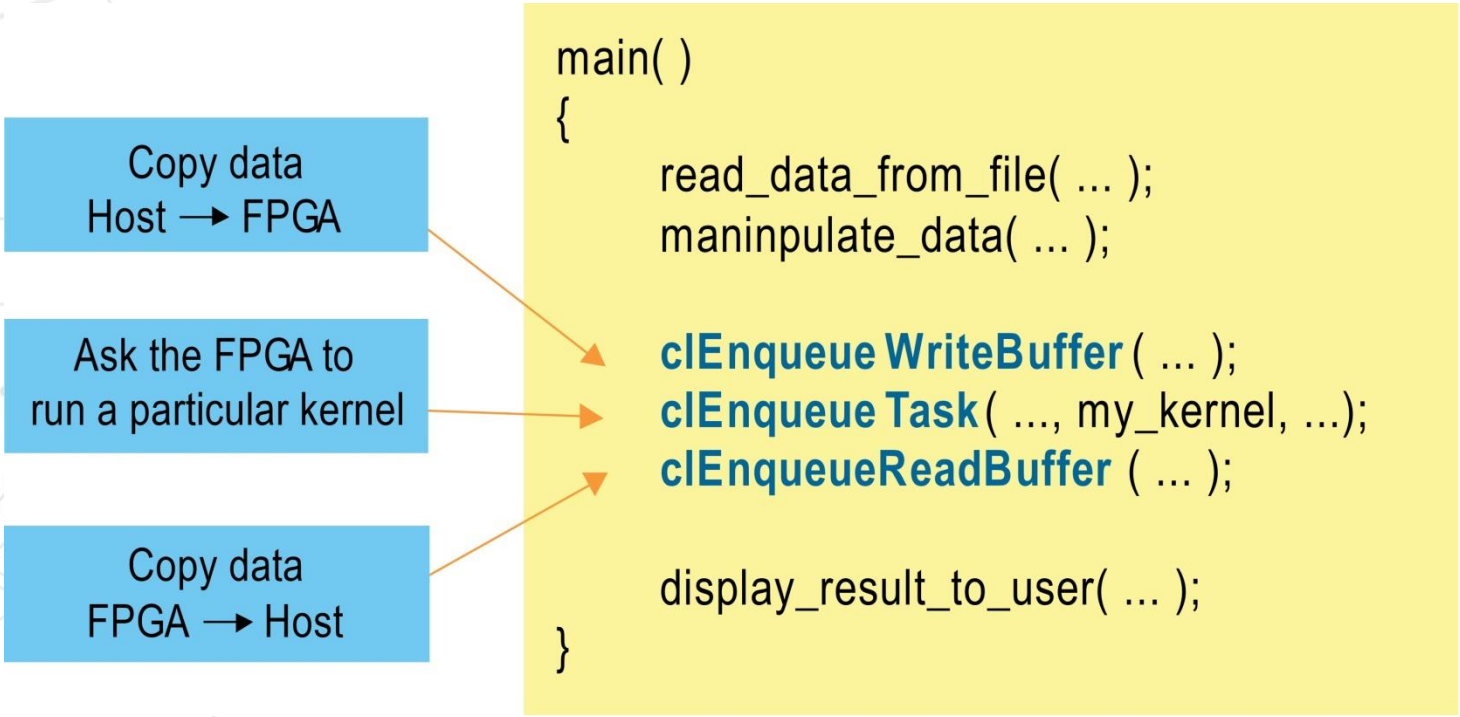
FPGA pains

- **Programmability, Programmability, Programmability**
  - Using Hardware Description Languages (HDLs)
  - At Register transfer level (RTL) abstraction
  - Create Custom Memory Hierarchies
  - Manage Communication with PC
  - Create PC side SW that plays nice with all this

OpenCL for FPGA

- **An unified programming model for accelerating algorithms on heterogeneous systems**
  - C based programming language
  - System level design (Host CPU+FPGA)
  - Memory Hierarchy auto generated
  - Host CPU-FPGA communication abstracted away
  - Potential to integrate existing VHDL/Verilog IP

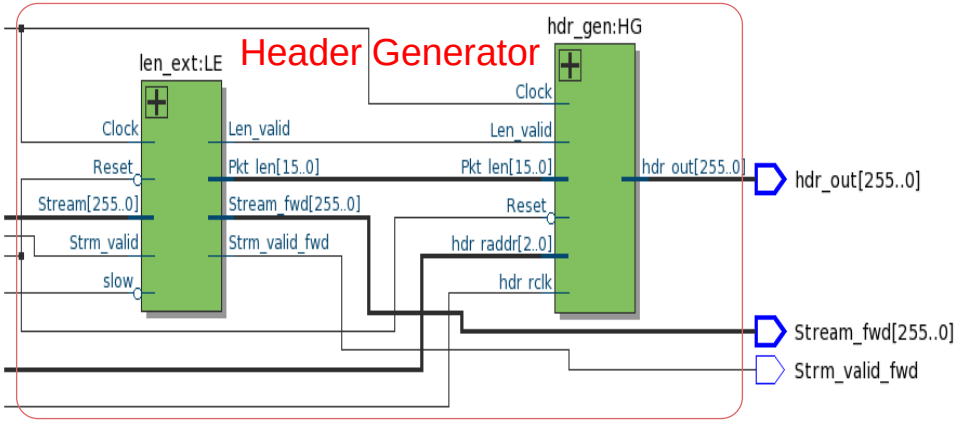
OpenCL for FPGA



End to end DAQ + Acceleration system with ‘OpenCL for FPGA’ ?

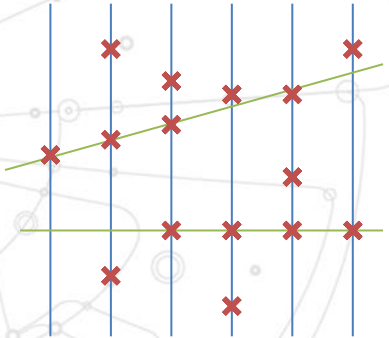
- **OpenCL spec targets**
  - Algorithm Acceleration
  - Not FPGA design
- **But, How about ‘OpenCL for FPGA’**
  - More than Acceleration?
  - A DAQ system with OpenCL?
- **Only one way to find out**
  - Go ahead and implement one

An existing FPGA DAQ system



Requirement	OpenCL Std spec	Altera OpenCL extension
IO, moving data between kernels	X Pipes in v2.0	Channels (IO -> Kernel, Kernel -> Kernel, Kernel ->IO)
Bit level manipulation, non std data width	X	Bitfields & Other mechanism
Control signals	X	X

OpenCL Algorithm Acceleration



Hough Transform

- Used for particle track reconstruction in LHCb for the future VertexDetector
- Find tracks from the Hit data of the detector
- Exisiting OpenCL GPU code ported to FPGA

- Erratum: on this slide a comparison measurement was shown which is erroneous and has been retracted. We will show a corrected measurement in the paper.

Conclusions

- **FPGAs have always been capable devices**
  - Performance, Versatility, Flexibility
- **But so have been limited by the usability**
  - Separate and HW oriented programming model
- **OpenCL is a game changer**
  - Unlocking the potential of FPGAs much easier
  - Sure, there are some road blocks
  - But future of OpenCL for FPGA is definitely bright

Thank You!

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