

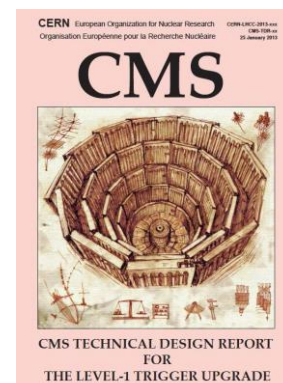
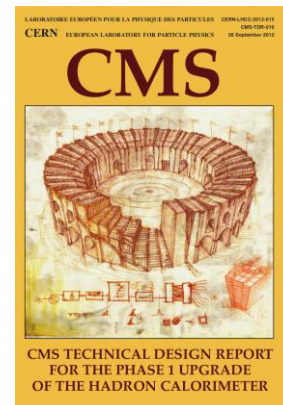
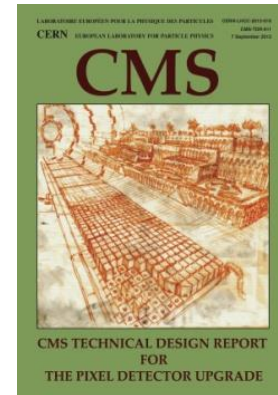
# CMS Phase 1 Upgrade Status

LHCC Upgrade Session  
J. Mans

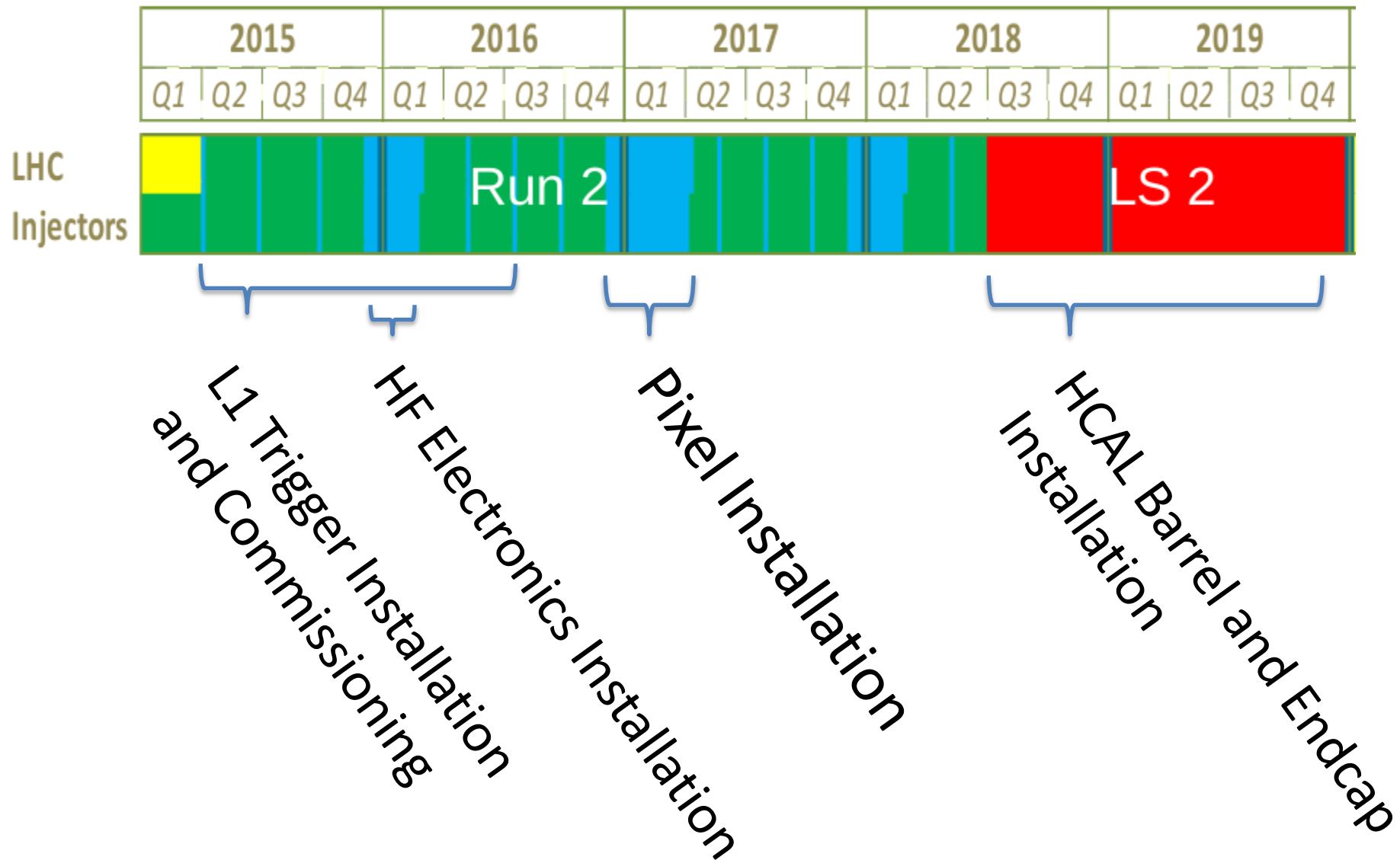
March 4, 2014

# Reminder: CMS Phase 1 Upgrade Scope

- Upgrade goals are to provide strong physics performance for luminosities up to twice the original design ( $2 \times 10^{34}$ ) and manage radiation-damage effects up to  $500 \text{ fb}^{-1}$
- Upgrades planned to three subsystems of CMS
  - Pixel tracker : four-layer barrel and 3 forward-disk pixel tracker with new readout chip (ROC) capable of higher hit rate
  - Hadron calorimeter : Installation of SiPM devices into barrel/endcap calorimeters and new electronics in the forward calorimeter allowing timing-based background rejection
  - Trigger : upgrade to the muon and calorimeter Level-1 trigger systems and global trigger processor to handle higher luminosities without loss of efficiency for key physics channels



# Schedule of the Installations

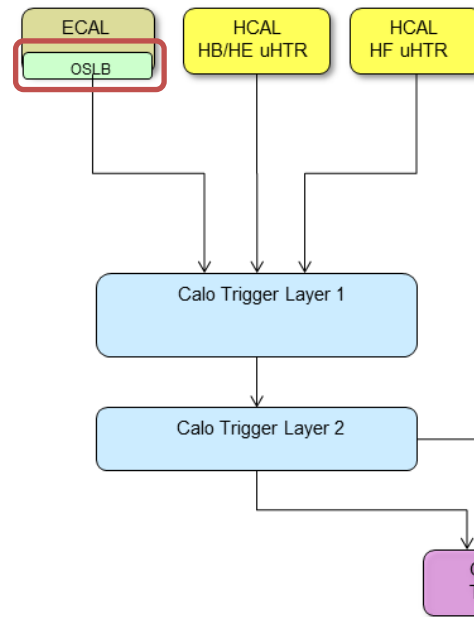


# **LEVEL 1 TRIGGER UPGRADE**

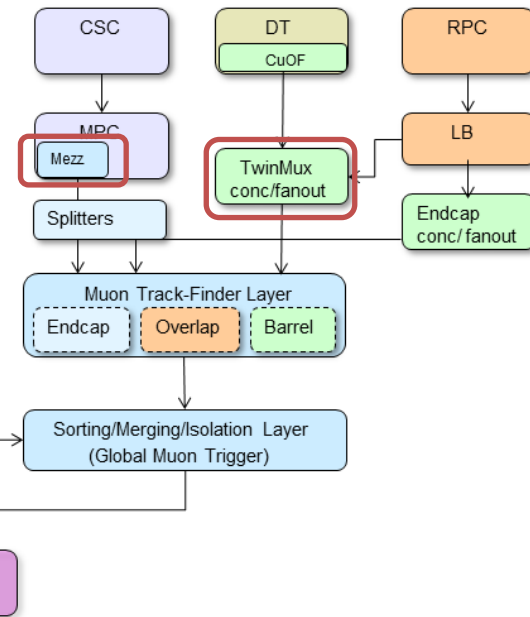
# Trigger Upgrade Strategy and Architecture

- Trigger rates are driven by the increase in luminosity, PU, and  $\nu_s$
- Mitigate by improving:
  - $e/\gamma$  isolation
  - $\tau$  id
  - muon  $p_T$  resolution
  - muon isolation
  - jets with PU sub.
  - L1 menu sophistication
- Build and commission upgrade in parallel with current trigger system in 2015 to safeguard physics, decouple from LHC schedule
- Target deployment: 2016
  - Installation begins during LS1 with electronics upgrades to provide parallel optical data paths to current and upgrade electronics

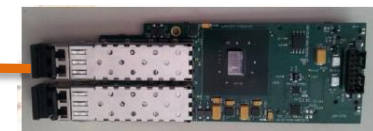
## Calorimeter Trigger



## Muon Trigger



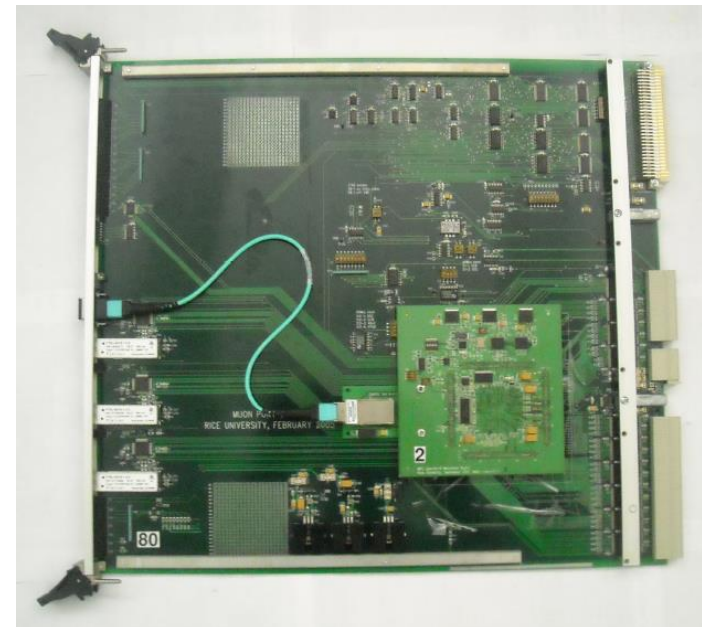
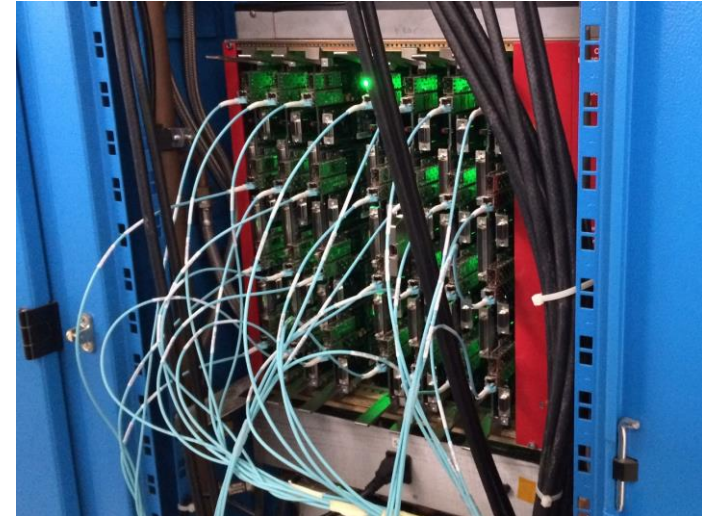
### oSLB (Calo Trigger)



### oRM (Calo Trigger)

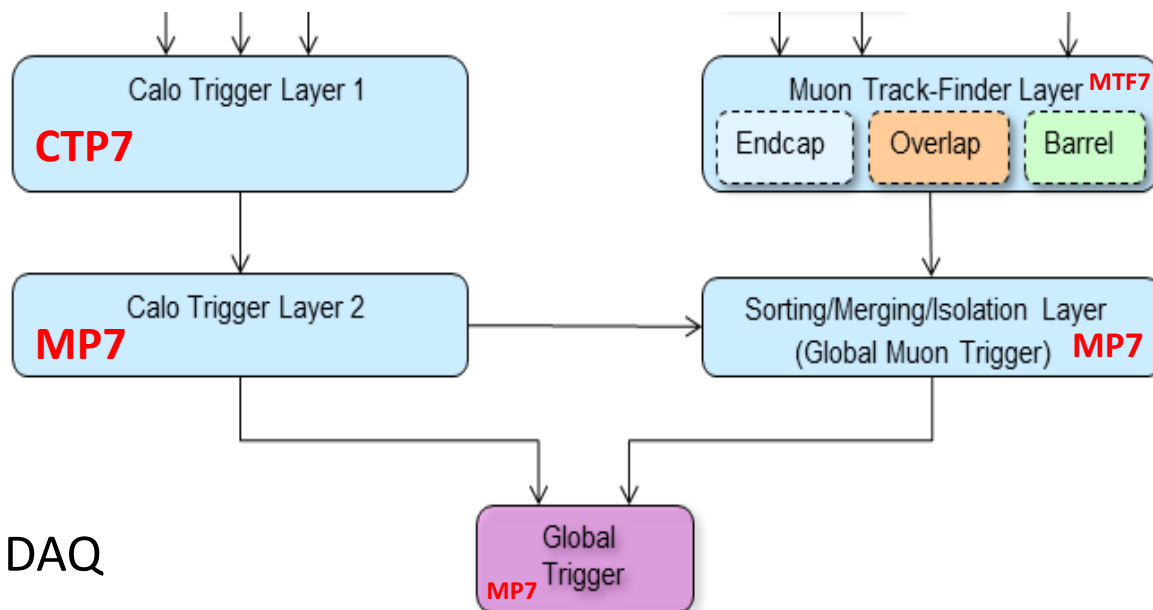
# Optical infrastructure upgrade status

- Optical SLB and RM mezzanine boards (ECAL)
  - All oSLB and oRM cards (650 each) have been delivered and are currently under production testing.
    - All oSLBs and 439 oRMs have passed JTAG tests
      - Only 1 oRM found faulty so far
    - 340 oSLB have passed optical link pattern tests as well as 28 oRMs validated in an RCT crate
  - Expect installation and commissioning by July
- Muon Port Card mezzanine boards (CSC muon system)
  - All 85 mezzanine cards are complete and under test → on track
  - 8 are at CERN ready to be installed for commissioning
  - Integration tests to legacy CSC Track-Finder and to prototype upgraded Muon Track-Finder successful
- DT “TwinMux” concentrator and fan-out
  - Prototype expected this month



# uTCA Architecture and Common Cards

- A “7” in the names of modules indicate the use of Xilinx Virtex 7 FPGAs
- L1 Trigger upgrades are based on uTCA electronics architecture and make substantial use of common cards

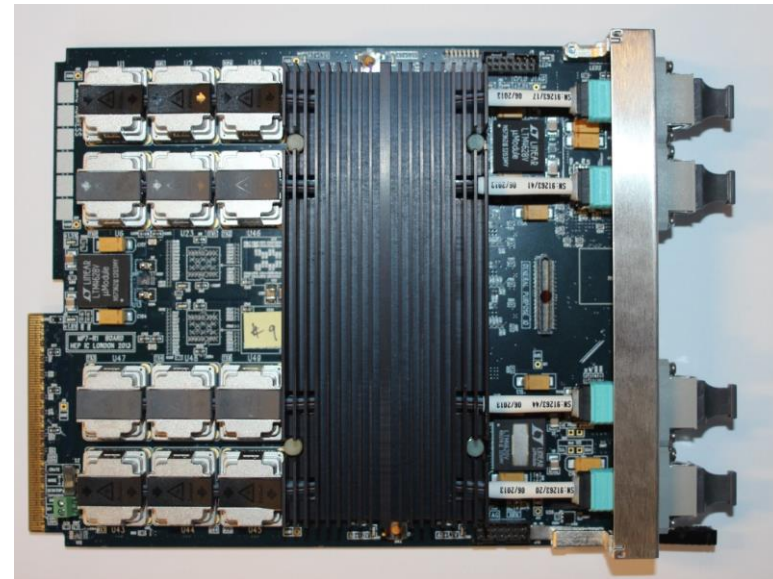
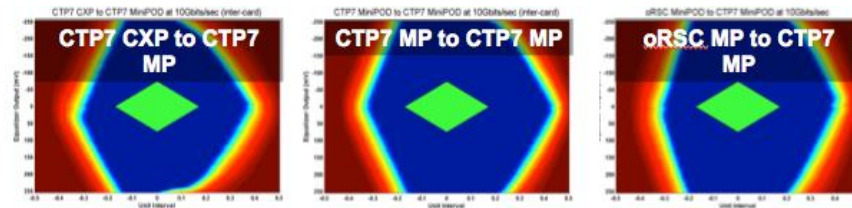
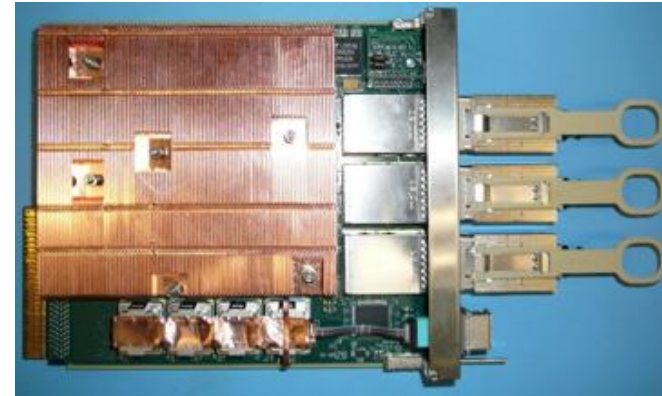


- AMC13 card for timing and DAQ
- MP7 card used in second layer of both calo and muon trigger, as well as global trigger
- Common muon track finder electronics across the full detector

- Firmware for different functions is substantially different, with some reuse of code modules
  - Reconciling requirements across different users takes time and engineering resources, but will have operational and support benefits for future operation

# CTP7 and MP7 Status

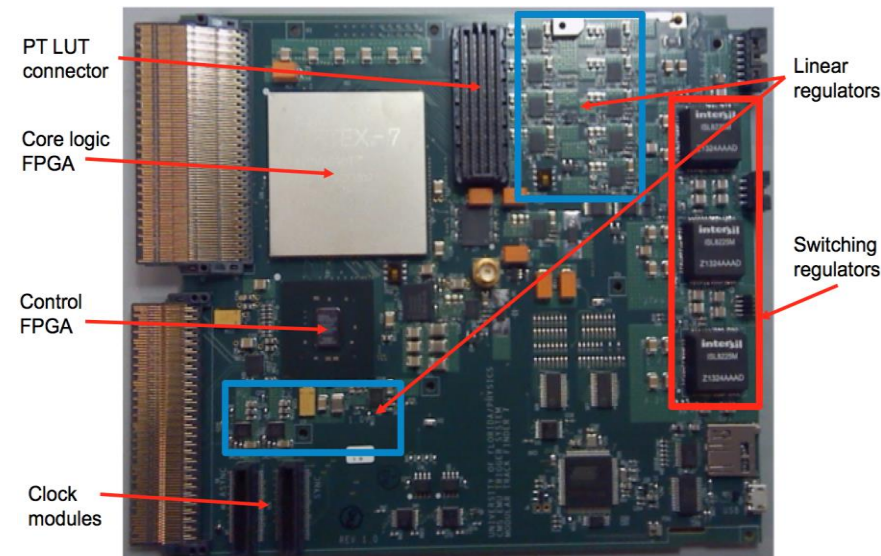
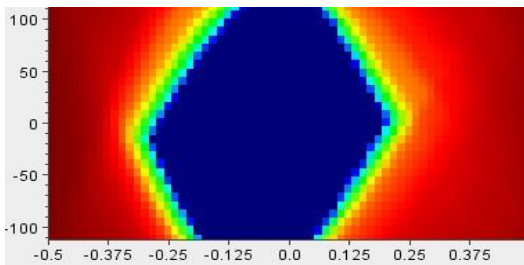
- CTP7 Status (Calo Layer 1)
  - Two assembled boards under test since Jan.
  - Eye scans taken during 134-link run show excellent margins @ 10 Gbps
- MP7 Status (Calo layer 2 and GT/GMT)
  - Cards have been delivered to other groups for firmware development (GT, GMT, and barrel muon)
- Full vertical slice in Bat.904 since Sept.including algorithms & emulators





# Muon Modular Track Finder Status

- Modular Track-Finder prototype →
- Hardware successfully tested:
  - FPGA base card - Virtex-6 version
  - 1GB RLDRAM mezzanine card (for PT assign)
  - Optical links card (range: 1.6 Gbps - 10 Gbps)
  - Backplane connector (up to 10 Gbps)
- “MTF7” Virtex-7 base card
  - Under test now
  - All 80 receivers and 28 transmitters working in loop back thru backplane @ 10Gbps



# Global Muon Trigger and Global Trigger Firmware Status

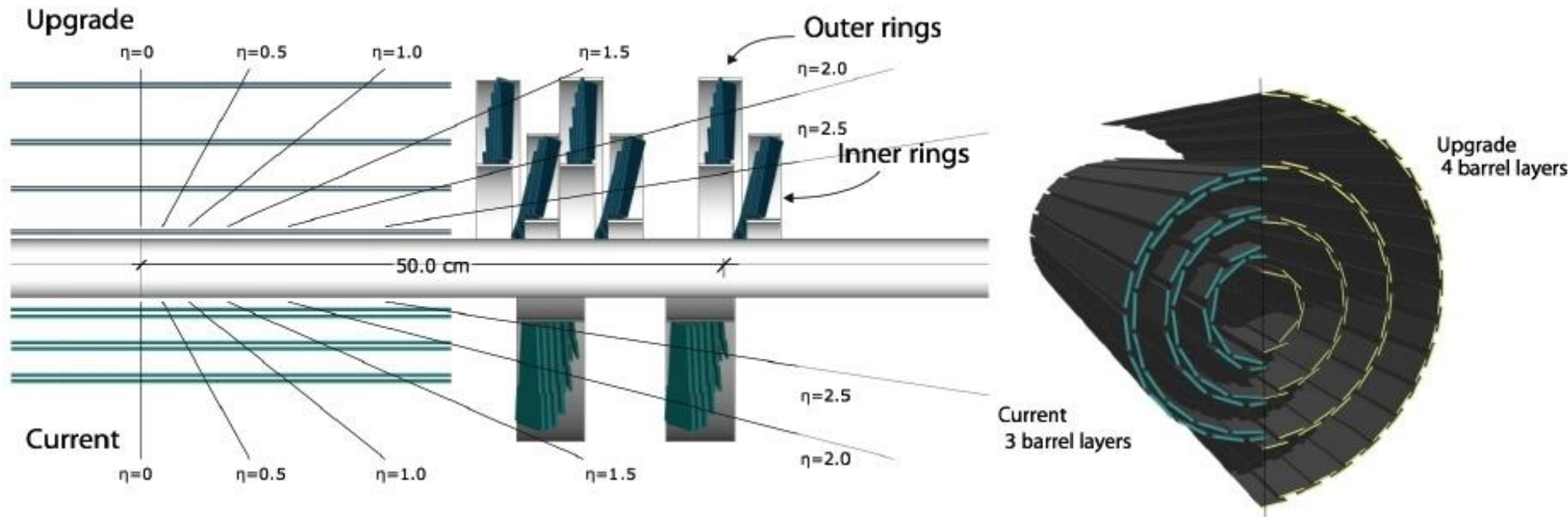
- Hardware platform is the MP7 processor for both
- $\mu$ GMT algorithm logic has been developed:
  - Sorting all 108 muons from Track-Finders to final 8 muons
  - Cancel-out logic for duplicates
  - Calorimeter-based isolation (incl. extrapolation + pile-up subtraction)
  - Estimated FPGA resource usage at 55% + DAQ logic
  - FPGA firmware compilation is in progress
  - Algorithm development on track
- $\mu$ GT
  - Object interfaces and data formats defined
  - Input patch panel design has been defined
  - Gaining experience with 10 Gbps links
  - First version of  $\mu$ GT menu is available

# Trigger Work Upcoming

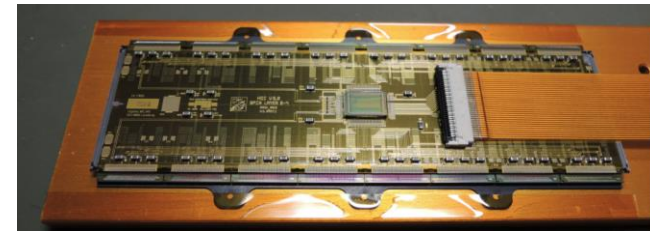
- A few upcoming integration tests (TDR)
  - Calo Layer 1 and Layer 2 integration test completed - Mar 2014
    - Electrical “IBERT” test only
  - ECAL, HCAL, Calo (both layers), GMT and GT integration test completed - July 2014
    - On track
  - Endcap TF, GMT and GT integration test completed - Sep 2014
    - On track
- Production of modules is on track
  - AMC13, MP7 module component procurement underway
  - CTP7 and MTF7 production later this year
  - Isolated small delays are well-within planned margin

# PIXEL UPGRADE STATUS

## Pixel Phase I Detector

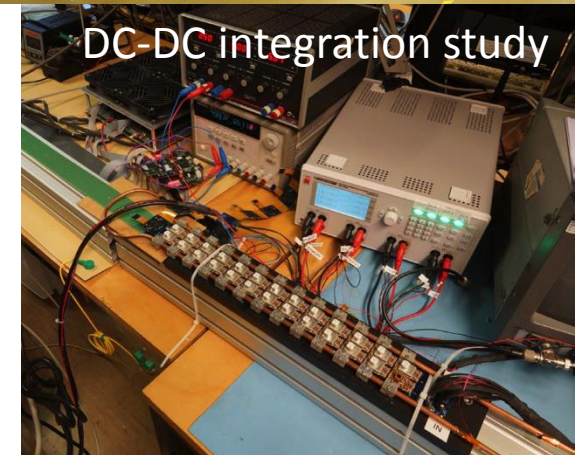
[TDR: CMS--TDR--011](#)

- 4 layers / 3 disks
  - One more space point: smaller inner radius (3 cm)
- New readout chip
  - Recovers inefficiency at high rate and PU
- CO<sub>2</sub> cooling, new cabling and powering scheme (DC–DC)
  - Less material
- Longevity
  - Tolerate 100 PU and survive to 500 fb<sup>-1</sup>, with exchange of innermost layer



# Pixel Phase I - General

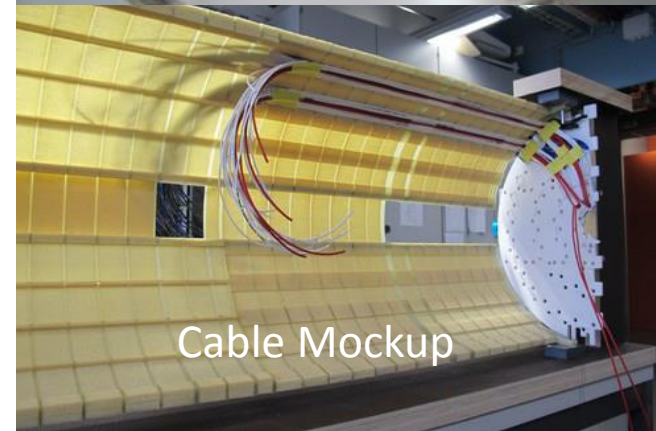
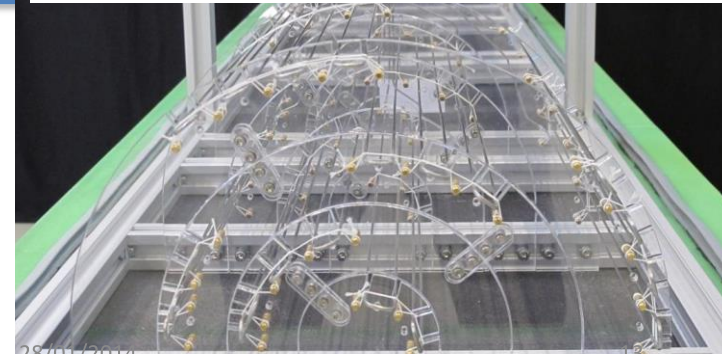
- Project PASSED a 2-day Engineering Design Review EDR 5th and 6th of December – organized by Technical Coordination
- Eng. wafers of the final PSIdigV2.1 ROC IN HAND
  - All tests VERY GOOD; modules have been built
  - These chips will be used for the pilot blade detectors
- Good progress on Token Bit Manager (TBM) chip design
  - Last ingredient for module construction
- DC-DC chip (FEAST2) submitted in December, expected back in March
  - Progressing on integration studies
- CO2 plant at the Tracker Integration Facility fully commissioned
  - Vacuum jacketed CO2 transfer lines INSTALLED onto CMS
  - Construction of final manifolds started



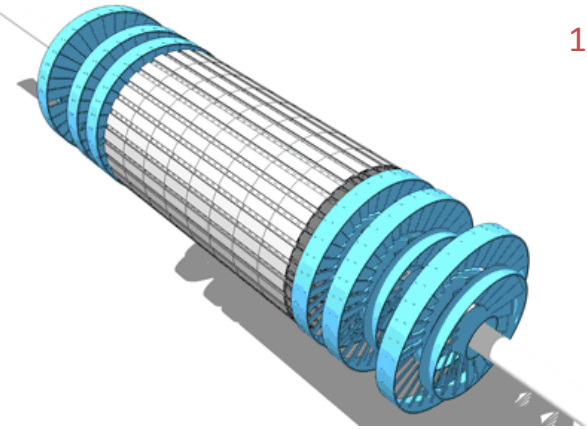
# Barrel Pixels (BPIX)

1:1 cooling BPIX cooling lines at CERN

- Good modules produced and testing specified
  - Starting a pre-production campaign (with V2 ROC chips) to qualify production chain and all production centers
- High density interconnects - pre-production in hand
- First batches of final production sensors received
- Work on supply tube progressing well
  - Electronics and mechanics
  - Cabling mock-up done
- Cooling piping replicate now at CERN for testing
- BPIX Mechanics mock-up ready for trial installation this year

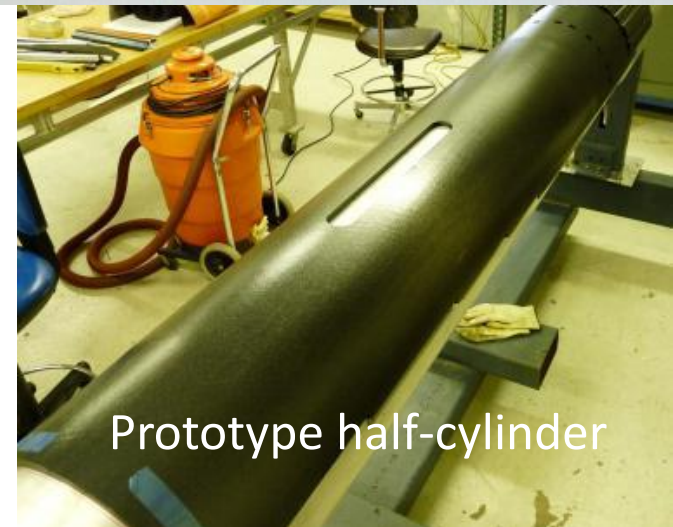


# Forward Pixels (FPIX)



- First FPIX modules built and tested in the US production centers
  - Exercise of Production and QA protocols
- Pilot Blade preparation on track
  - Will use final ROC
- Sensors from new 6" wafer production connected to chips, irradiated  $1.2E15$  1MEV\_N\_equiv. and are at the beam test right now
- Prototypes on Opto-hybrids look good
- Had some problems with current FPIX High-Density Interconnects
  - Good progress on solutions
- FPIX Mechanics mock-up ready for trial installation this year
- Good progress on mechanics in general
  - and on thermal management

Prototype Pixel Opto Hybrid

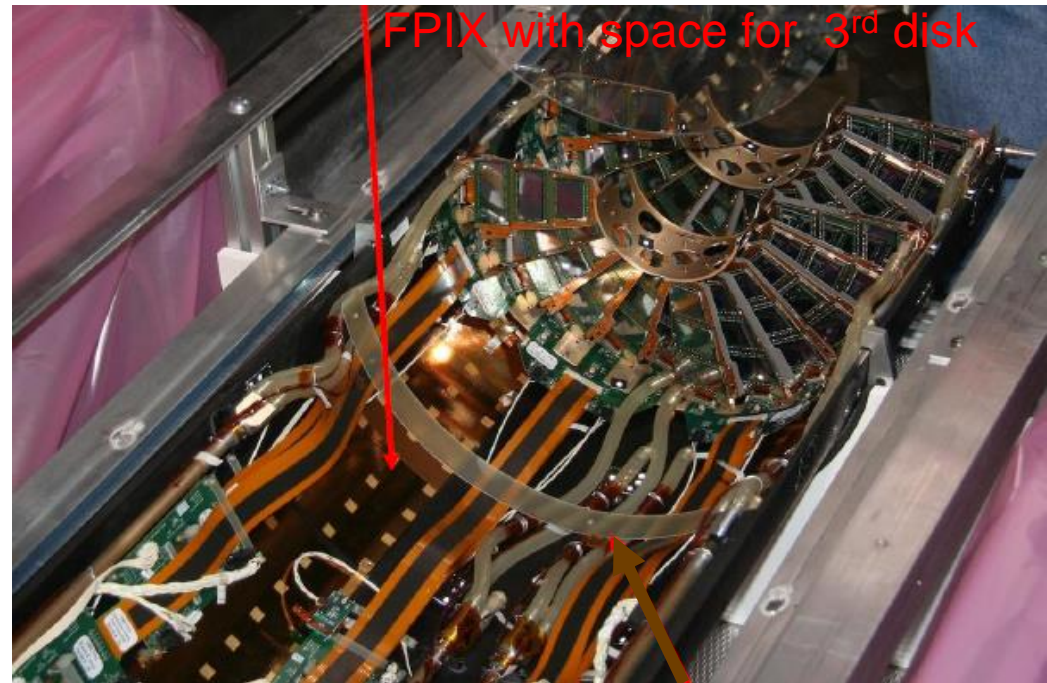


Prototype half-cylinder



## Pilot Detector and Ongoing Work

- CMS has benefitted greatly from pre-installation of small sections of upgrade hardware into the detector during operations
  - E.g. SiPMs in outer HCAL
- Pilot pixel detectors will be installed during LS1 including both DC-DC and linear-powered modules
  - Study performance of ROC in-situ
  - Head-start on DCS integration
  - Testbench for uTCA FED testing
- Plans for the pixel over the next six months
  - Launch DC-DC converter production after FEAST2 validated
  - Sensor, optohybrid production continues
  - TBM chip validation, engineering run
  - Module production beginning in August



# **HCAL UPGRADE STATUS**

# HCAL Phase 1 Upgrade Primary Components

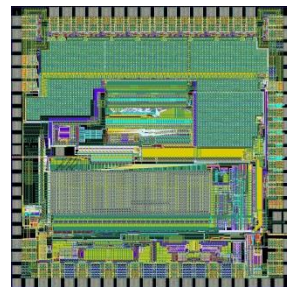
- Improved photodetectors
  - HB/HE: HPD → SiPM (allows longitudinal segmentation of readout)
  - HF: single-anode PMT → dual-anode readout PMTs (improved discrimination of anomalous signals)
- New front-end electronics, including TDC
- New back-end electronics ( $\mu$ TCA) to support larger data volumes

**HPDs**

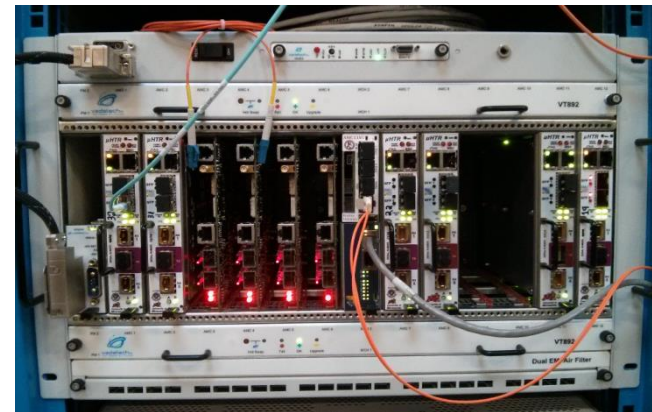
**SiPMs**



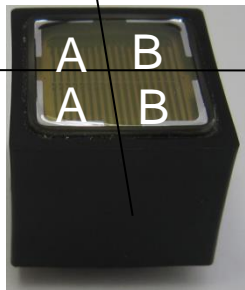
**QIE10 (HF)**  
**QIE11 (HBHE)**



**New  $\mu$ TCA Back-end**



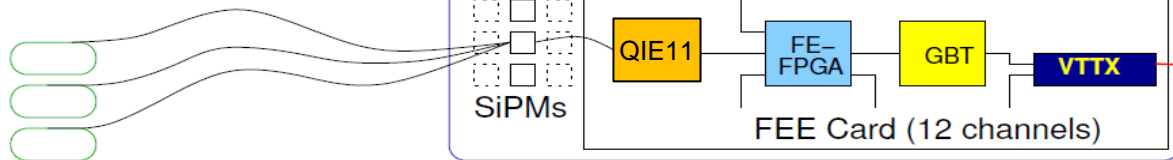
**Single to dual readout PMTs**



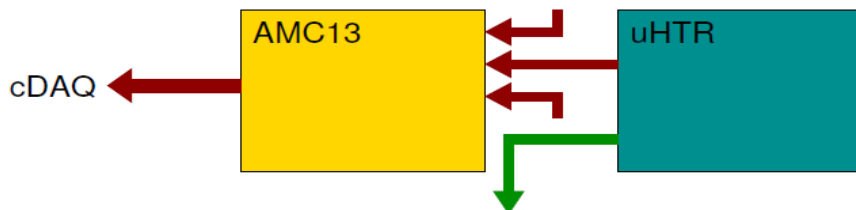
# HCAL Phase-1 Upgrade: Timeline

**HB**  
**HE**

Detector

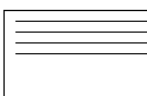


**Front-end**  
**2019 (LS2)**

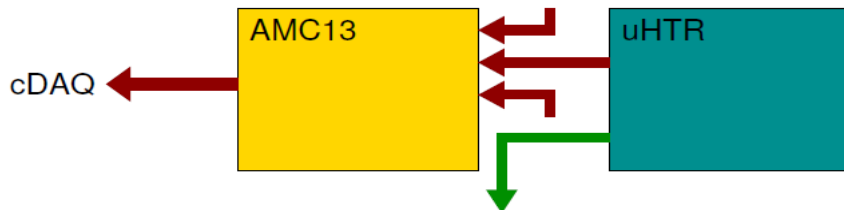


**Back-end**  
**2015-2016**

**HF**



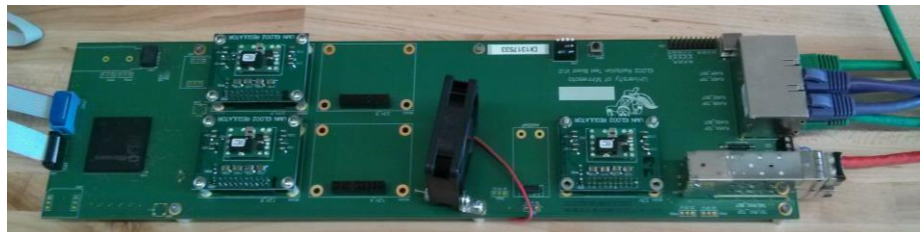
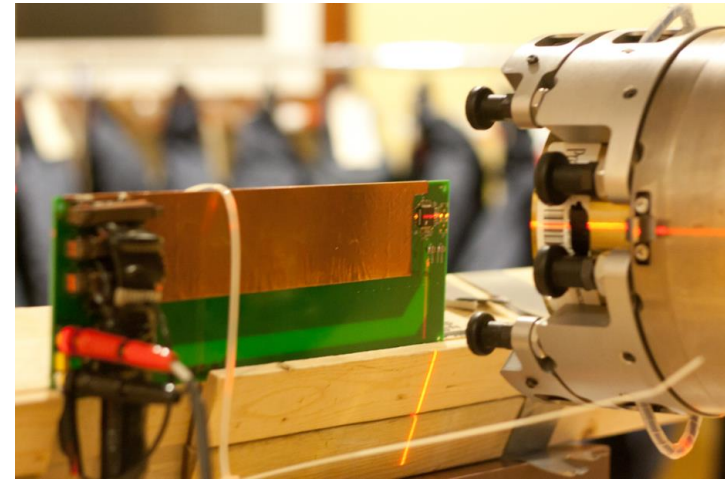
**Front-end**  
**Feb 2016**  
**(YETS)**



**Back-end**  
**2014 (LS1)**

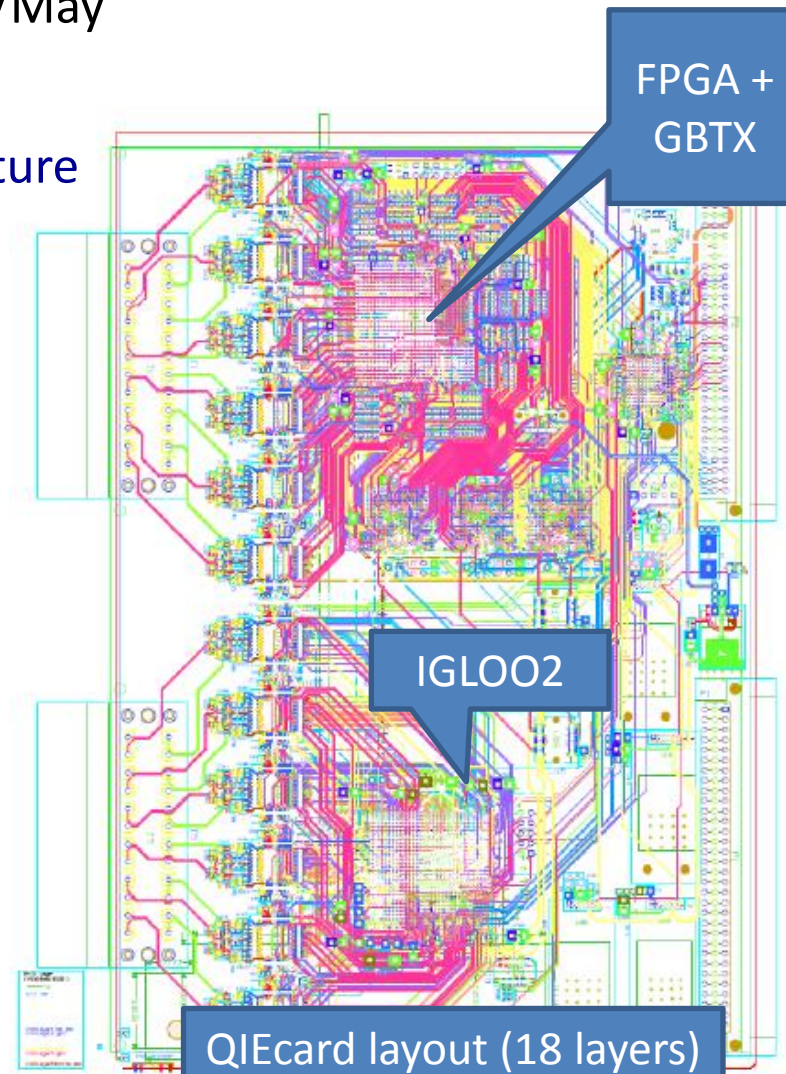
# Key Electronics Components

- QIE10 provides integrating ADC and TDC functionality for the HF upgrade
  - Prototypes show excellent performance
  - Radiation tests show acceptable SEU rate, device function beyond  $6 \times 10^{12}$  n/cm<sup>2</sup>, 250 kRad (expected  $2 \times 10^{12}$  n/cm<sup>2</sup>, 3 kRad)
- First prototypes of QIE11 for HB/HE, which provide a programmable current shunt to handle leakage current growth in irradiated SiPMs, are performing as expected
- GBTX serializer has been of concern, particularly for HF upgrade
  - Alternative solution: Microsemi Igloo2 FPGAs which allow the combination of the data formatting function (ProASIC3L) and serialization function (GBTX)
  - Device is able to stably transmit at 5 Gbps
  - Initial radiation tests show acceptable SEU performance (primarily in PLLs), tests on high-speed serializer still to be done



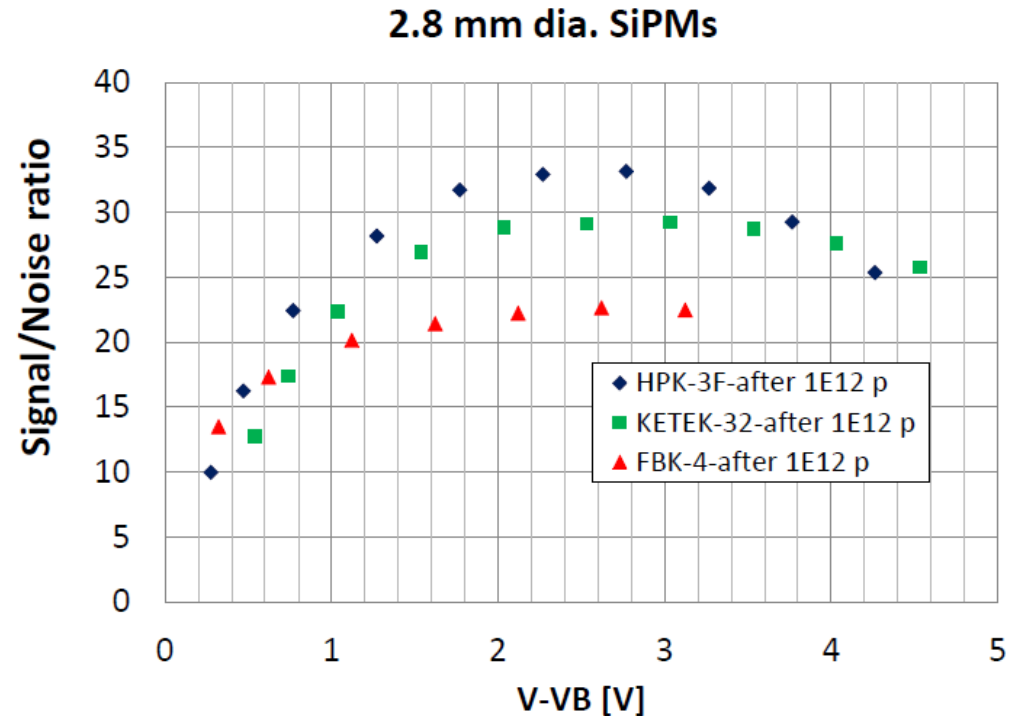
# HF Upgrade Electronics Status

- uHTRs and AMC13s making good progress
  - Delayed by 6 months relative to TDR schedule, mostly due to funding issues
  - On track for first full production crate in April/May
  - Successful integration testing with oRM
- Prototype Front-End Electronics under manufacture
  - HF QIE readout card designed to test both Igloo2 and GTBX
  - Control system (ngCCM) matching QIE readout card schedule
  - After bench and beam (FNAL) testing, pre-production cards will be prepared by Turkey and Brazil
  - Production readiness review expected by mid Fall 2014



# HB/HE Status

- Prototype SiPM devices irradiated to  $10^{12}$  p/cm<sup>2</sup> equivalent, with excellent performance after testing
- Pre-production cycle is being prepared now, with final-specification packaging
- Development of bias-board circuitry is ongoing
- Design of QIE card will follow path set out by HF QIE card, later in the year
- uHTRs and AMC13 modules for the HB/HE backend will begin production over the next six months (April for AMC13)



# Conclusions

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- Three TDR projects continue to make good progress
- Technical requirements are being met by prototypes and pre-production components
- Management focus is moving to execution of production, quality assurance testing, and preparations for installation for many parts of the upgrade
- Phase 1 Upgrades should be on-time to deliver physics performance for CMS