Intelligent Pixels: The SOIPiX R&D programme and applications

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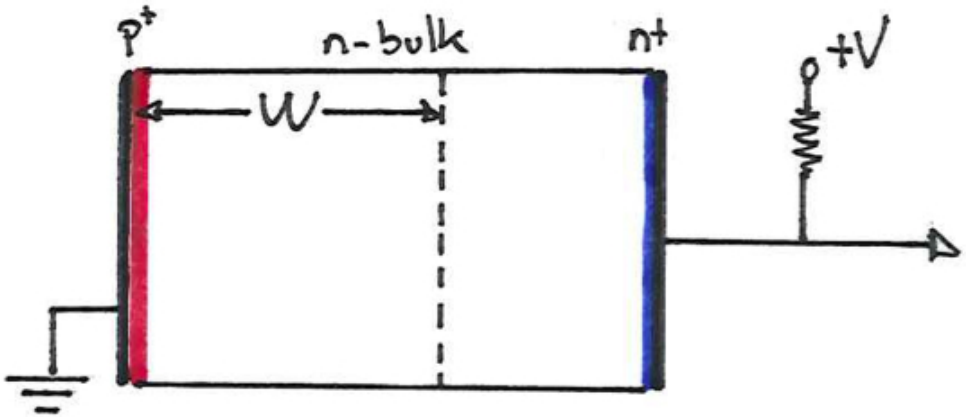
1. Introduction
2. SOI technology
3. SOIPIX project
4. Applications
5. Summary

Semiconductor sensors

The basis of semiconductor detectors is a reverse bias pn-junction

- In the depletion layer
  - No free charge carriers
  - Presence of an electric field
- If radiation pass through
  - e-h pairs generation in the depletion layer
  - Drift of charge carriers $\rightarrow$ signal induction



$$W \simeq \sqrt{\frac{2\varepsilon V}{qN}}$$

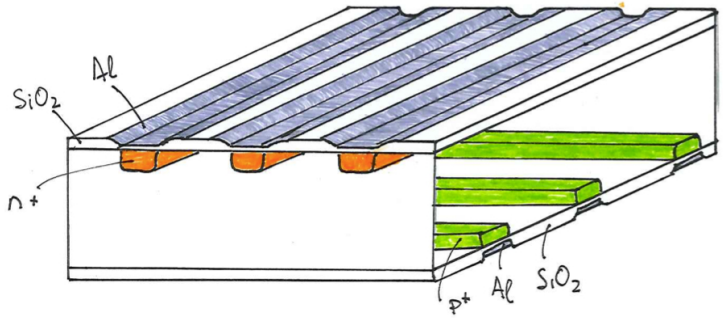
$W \uparrow$ if: $V \uparrow$

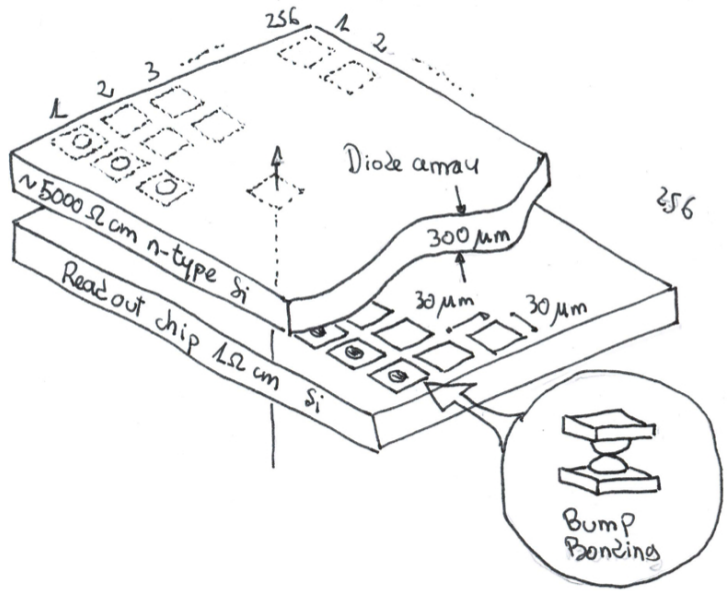
$N \downarrow$ HR wafers

Semiconductor structures

Semiconductors can be manufactured in various configurations:

- Pads
- micro-strips detectors
  - single sided
  - double sided
- Pixel detectors
  - Hybrid detectors
  - Monolithic pixel (MAPS)
  - Charge Coupling Devices (CCD)
- Silicon Drift Chambers





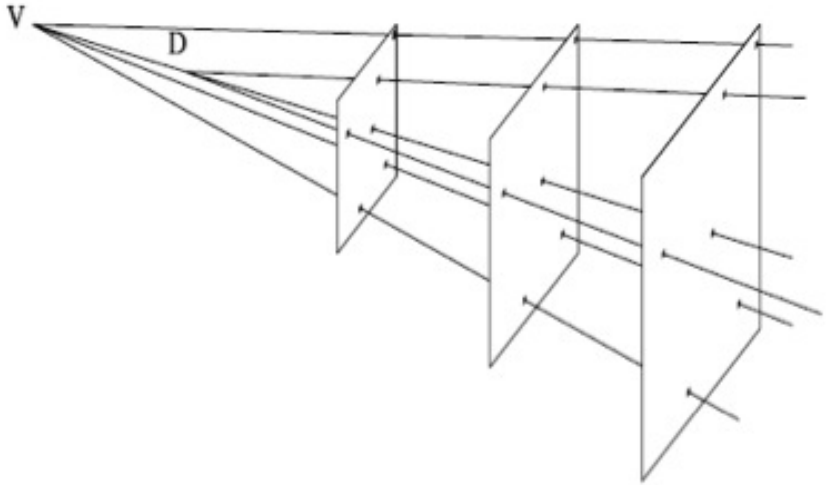
Pixel Detectors

- Target applications:
  - Particle Physics
  - Astroparticle
  - Astronomy and Astrophysics
  - X-ray, γ-ray imaging: medical, research, industry
  - Medical imaging
  - High Speed imaging
  - ...

- Pixel detectors used in demanding high energy physics applications such as at the Large Hadron Collider, ILC, B-factories.
- Innermost part of a detector is often the tracker
  - Resolution in space and/or time
  - Material budget
  - Radiation hardness

Pixel Detectors

- Spatial resolution to distinguish vertex and secondary decays

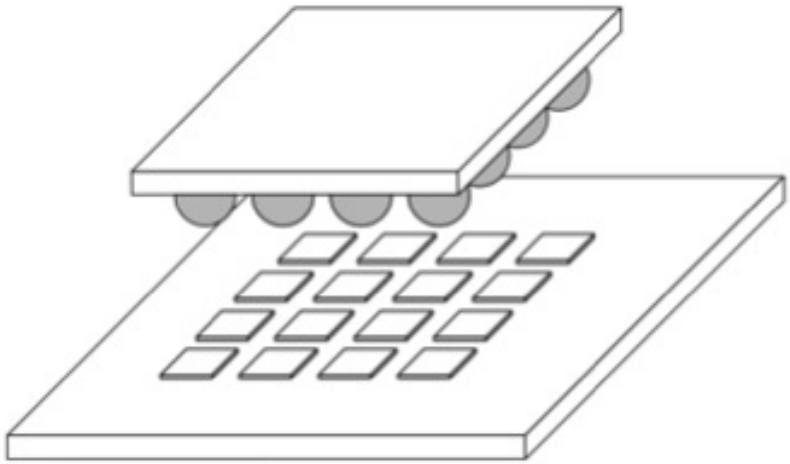


- Time resolution to cope with high rates
- Low material budget to reduce scattering
- Radiation hardness as detectors are close to the interaction point.

- Typical sizes: 20μm x 20μm
  - 2 cm x 2 cm sensor $\rightarrow 10^6$ readout channels
  - Power consumption per pixel should be low

Hybrid Detectors

- Current state of the art
- Sensor and readout electronics fabricated on separate wafers of different resistivities
- Connected together by bump bonding technique:



- "Complicated" procedure
- Costly in time and money
- Limits material budget
- Alignment and bump ball limits pixel size

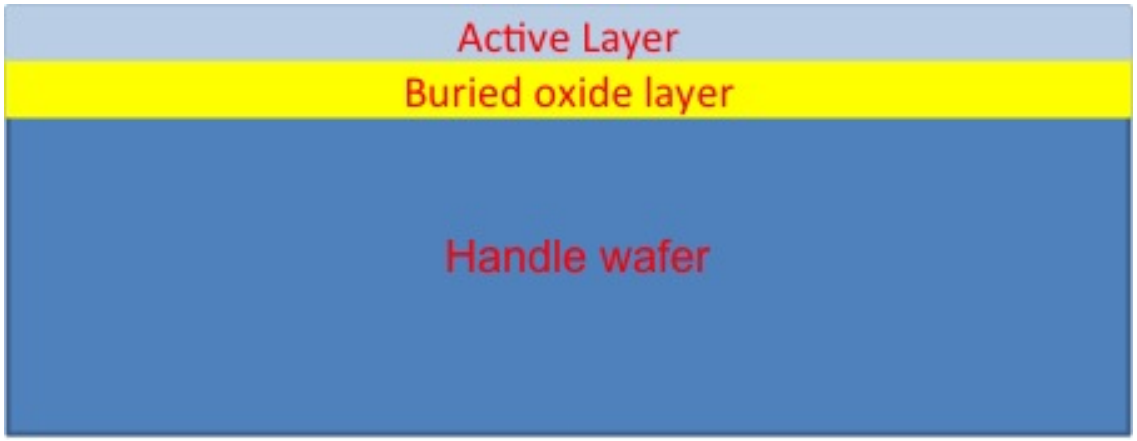
Monolithic Detectors

- Sensor and readout electronics developed in same silicon wafer
- Potentially overcome hybrid detector limitations and costs
- Research is ongoing on monolithic silicon detectors:
  - MIMOSA, CMOS sensors
  - DEPFET, Depleted Field Effect Transistor
  - CCDs (buried channels)
  - HVCMOS
- SOIPIX: Silicon-on-Insulator(SOI) technology

2. SOI technology
   - Description
   - SOI Detector
   - SOI feautures

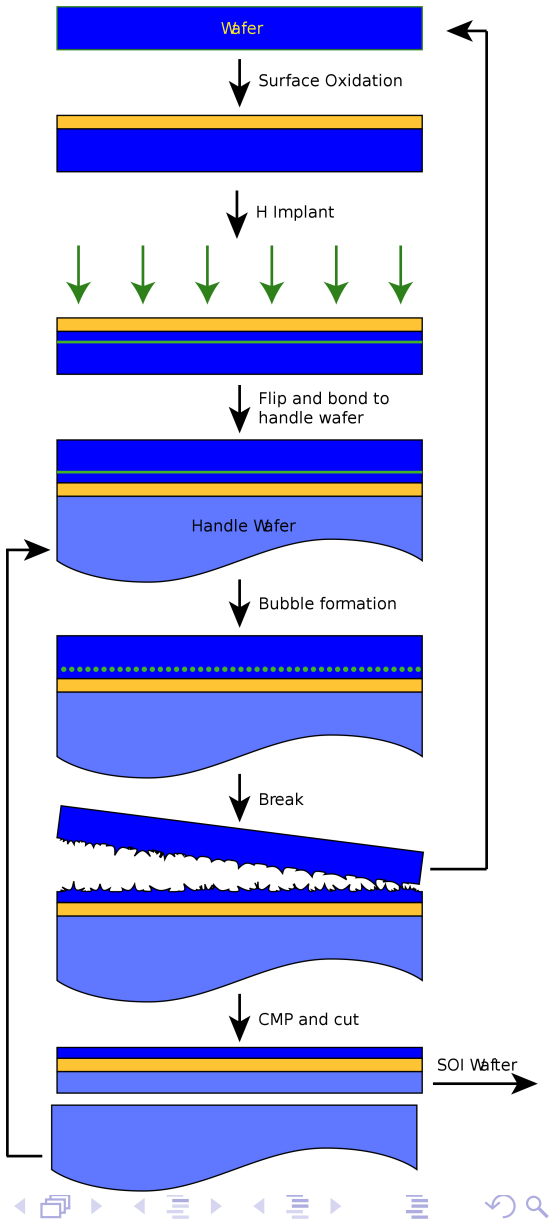
Silicon-on-Insulator Wafer

- Top active layer: a few tens of nm
- Buried oxide layer (BOX): a few hundreds of nm
- Handle wafer: a few hundreds of μm
  - High resistivity required for sensor development



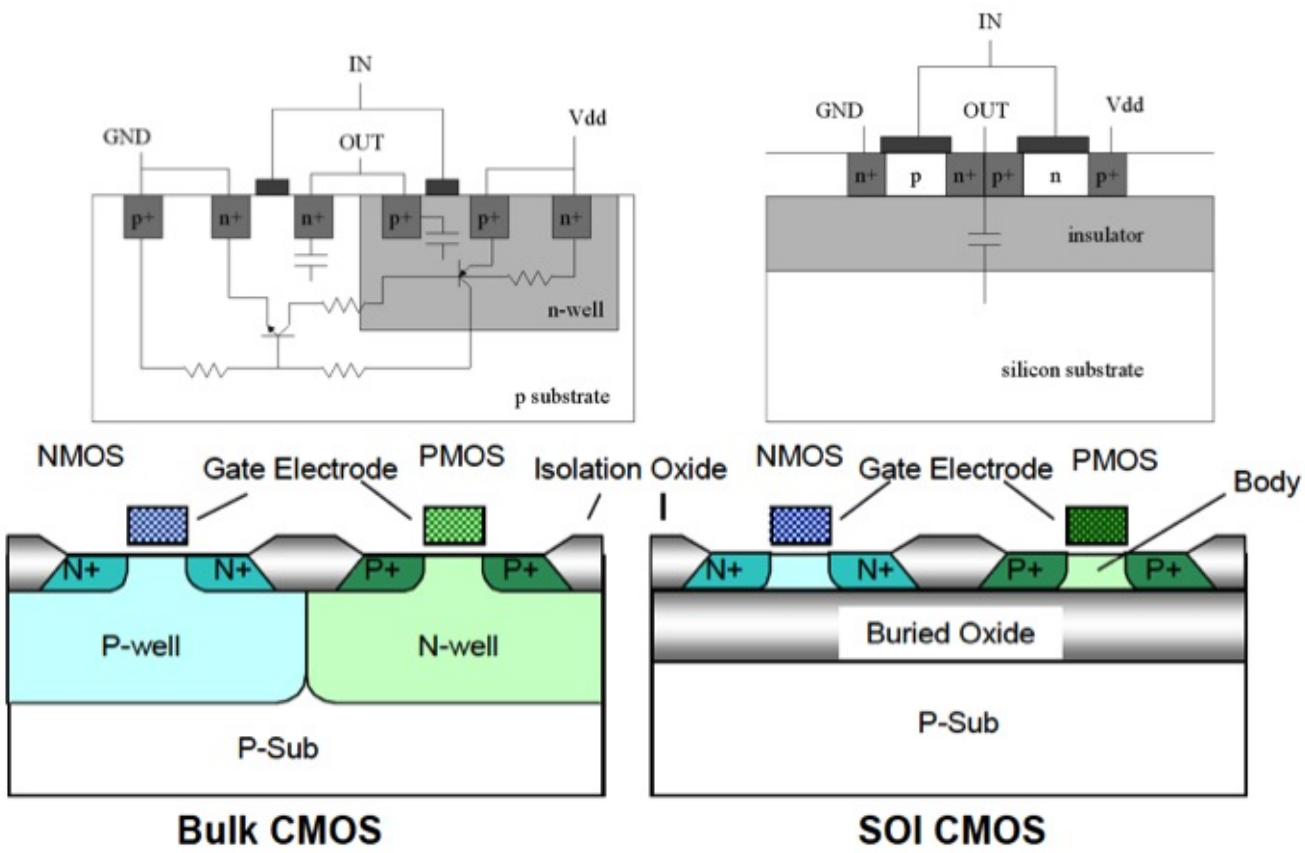
Silicon-on-Insulator Technology

- First field effect transistor patent in 1928 was for a device similar to current SOI but no evidence this device ever worked
- Specialized use for military and space applications due to radiation tolerance
- Mass production began in 1998 with IBM's PowerPC
- SIMOX and wafer bonding such as Smart Cut processes to create wafers
- Wafer bonding of interest for detector development since active layer and hand wafer can be different substrates



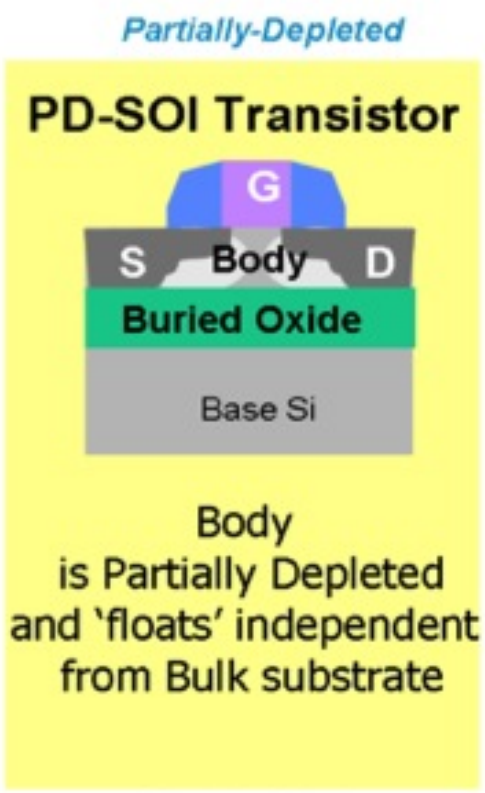
SOI vs bulk Technology

- SOI technology provides improved parasitic performance over traditional bulk technology
- Insulation from substrate removes parasitic structures
- In SOI each device is completely isolated by oxide



PD-SOI vs FD-SOI

Faces many barriers to further miniaturization



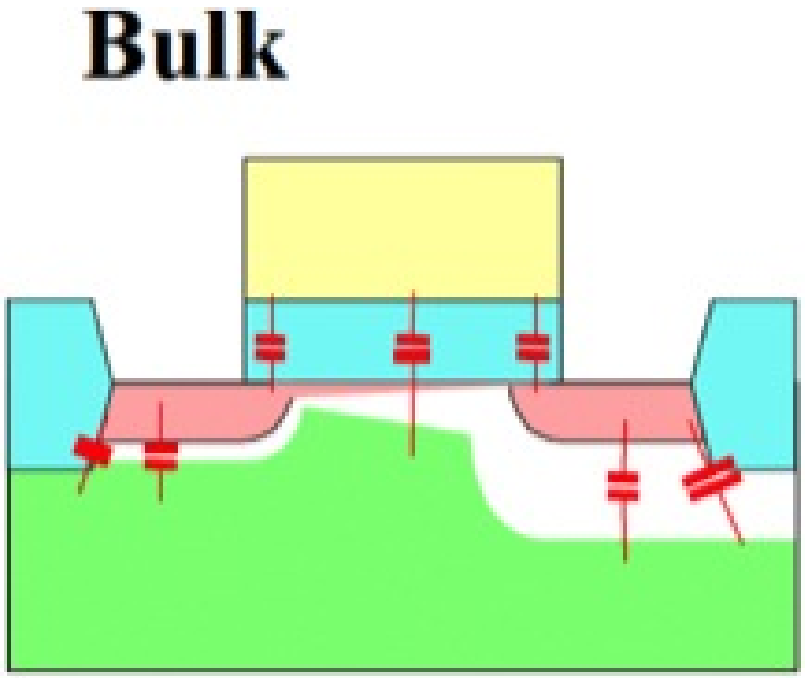
Floating Body boosts performance but introduces some peculiarities (History Effect, kink)

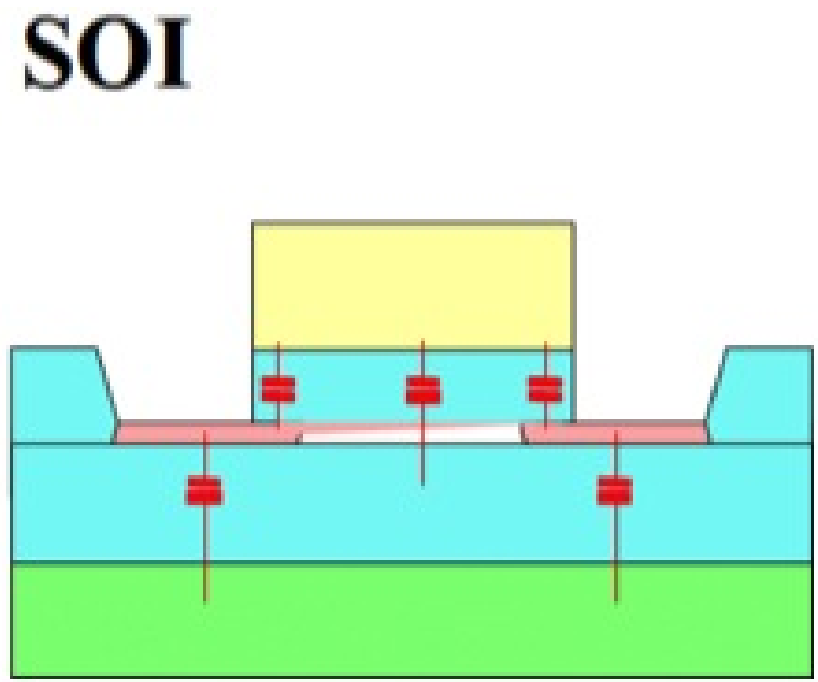
Tsi ~ 70nm . Tbox ~ 145nm

Addresses scalability issues
No History Effect
No kink effect

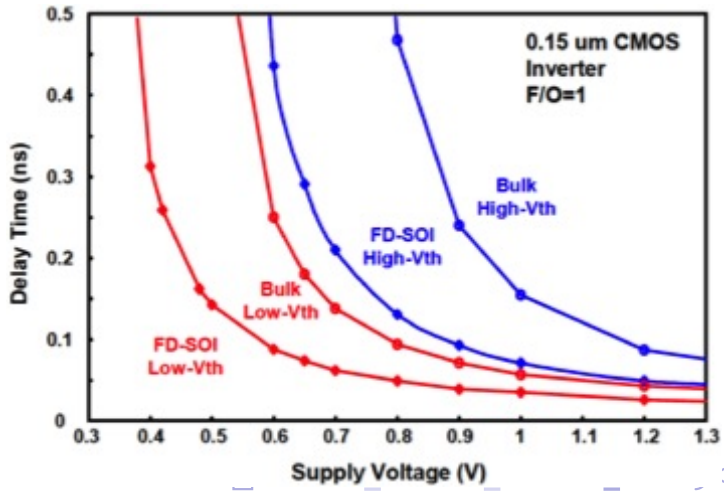
Tsi ~5-10nm (e/o process)
Tbox ~ 145nm / Tutbox ~ 10-30nm

Small Junction Capacitance

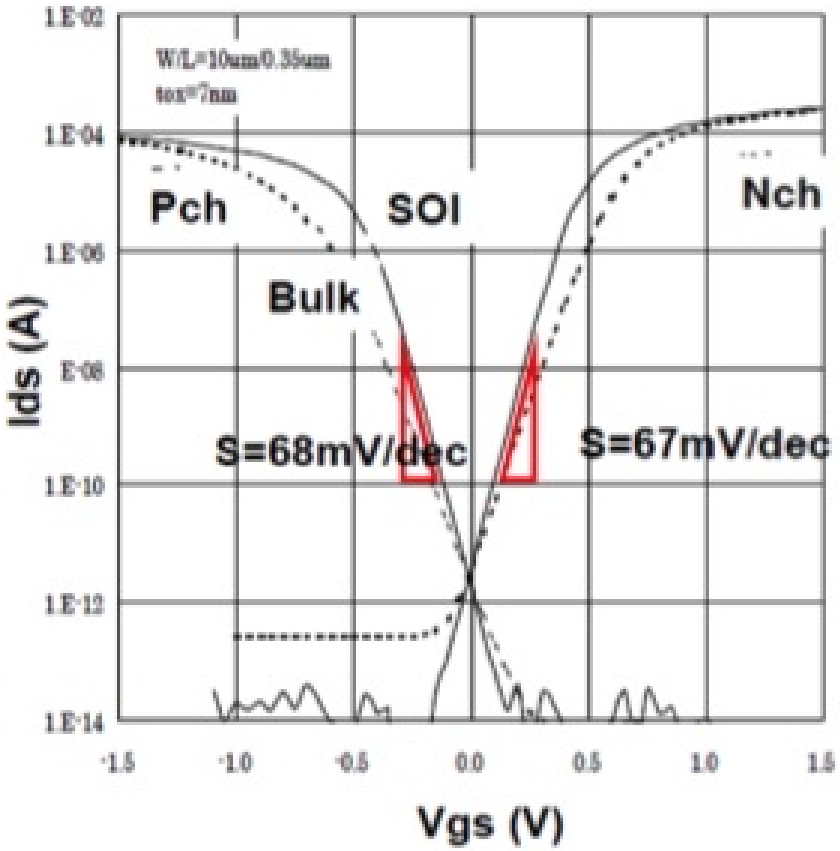


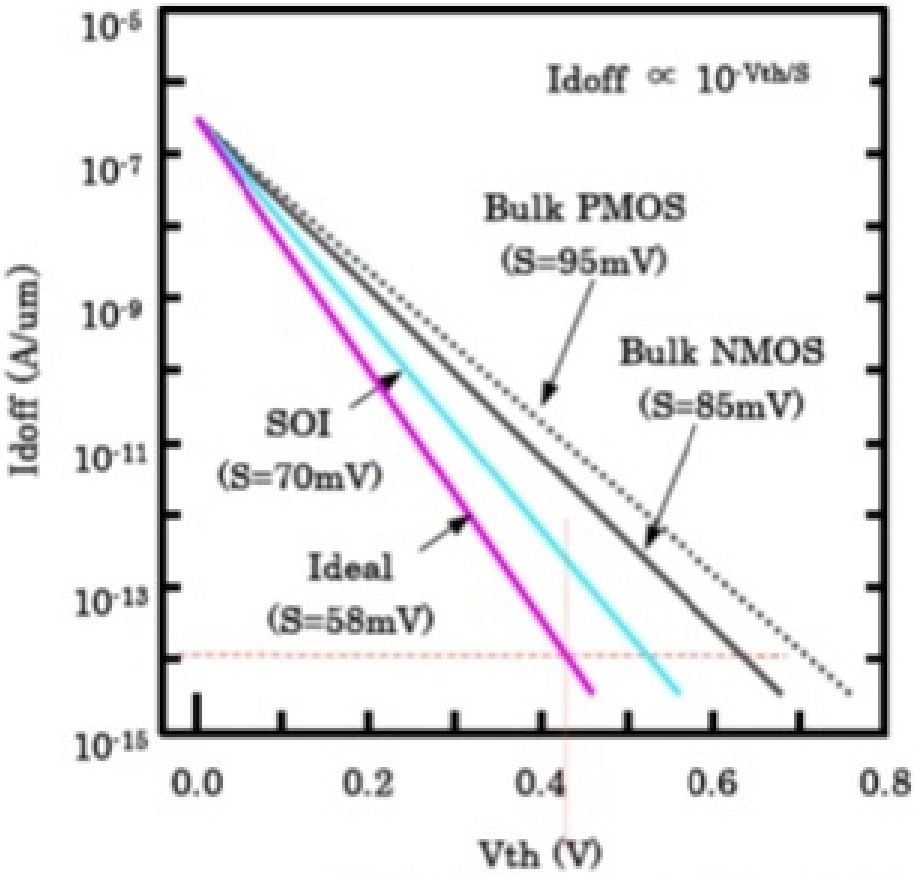


- Junction Capacitance in FD-SOI is $\sim \frac{1}{10}$ of bulk technology
- Gate capacitance is 30-40% lower
- higher speeds



Low power consumption

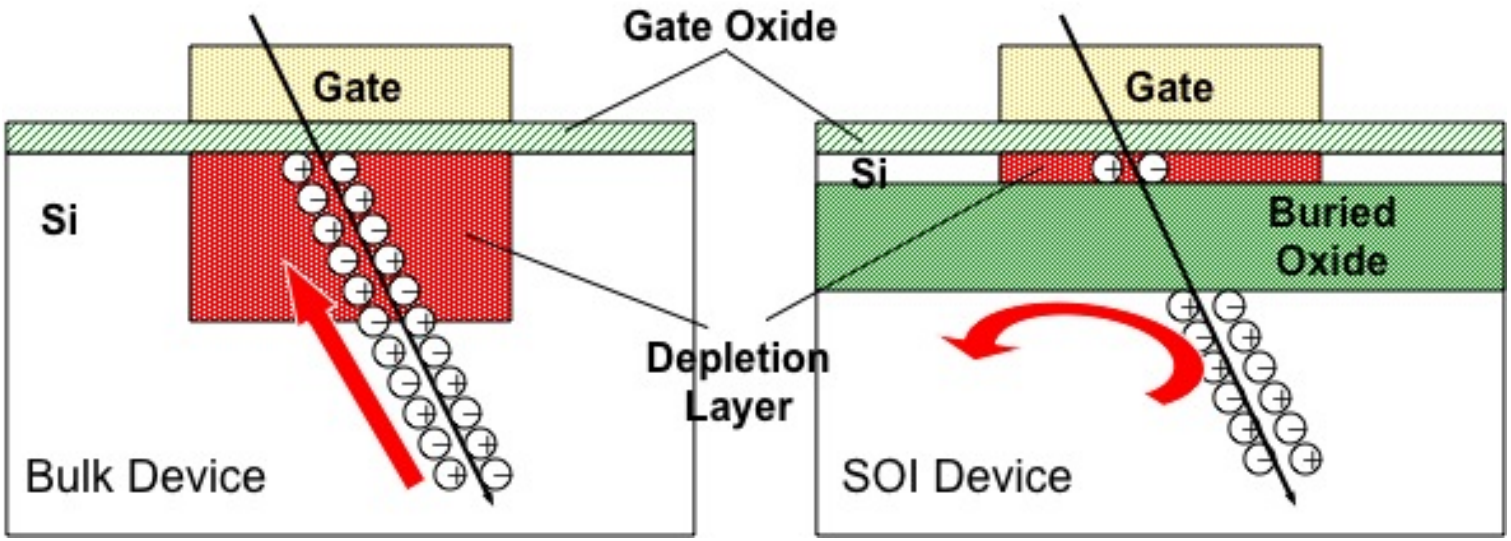




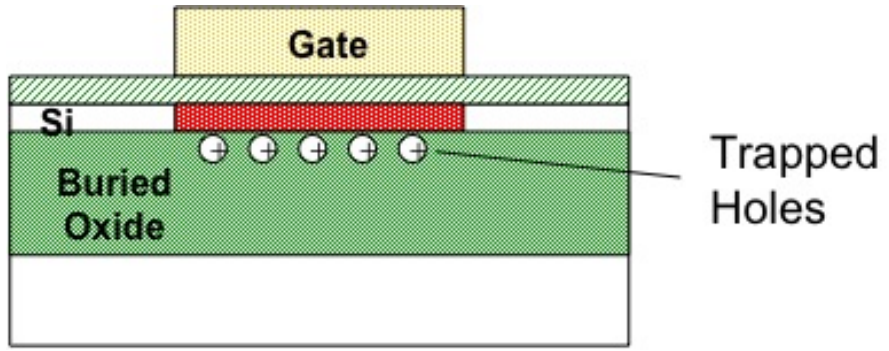
- Gate voltage is not wasted to deplete the bulk.
- Lower Threshold is possible without increasing Leakage Current.

Radiation Tolerance

SOI is immune to Single Event Effect:

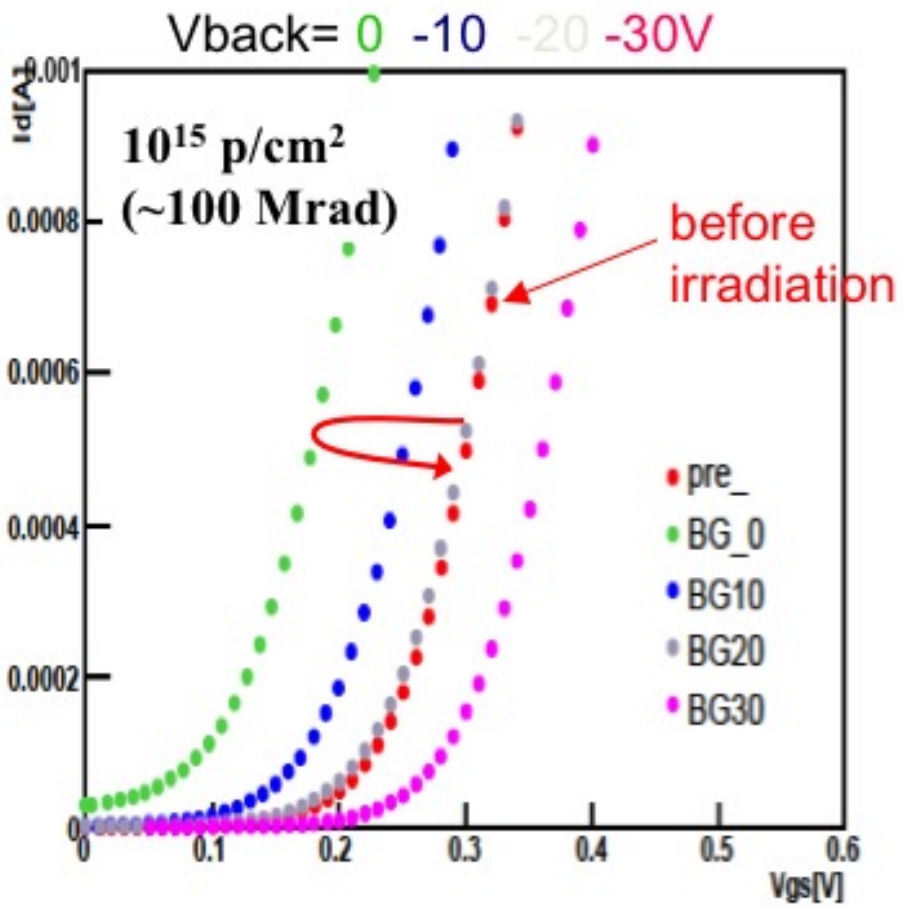


but not necessary strong to total ionization dose due to the thick BOX layer



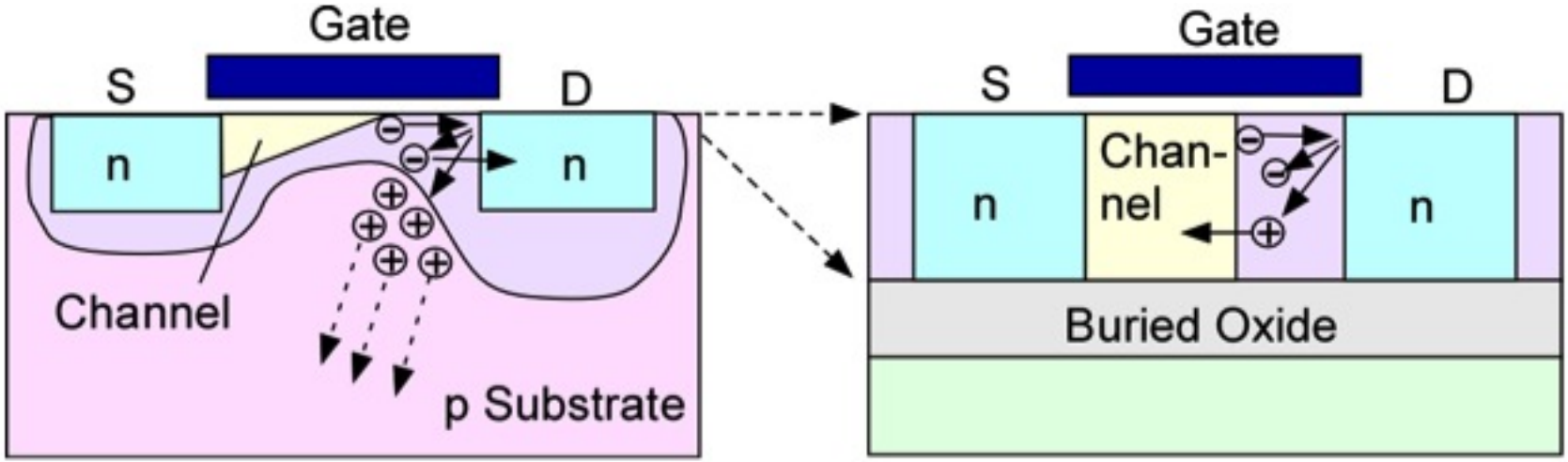
TID Damage Compensation

- V_{th} can be changed polarising back plane
- Leak current and V_{th} resumes to nearly original value by biasing back side



Standard SOI wafer
Only transistors on Top layer
No implants in Bottom layer

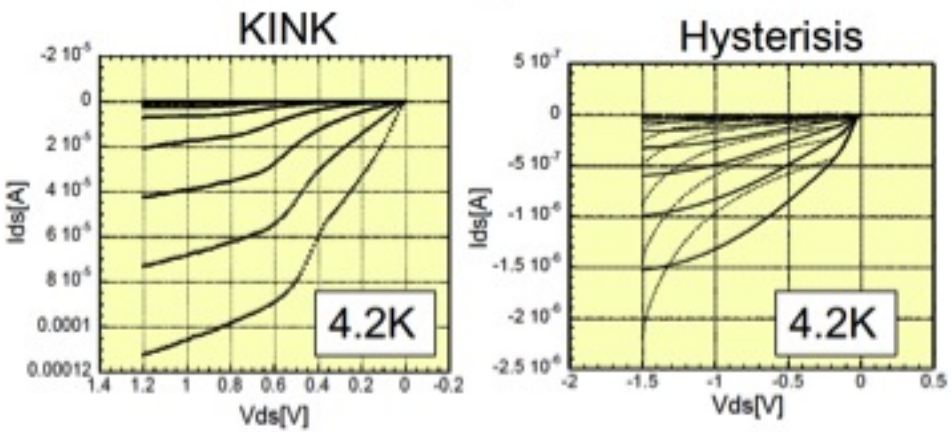
Operation at Cryogenic Temperature

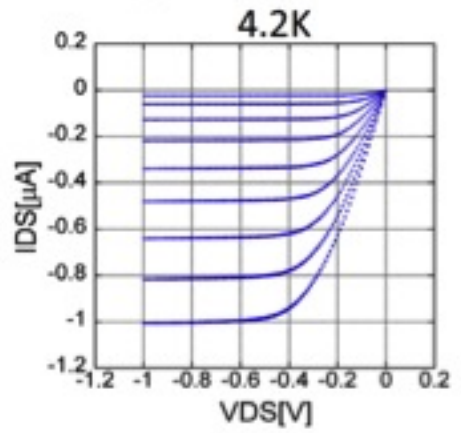


Bulk MOS

4.2K

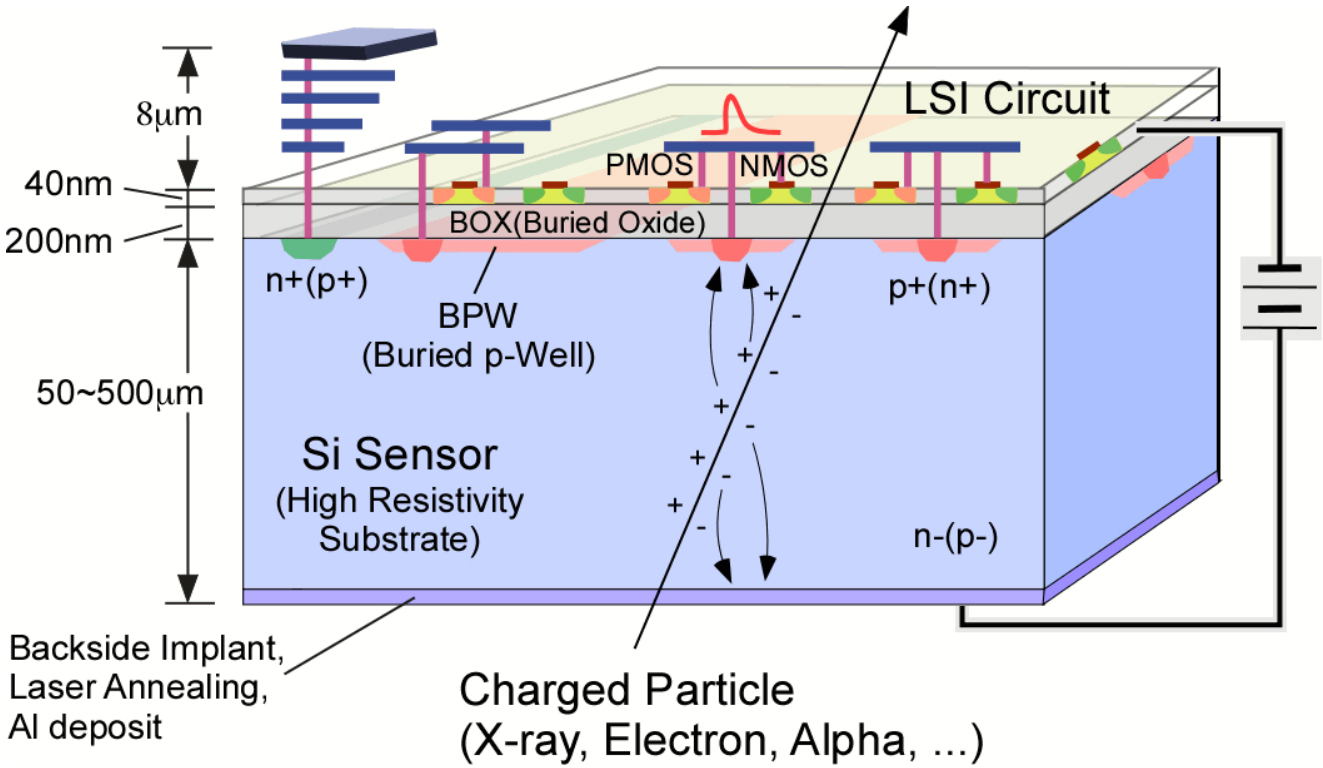
SOI MOS





SOI Monolithic Detector

- Use SOI wafer to develop monolithic detector
  - Top active layer holds readout electronics
  - Bottom handle wafer (HR) contains sensor
  - Middle silicon oxide layer insulates the electronics from the sensor
- Depletion voltage applied to the sensor in handle wafer



SOI features

- No mechanical bonding.
  - Semiconductor process only: high reliability, low cost are expected.
  - Less material that reduces multiple scattering
  - No bump pads and smaller pixel sizes possible
- Fully depleted thick sensing region with low sense node capacitance $\rightarrow$ large conversion gain and low noise operation are possible
- Full CMOS circuitry can be implemented on each pixel
- SEE cross section are very small. Latch-up mechanism, which destroys conventional bulk CMOS LSI, is absent.
- Can be operated in wide temperature (1K-570K) range,
- Based on Industry Standard Technology.
- Emerging 3D integration techniques are a natural extension of the technology.

3. SOIPIX project
   - SOIPIX collaboration
   - SOIPIX technology
   - SOI Issues
   - Buried p-Well
   - Double SOI
   - Nested Well
   - 3D Integration

SOIPIX collaboration

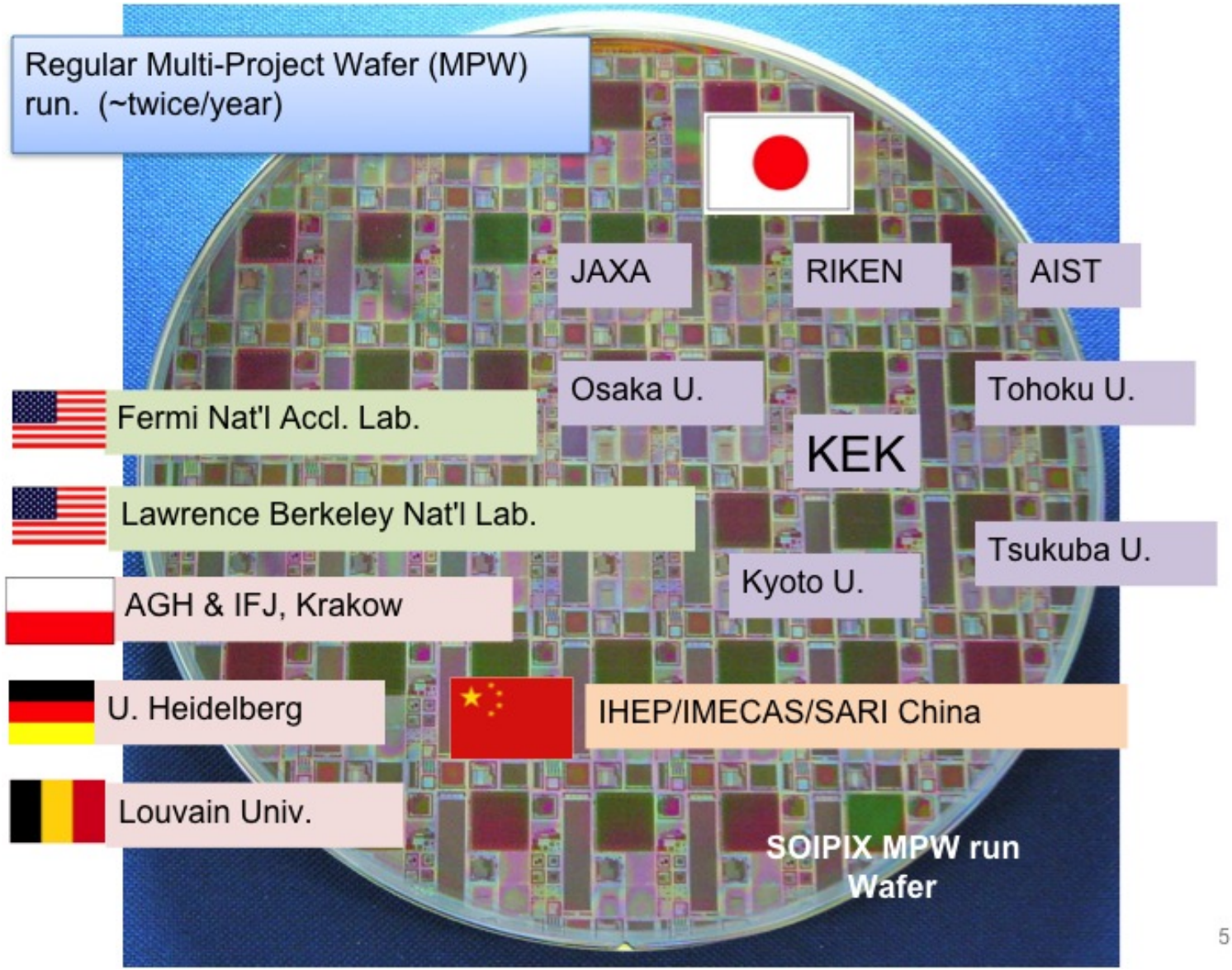
- R&D collaboration aiming to study the feasibility of using SOI technology as a radiation detector

  `http://rd.kek.jp/project/soi/`

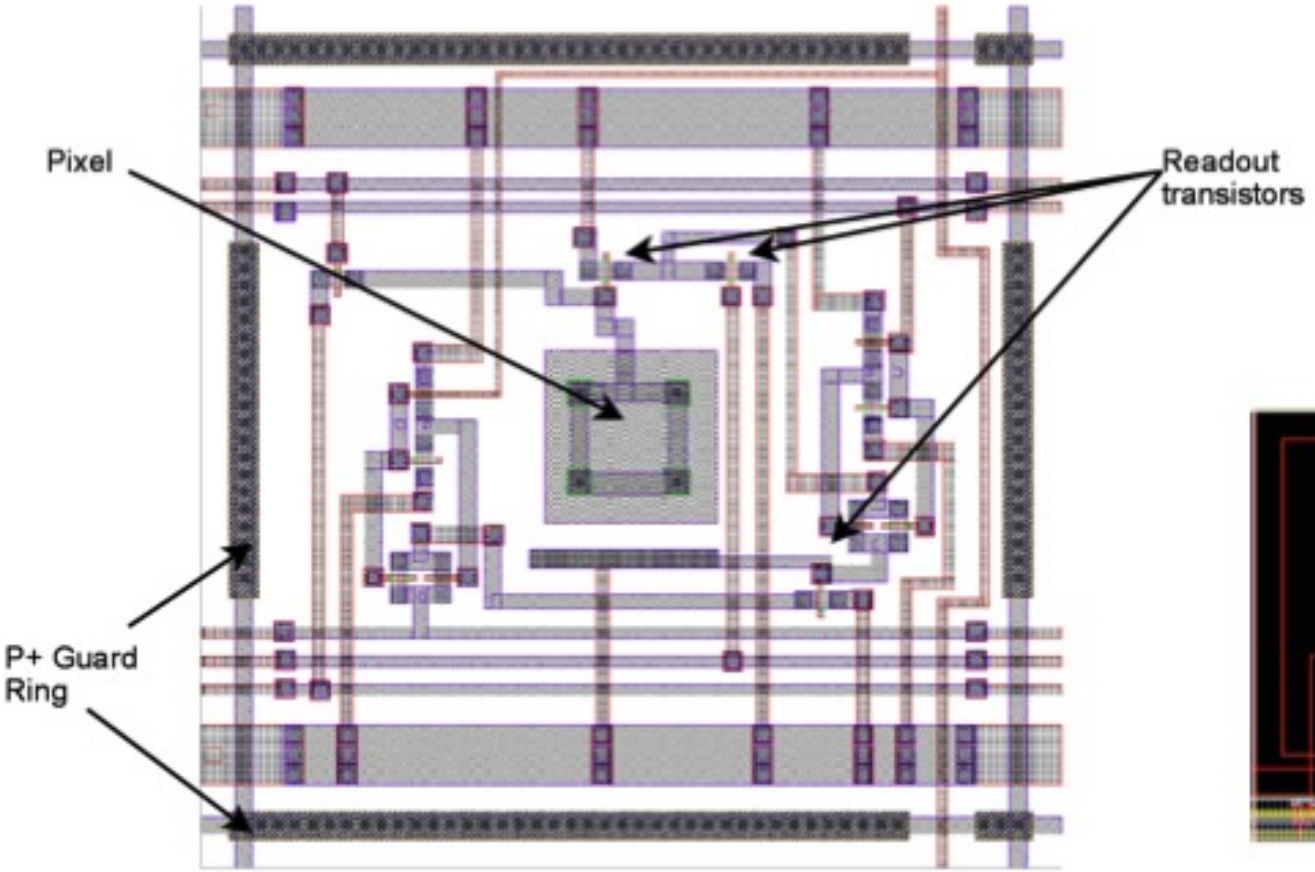
- Close collaboration with Lapis Semiconductor Co (former OKI Semiconductor Co)
  - Industrial partnership essential to develop new techniques
  - Privileged relation with KEK
  - At the origin of most of the technological advancements in this project

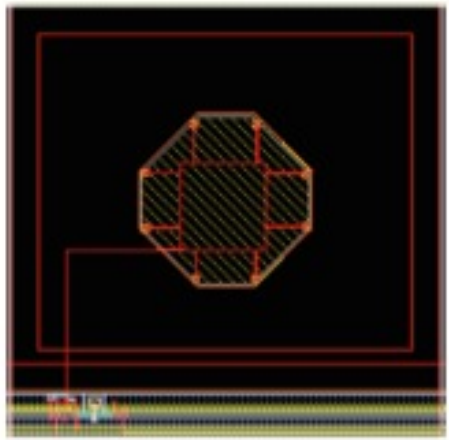
- Lapis 0.2μm FD-SOI

SOIPIX - MPW


Regular Multi-Project Wafer (MPW) run. (~twice/year)
JAXA
RIKEN
AIST
Osaka U.
Tohoku U.
Fermi Nat'l Accl. Lab.
KEK
Lawrence Berkeley Nat'l Lab.
Tsukuba U.
Kyoto U.
AGH & IFJ, Krakow
U. Heidelberg
IHEP/IMECAS/SARI China
Louvain Univ.
SOIPIX MPW run
Wafer
5

Size and Technology matters



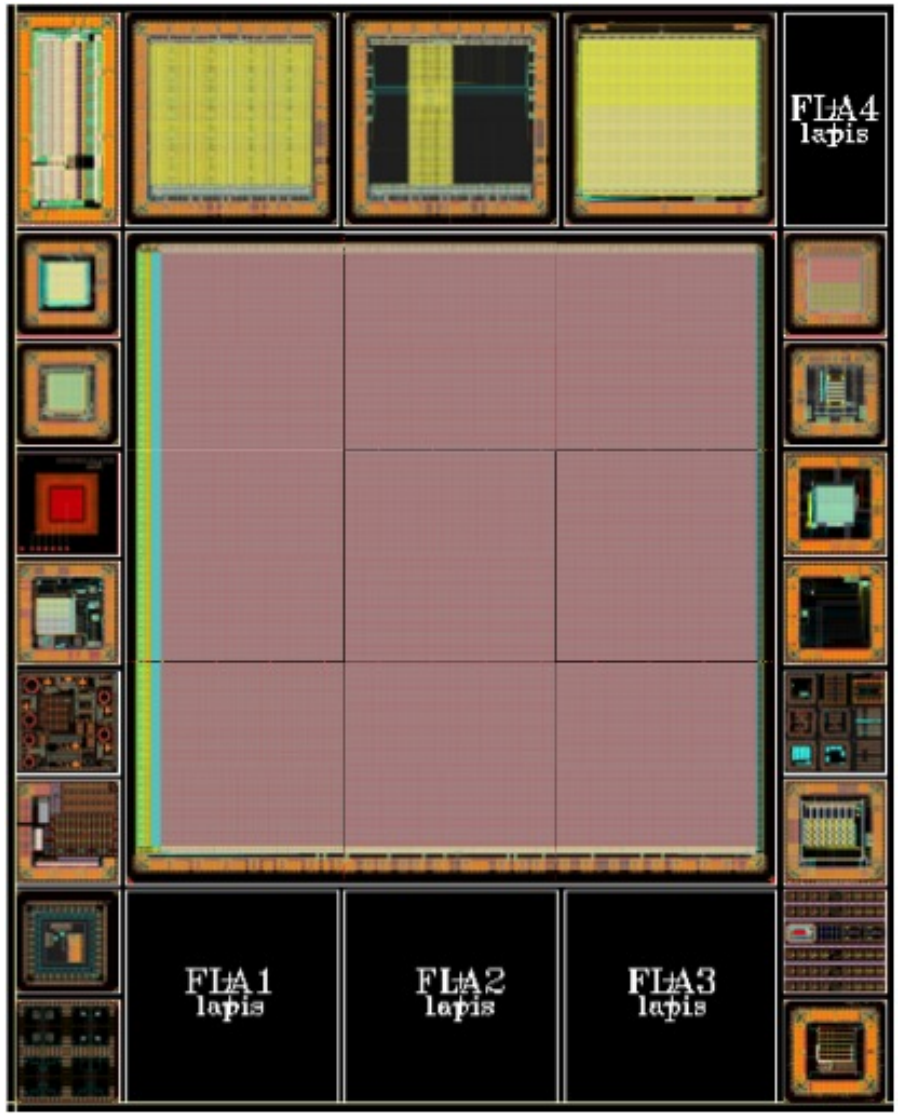


WINFAB (2 μm)
1 metal layer + 1 poly

LAPIS (0.2μm)
5 metal layers + 1 poly

SOIPIX - Mask

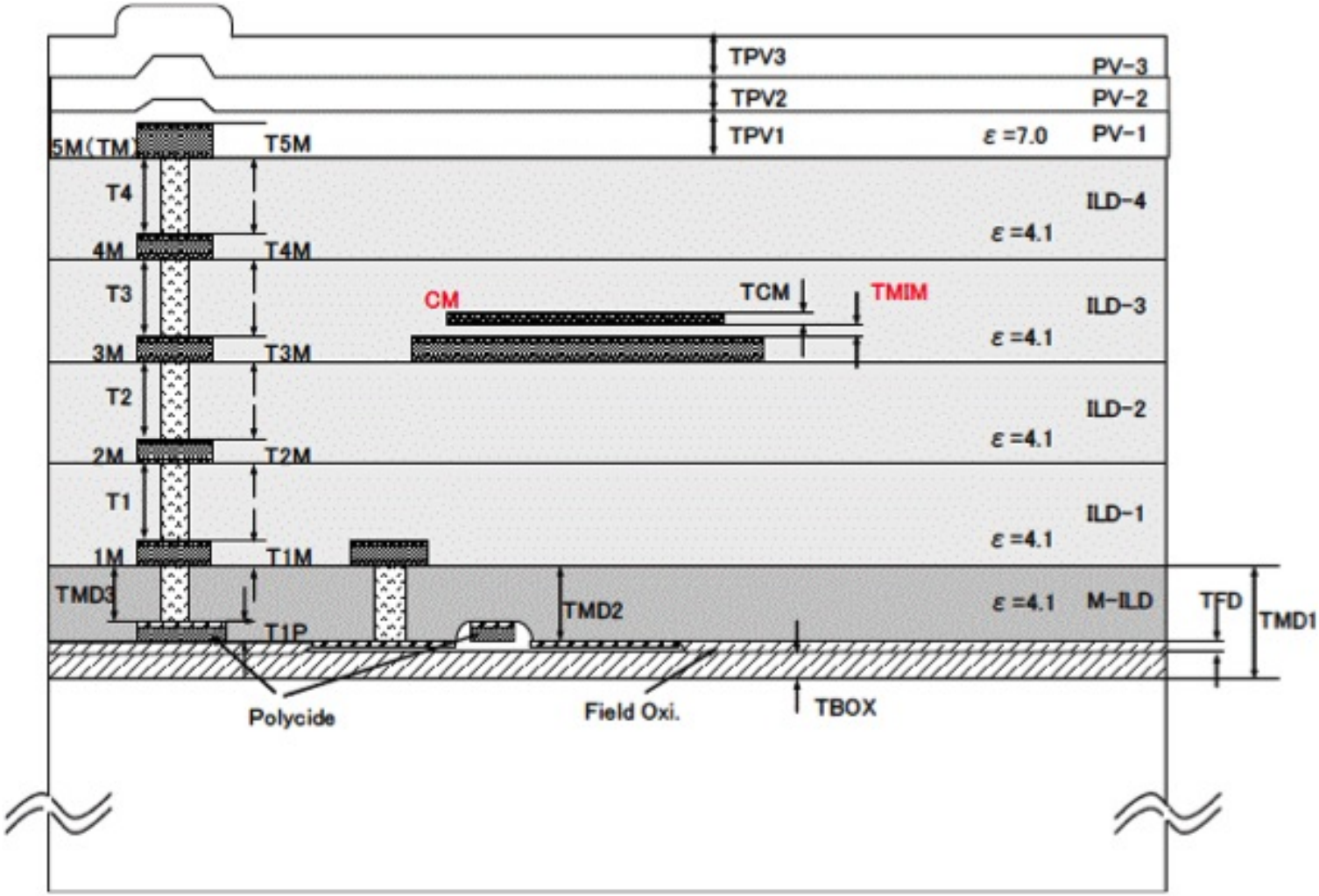
- Mask size: 24.6mm x 30.8mm
- Smallest chip area: 2.9mm x 2.9mm
- I/O structures available



Lapis 0.2μm FD-SOI Pixel Process

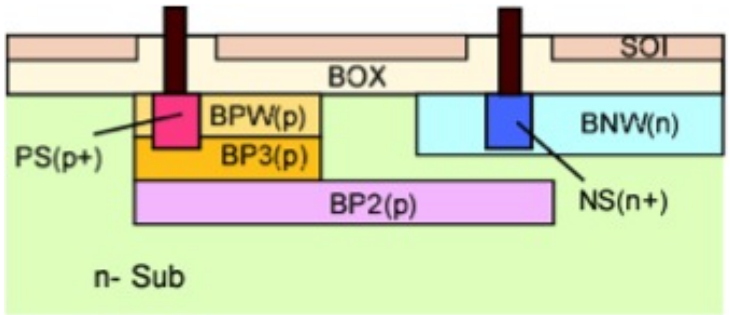
Process	0.2 μm low-leakeage FD SOI CMOS 1 Poly, 5 Metal layers MIM Capacitor (1.5 fF/μm^2), DMOS Core (I/O) Voltage = 1.8 V (3.3 V)
SOI wafer	Diameter: 200 mm; 720 μm thick Top Si: Cz $\sim$18 Ω-cm, p-type, $\sim$40 nm thick Buried Oxide: 200 nm thick Handle wafer: Cz(n)$\sim$700Ω-cm FZ(n)$\sim$7kΩ-cm FZ(p)$\sim$25kΩ-cm
Backside	Thinned to 100-500 μm mechanical grinding, chemical etching Back side implant, laser annealing and Al plating (200 nm)
Transistors	Normal and low threshold transistors for both core and IO Three structures: body floating, source-tie and body-tie

SOI process: Top Si

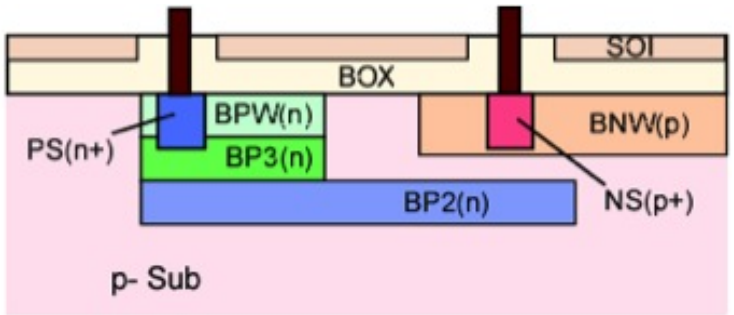


SOI process: Bottom Si

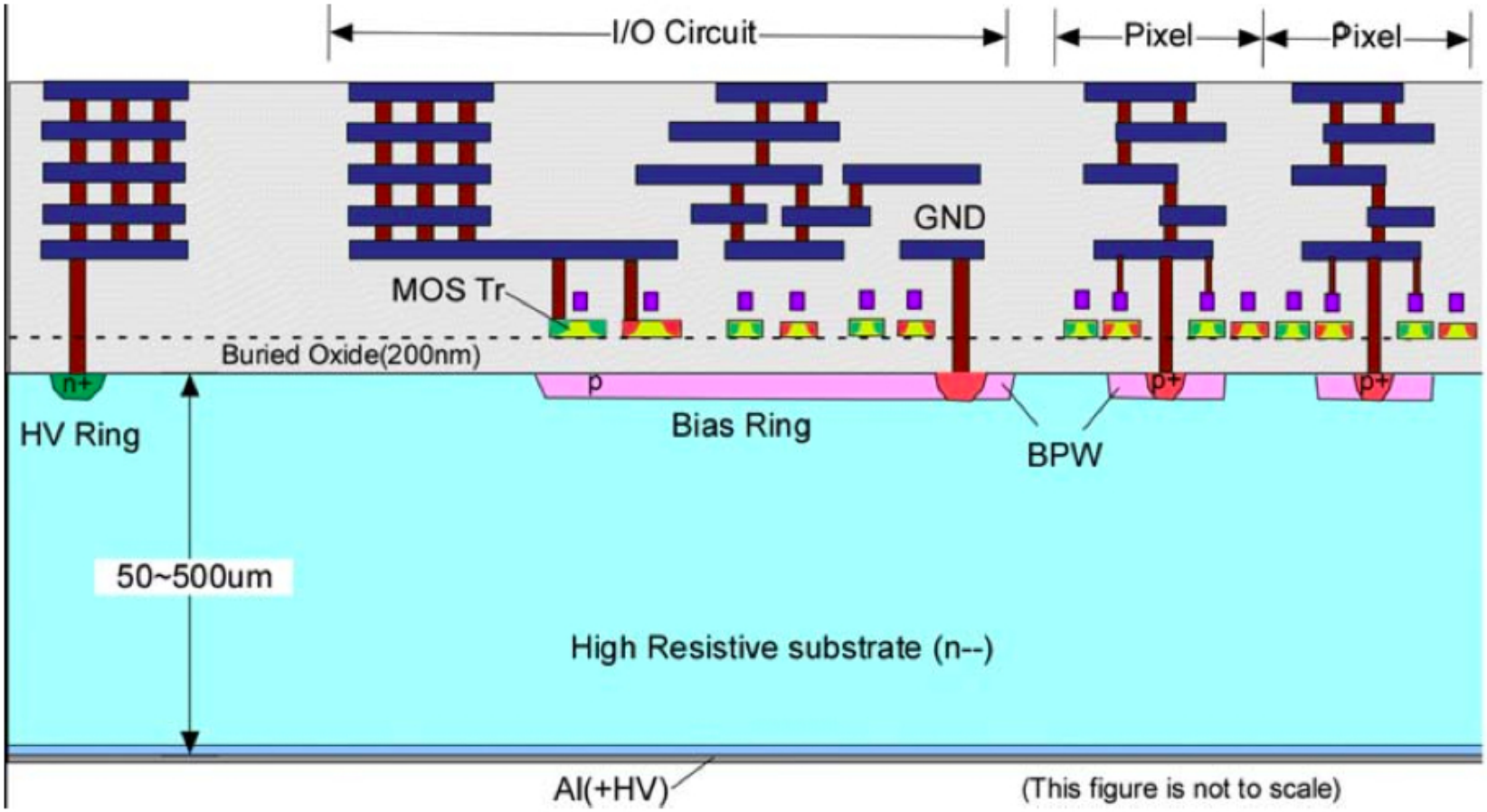
- Implants (PS,NS) high density layer (Open Top Si and BOX)
- Buried wells (BPW,BP2,BP3,BNW) low density buried layer
- For p-type substrate, dopants are changed to create reverse polarity by using the same mask layers.
- Doping density and depth can be changed on request



Normal Process for n- substrate

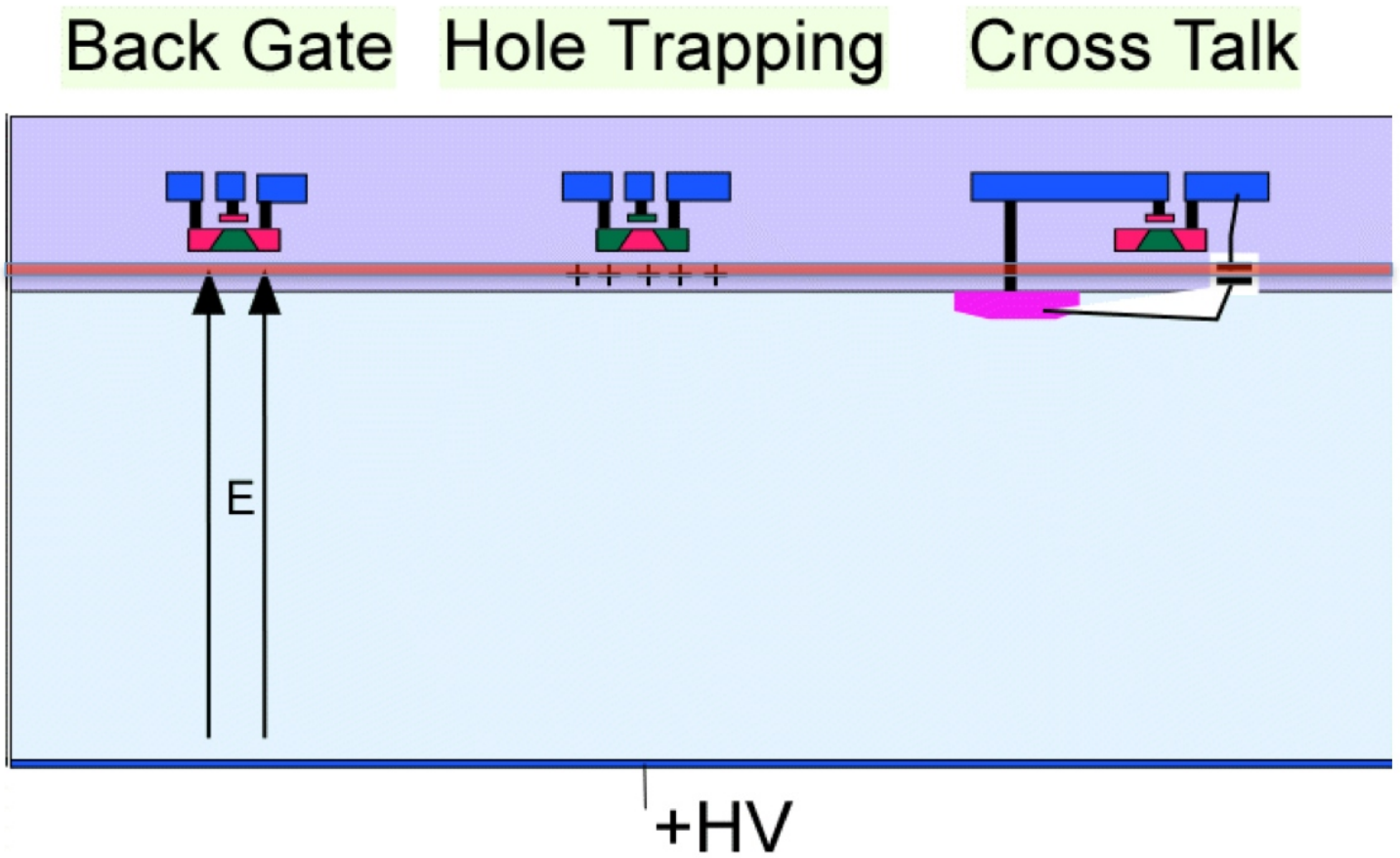


Reverse Process for p- substrate


I/O Circuit
Pixel
Pixel
GND
MOS Tr
Buried Oxide(200nm)
n+
HV Ring
p
Bias Ring
p+
p+
BPW
50~500um
High Resistive substrate (n--)
Al(+HV)
(This figure is not to scale)

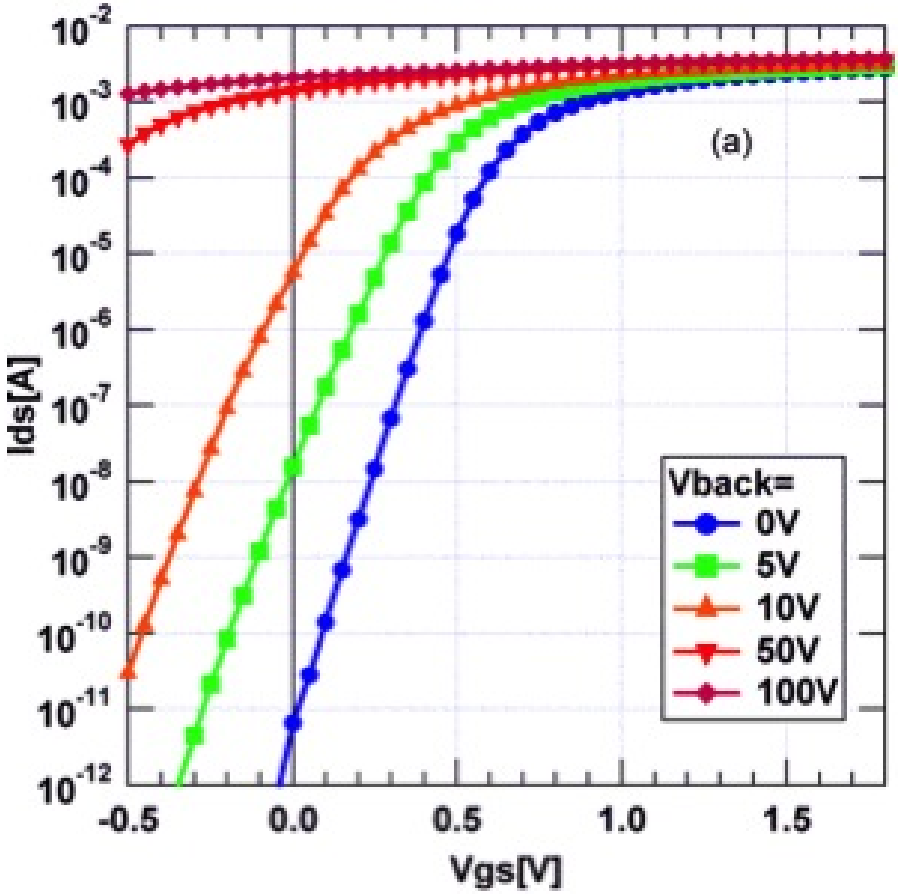
Issues in SOI pixel

Sensors and electronics are located very close.



Backgate effect

Since sensor and transistors are located very close (∼200 ns), transistors become ON when high voltage is applied to the sensor

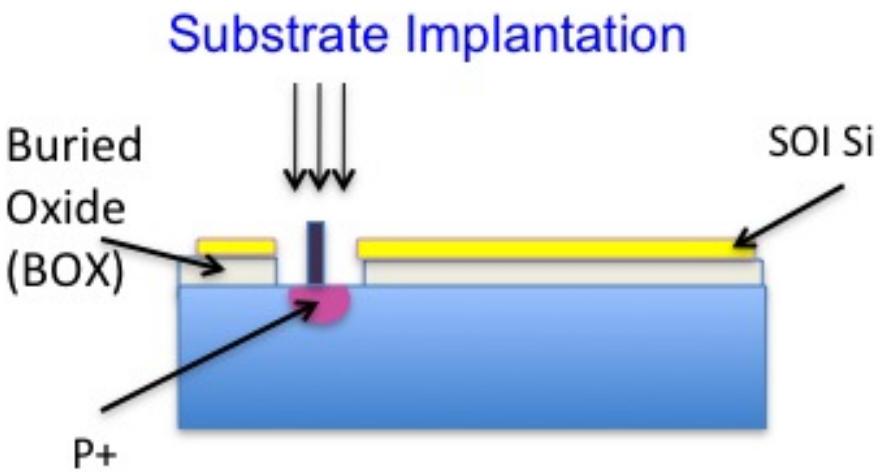


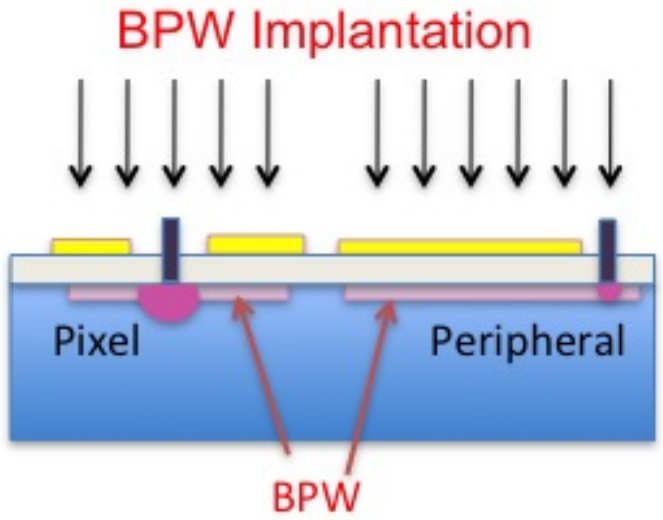
- Solution:

  Shield the electric field of the transistor from the sensor voltage

- Three shielding structures proposed so far:
  - Buried p-Well (BPW)
  - Double SOI (SOI2)
  - Nested Wells

Buried p-Well (BPW)



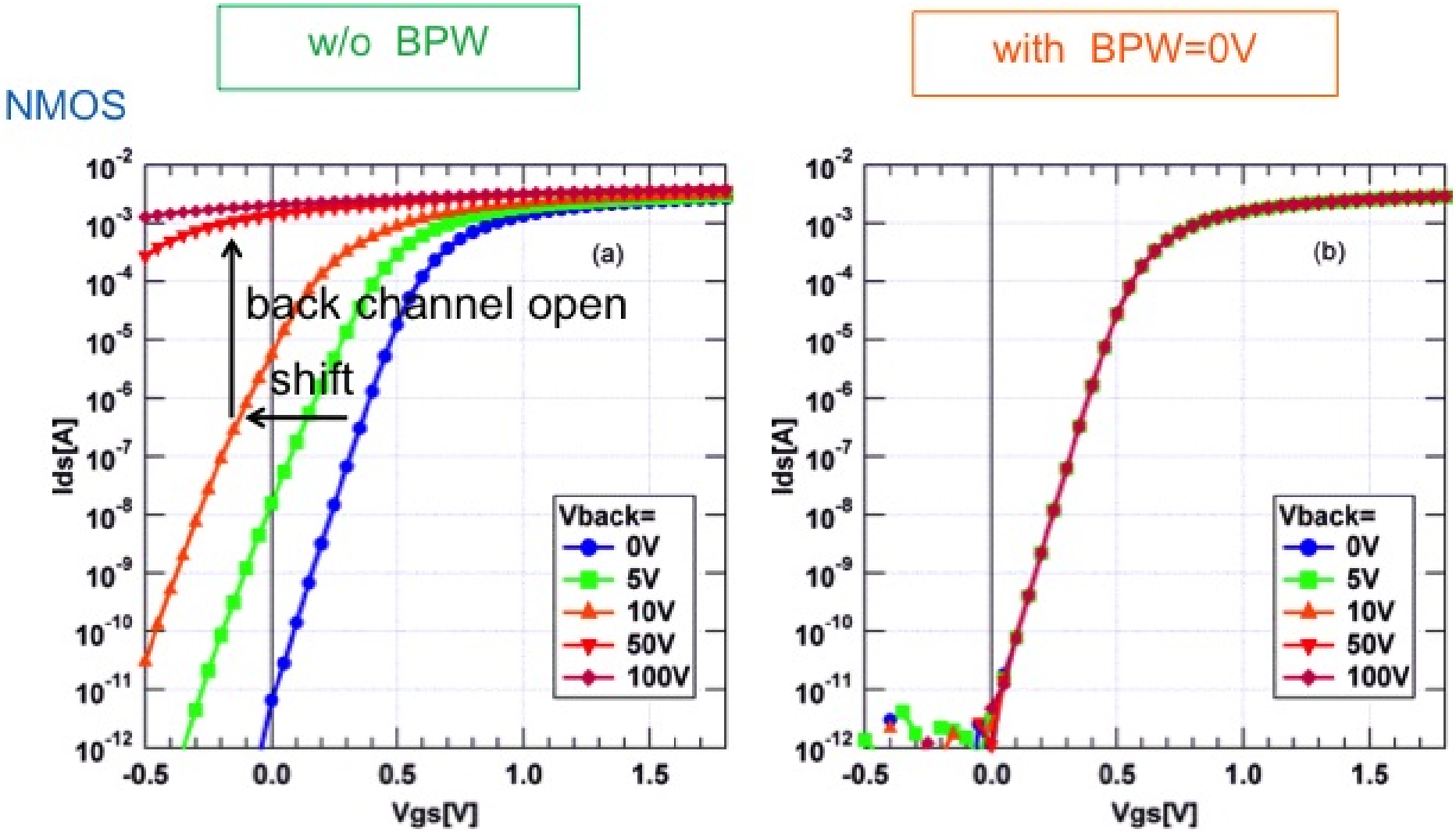


- Cut Top Si and BOX
- High Dose

- Keep Top Si not affected
- Low Dose

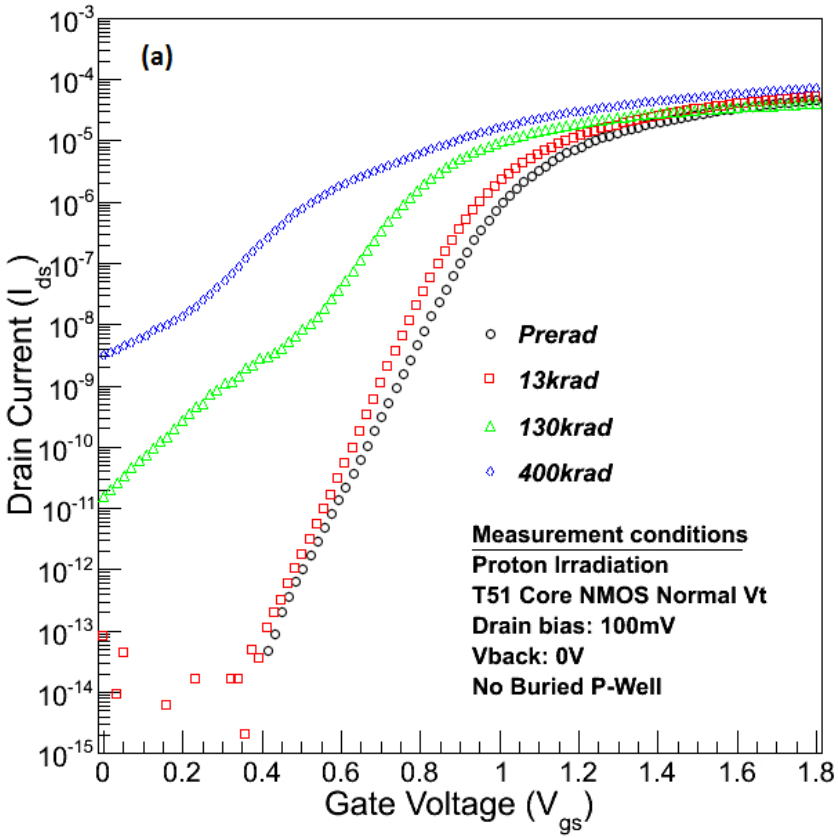
- Suppress the Back Gate Effect
- Shrink pixel size without loosing sensitive area
- Increase break down voltage with low dose region
- Less electric field in the BOX which improve radiation hardness

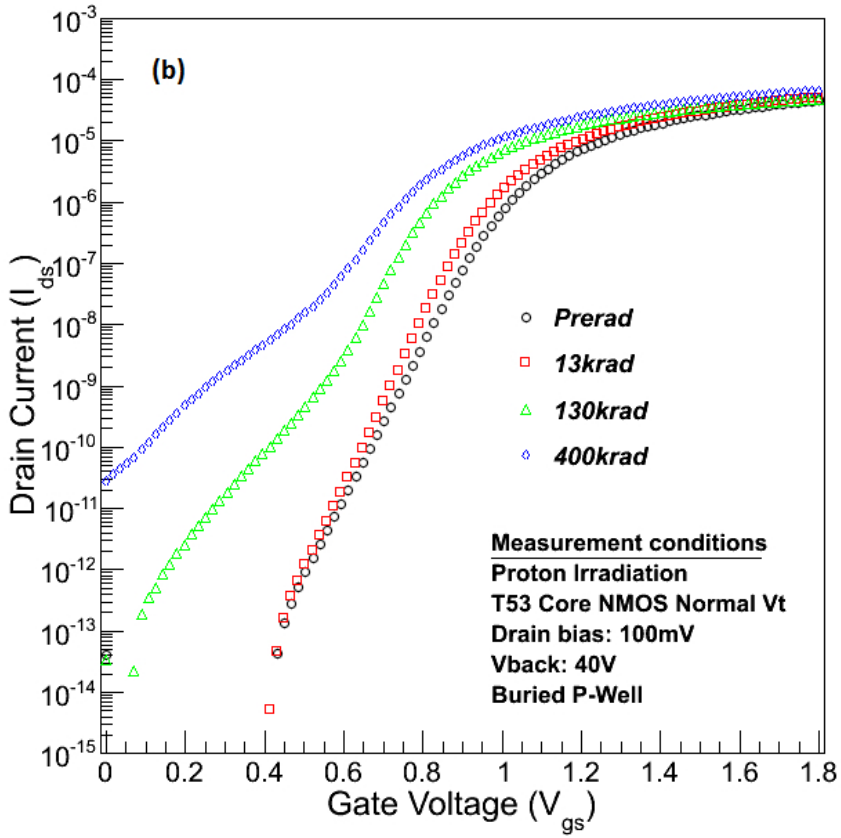
BPW: Back gate effect



BPW: radiation hardness

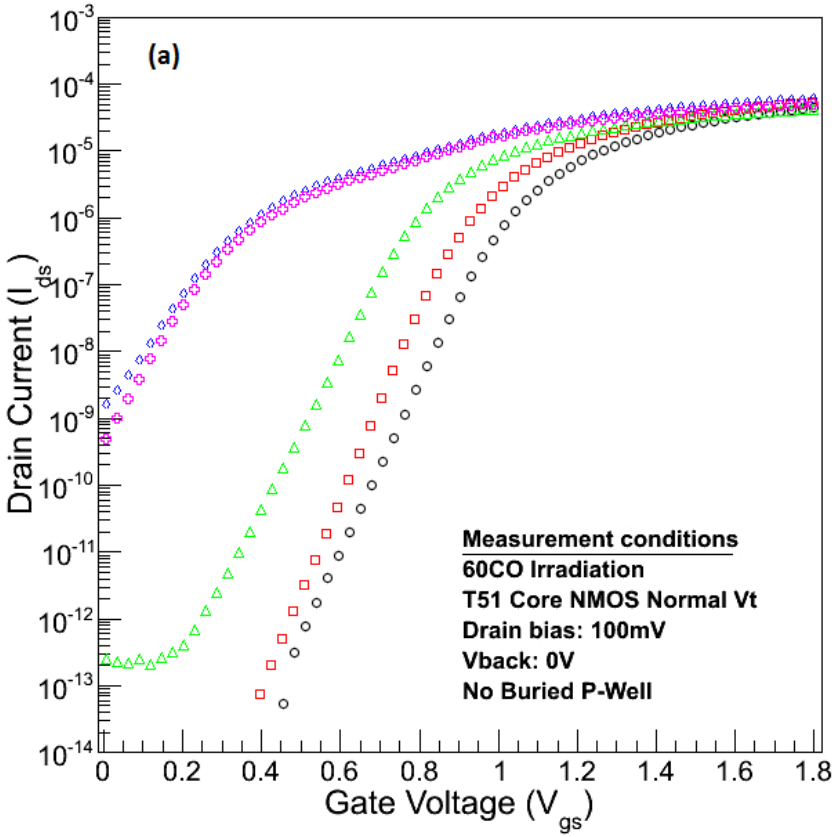
Irradiation with 60 MeV protons

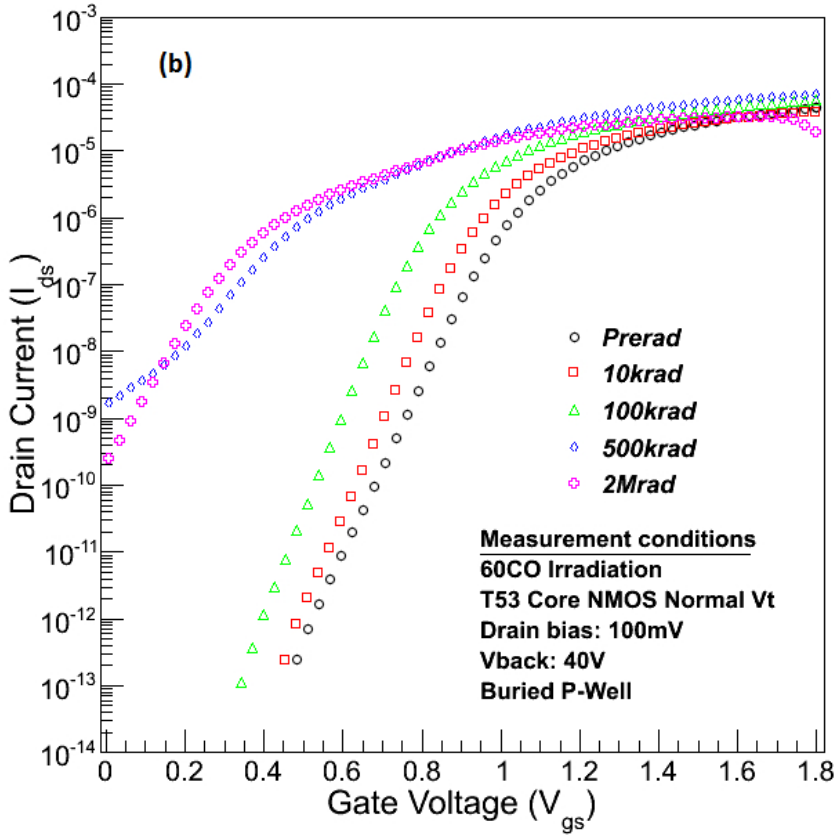




BPW: radiation hardness

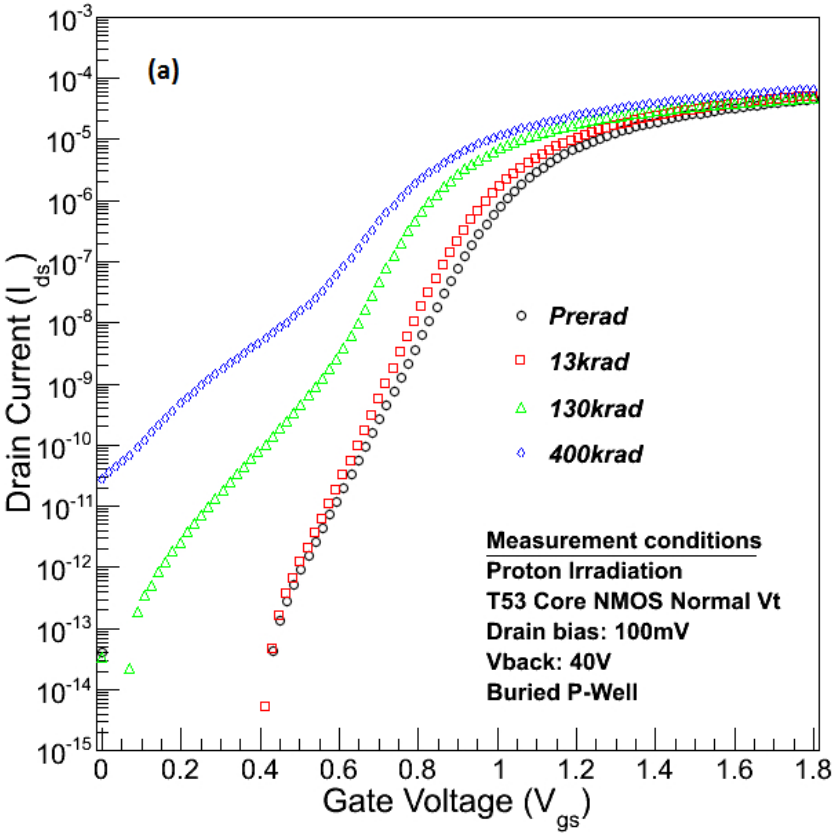
Irradiation with ^{60}Co

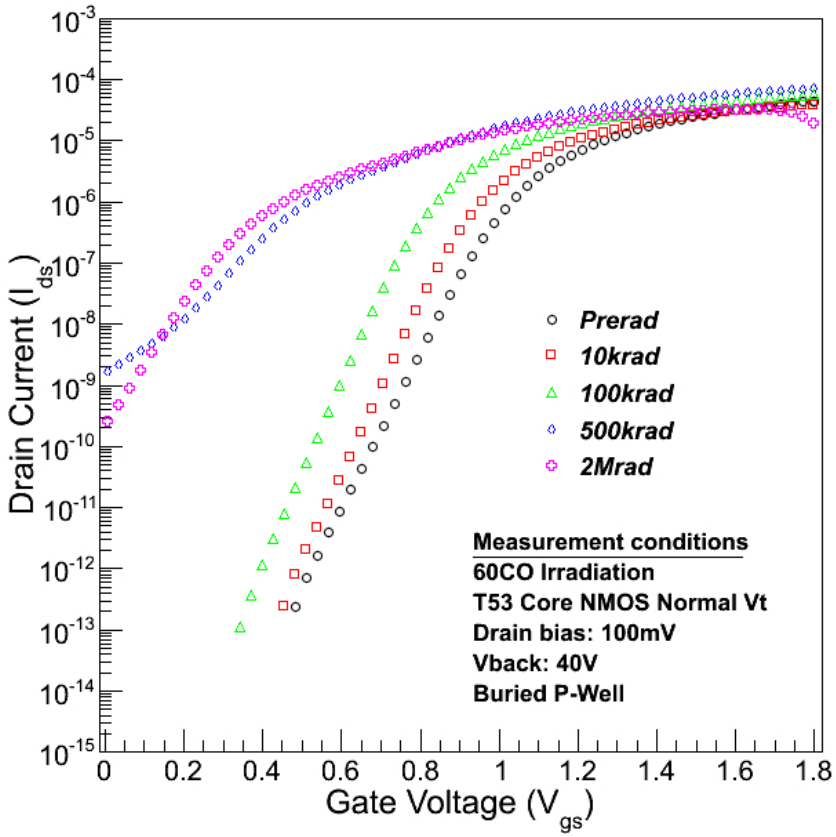




BPW: radiation hardness

Comparison 60 MeV protons and ^{60}Co



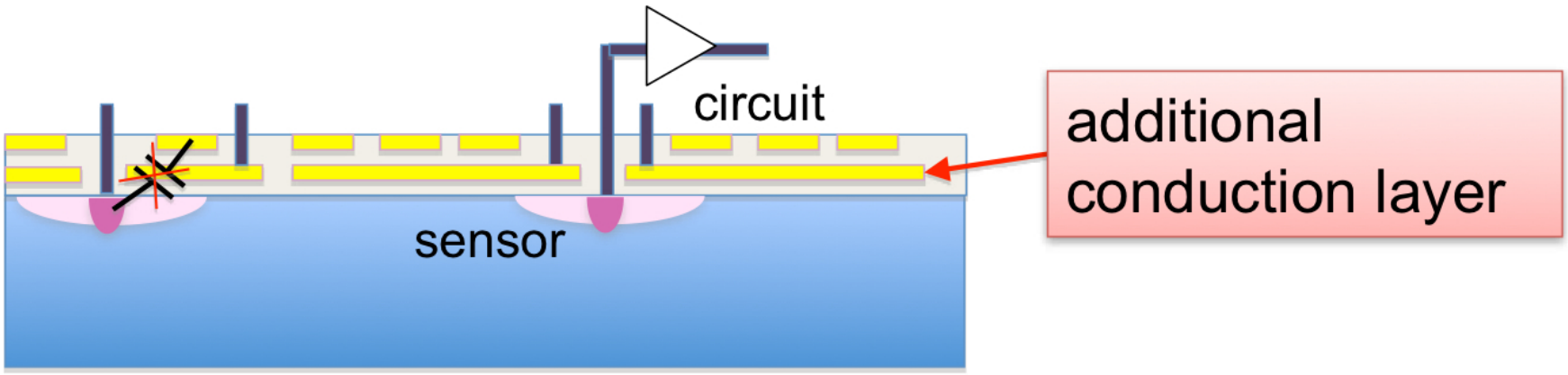


BPW summary

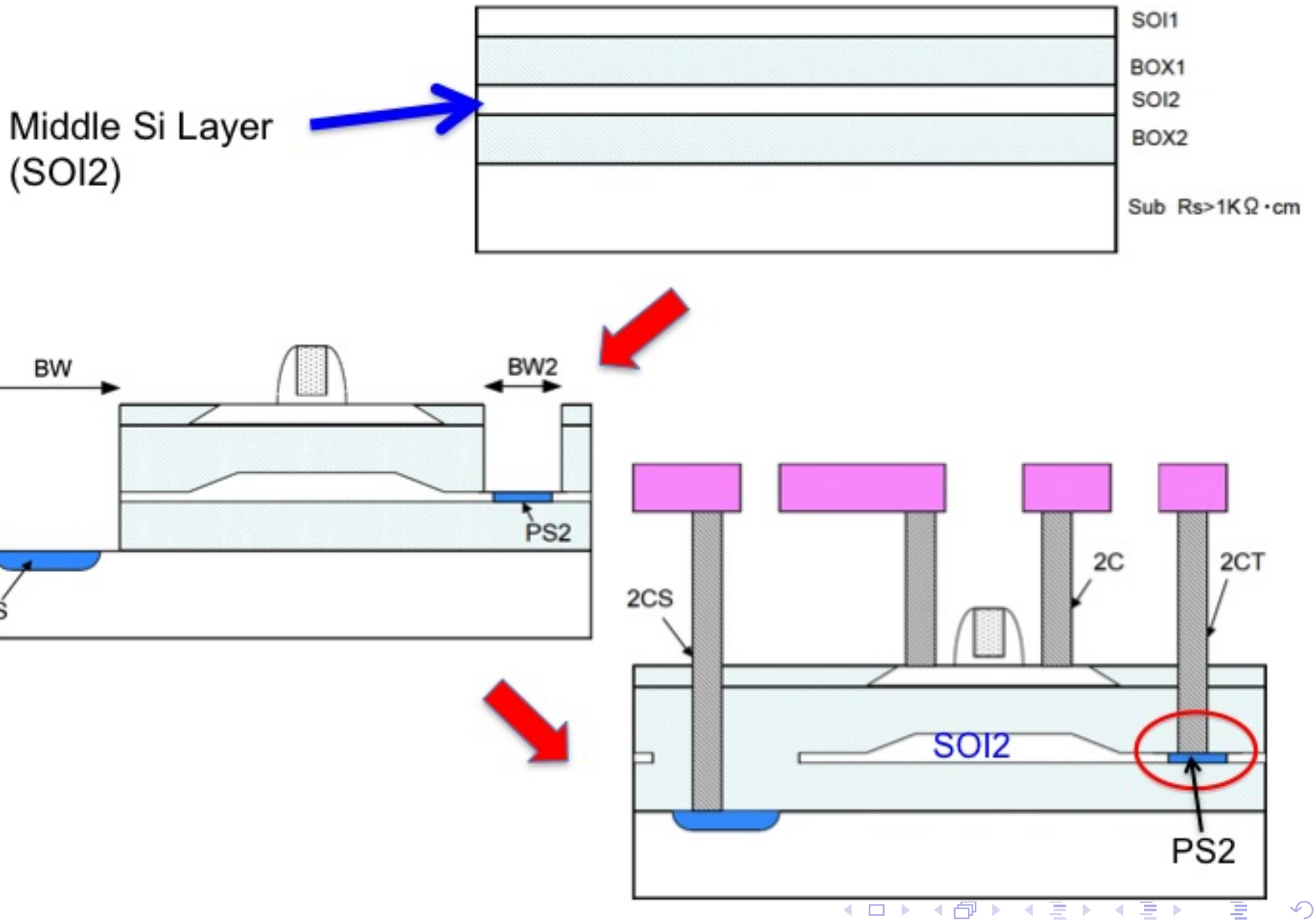
- BPW protects for backgate effect
- BPW does not protect for hole trap in BOX
- No possibility to compensate the generated electric field

Double SOI

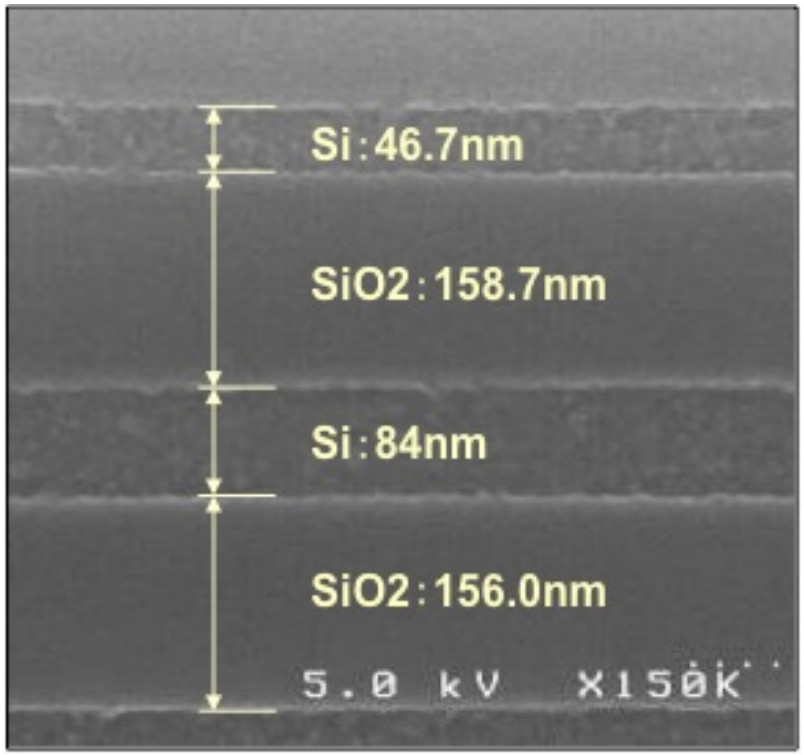
- Shield transistors from bottom electric field
- Compensate electric field generated by the trapped hole in the BOX.
- Reduce crosstalk between sensors and circuits.

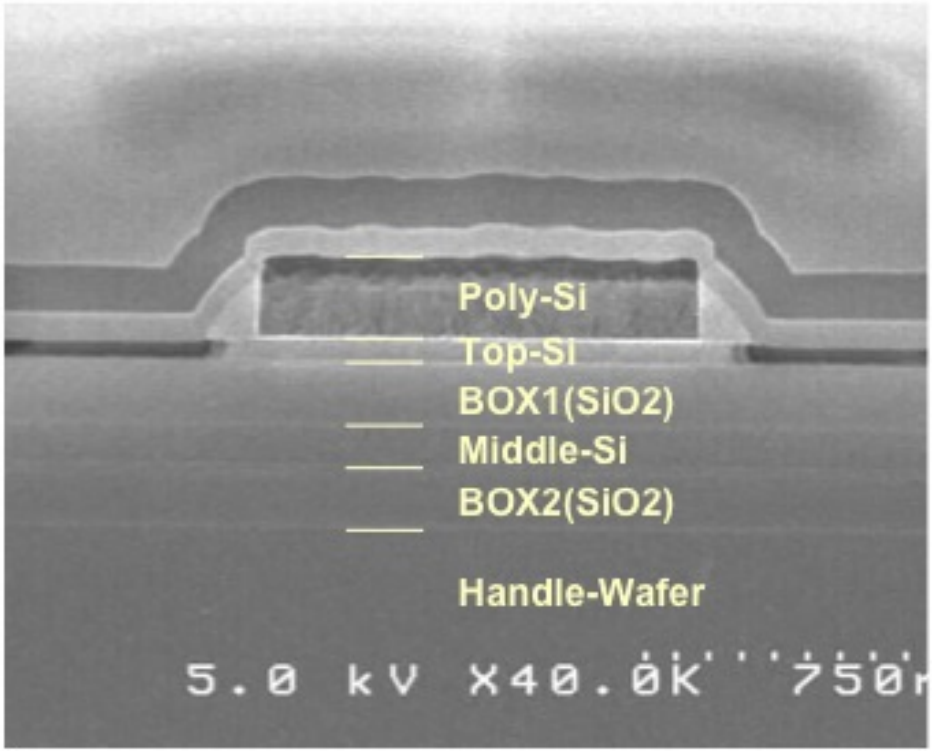


Double SOI Process



SOI2 - SEM



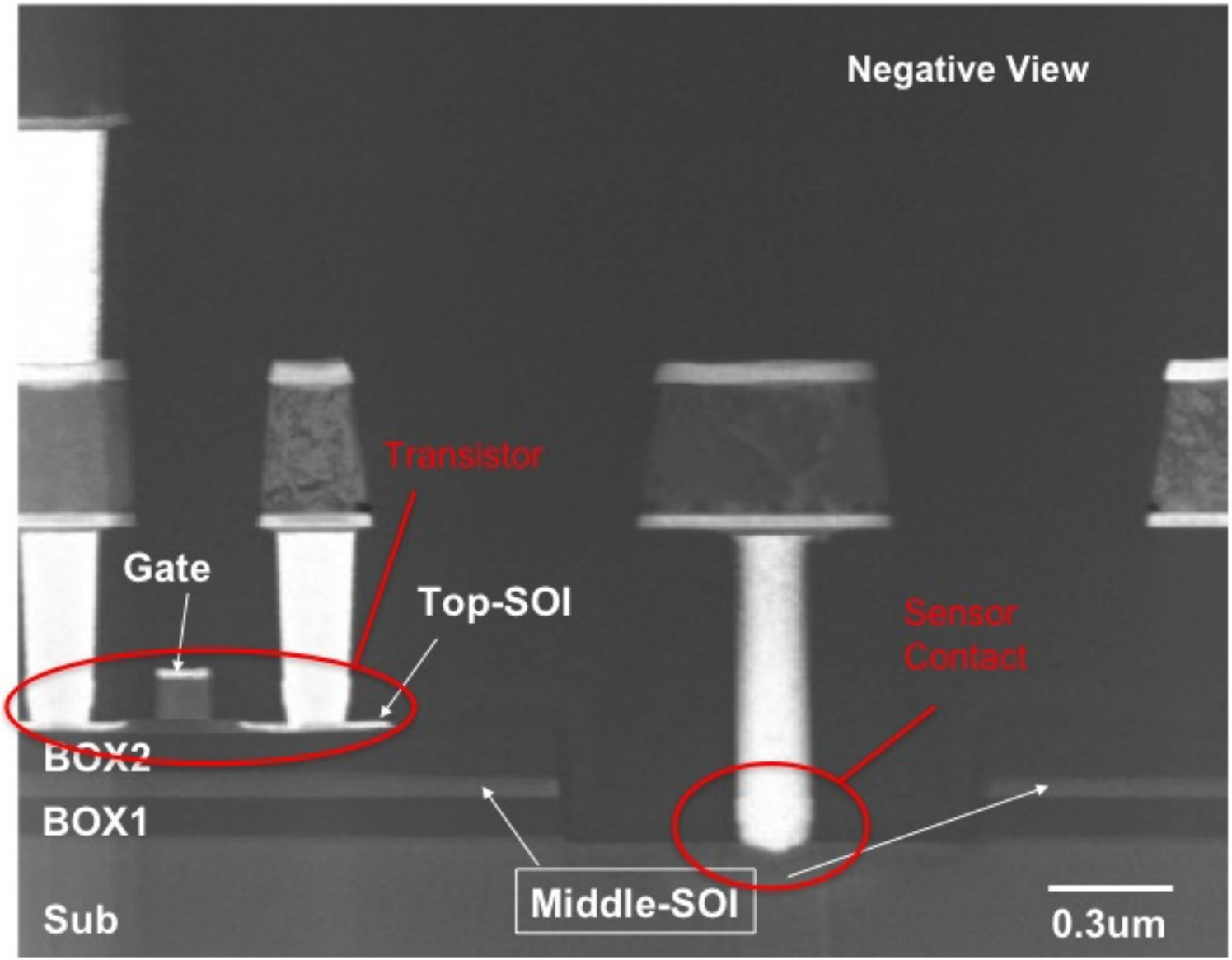


Resistivity of the middle Si is ∼10 Ω-cm

with $CoSi_2$: ∼170 kΩ/□

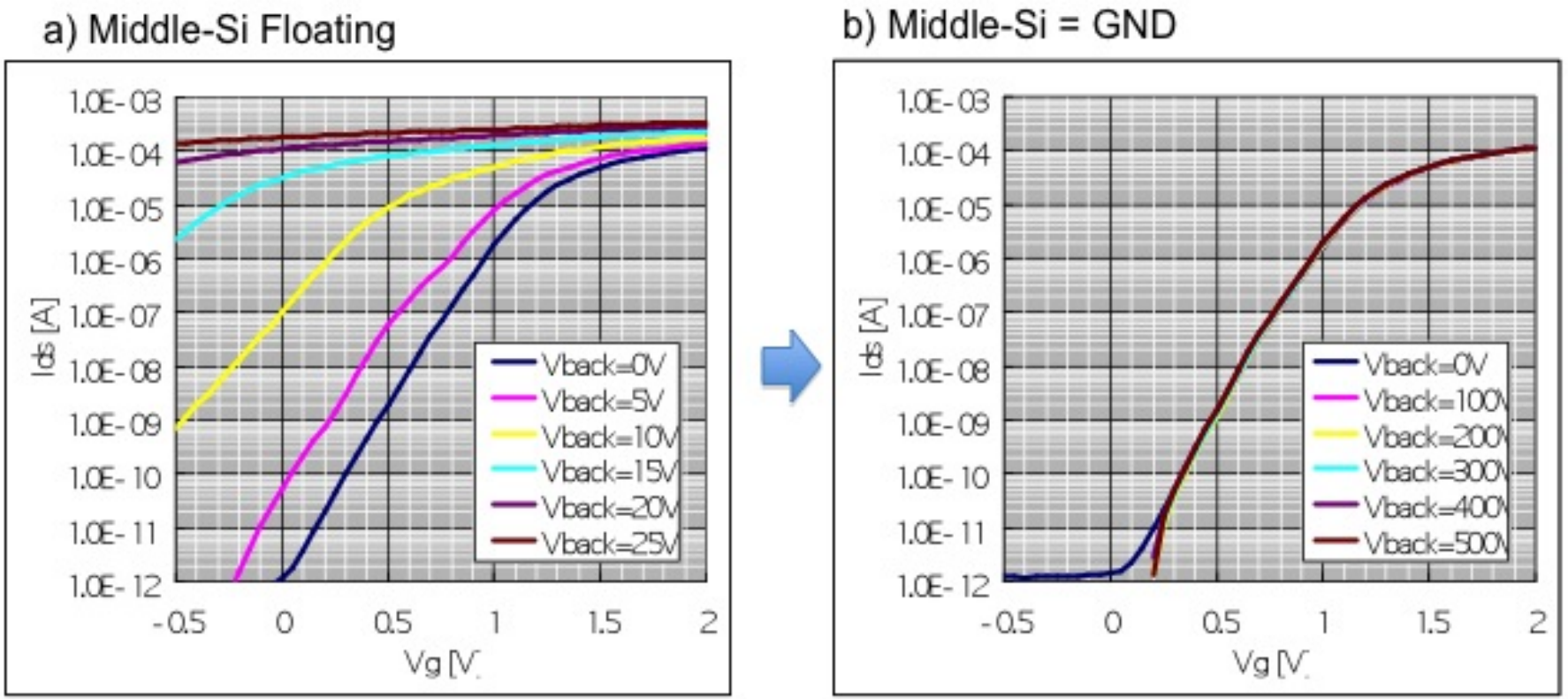
w/o $CoSi_2$: ∼1 MΩ/□

SOI2 - SEM

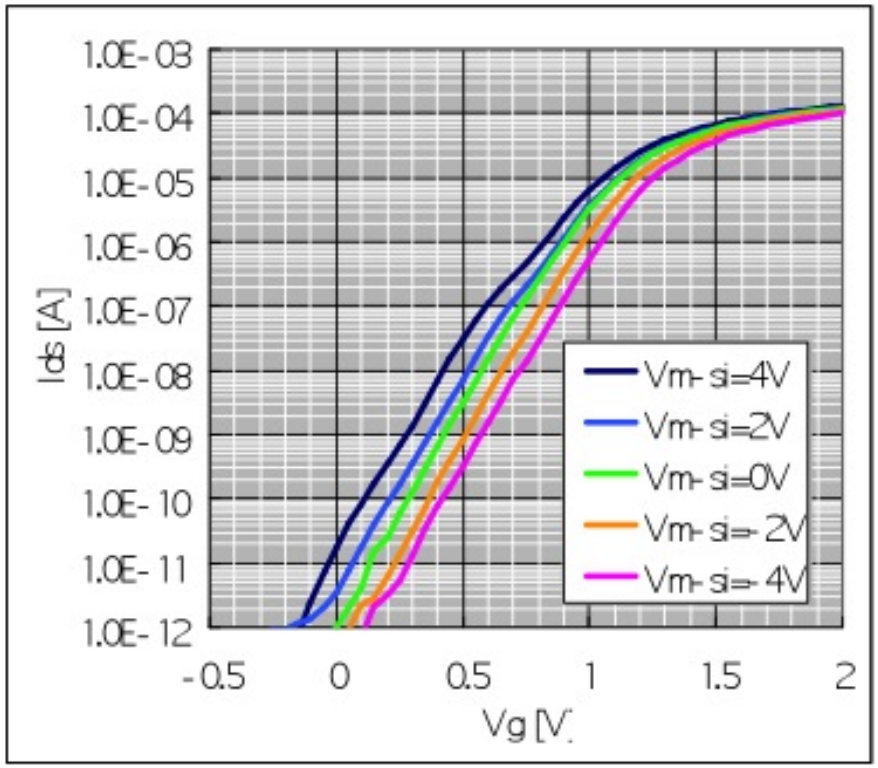

Negative View
Transistor
Gate
Top-SOI
Sensor
Contact
BOX2
BOX1
Sub
Middle-SOI
0.3um

SOI2: Back Gate Effect

Back-Gate Effect is fully suppressed with the middle Si layer at fixed voltage



V_{th} control with middle Si layer

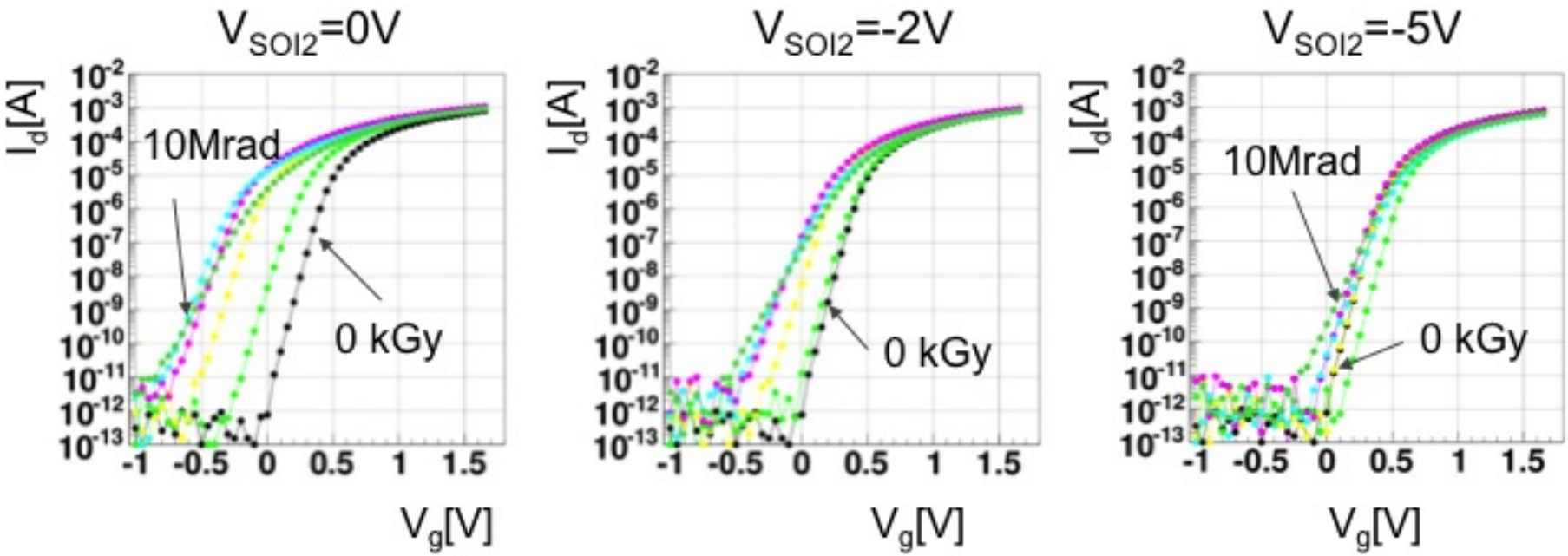


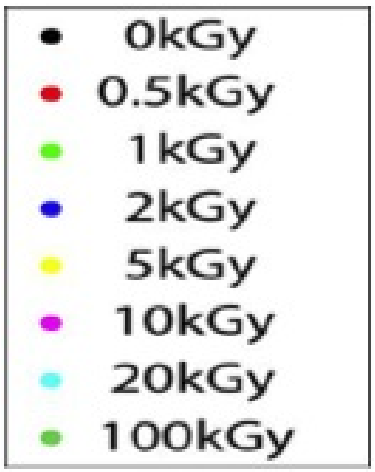
NMOS
Core Normal-Vt
L / W = 0.2 / 5.0 um
Vd=0.1V
Vback: floating

Threshold voltage of a transistor is controlled with the bias voltage of the Middle-Si layer.

This indicate effects of the trapped charge in the BOX can be compensated with the bias voltage.

Gamma-ray Irradiation Test

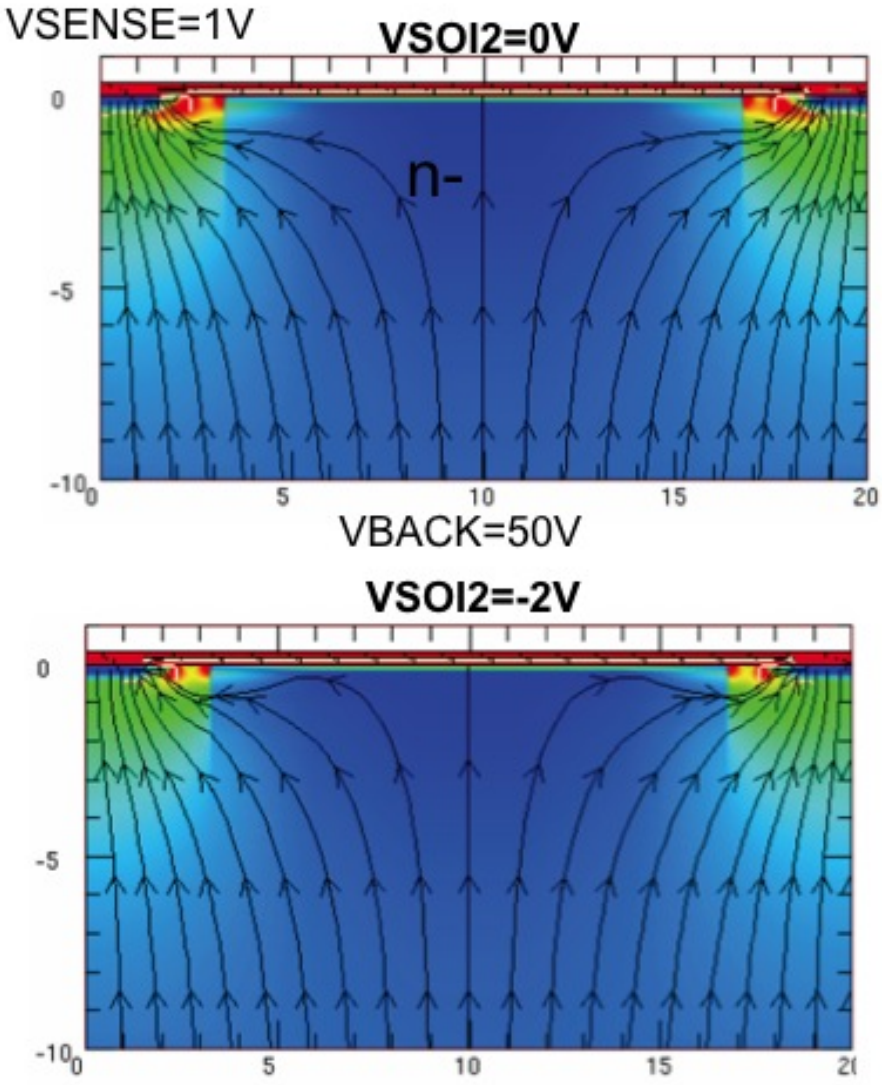




- By setting V_{SOI2} ~-5V, Id-Vg curve returned nearly to pre-irradiation value.
- V_{SOI2} to be applied depends on dose received

SOI2: Summary

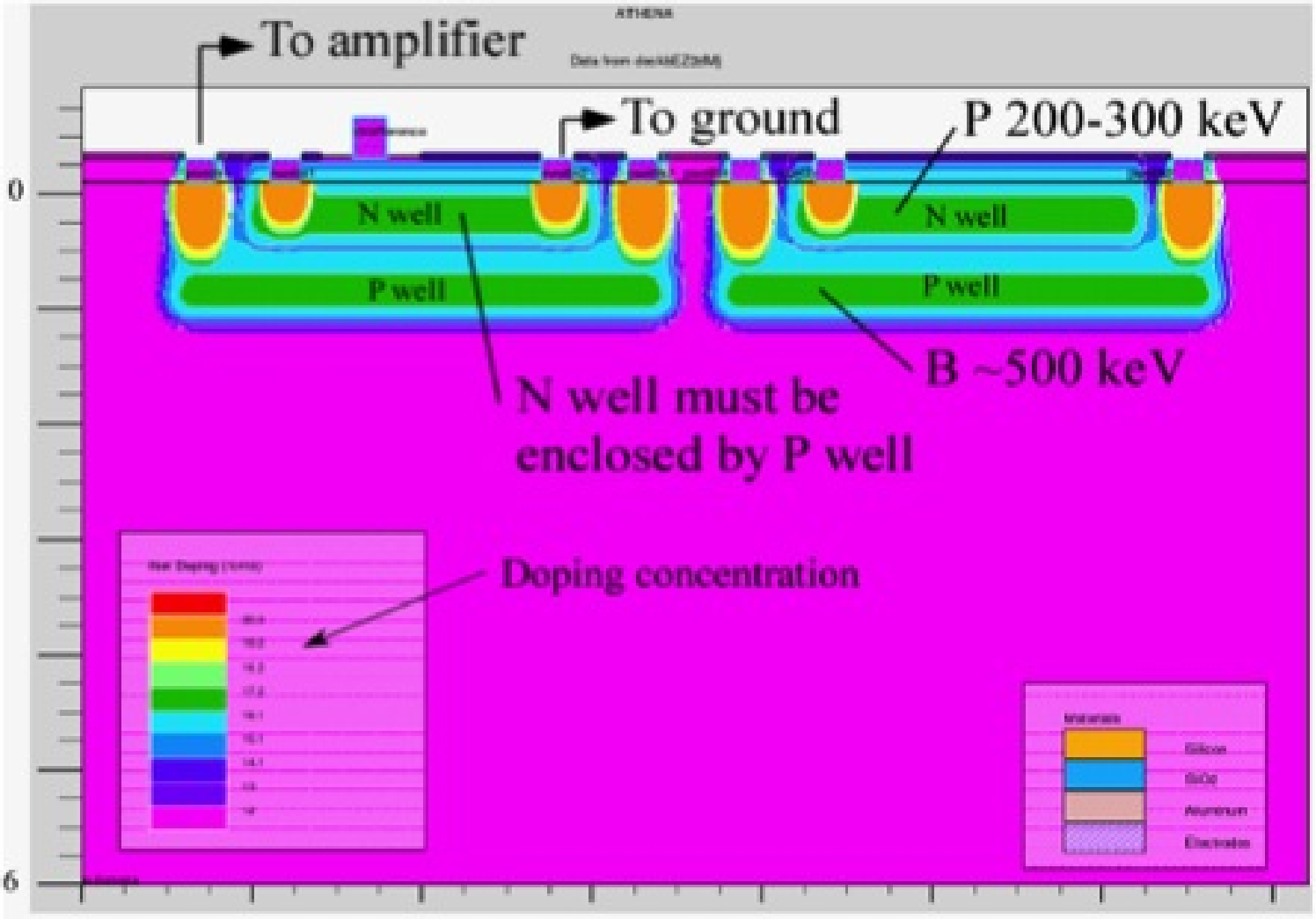
Effect of middle Si layer on Charge Collection



- SOI2 protects against backgate effect
- To compensate trapped hole effect $\rightarrow$ negative SOI2 voltage is necessary.
- To push electrical flux lines to sense node $\rightarrow$ positive SOI2 voltage is necessary.
- It is better to use p-type substrate instead of n-type

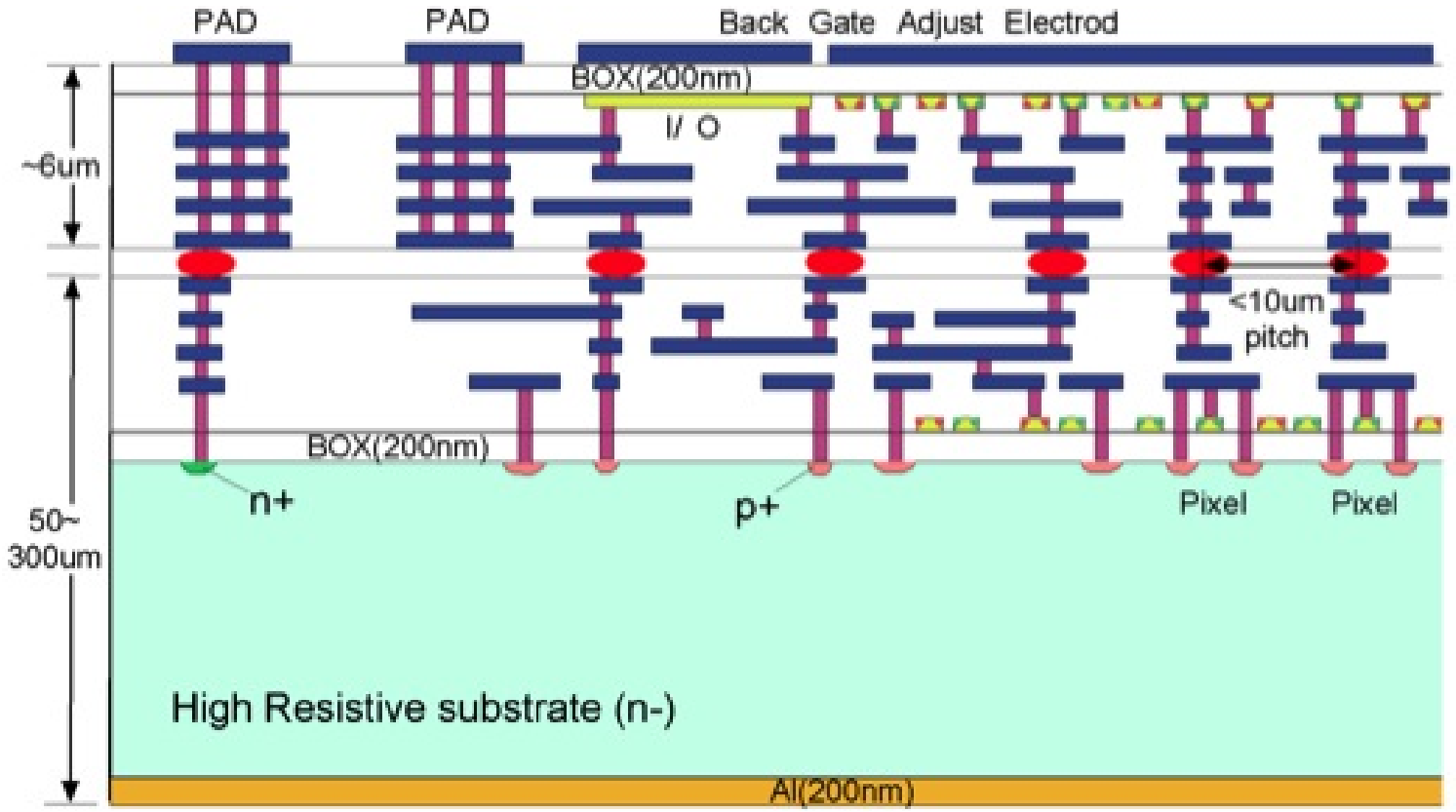
Nested Well Structure

- Signal is collected with the deep buried p-well
- Back gate and cross-talk are shielded with the buried n-well



3D integration

- 3D vertical Integration technique is expected to play an important role in future high performance pixel detector
- SOIPIX can be naturally extended with 3D technology
- First test with 3D test chips done . (μ-bump technology $\sim$5 um pitch)

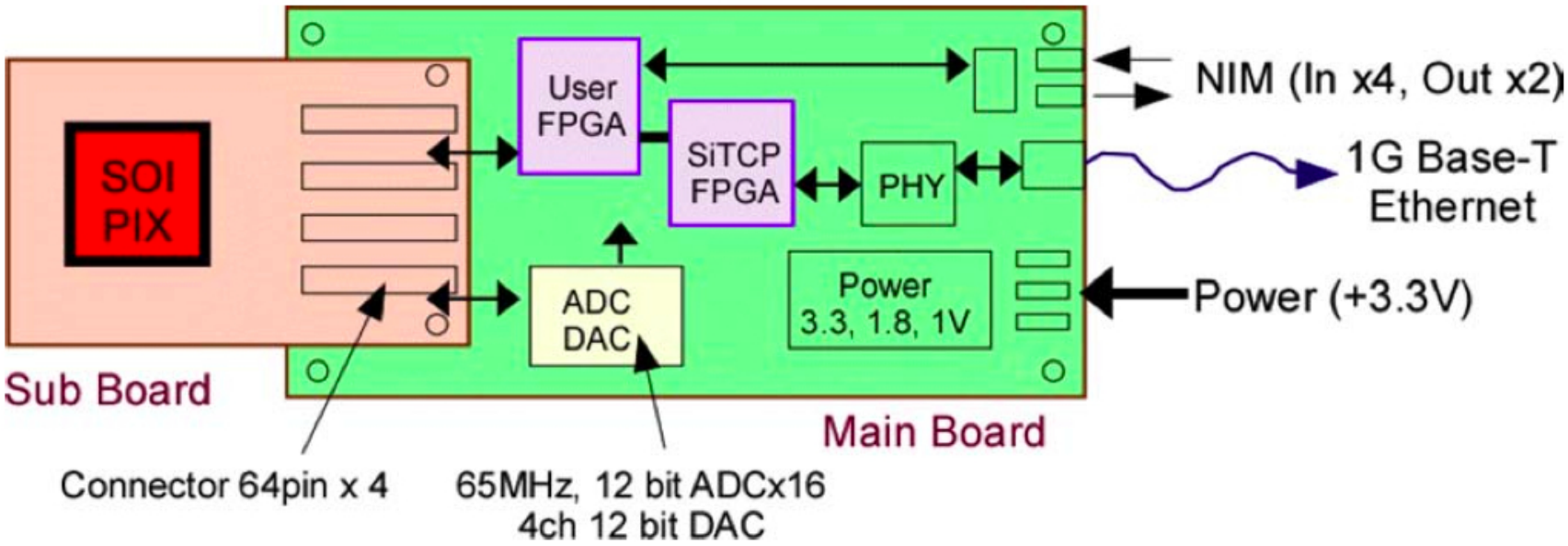


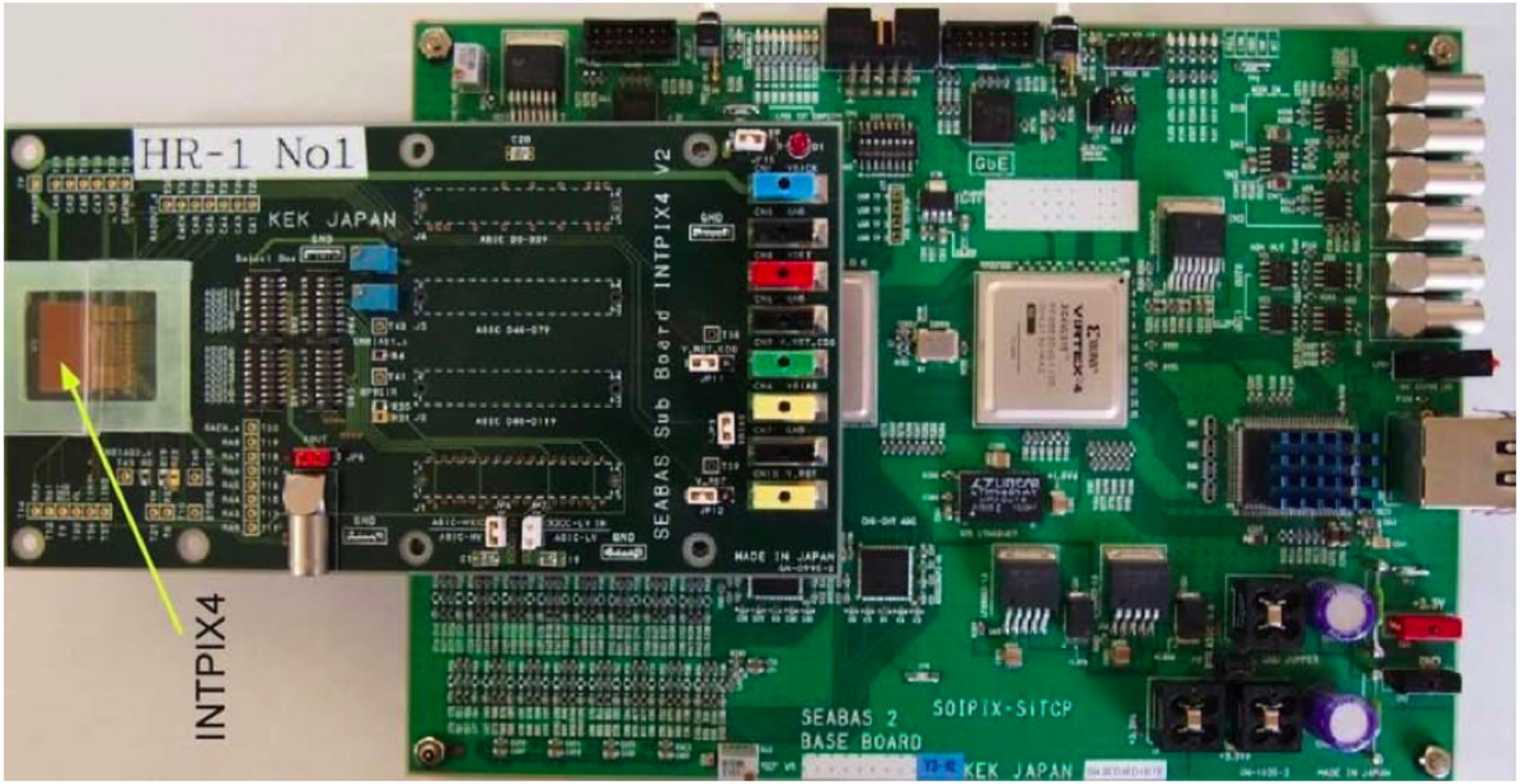
4. Applications
   - SEABAS
   - INTPIX
   - X-ray detectors
   - Vertex Detectors
   - On-going projects

SEABAS Readout board

SEABAS = SOI EvAluation BoArd with Sitcp

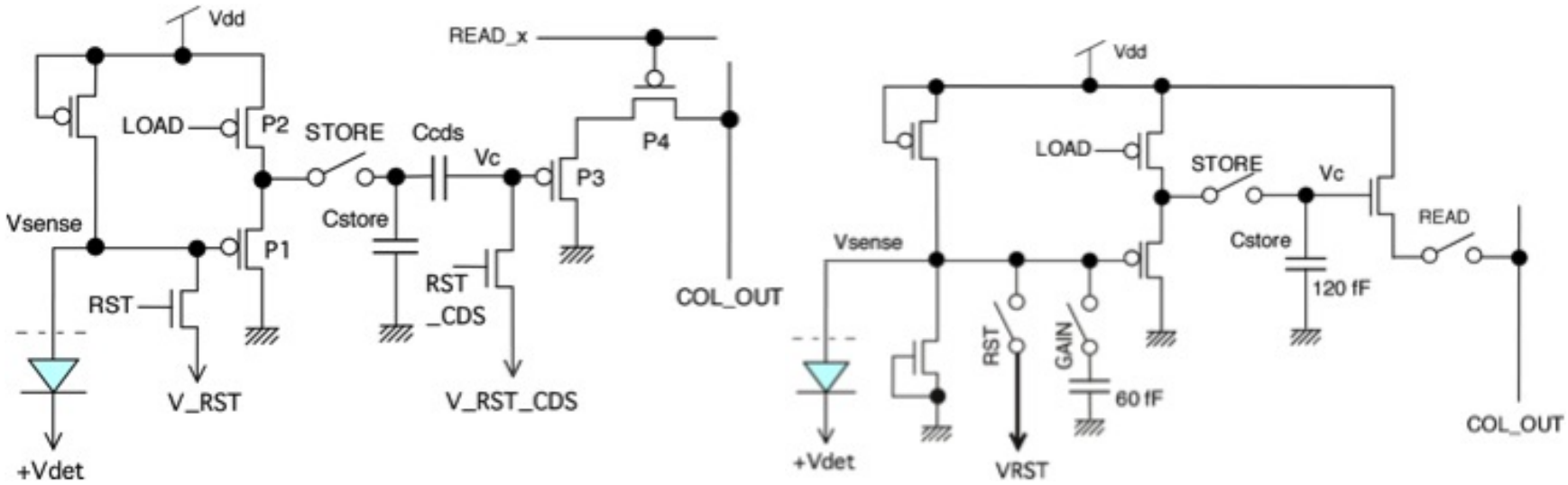
- 2 FPGAS: - control SOI chips
  - data transfert through Ethernet
- Daughter board to host SOIPIX chip
- 70 frame/sec with INTPIX4 (425k pixels)




HR-1 No1
KEK JAPAN
SEABAS Sub Board INTPIX4 V2
MADE IN JAPAN
INTPIX4
SEABAS 2
BASE BOARD
SOIPIX-SiTCP
KEK JAPAN

Integration type Pixel Detector

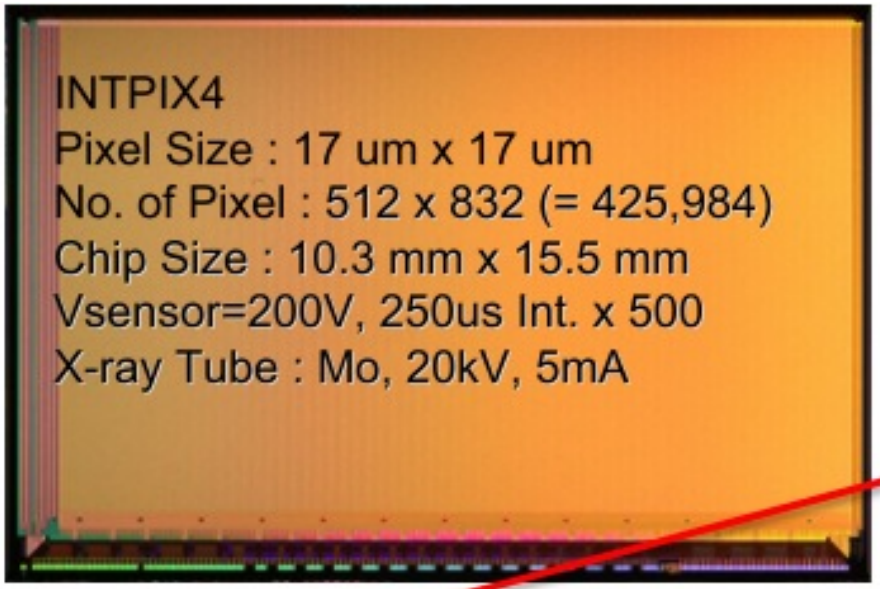
- Main SOI detector development so far
- Basic circuit (source follower)

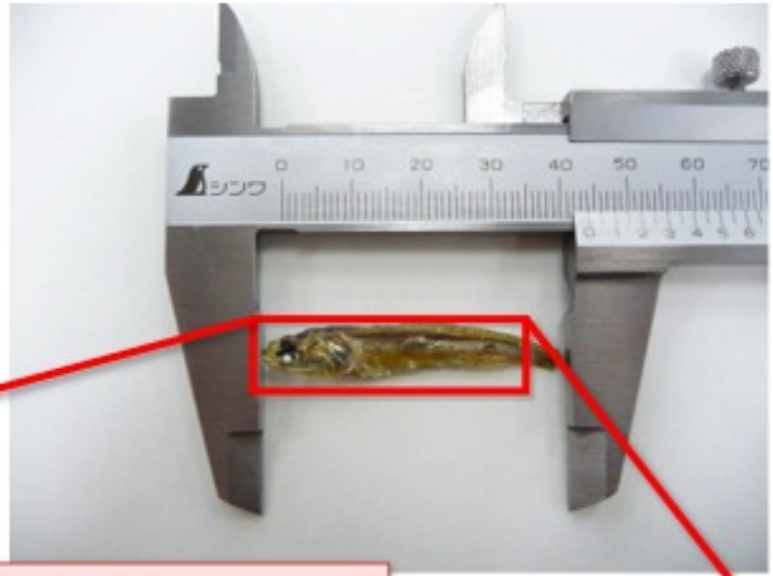


- CDS circuitry on pixel or in column circuitry
- Typical pixel size 12μm$\times$ 12μm

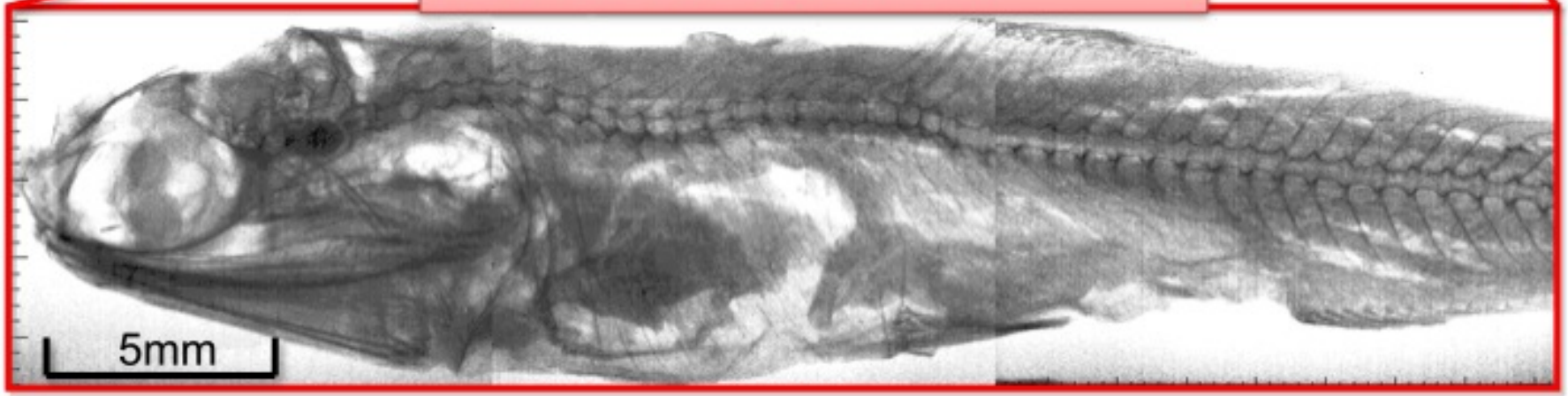
INTPIX detectors

	DIPIX1/2	FPIX1	INTPIX4	INTPIX5/6
Pixel Size [um]	14 x 14	8 x 8	17 x 17	12 x 12
Chip Size [mm]	5 x 5	6 x 6	10.2 x 15.4	12.2 x 18.4
CDS	Pixel	-	Pixel	Column
Store Switch	yes	-	Yes	Yes
Gain	Fix 9.3 uV/e	Fix 28 uV/e	Fix 12.6 uV/e	2 gain 16/2.5 uV/e
Max. Charge	110 ke-	40 ke-	80 ke-	70/460 ke-
No. of Pixels	256 x 128 x 2 $\sim$65 kpix	512 x 512 $\sim$260 kpix	512 x 832 $\sim$430 kpix	896 x 1408 $\sim$1260 kpix
No. of Output	1	1 or 9	1 or 13	1 or 11
Rolling Shutter	-	yes	-	yes





Fine resolution & High Contrast

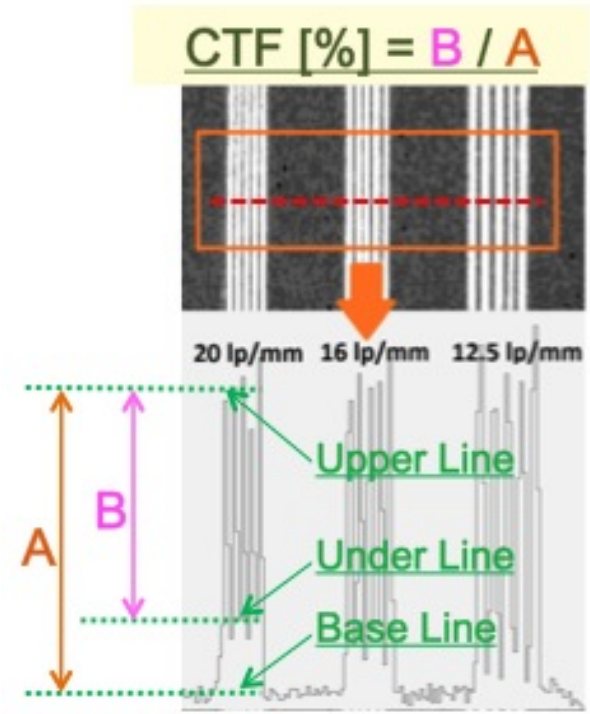


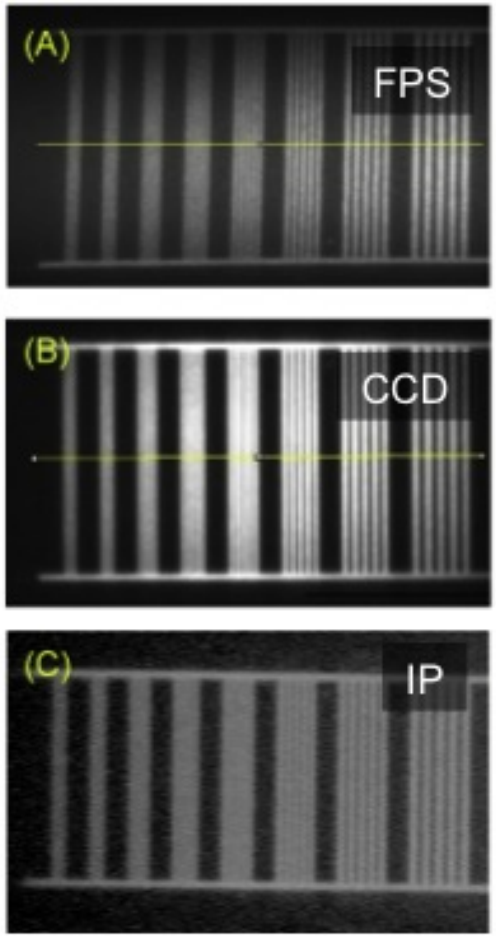
X-ray Image of a small dried sardine taken by a INTPIX4 sensor (3 images are combined).

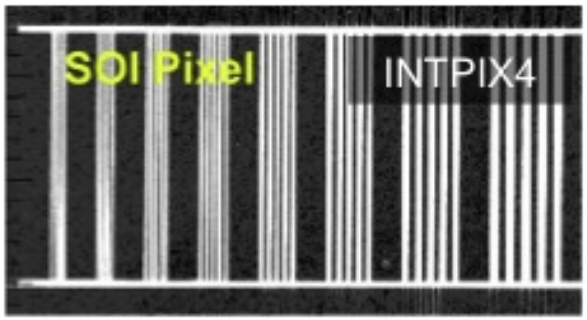
61

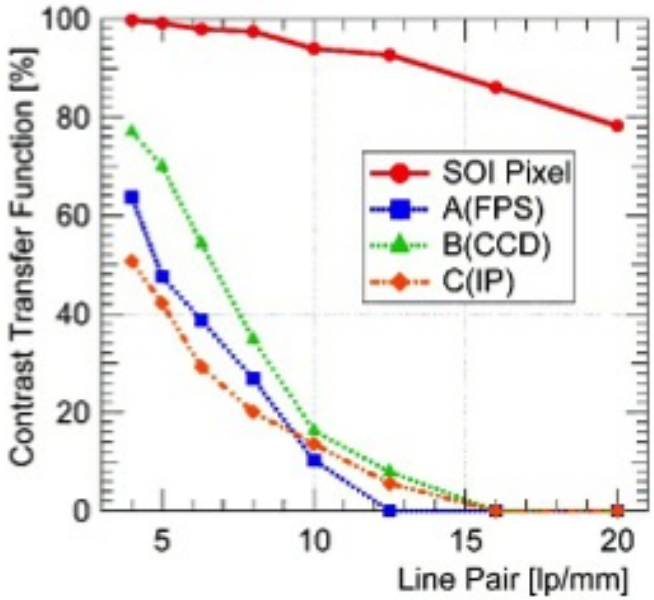
Spatial Resolution: Contrast Transfer Function

Comparison of contrasts with commercial X-ray devices:
INTPIX4, Flat Panel Sensor (FPS), CCD, Imaging Plate (IP)



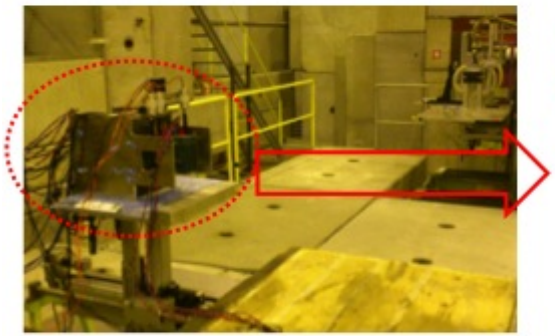


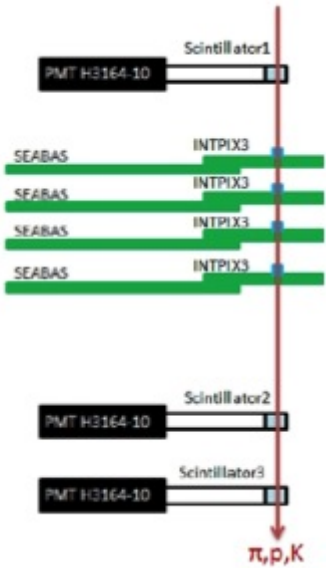




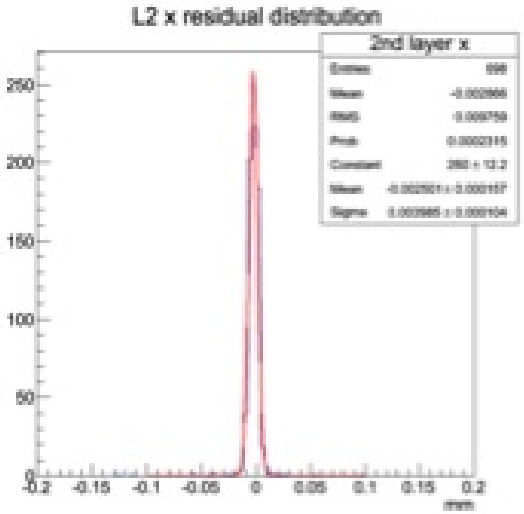
High-energy particle test beam

- CERN SPS
- 120 GeV
- π^+ 55%, p 39%, K^+ 5%
- 4 layers of INTPIX (16x16μm)

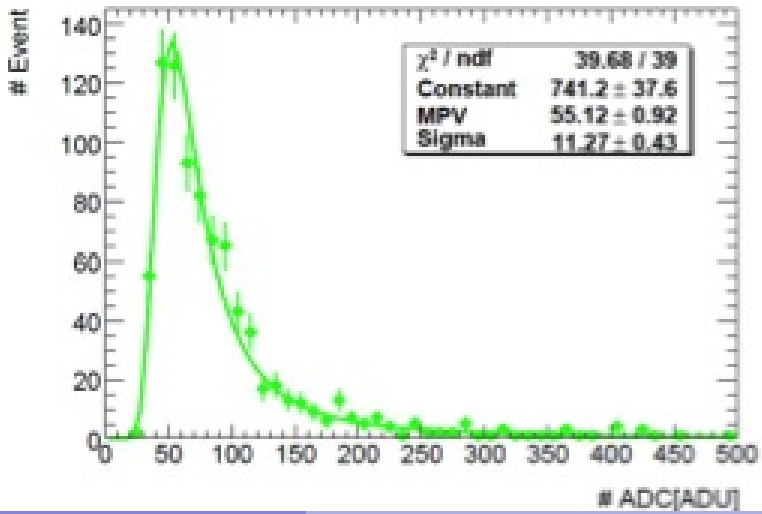




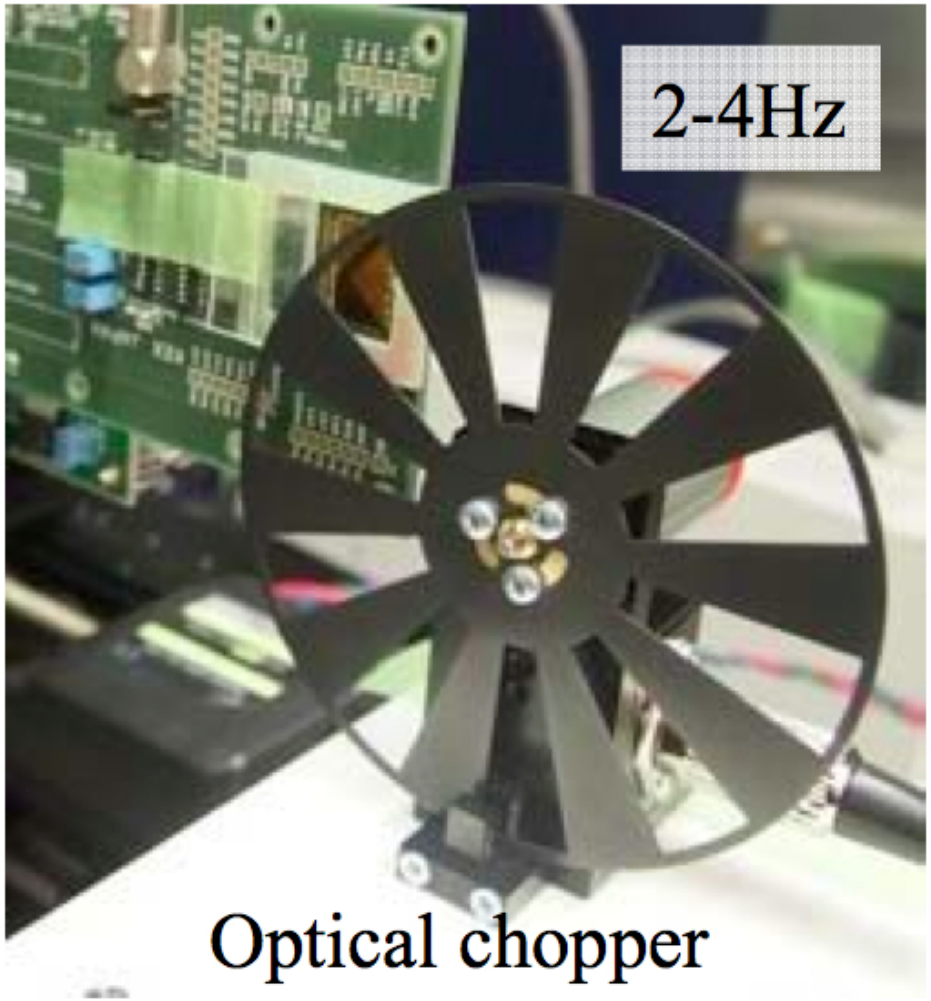
260 μm CZn

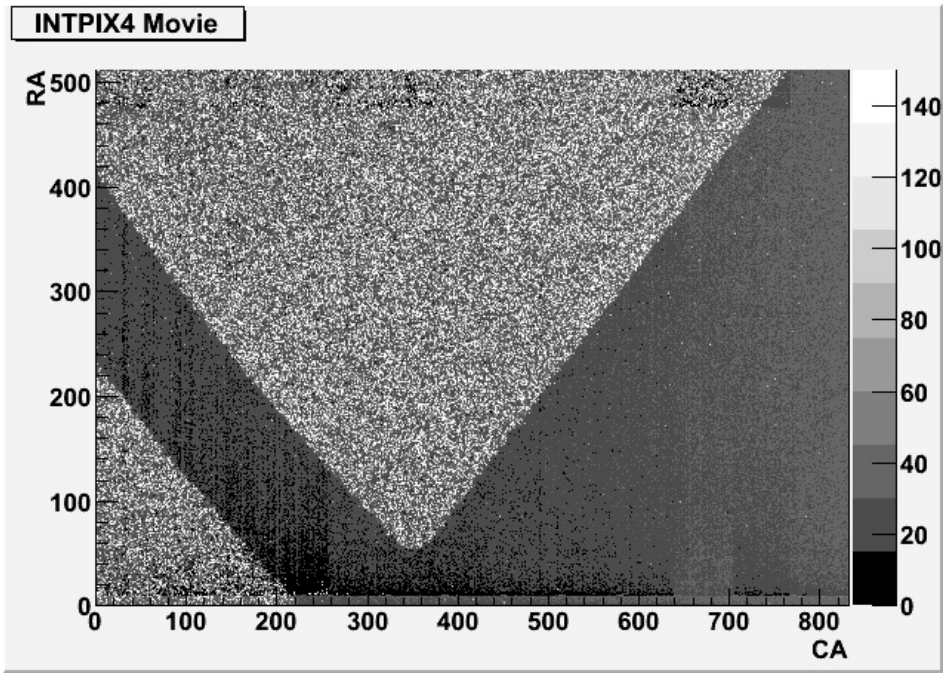


50 μm CZn



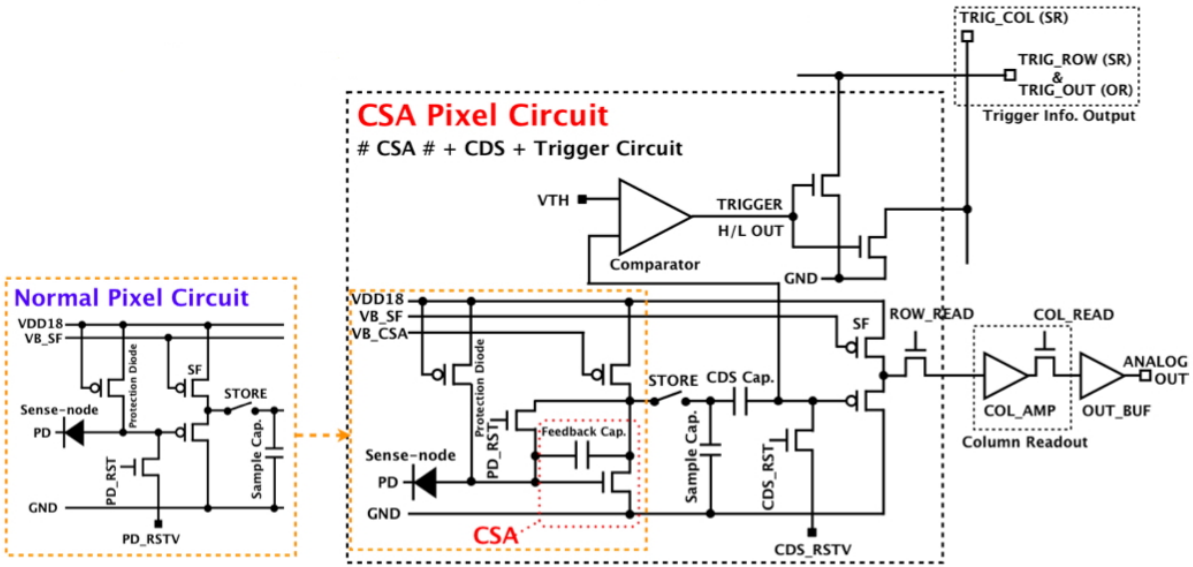
Optical chopper movie

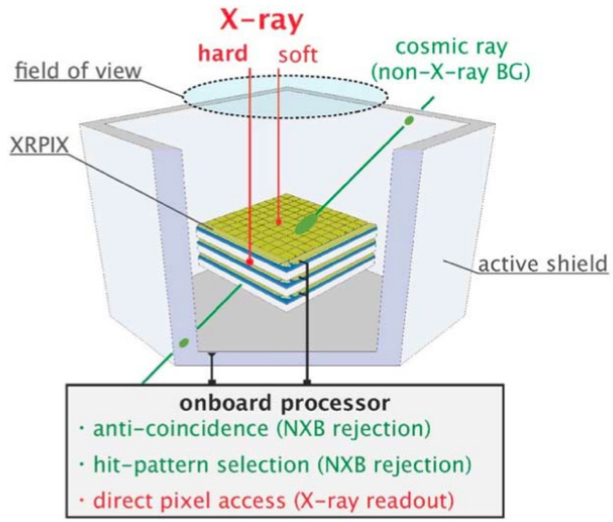




XRPIX

- XRPIX: developed for a X-ray astronomical satellite
- Basic structure
  - Source follower or CSA, both with on-pixel CDS
  - Trigger generator
- Trigger + active shield pixel → charged particle bkg removed

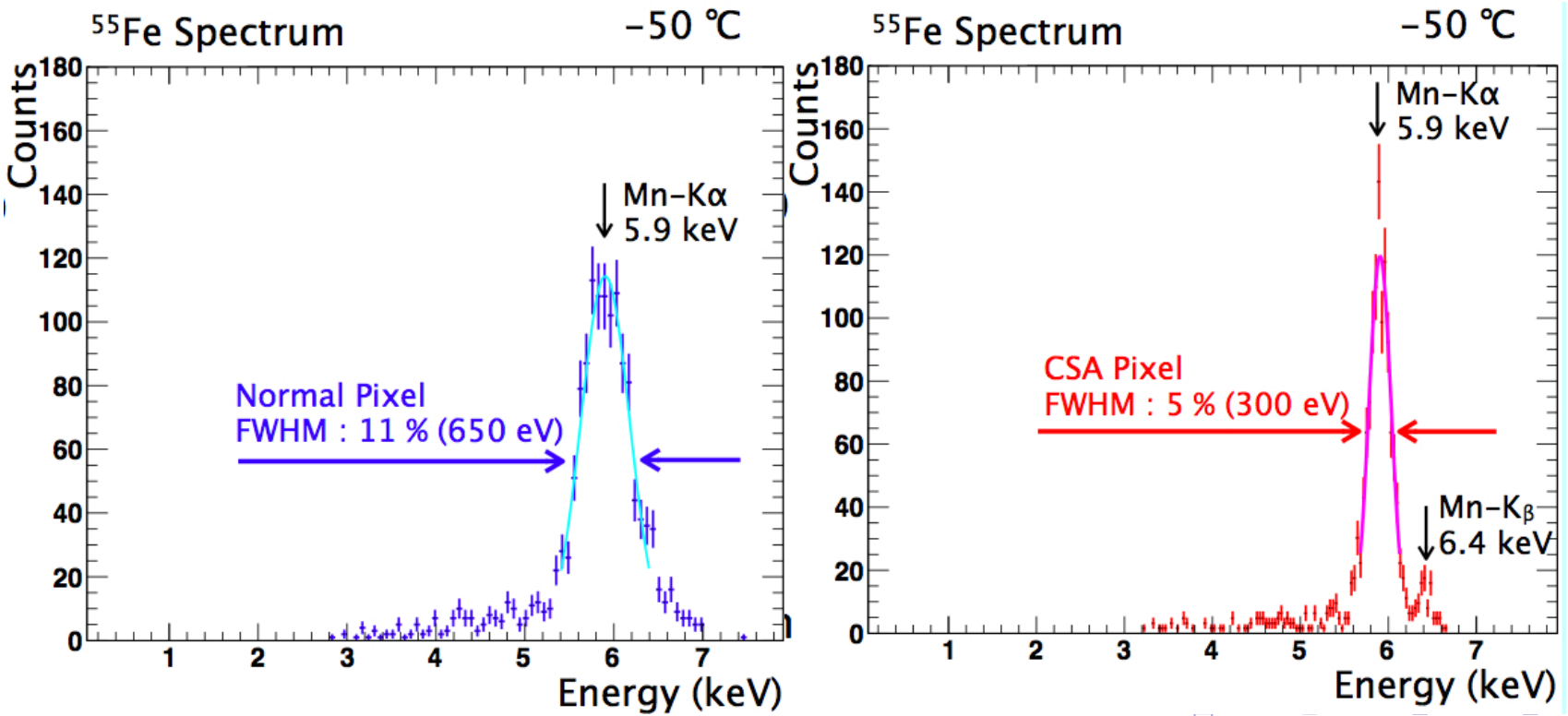




XRPIX: CSA vs source follower

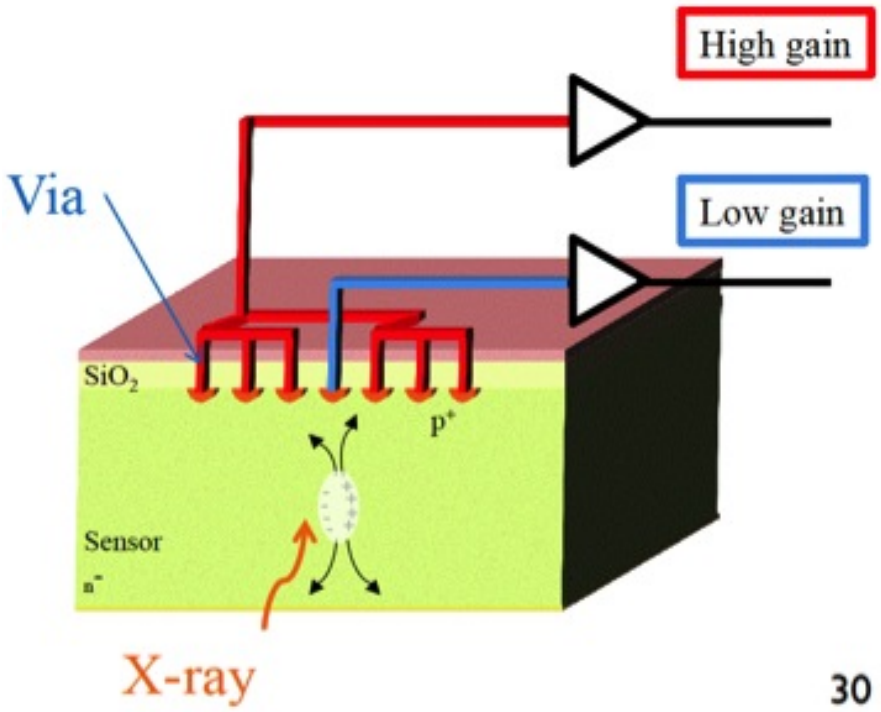
- Better performances with CSA

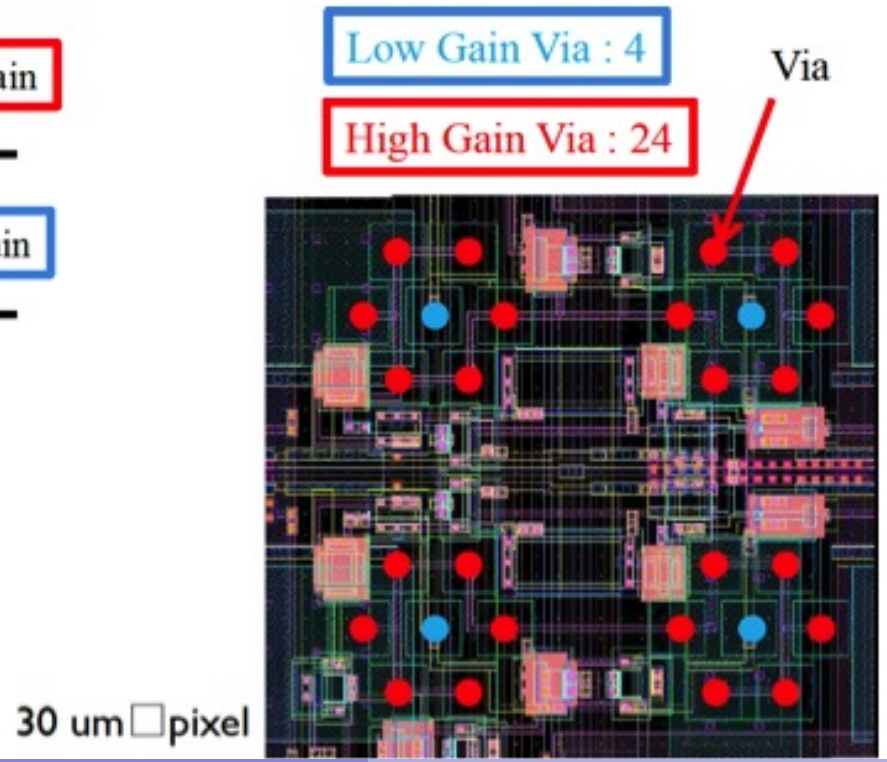
	Normal	CSA
Gain	5.2 μV/e$^-$	17.9 μV/e$^-$
Noise	76 e$^-$	33 e$^-$
FWHM	650 e$^-$ @ 5.9 keV	650 e$^-$ @ 5.9 keV



SOPHIAS

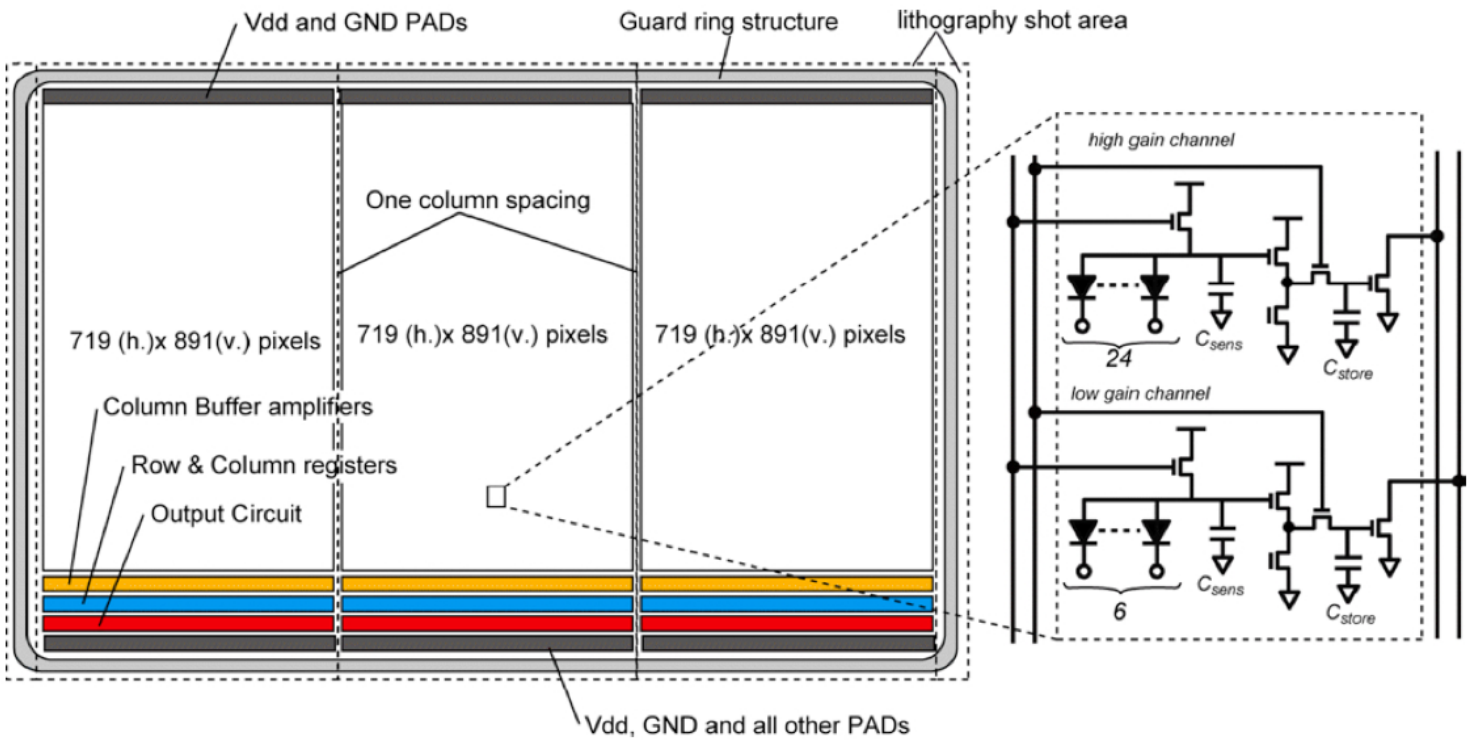
- Silicon-On-Insulator Photon Imaging Array Sensor
- Developed for X-ray Free Electron laser Facility SACLA
- 1.9 Mpixel (30 μ m)
- 40% quantum efficiency at 20 keV X-ray with 500 μm thick handle wafer
- Two gains to reach large dynamic range



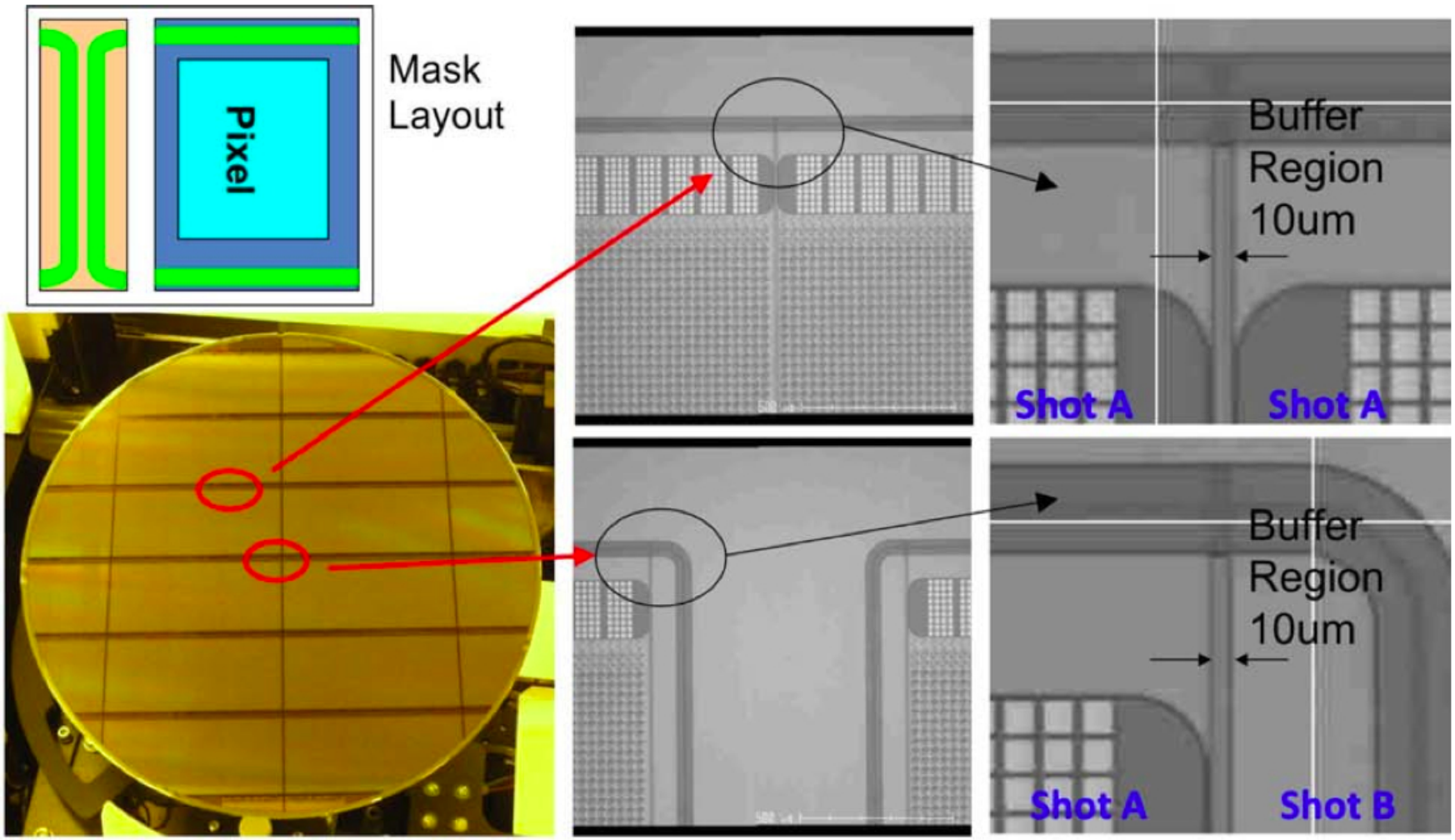


SOPHIAS: Stitching

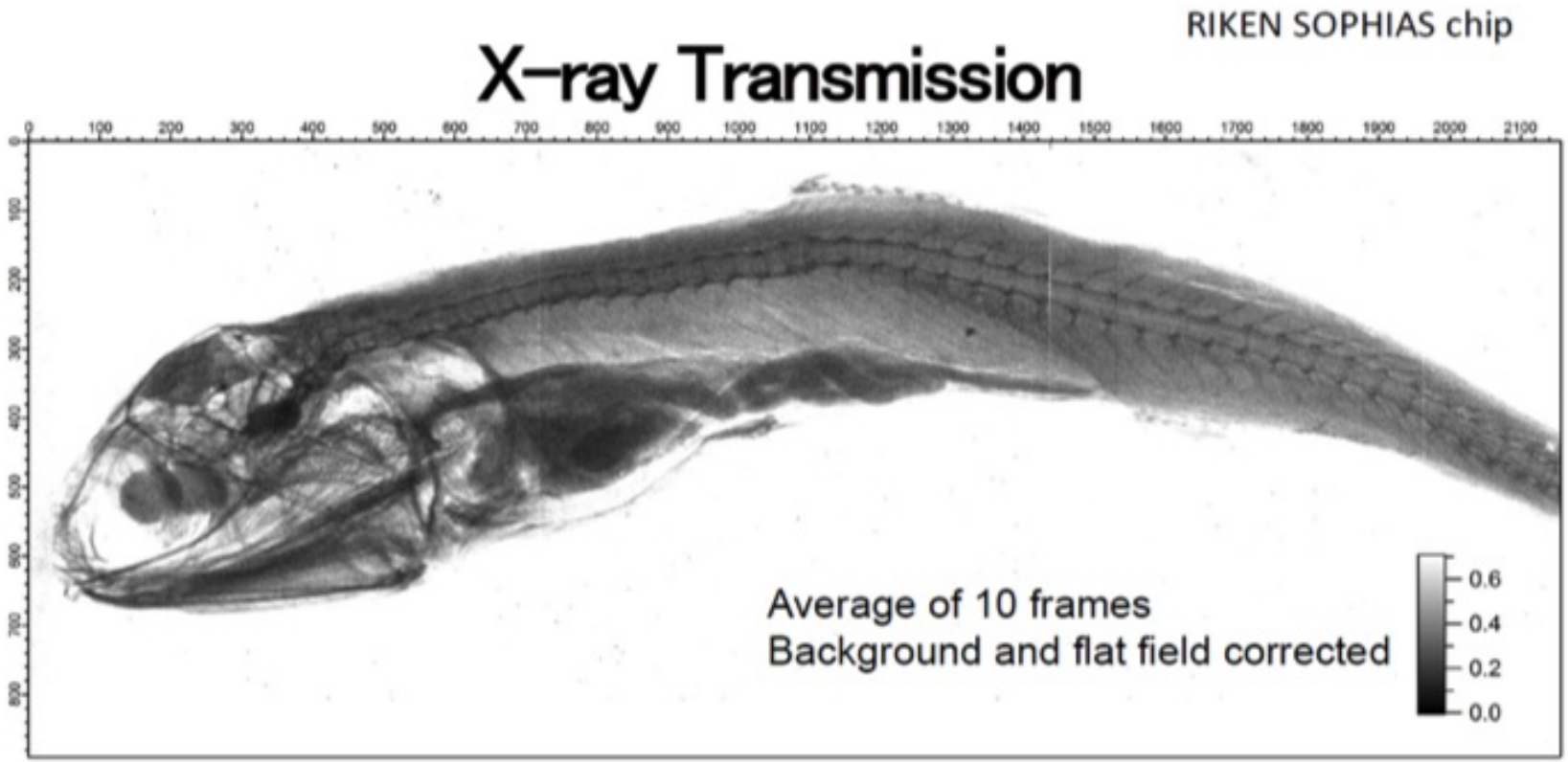
- Mask limited to 24.6mm x 30.8mm
- Stitching technique to build large formats with one mask
- 10 μm buffer region and only minimum number of layers connected (PS,NS,metal1)



SOPHIAS: Stitching



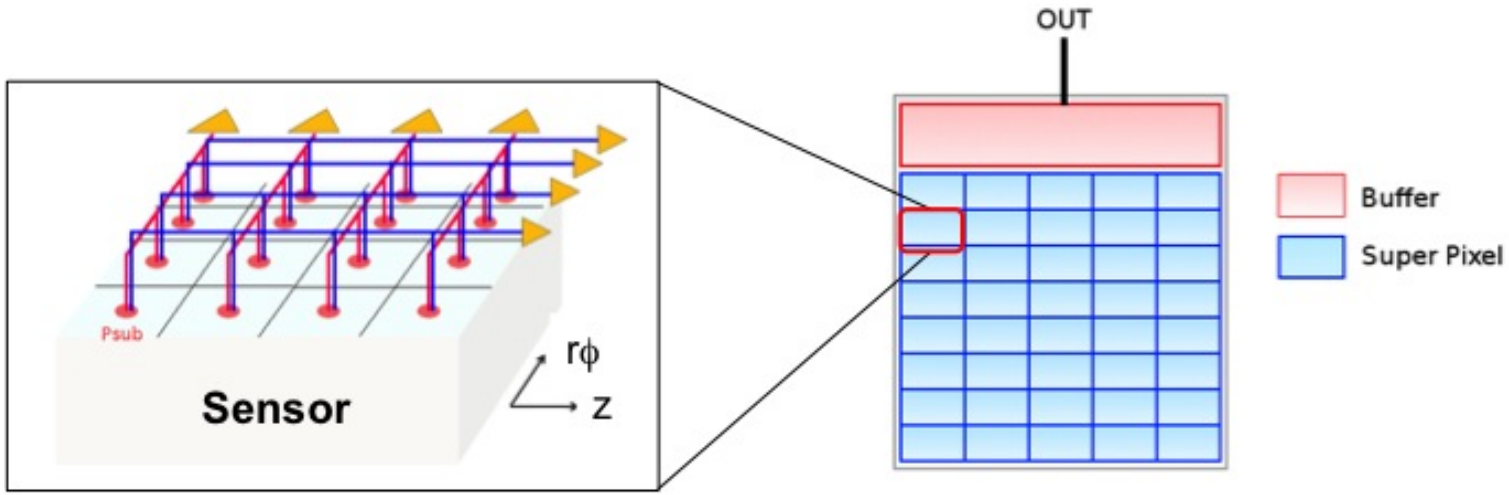
SOPHIAS



- Source-sample : 200 mm
- detector-sample : 600 mm
- X-ray : 40 kV, 800 uA
- Cu target
- X-ray source size : ~3 um
- Exposure time : 10 msec
- Temperature : room temperature

PIXOR

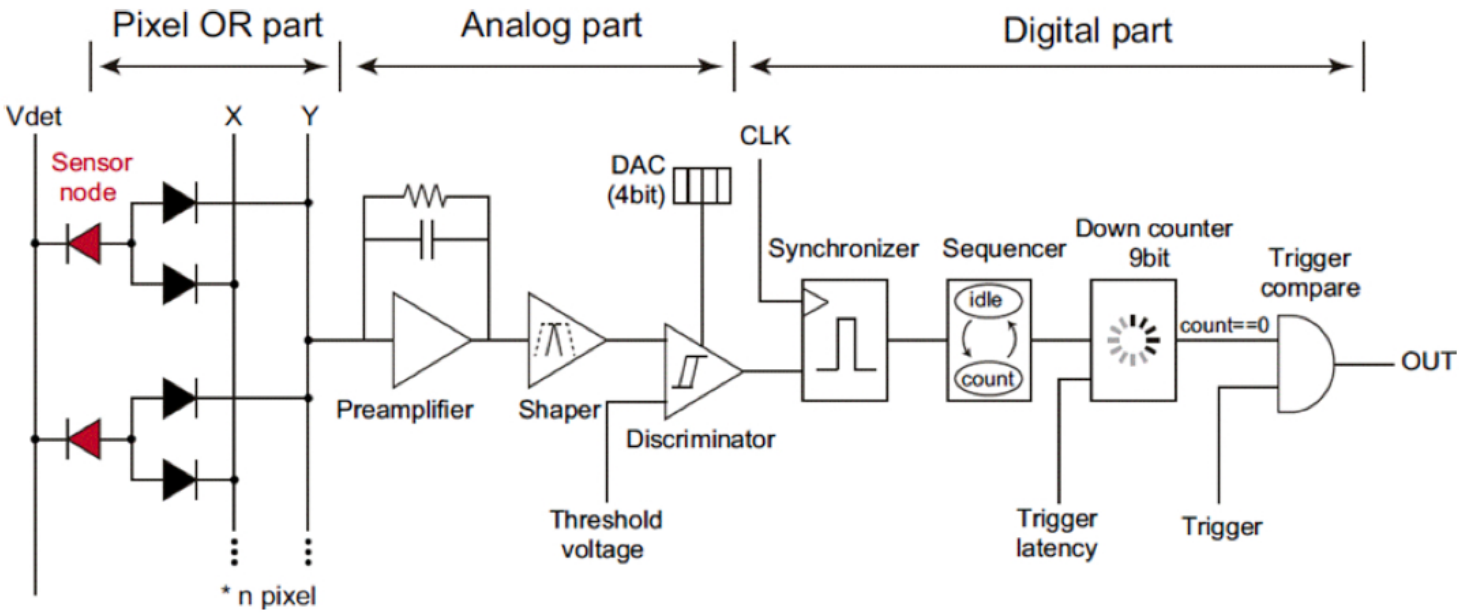
- R&D for a future vertex detector at Belle II
- PIXOR = PIXel OR
  - Define NxN matrix (superpixel)
  - Columns and Rows ORed separetely



PIXOR pitch	25um x 40mm
sampling rate	42.33MHz
Pixel OR	16
thickness	100um
trigger latency	5us
occupancy(L3)	0.0165

PIXOR

- Reduce $N^2 \rightarrow 2N$ readout channels
  - Keeping resolution as same as pixel.
  - Earn the circuit area/pixel $\rightarrow$ complex circuitry
  - Ghost can be suppressed with proper #OR



ON-going projects

- INTPIX : General Purpose Integration Type (KEK)
- SOPHIAS : Large Dynamic Range for XFEL (Riken)
- PIXOR : Belle II Vertex Detector (Tohoku U.)
- XRPIX : X-ray Astronomy in Satellite (Kyoto U.)
- STJPIX : Superconducting Tunnel Junction on SOI (Tsukuba U.)
- CNTPIX : General Purpose Counting Type (KEK)
- LHDPIX : Nuclear Fusion Plasma X-ray (KEK, NIFS)
- MALPIX : TOF Imaging Mass Spectrometer (KEK, Osaka U.)
- TDIPIX : Time Delaying Integration for X-ray Inspection (KEK)
- MAMBO : General Purpose Counting. Nested well (Fermilab)
- TRAPPISTe: General Purpose Tracking Detector (UCLouvain)
- — : General Purpose Integration type (AGH-Krakow)
- ....

5. Summary

Summary

- SOIPIX collaboration have developed SOI Pixel process and fabricated many kinds of monolithic pixel detectors
- SOIPIX have twice/year regular MPW runs with increasing number of users.
- Many new process technologies have been developed to overcome SOI problems;
  - Buried P-well, Double SOI, Nested well structure
  - High resistive SOI wafer
  - Stitching
  - Vertical integration

- Double SOI of p-type substrate looks promising for rad-hard counting-type pixel detector.