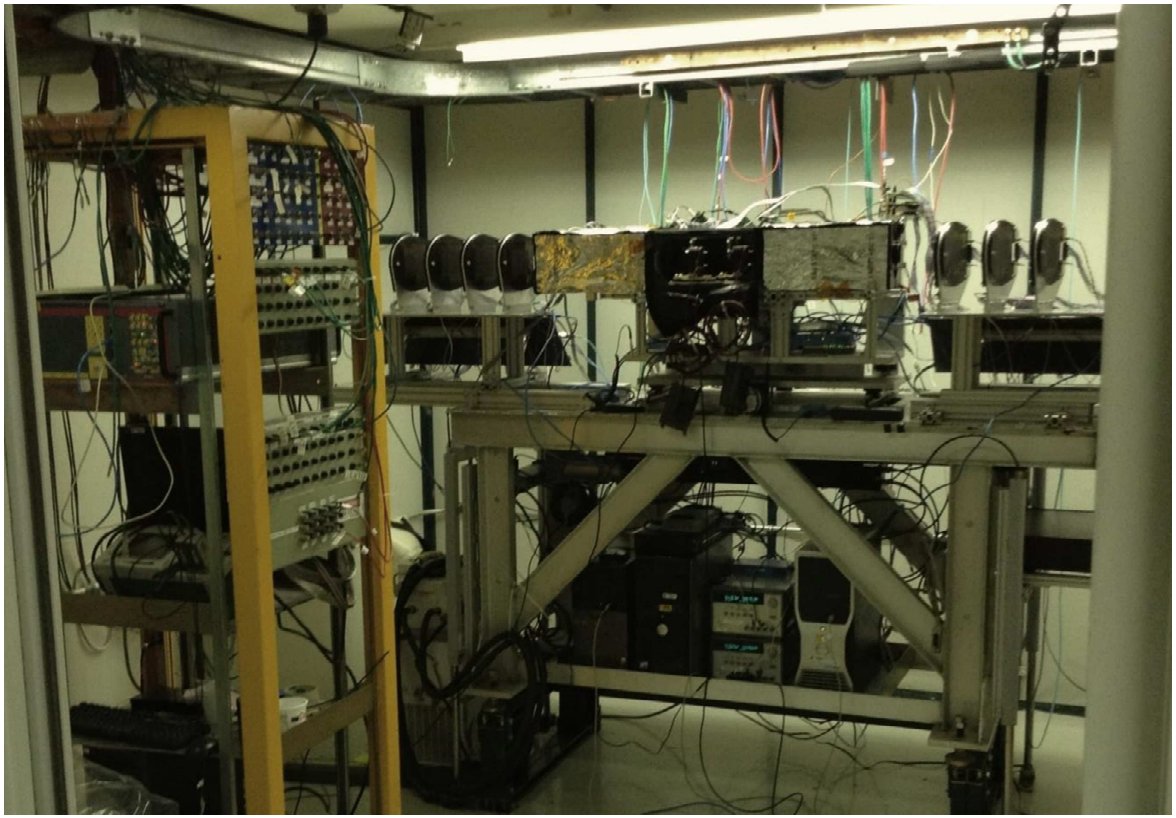
New Test Infrastructures for Future Particle Physics Experiments and Upgrades

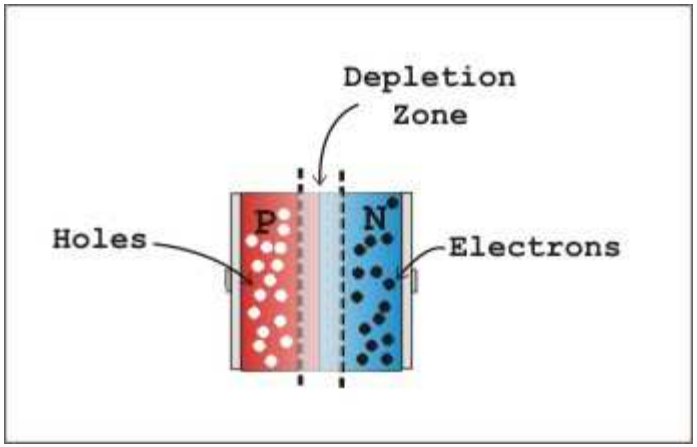


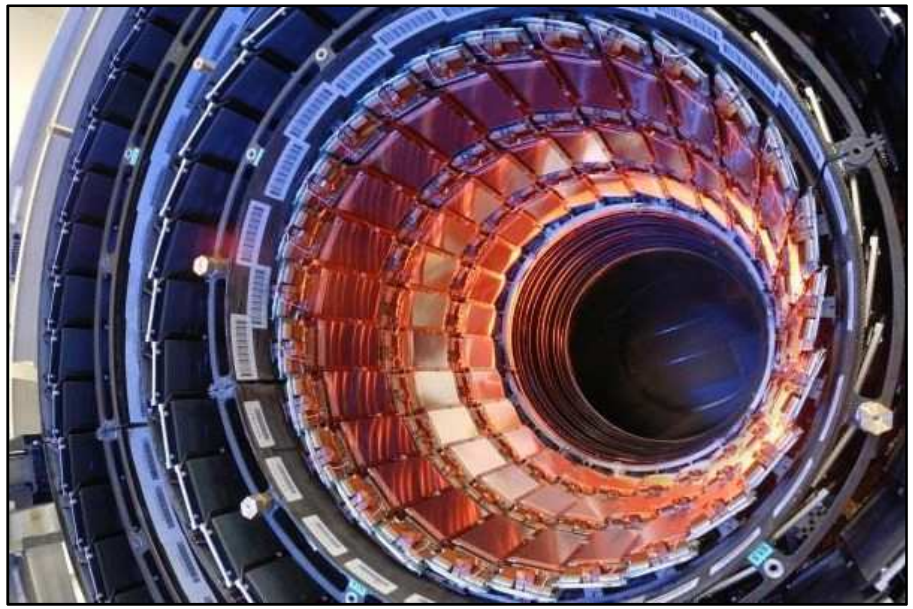
NSF CAREER award 6807134

A Silicon Strip Telescope for the Fermilab Testbeam Facility

Matthew Jones
Purdue University

Silicon Detector Systems





Plan for today's Lecture

Practical aspect:

I will provide a description of the silicon strip telescope developed for the Fermilab test beam facility.

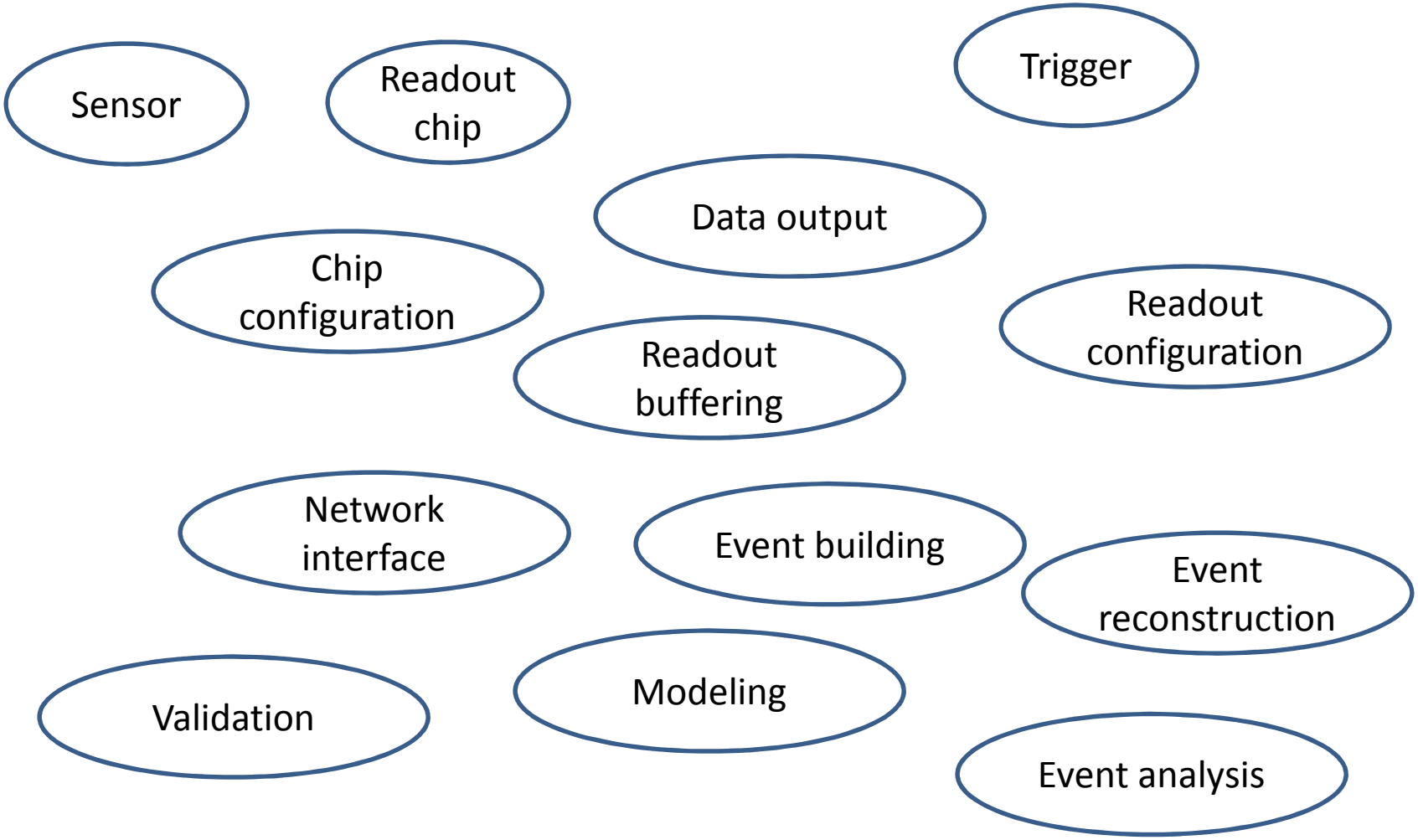
Pedagogical aspect:

I will use it as an example to illustrate the design of a complete silicon-based detector and data acquisition system.

Appologies:

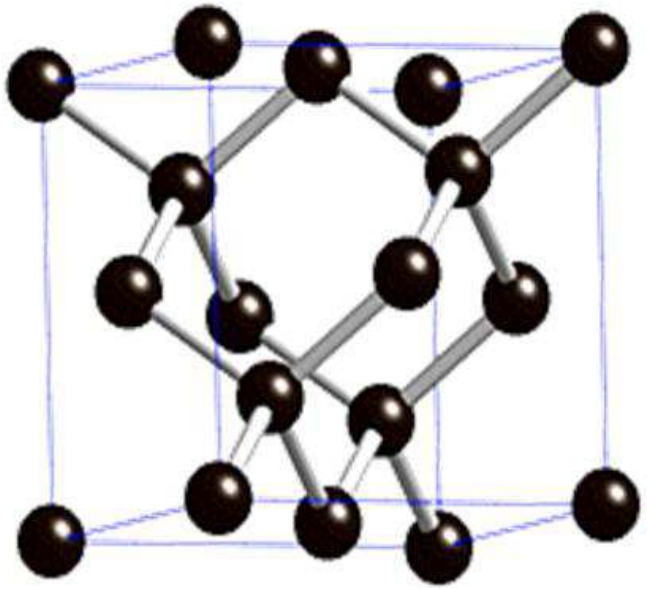
Many participants are already familiar with at least some of these concepts…

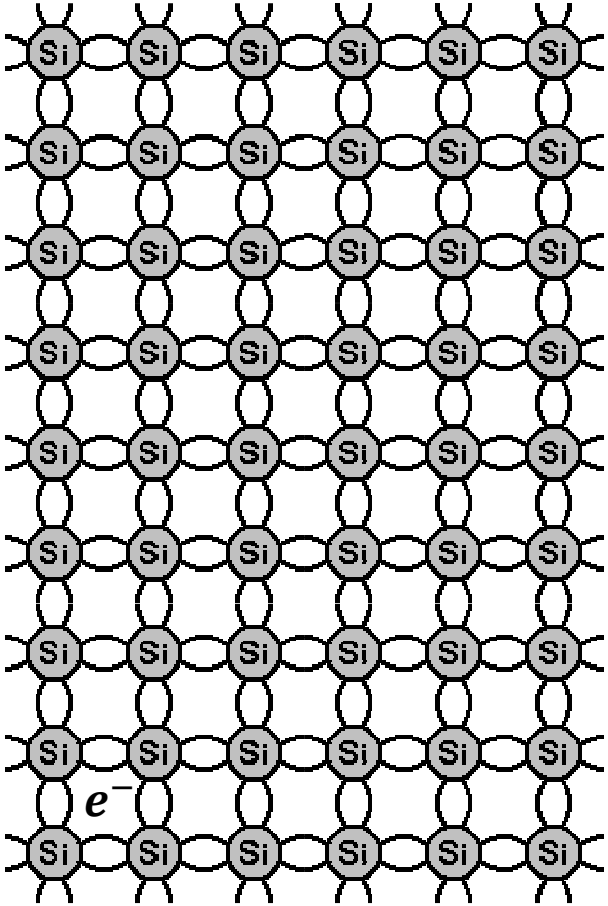
System Architecture



Silicon Strip Sensors

Silicon

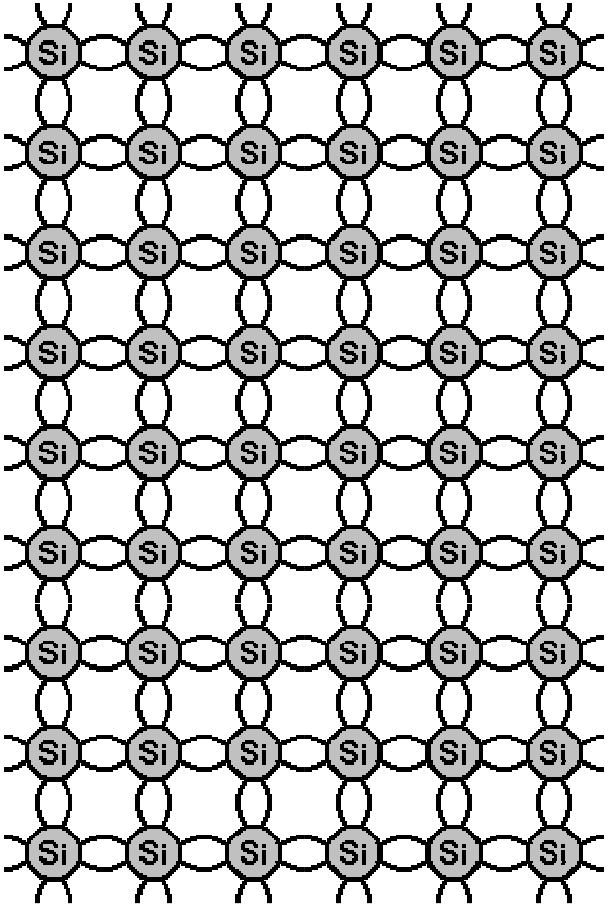




$$\vec{J} = qn\vec{v}$$

$\vec{E}$

Silicon



Mobility, μ: $\vec{v}_e = -\mu_e \vec{E}$

$\vec{v}_h = \mu_h \vec{E}$

At 300 K:

$\mu_e \approx 145\ \mu\text{m}^2/\text{V}\cdot\text{ns}$

$\mu_h \approx 45\ \mu\text{m}^2/\text{V}\cdot\text{ns}$

Example:

$d = 320\ \mu\text{m}$ and $V = 100\ \text{V}$

Electric field: $E = 0.313\ \text{V}/\mu\text{m}$

Carrier speed:

$v_e = 45\ \mu\text{m/ns}$

$v_h = 14\ \mu\text{m/ns}$

Drift time:

FAST →

$T_e = d/v_e = 7\ \text{ns}$

$T_h = d/v_h = 23\ \text{ns}$

Doped Silicon

Conductivity of intrinsic silicon, $n_e = n_h = n_i$:

$$\vec{J} = en_i(\mu_h + \mu_h)\vec{E} = \sigma_i\vec{E}$$

Intrinsic carrier density is very low:

$$n_i \sim 10^{10}\ \mathrm{cm}^{-3} \text{ at 300 K}$$

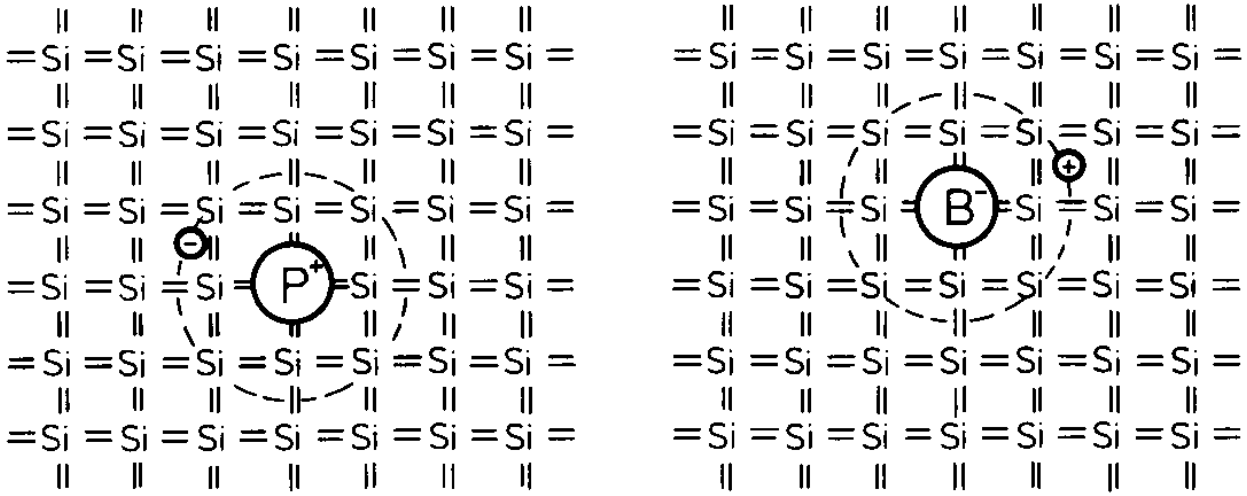
Number density of Si atoms: $n_{Si} = \frac{\rho}{m}N_A = 5 \times 10^{22}\ \mathrm{cm}^{-3}$

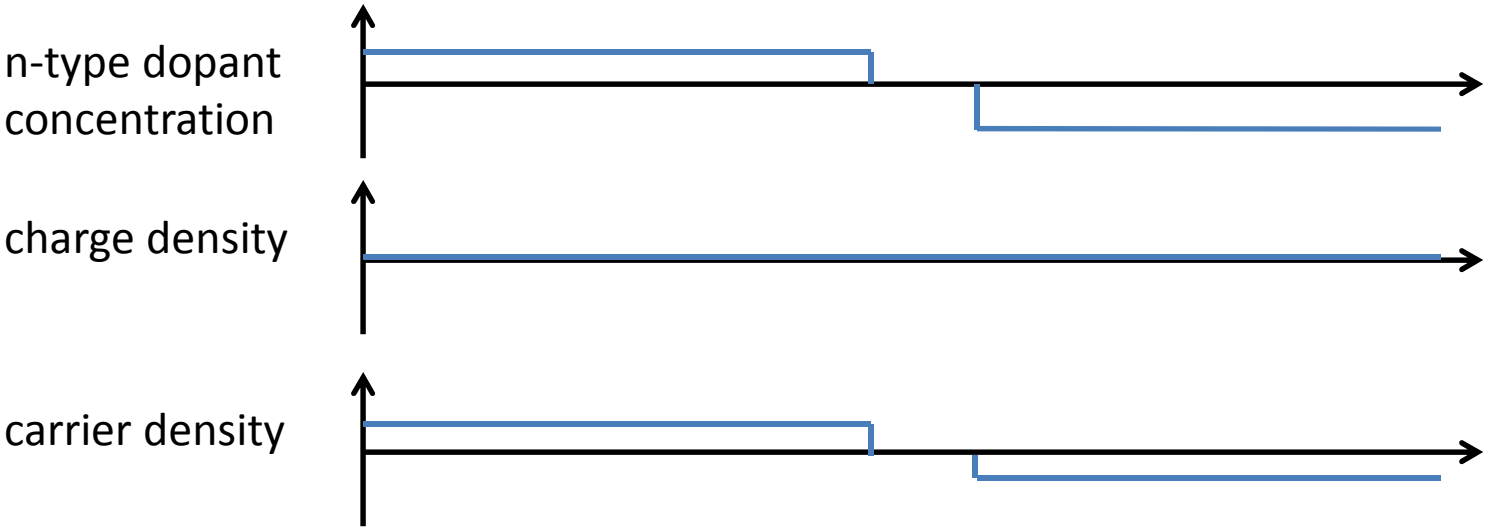
Doped silicon:

A small number of donor or acceptor atoms will completely determine the conductivity:

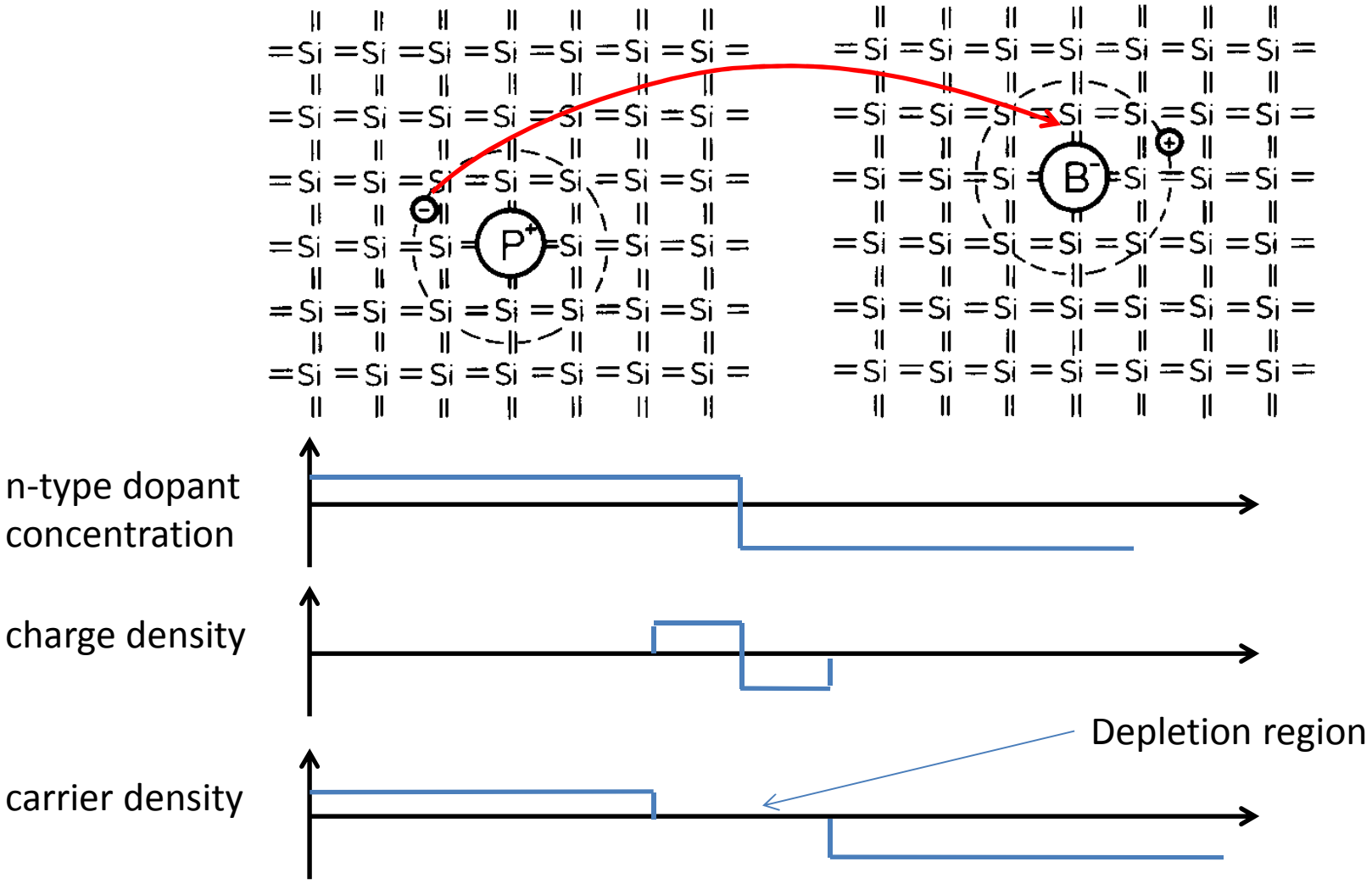
- $n_{Si} \gg n_D \gg n_i$
- Phosphorus (donates electron – n-type Si): $\sigma_n = en_D\mu_e$
- Boron (makes a hole – p-type Si): $\sigma_p = en_D\mu_h$

P-N Junction

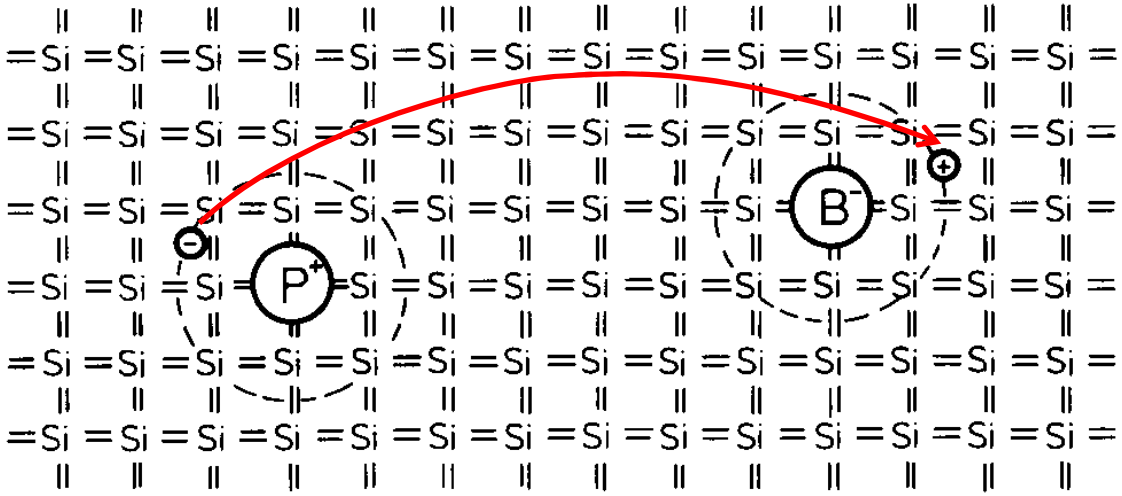

P+
B-


n-type dopant concentration
charge density
carrier density

P-N Junction


P+
B-
n-type dopant concentration
charge density
carrier density
Depletion region

P-N Junction



$\vec{E}$

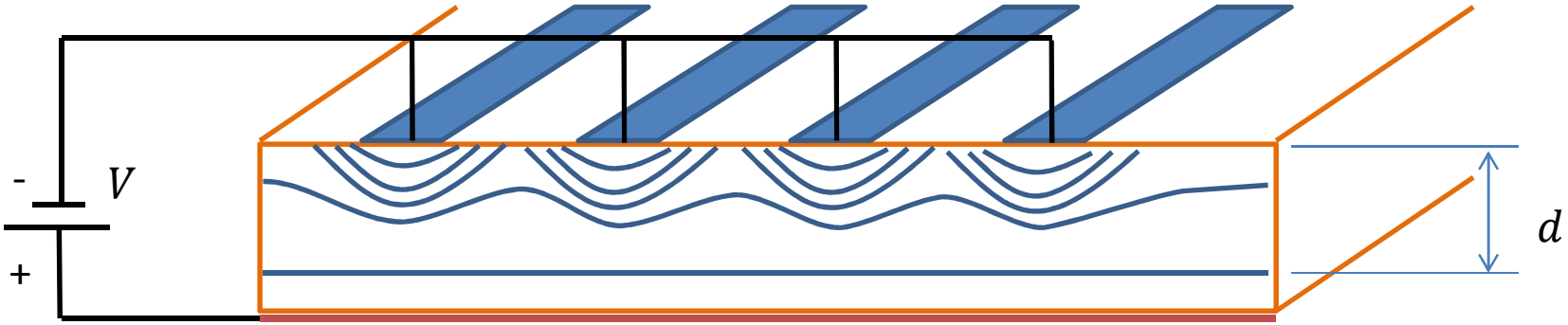
Depletion region

carrier density

Charge carriers in depletion region created by:

- Thermal excitation
- **Ionizing radiation**
- Defects that result in dangling bonds

Silicon Strip Sensors



- Width of depletion region:

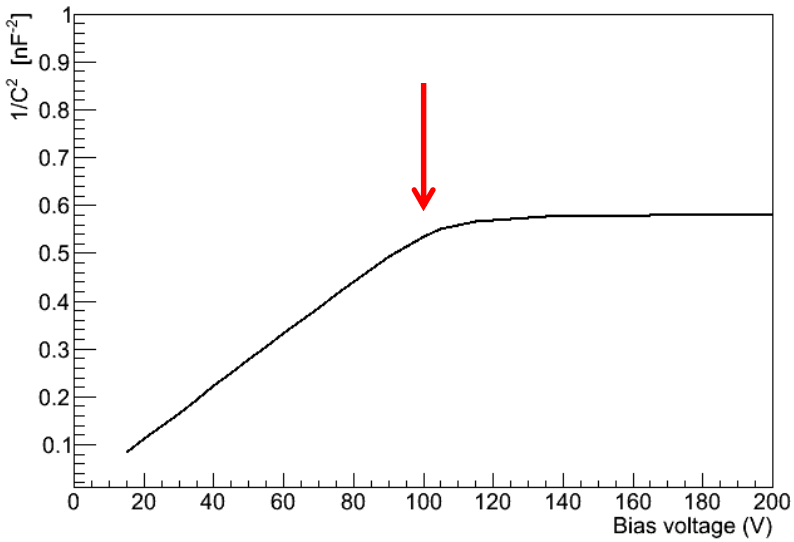
$$d = \sqrt{2\varepsilon\rho\mu V}$$

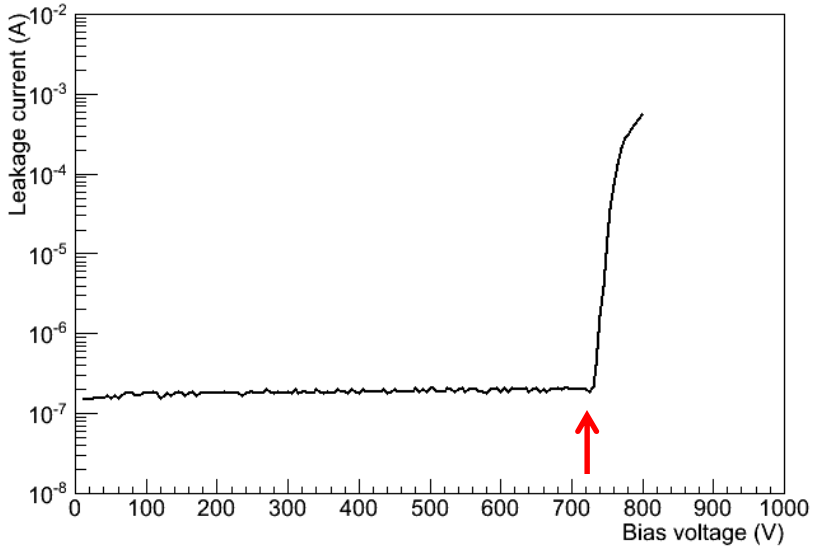
- Parallel plate capacitor:

$$C = \frac{\varepsilon A}{d}$$

$$\frac{1}{C^2} \propto V$$

Silicon Strip Sensors





Fully depleted at about 100 V.

Breakdown at 750 V.

Silicon Strip Sensors

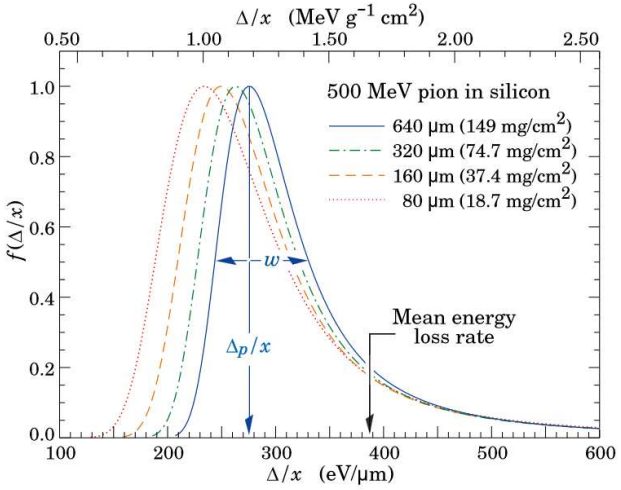


Figure 31.8: Straggling functions in silicon for 500 MeV pions, normalized to unity at the most probable value δ_p/x. The width w is the full width at half maximum.

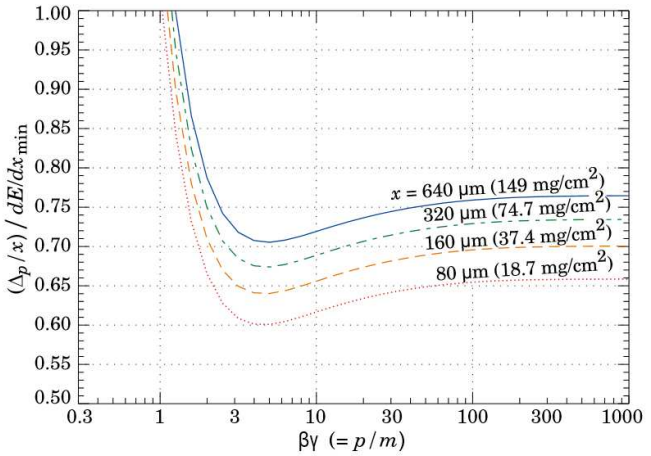


Figure 31.9: Most probable energy loss in silicon, scaled to the mean loss of a minimum ionizing particle, 388 eV/μm (1.66 MeV g^{-1}cm^2).

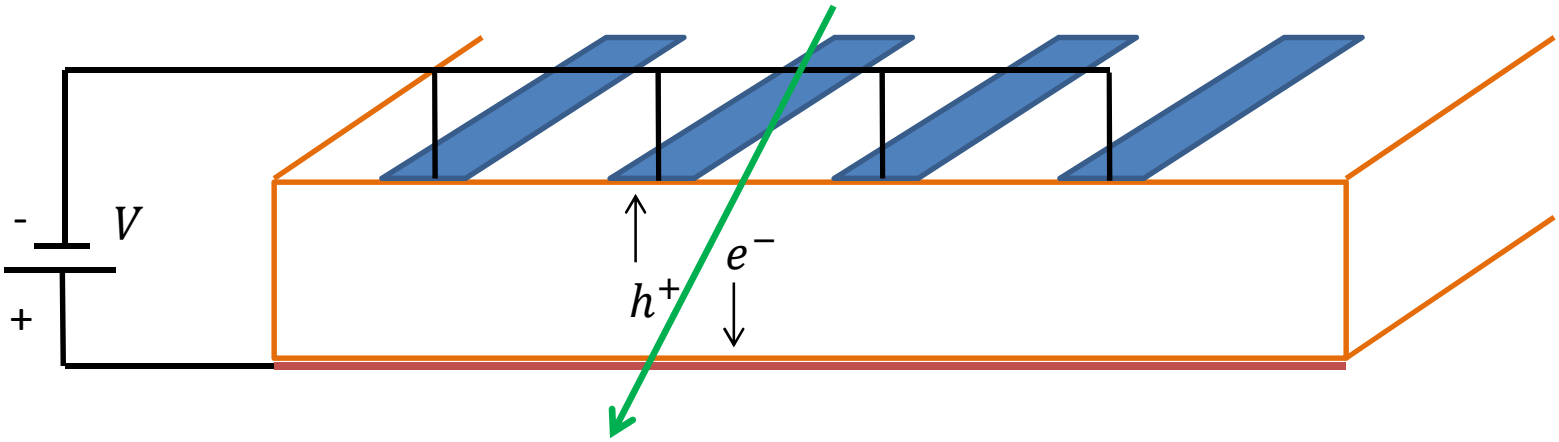
Mean energy loss of a MIP in 320 μm thick sensor:

$$\langle \Delta \rangle = (377\ \text{eV}/\mu\text{m}) \cdot (320\ \mu\text{m}) = 120\ \text{keV}$$

Energy needed to produce electron-hole pair: 3.6 eV

A MIP produces about 33,000 e-h pairs

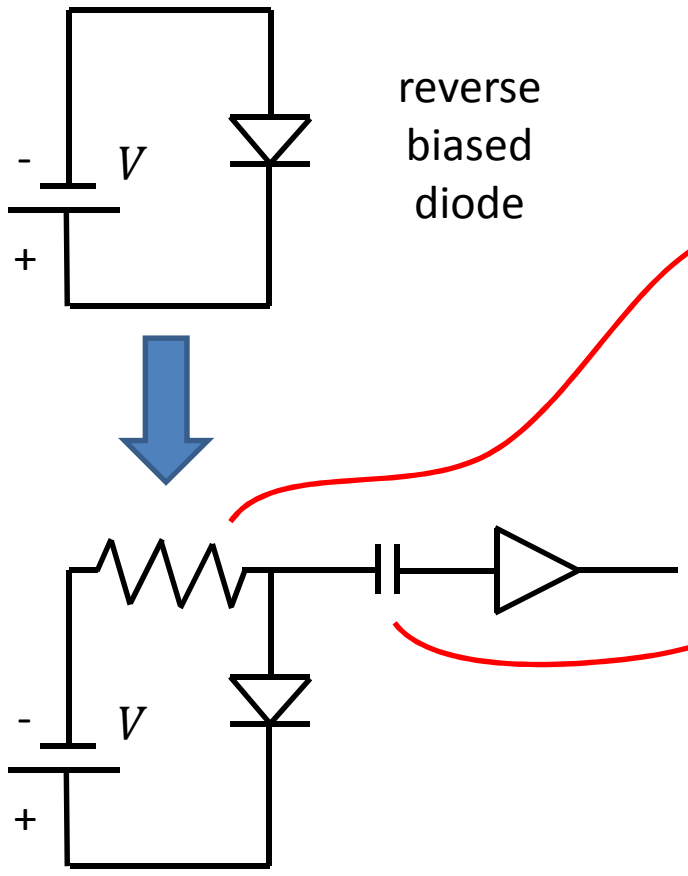
Signal Formation

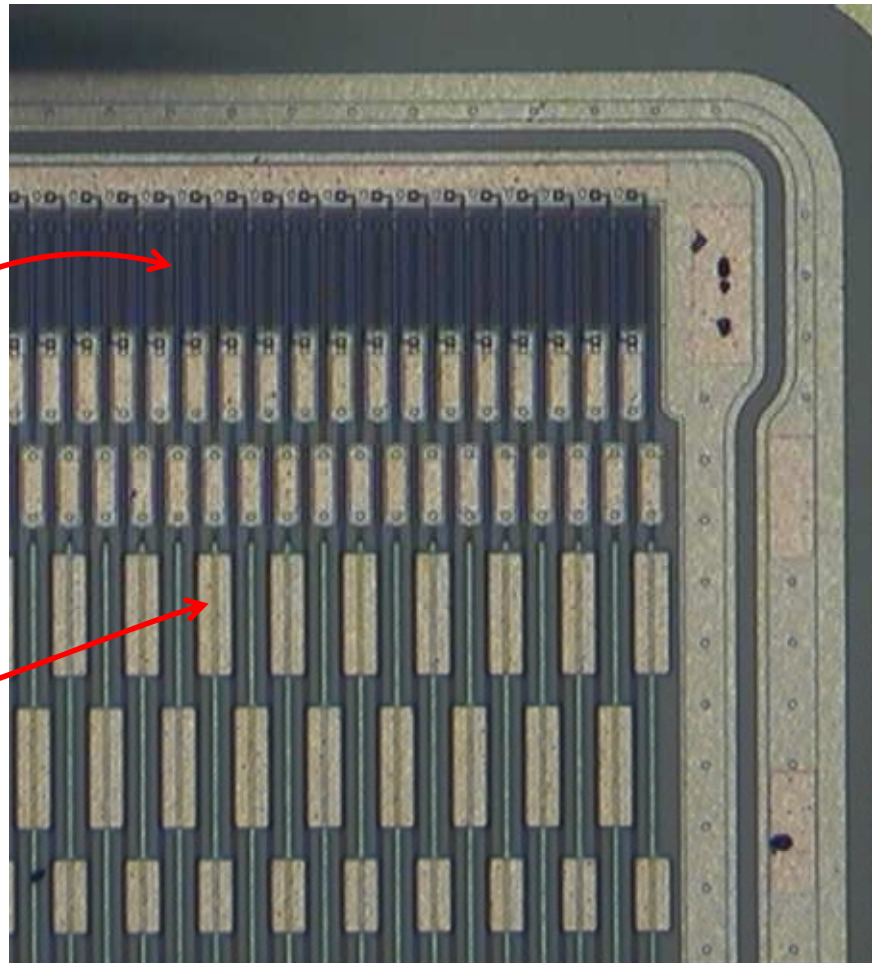


- Motion of charge carriers in the electric field induces a voltage pulse on the strips
- Current must flow to maintain constant potential difference
- Signal processing:
  - Amplification
  - Pulse shaping
  - Discrimination
  - Timing
  - Charge measurement

Signal Formation

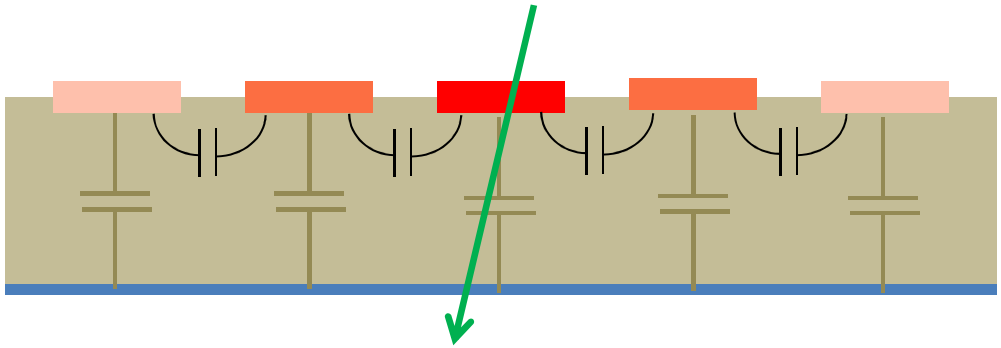
- Equivalent circuit:





Signal Formation

- Strips are long and parallel → capacitive coupling



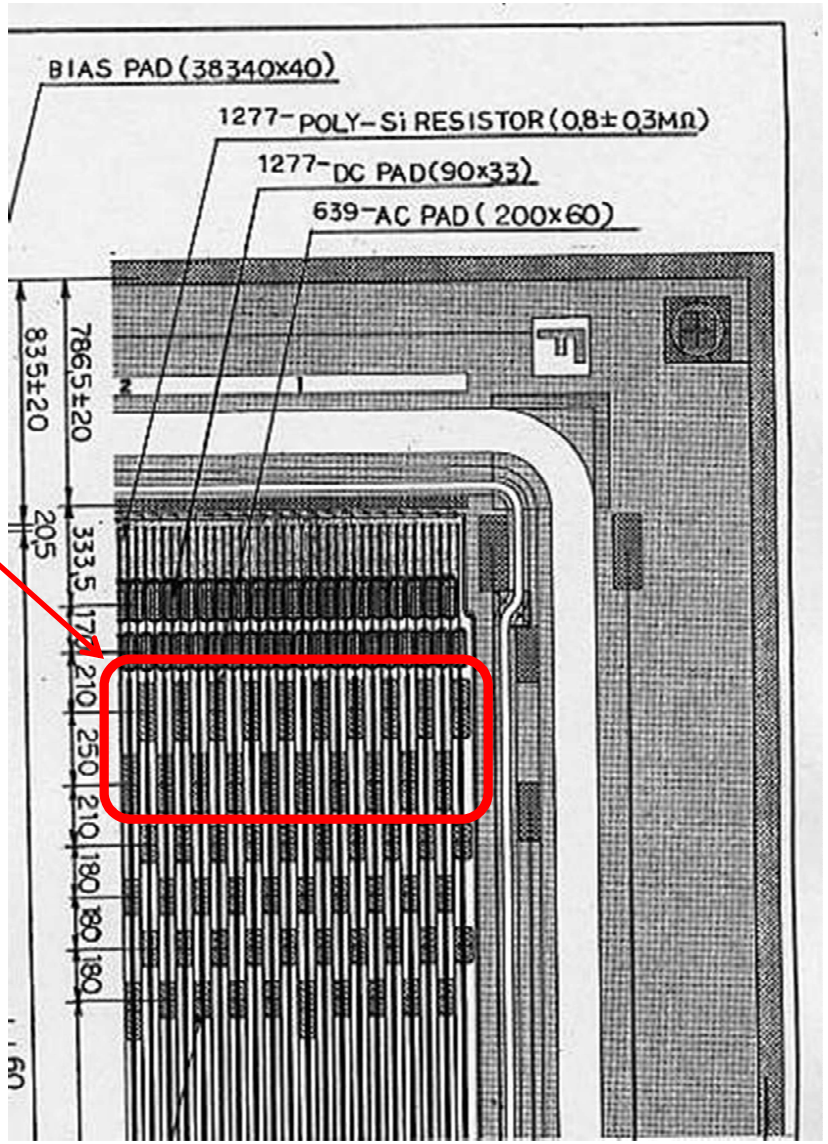
- Capacitance between strips i and $i \pm n$: C/n
- Signals will also be induced on adjacent strips
- Improved spatial resolution using weighted mean:

$$\bar{x} = \frac{\sum Q_i x_i}{\sum Q_i}$$

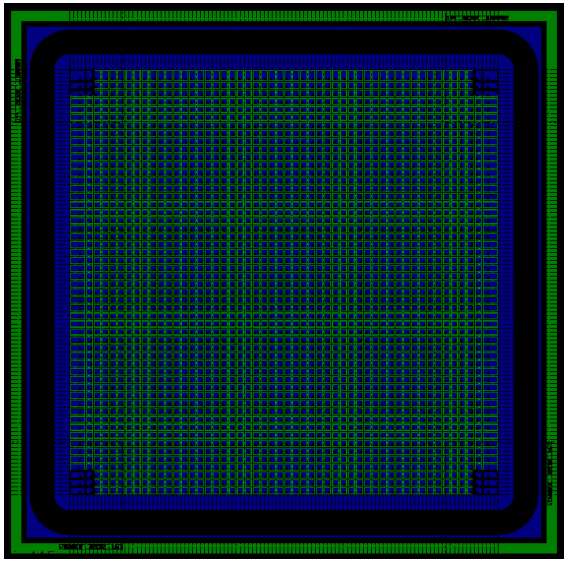
- *Not necessary to read out every strip.*

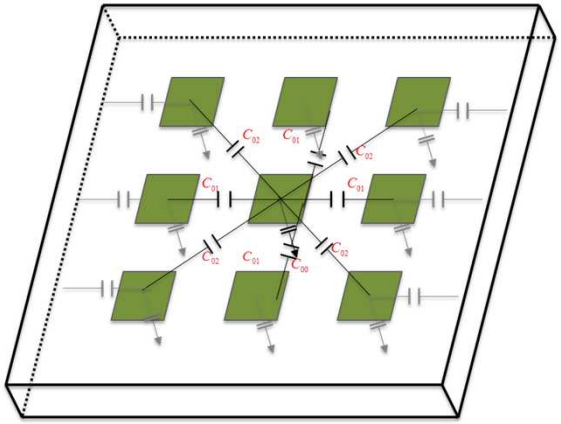
DØ Strip Sensor

- 320 µm thick
- 639 strips
- 30 µm strip pitch
- 60 µm readout pitch
- Sensitive area:
  3.8 cm x 9.8 cm
- Fully depleted at ~100 V



Comparison with Pixels





- Less symmetry
  - electric fields are more complex
- Capacitive coupling to adjacent pixels
  - Difficult to model based purely on geometry
- No space for large poly-silicon resistors
  - Readout chip must sink leakage current

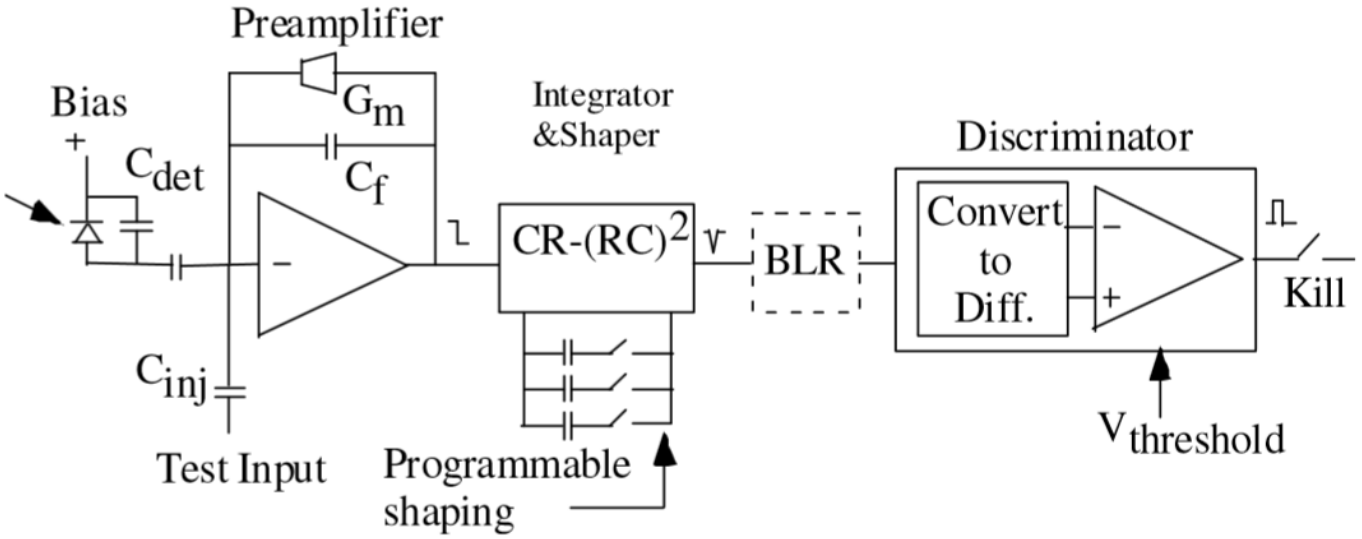
Silicon Sensor Readout

General Features

Readout chips are often required to provide:

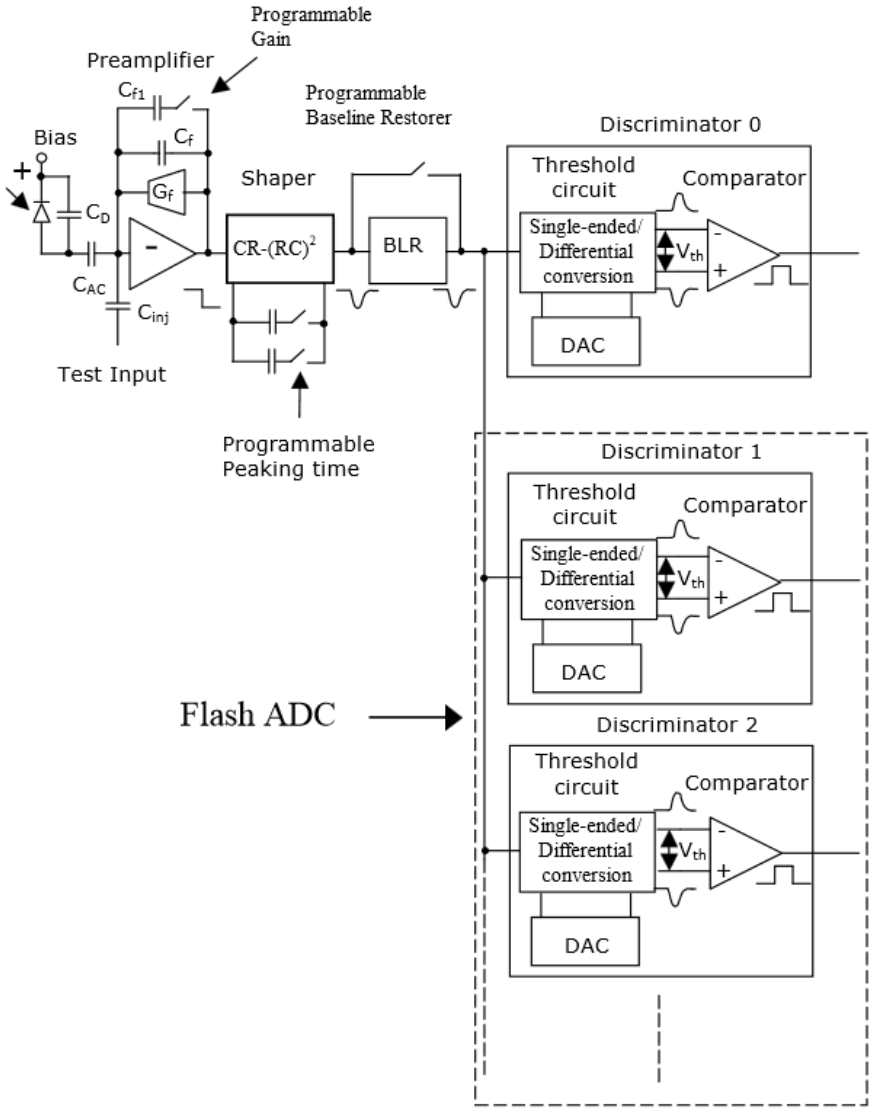
- Low thresholds
- Low noise
- Fast response
- Charge measurement
- Continuous or triggered readout
- Data buffering
- Configuration of internal voltages
- Ability to kill hot channels
- Calibration/trimming of thresholds

Example: FSSR2 Readout Chip



- Analog section replicated on 128 channels
- Configuration voltages shared among all channels
- Charge injection and kill feature provided on individual channels

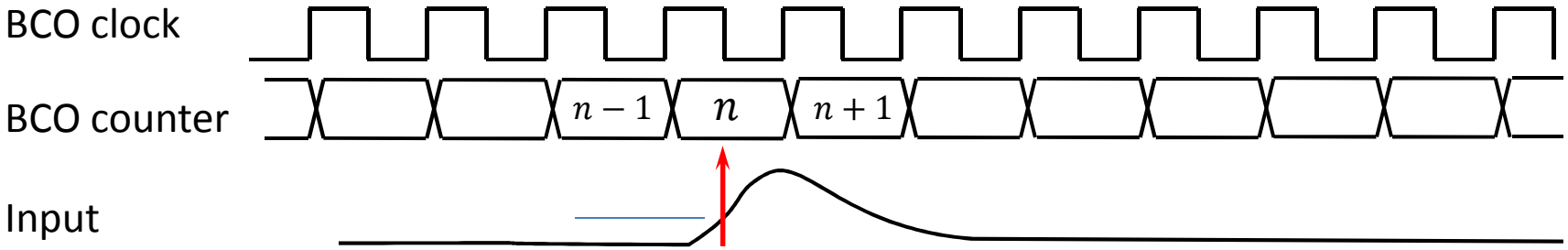
Example: FSSR2 Readout Chip



- Limited, but very useful charge measurement
- 8 programmable thresholds common to all channels
- Each hit strip provides 3 bits of ADC information.

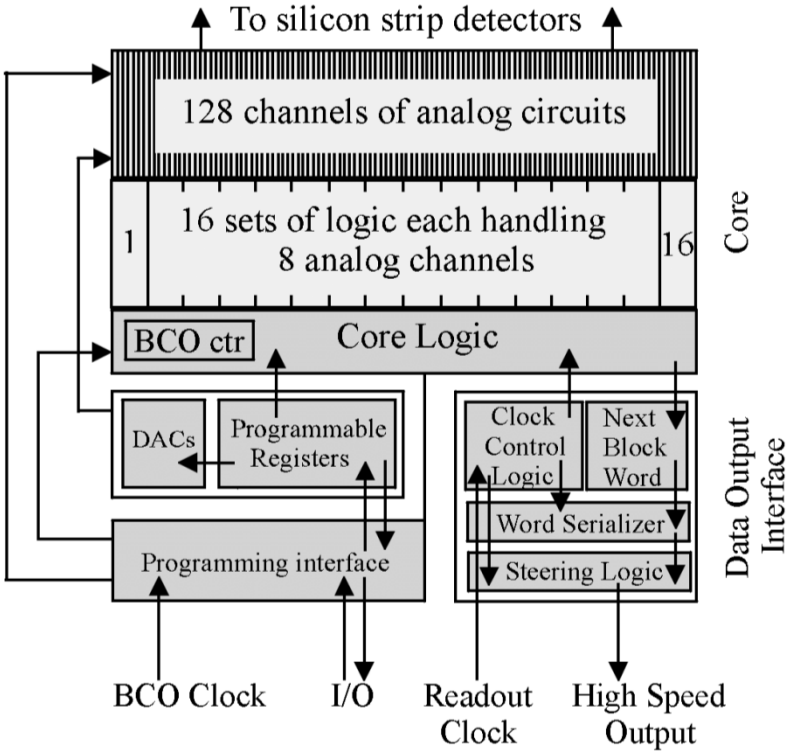
Example: FSSR2 Readout Chip

- Two alternative approaches:
  - External trigger initiates readout for a specific event
  - Each event is tagged with a time stamp that is common across all system components (data output is not time-ordered!)



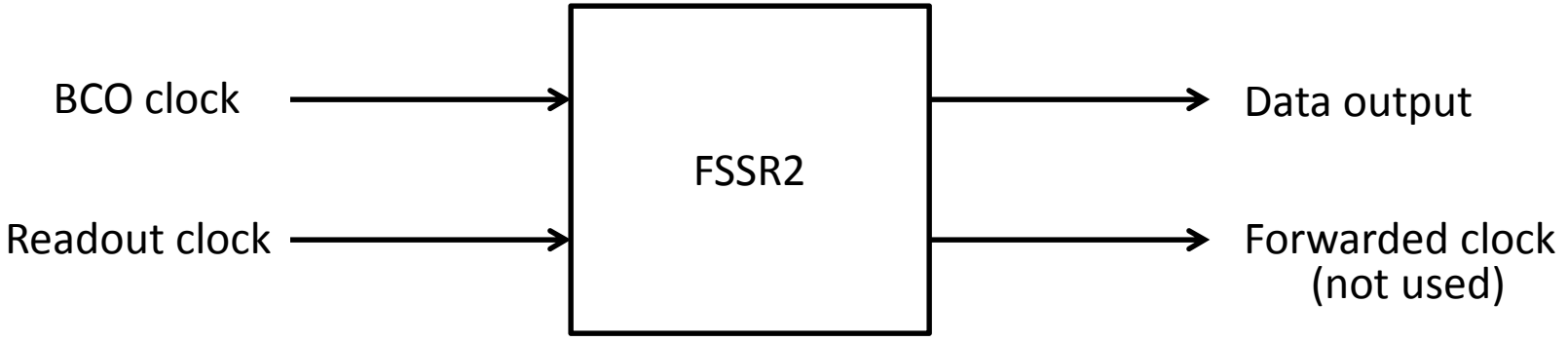
- Output data for each hit strip:
  - Channel number (128 channels → encoded using 9 bits)
  - ADC measurement (3 bits)
  - Beam crossing (time stamp/BCO) counter number (8 bits)

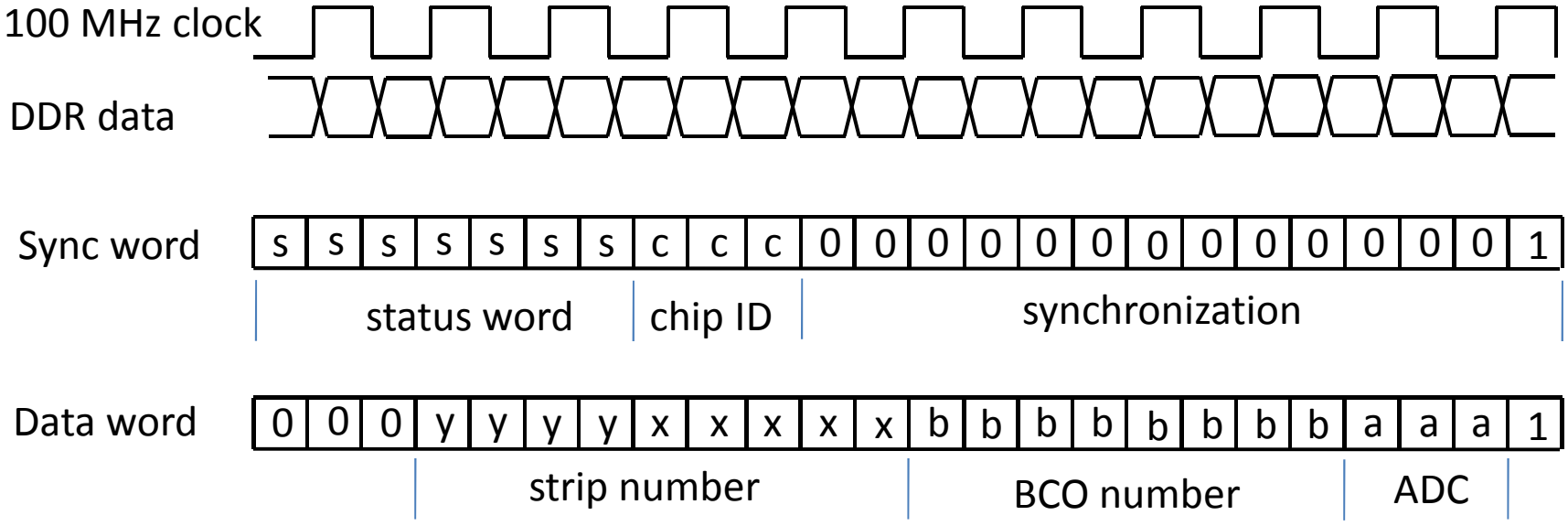
FSSR2 Readout Chip



- 0.25 µm CMOS process
- 128 analog inputs
- 8 programmable 8-bit thresholds
- Independent BCO and readout clocks
- Readout clock runs at up to 100 MHz
- DDR serial output on 1,2,4,6 LVDS pairs
- “Fast-OR” trigger output

FSSR2 Readout



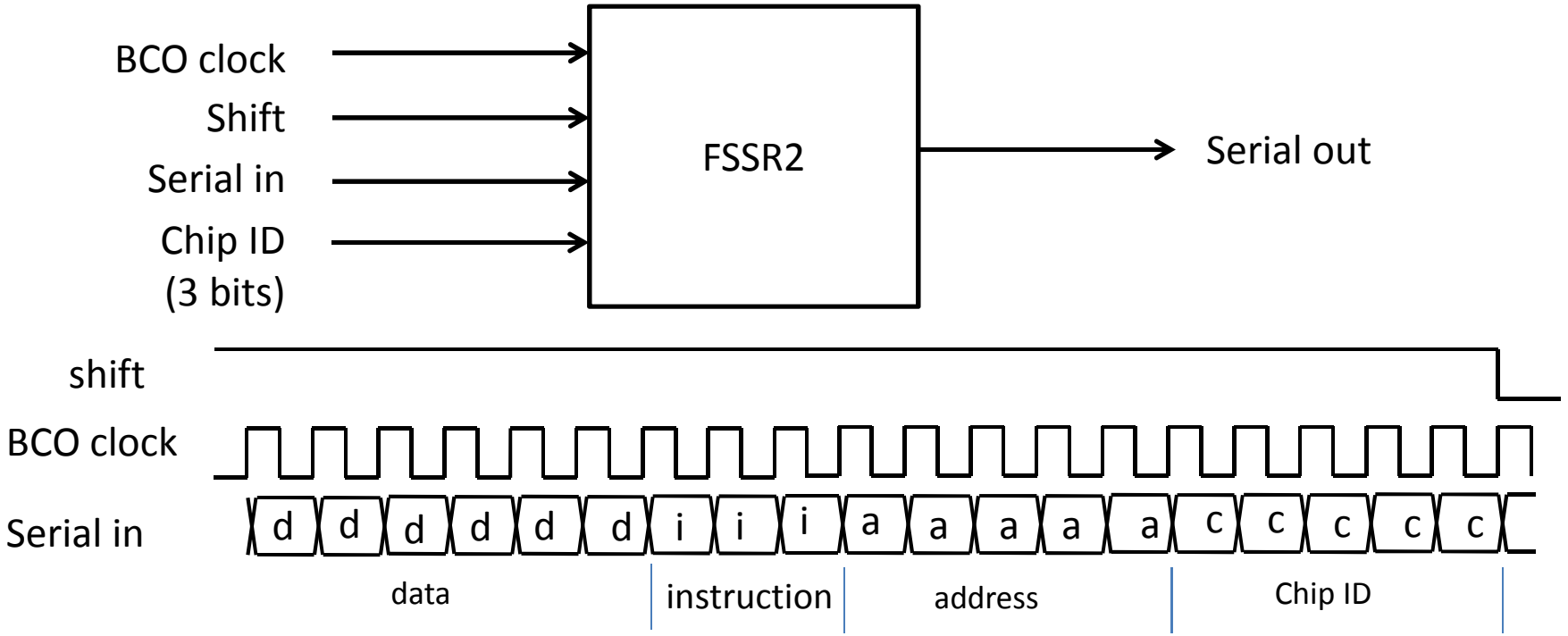


FSSR2 Configuration

	No.	Register	Default	Notes
DAC's	1	Pulser Data	0	
	2	Pulser Control	0	
	3	Integrator Vbn	139	Rarely changed
	4	Shaper Vbp2	116	
	5	Shaper Vbp1	121	
	6	Base-line Restorer Vbp1	80	
thresholds	7	Discriminator Vtn	FF	
	8	Discriminator Vtp<0>	0	
	9	Discriminator Vtp<1>	0	
	10	Discriminator Vtp<2>	0	
	11	Discriminator Vtp<3>	0	
	12	Discriminator Vtp<4>	0	
	13	Discriminator Vtp<5>	0	
	14	Discriminator Vtp<6>	0	
	15	Discriminator Vtp<7>	0	
configuration	16	Active Lines	0	0= 1 Line, 1= 2 Lines, 2= 4 Lines, 3= 6 Lines
	17	Kill Select	N/A	
	18	Inject Select	N/A	
	19	Send Data	0	0= Send No Data 1= Send Data
	20	Reject Hits	1	0= Accept Hits 1= Reject Hits
	24	Smart Programming Reset	N/A	
	27	Digital Control Register	0	
	28	Smart Core Reset	N/A	Default Command = Reset Hits Reset Command = Reset BCO Counter Set Command = Reset Hits and BCO Counter
	30	Acquire BCO Number	0	

FSSR2 Configuration

- Chip configuration is a relatively “slow” operation
- Most registers are changed only after power up or reset
- High speed interface not required



Comparison with other ROC Interfaces

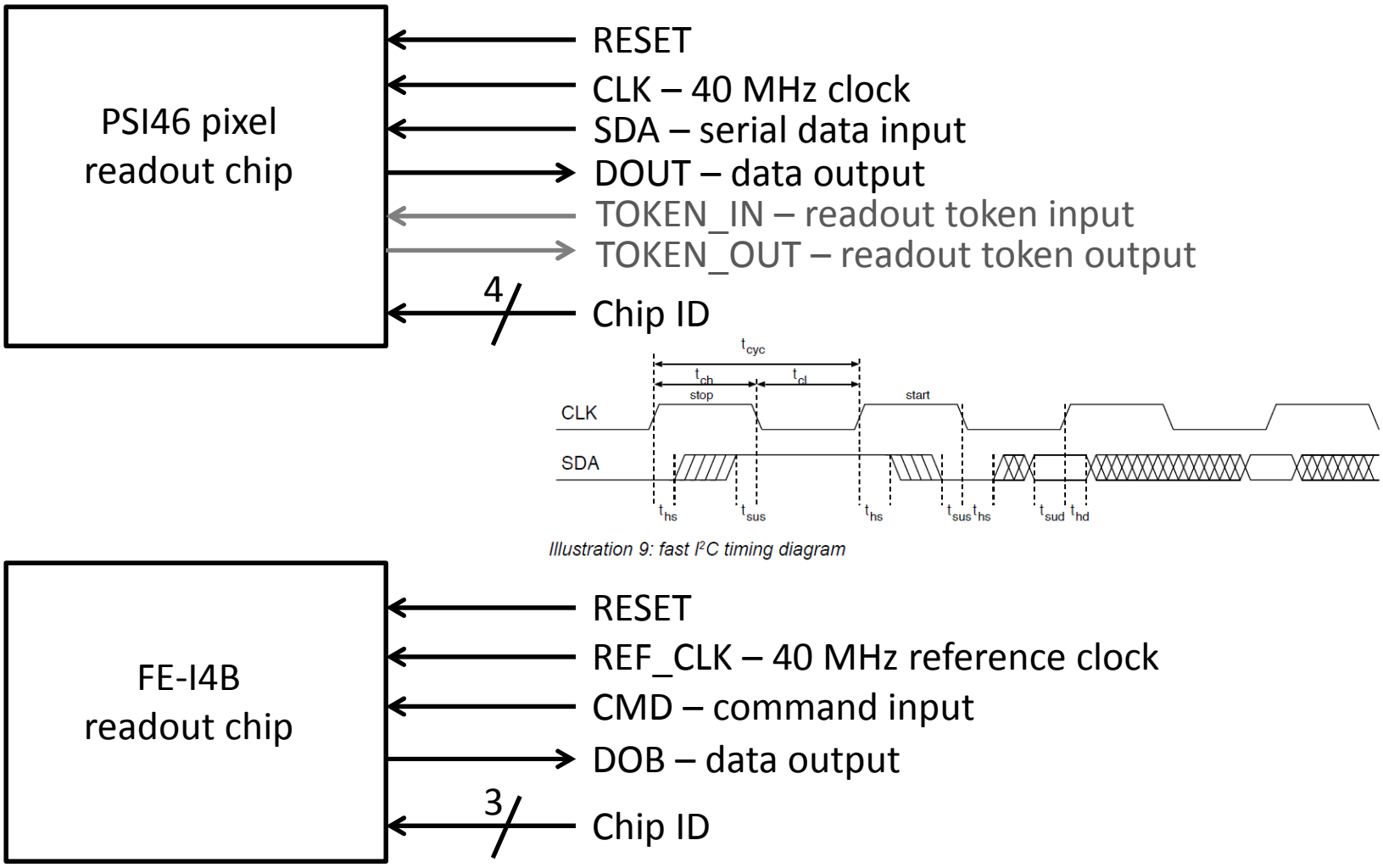
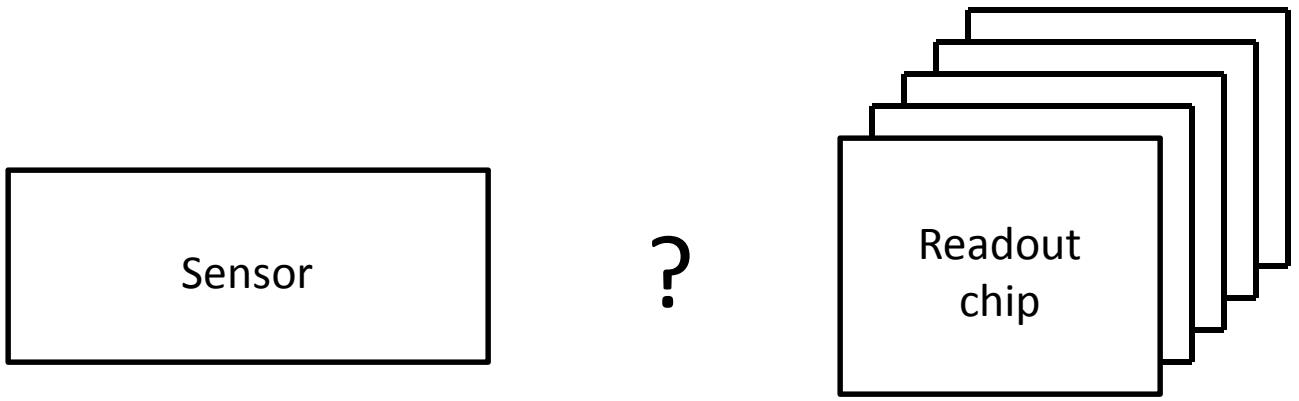


Illustration 9: fast I²C timing diagram

Intermission

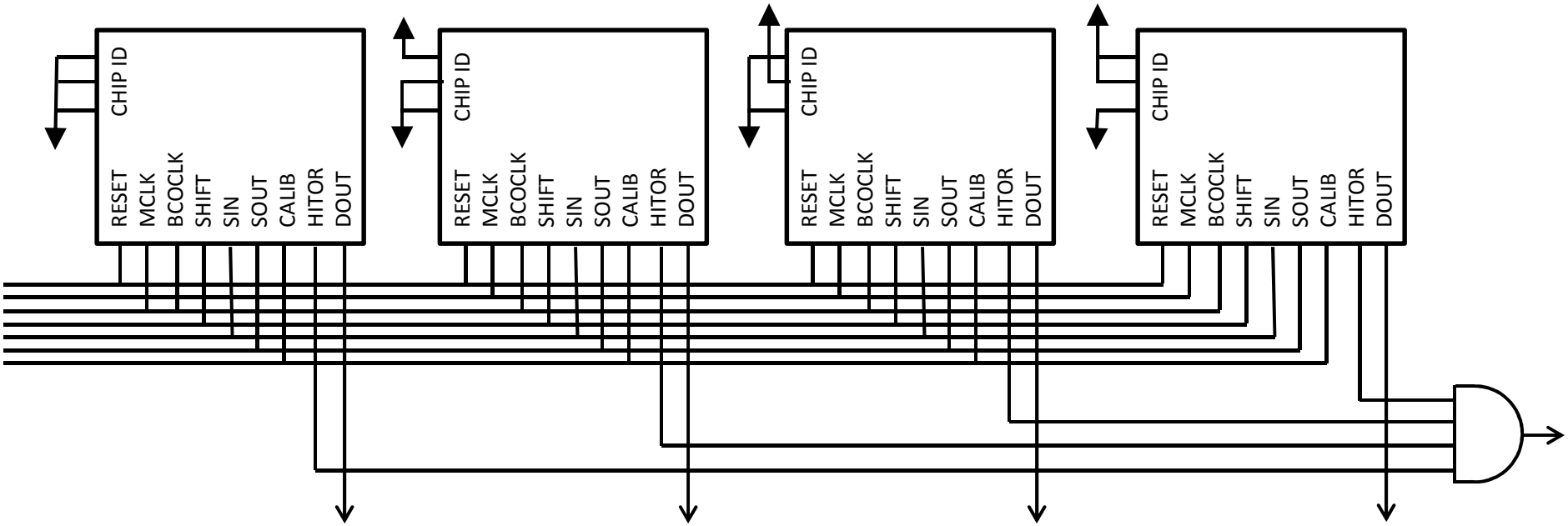
Readout Systems

Detector and Readout Systems



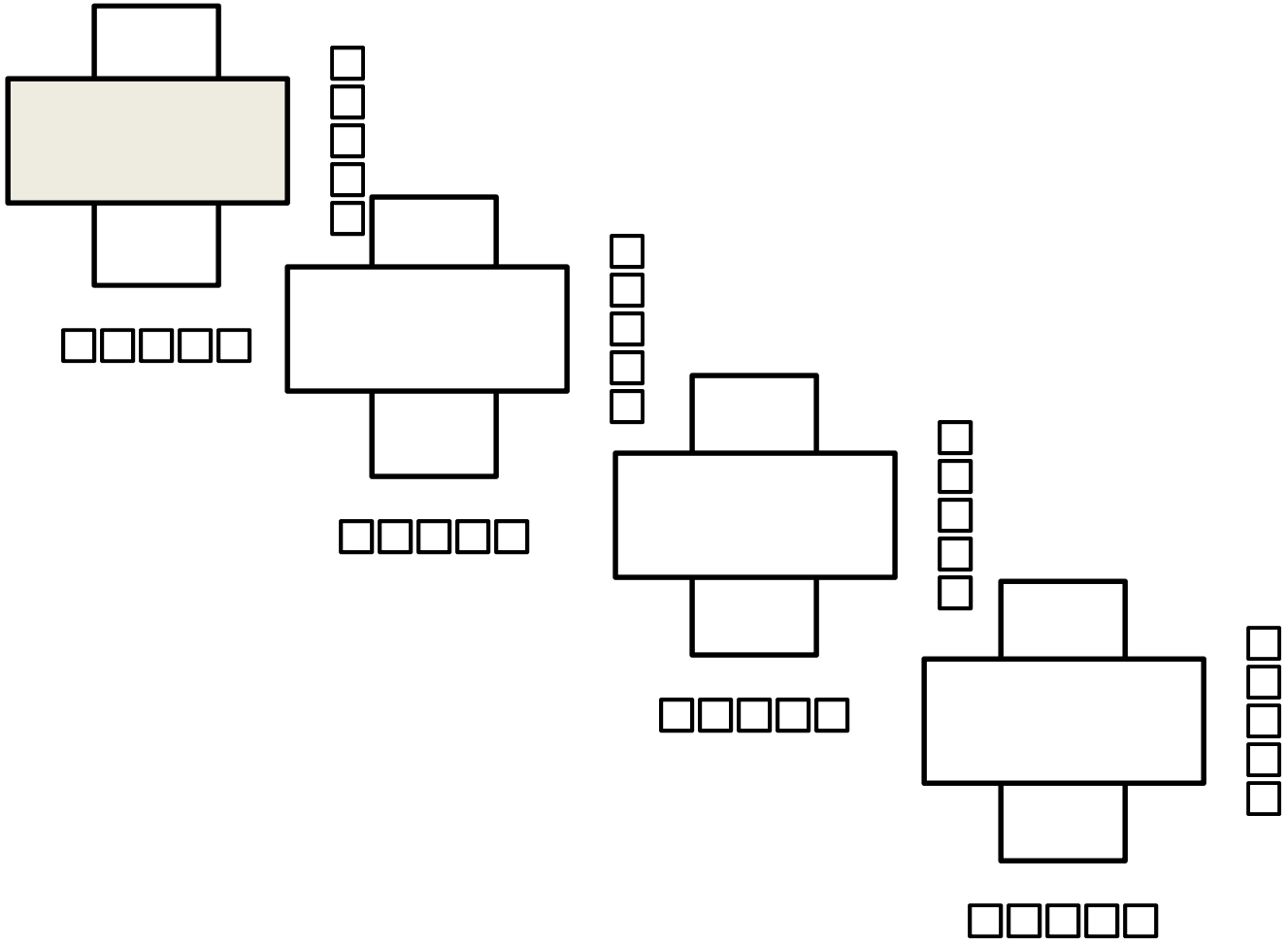
This just instruments one sensor…

Sensor Module Interface



- "Slow" signals can be bussed
  - Reset and clock signals common to all chips
  - Serial input addresses individual chips by chip ID
- Fast outputs can:
  - Drive individual pairs of conductors
  - Processed on the module (simple logic or complex ASIC)
  - Share a common bus (requires additional logic to coordinate)

Detector Readout Systems



Detector Readout Systems

- Recognize the natural hierarchy
  - Development of detector system “modules”
- Simplifies design and construction
  - Independent testable units
  - Minimize impact of single component failures
- Identify interconnects between components
  - Equally important aspect of system design
- Multiple parallel hierarchies:
  - Sensors and readout
  - Power distribution
  - Slow controls/safety monitoring
  - Cooling

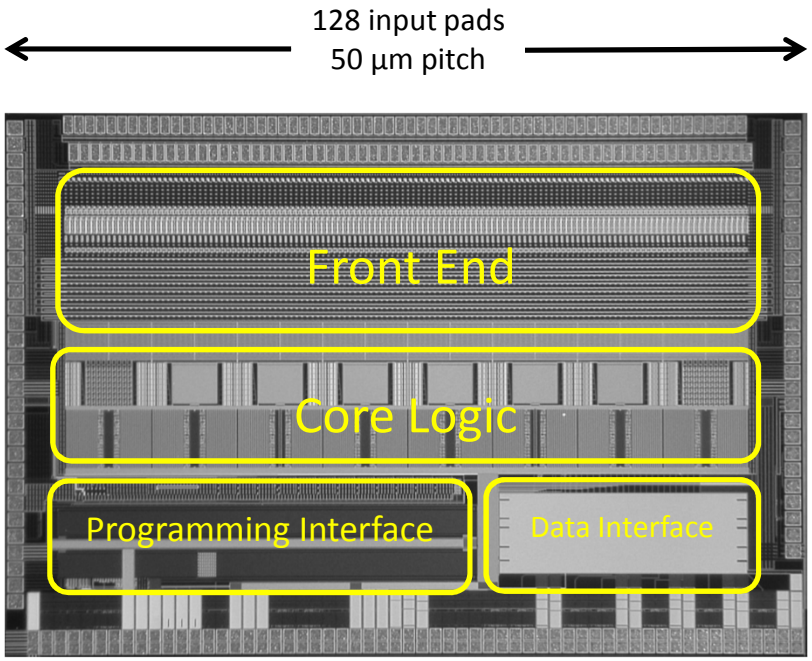
Module Assembly Methods

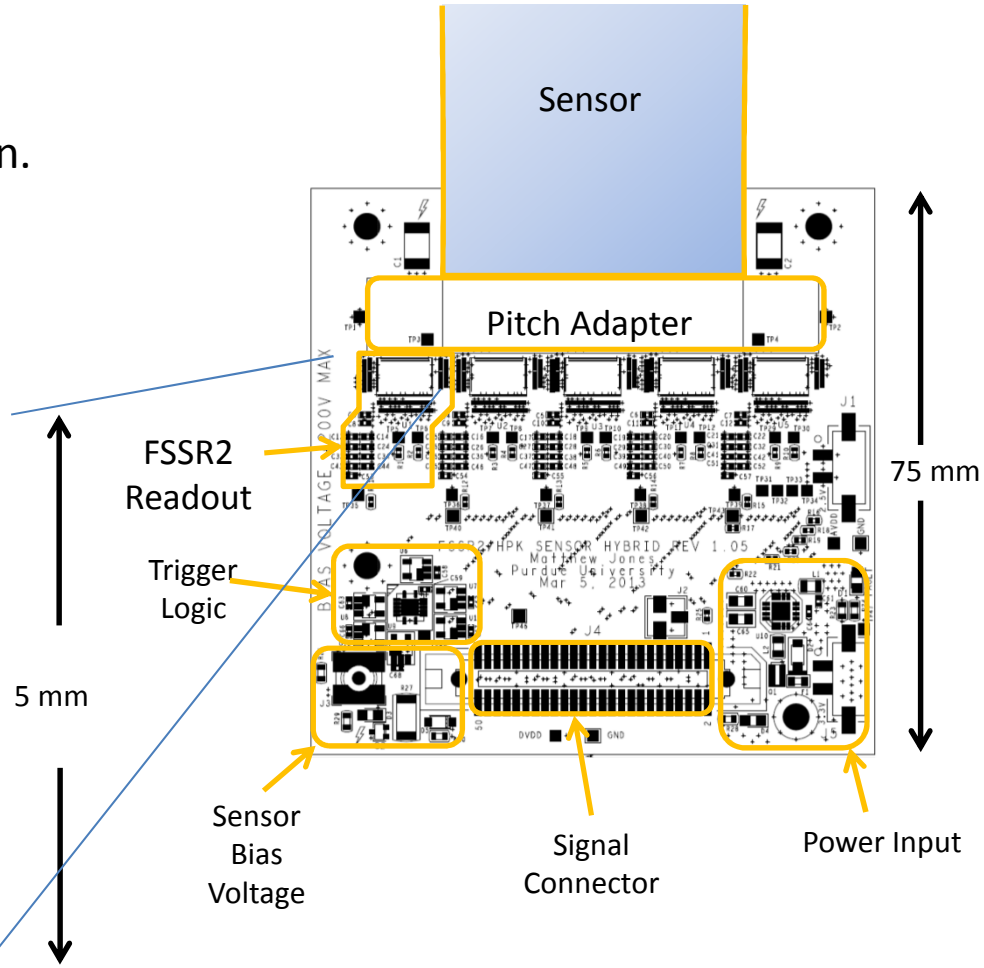
- Components mounted on a substrate material
  - Conventional PCB or low mass hybrid material
  - Might provide mechanical stability
- Connections typically made by wire bonds
  - Important to design so that wire bonding is possible
- Tradeoffs:
  - Complex, highly integrated module
    - Higher risk during design phase
    - Manufacturing yield
    - Simpler to assemble into system
  - Module constructed from tested components:
    - Simpler to design
    - Re-workable?
    - More complex assembly process

Sensor/FSSR2 module

FR4 printed circuit board:

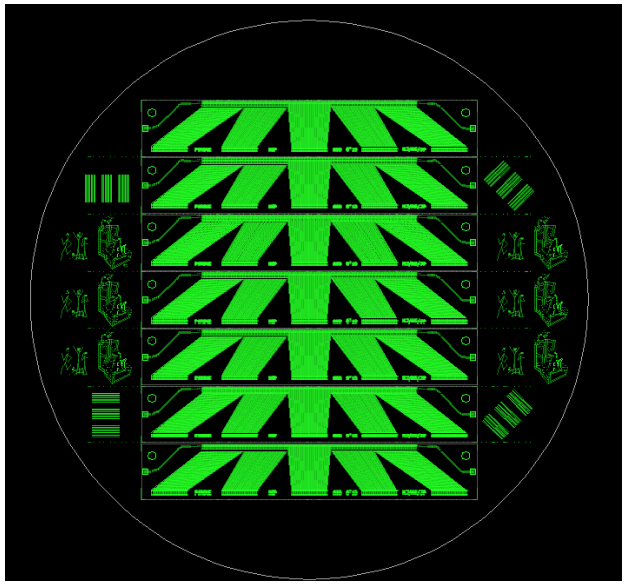
- 4-layers (sig, sig, gnd, pwr)
- 3 mil (76 µm) minimum trace width/spacing.
- Input voltage protection and regulation.
- Individual chip ID's defined by layout.

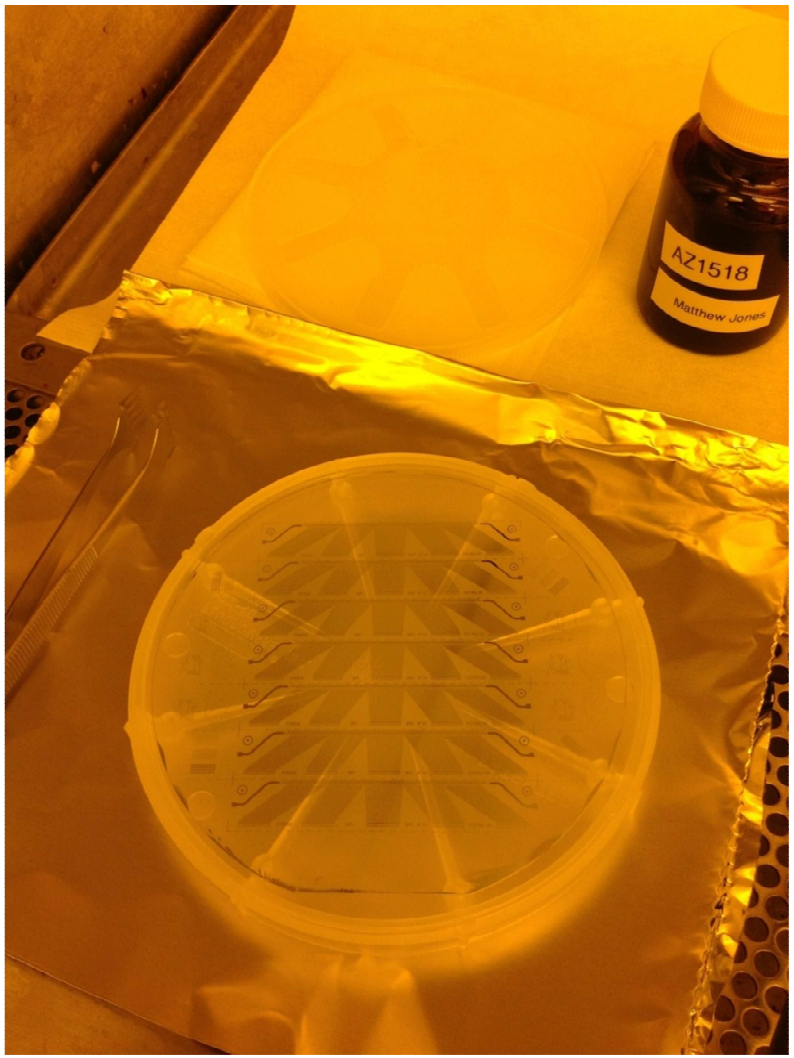




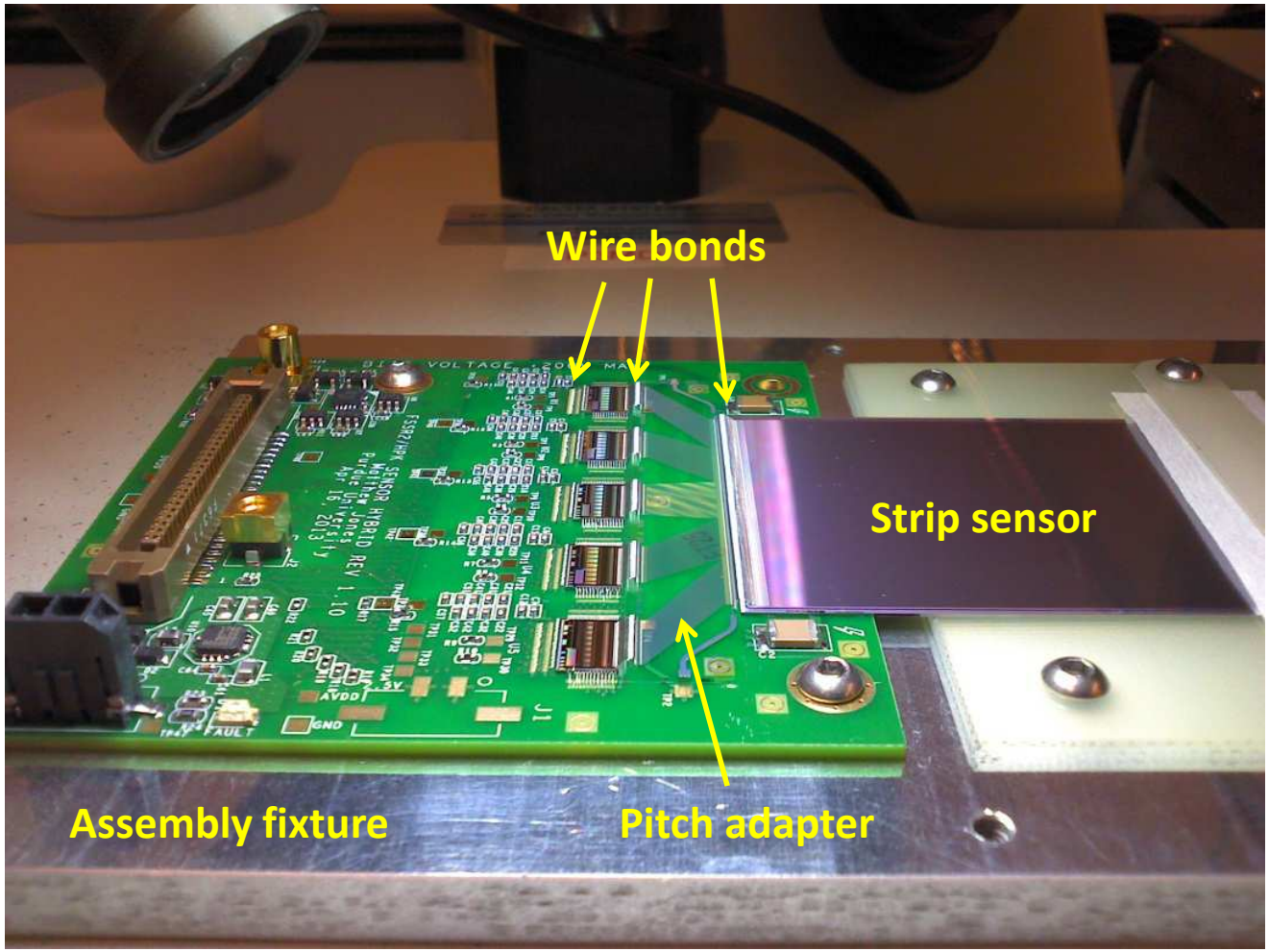
FSSR2 Pitch Adapter

- 500 µm thick borosilicate glass substrate
- 30 nm Ti + 1 µm Aluminum
- Line width: 15 µm
- Smallest spacing space: 11 µm
- *Conventional lithography and wet etching using university clean room facilities.*
- *Large volume commercial production can sometimes present a challenge.*

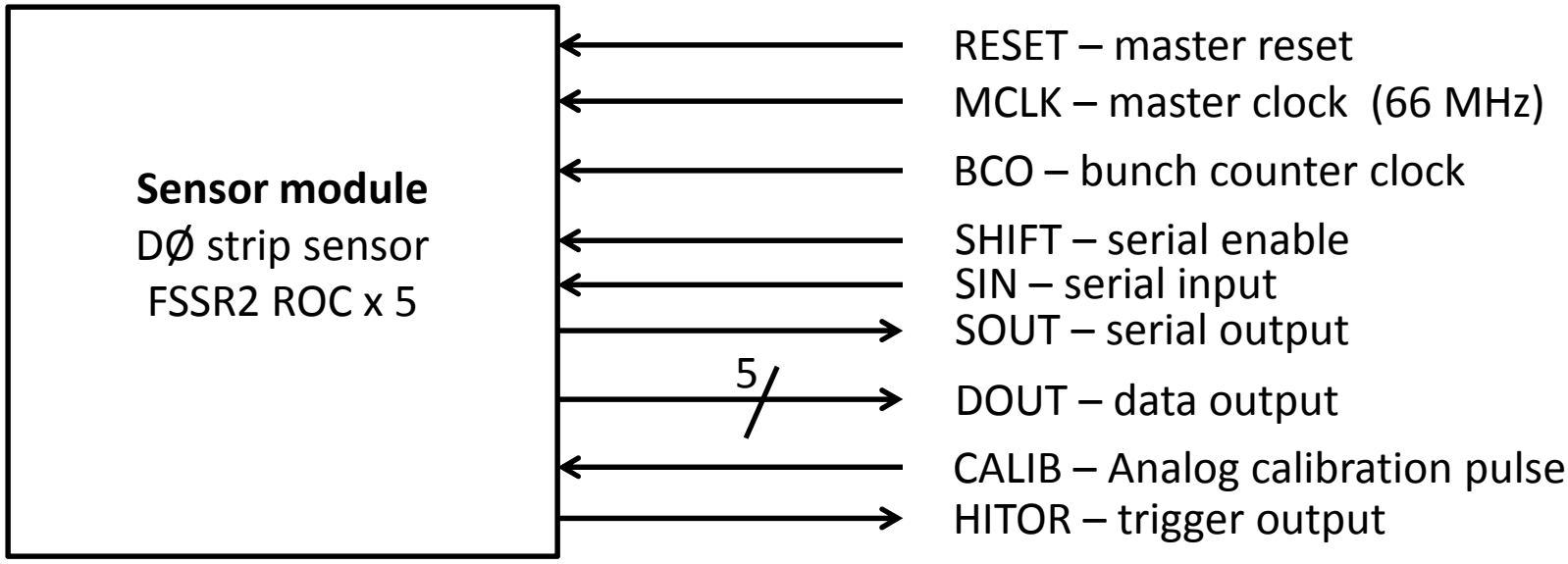




Sensor Module Assembly



Sensor Module Interface



- All signals are LVDS differential pairs
- Output drivers on readout chips interface directly with cable
- Serial input/output multiplexed between 5 readout chips

Module Interface

- Each module requires
  - Reset and clock signals
  - Serial interface for programming
  - Analog calibration pulse, driven using a DAC

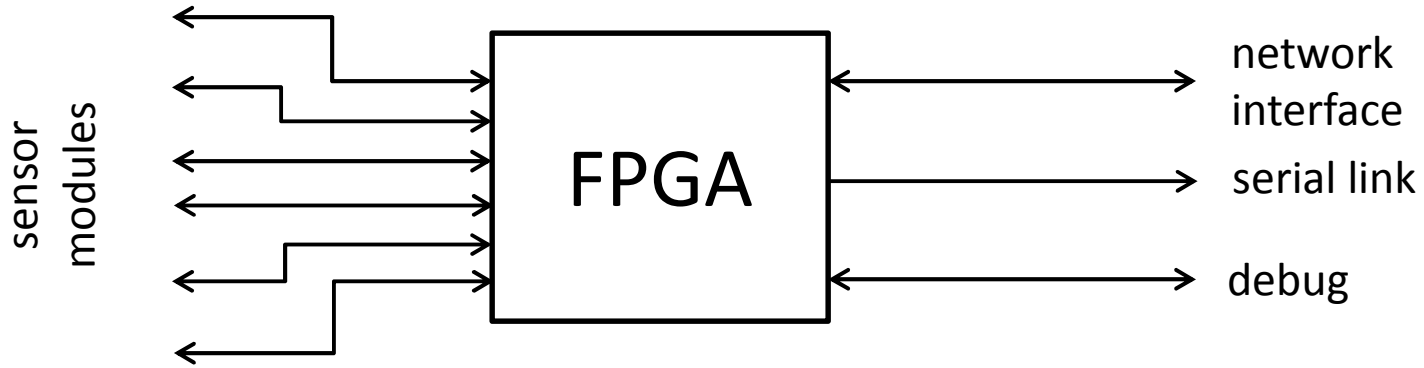
  } 8 pairs

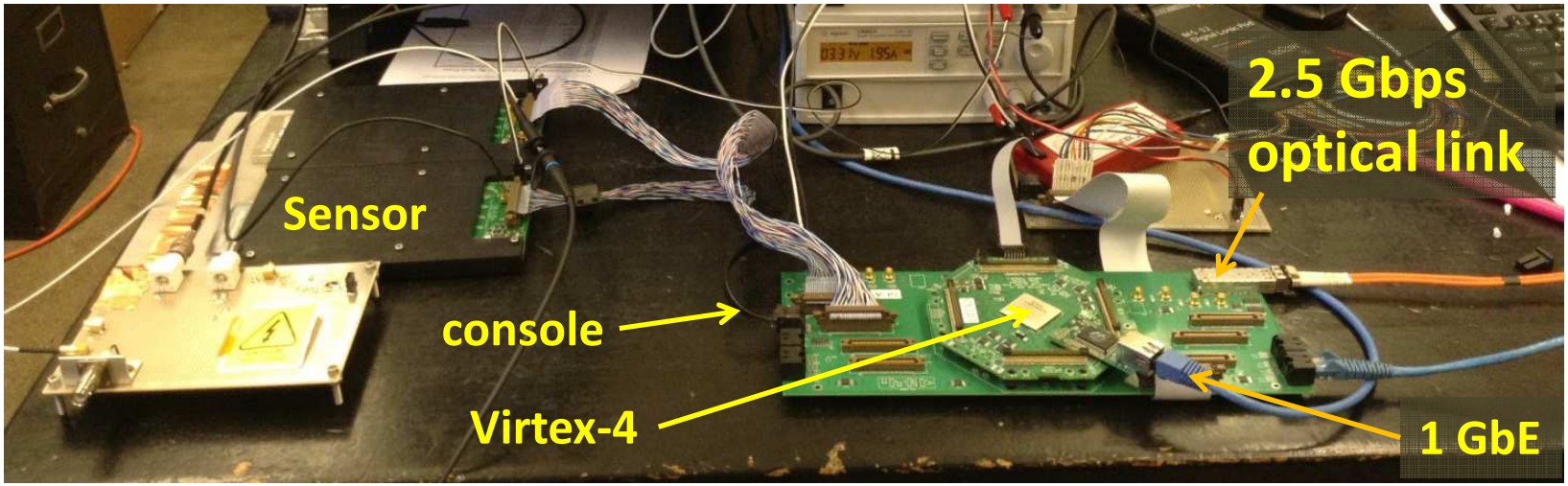
- Each module provides
  - Trigger output
  - Digitized strip data

  } 2 (or 3) pairs

- Digital interfaces are most conveniently provided using programmable logic
  - ***Xilinx***
  - Altera
  - Actel, Microsemi (IGLOO2), …

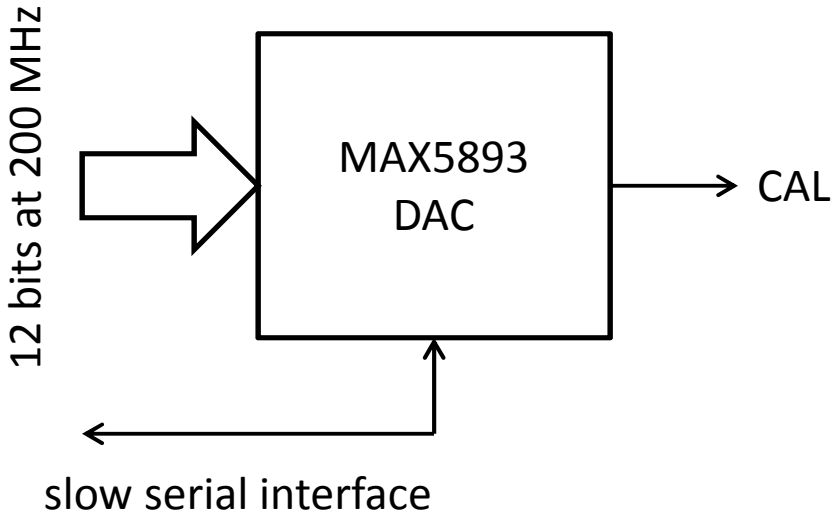
Readout Architecture





Support Circuits

- An analog calibration pulse can inject charge into selected channels.
- FPGA drives a DAC:



- Modern FPGAs can drive network interfaces directly (eg. Virtex-6 series)
  - Interface only to dedicated pins
  - Requires stable reference clock
- Alternatively, use dedicated interface components with a parallel data interface to FPGA:
  - Marvell 88M1111 GbE interface
  - TLK3101 2.5 Gb serializer/deserializer
  - Drives COTS SFP+ module for physical interface

Data Buffering

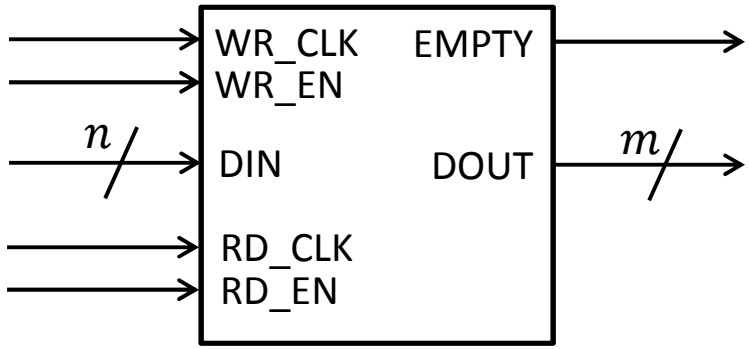
General problems:

Instantaneous input data rate exceeds output bandwidth

Different input and output clock domains

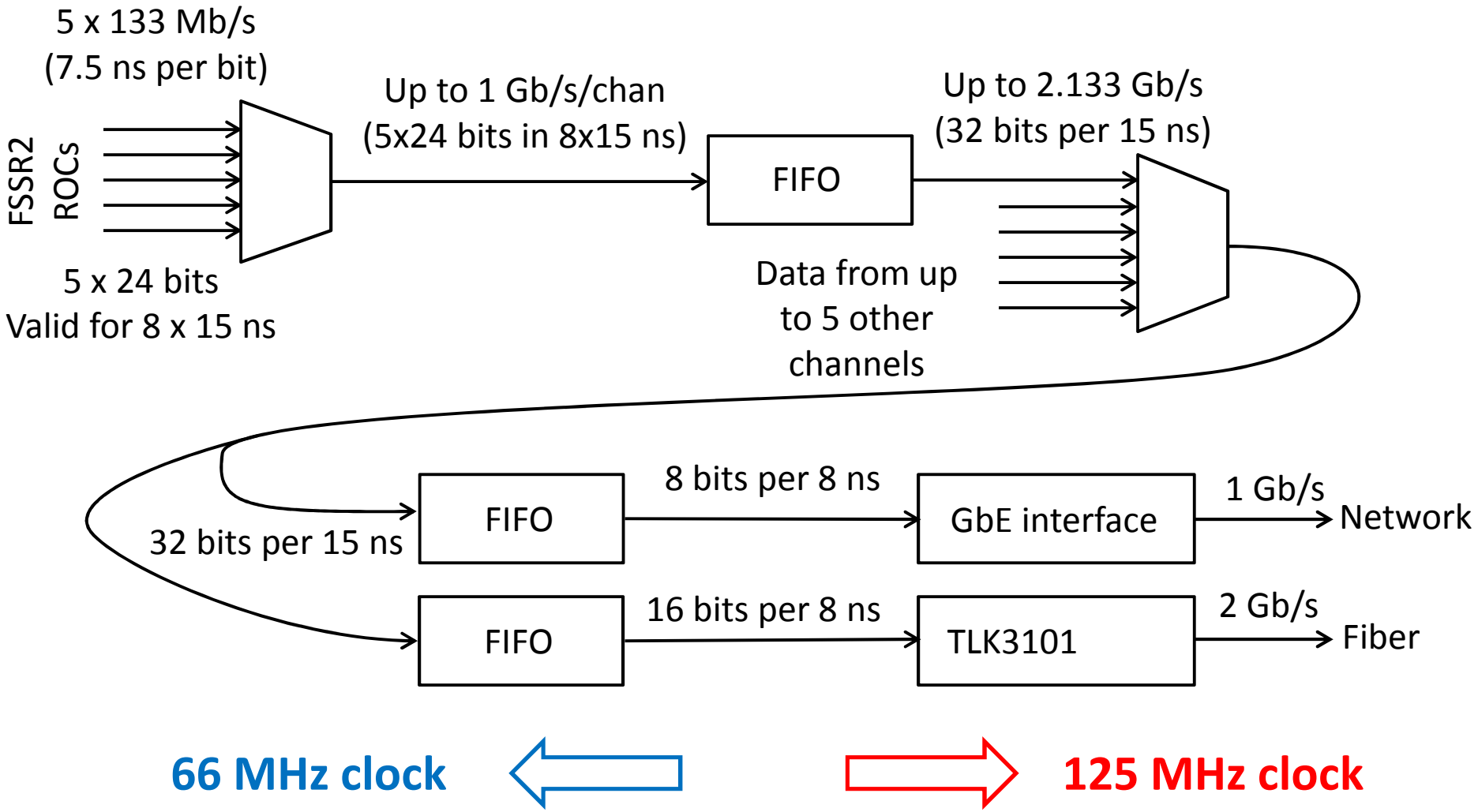
FIFO architecture:

Dual port RAM with independent, sequential address pointers.

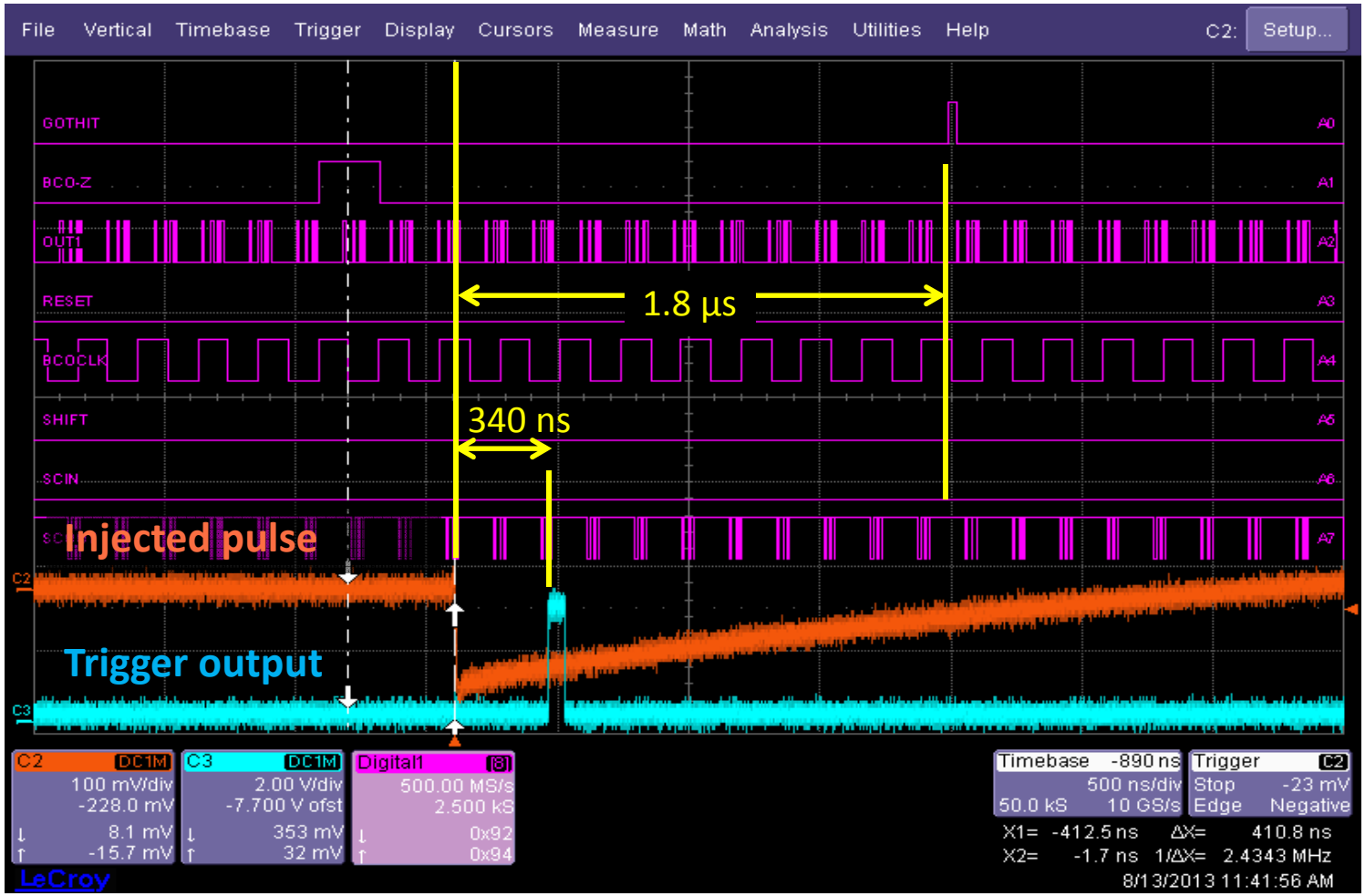


Output bandwidth must exceed input bandwidth (on average).

Data Buffering

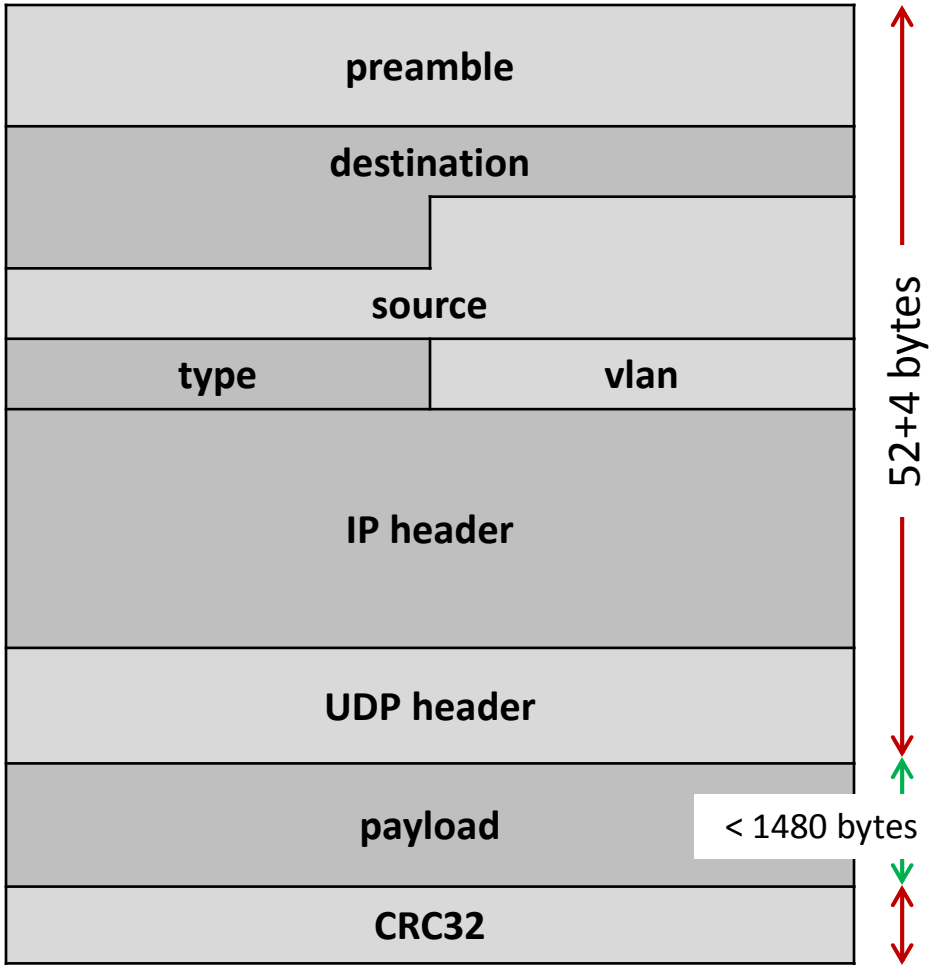


Fast Trigger Signal



Serial Data Transfer

- Framed data:
  - Well defined format
  - Routable on standard networks (eg. Ethernet)
  - Latency
  - Efficiency
- Streaming data:
  - Point-to-point links
  - Low latency
  - Word alignment



Output Data

- Self describing 32-bit words
  - Hit strip data

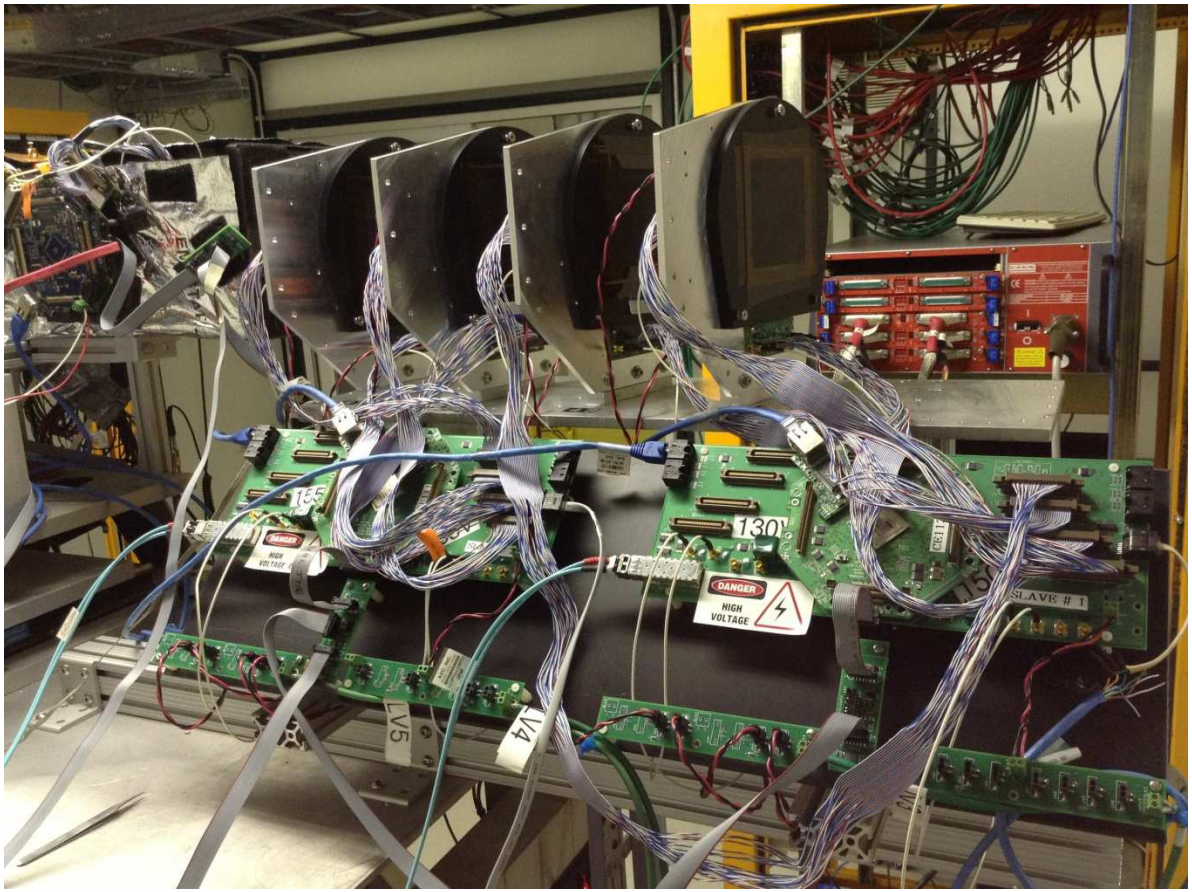
8 bits: STIB + channel + chip	9 bit strip #	3 bit ADC	8 bit BCO

  - 48-bit BCO counter is read out within 128 clock cycles of any strip or trigger data
  - Trigger inputs

8 time bins, input n+1	8 time bins, input n	8 bit BCO

  - 40-bit trigger number
  - Other definitions for DUT data
    - PSI-46
    - FE-I4B
    - Others?

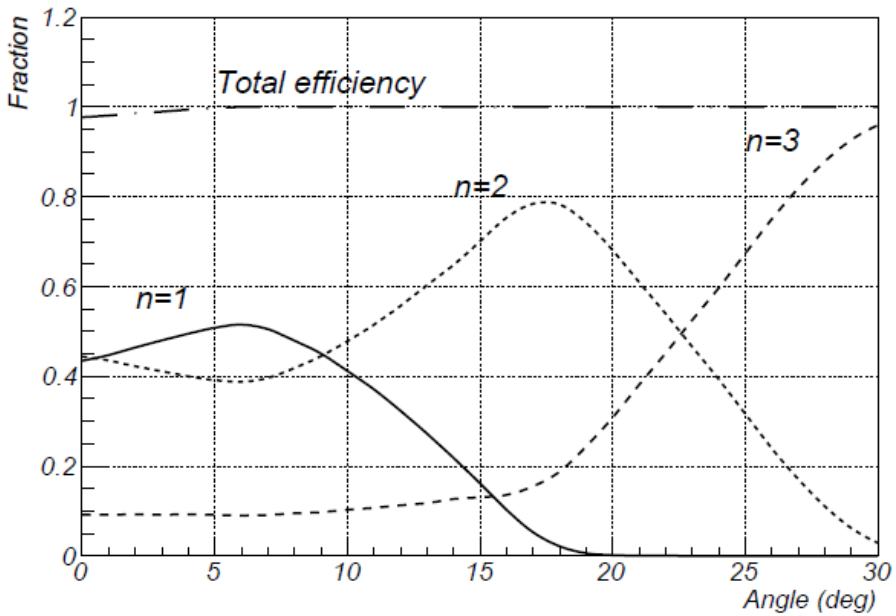
Test Beam Facility

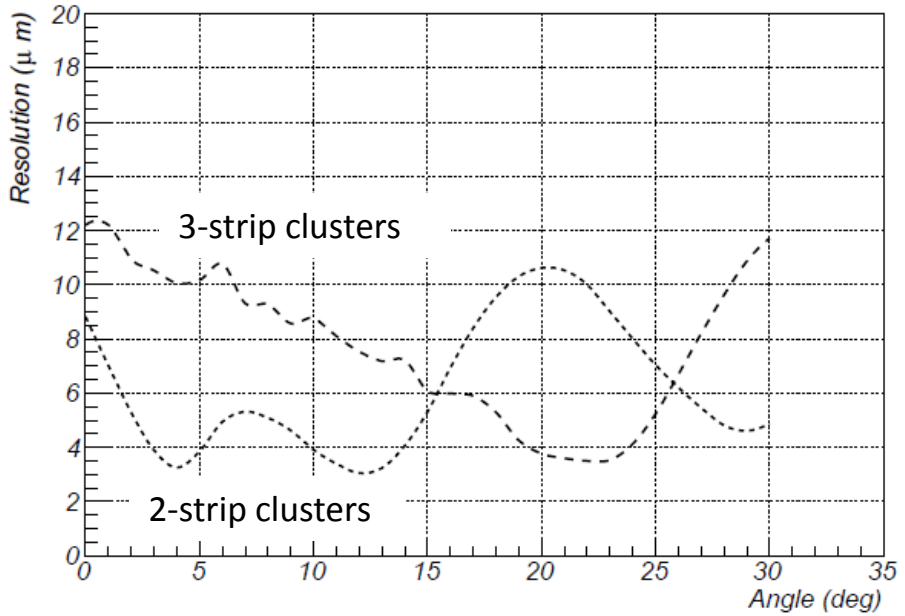


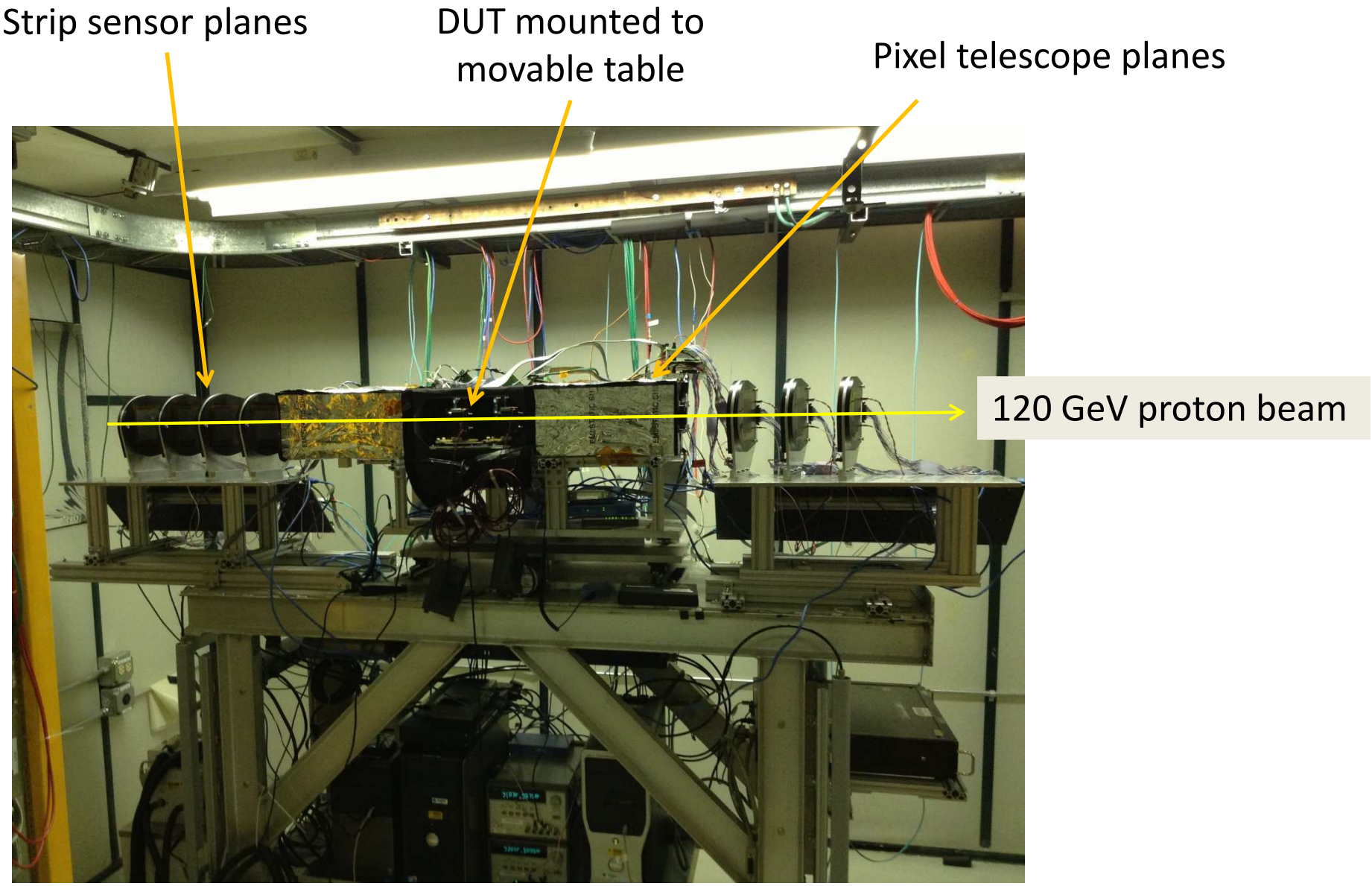
Event Reconstruction

- Serial data is sorted by BCO number to form events
- Hits are sorted by strip number to form clusters

$$\bar{x} = \frac{\sum Q_i x_i}{\sum Q_i}$$





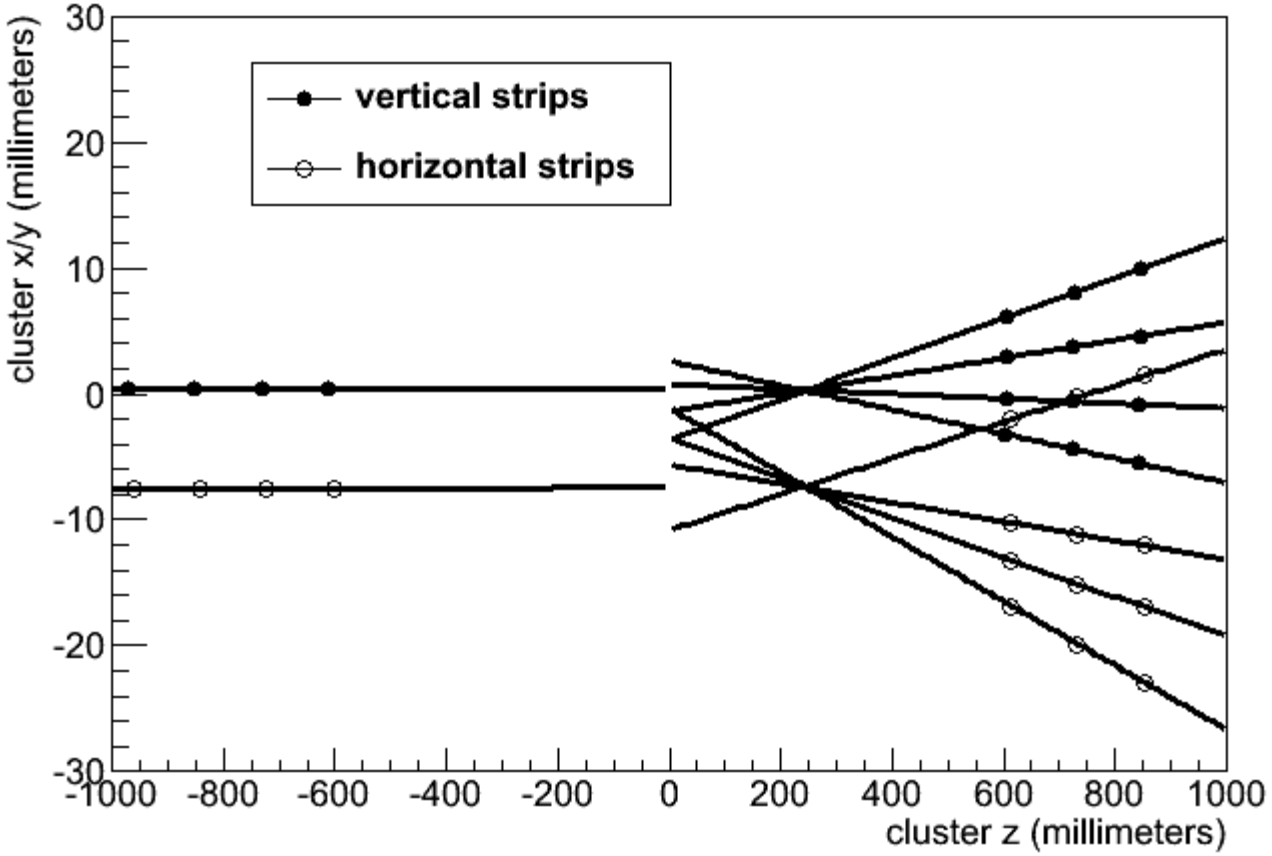

Strip sensor planes
DUT mounted to movable table
Pixel telescope planes
120 GeV proton beam

DUT Mounting Assembly

Larger DUT assemblies may be mounted using the telescope plane mechanics.

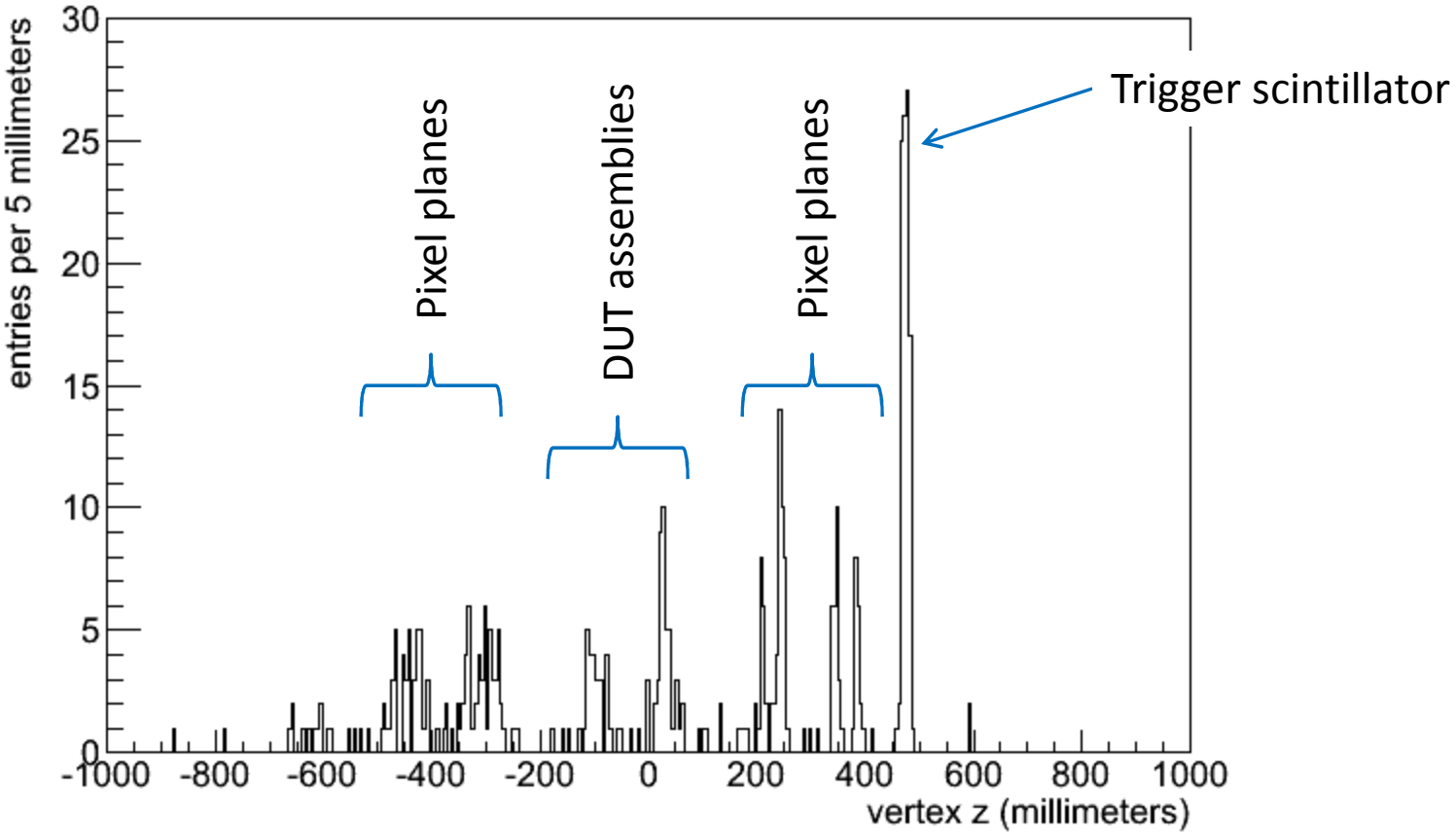
Event Example

Low occupancy – pattern recognition is relatively easy.
Track fit using Kalman filter.

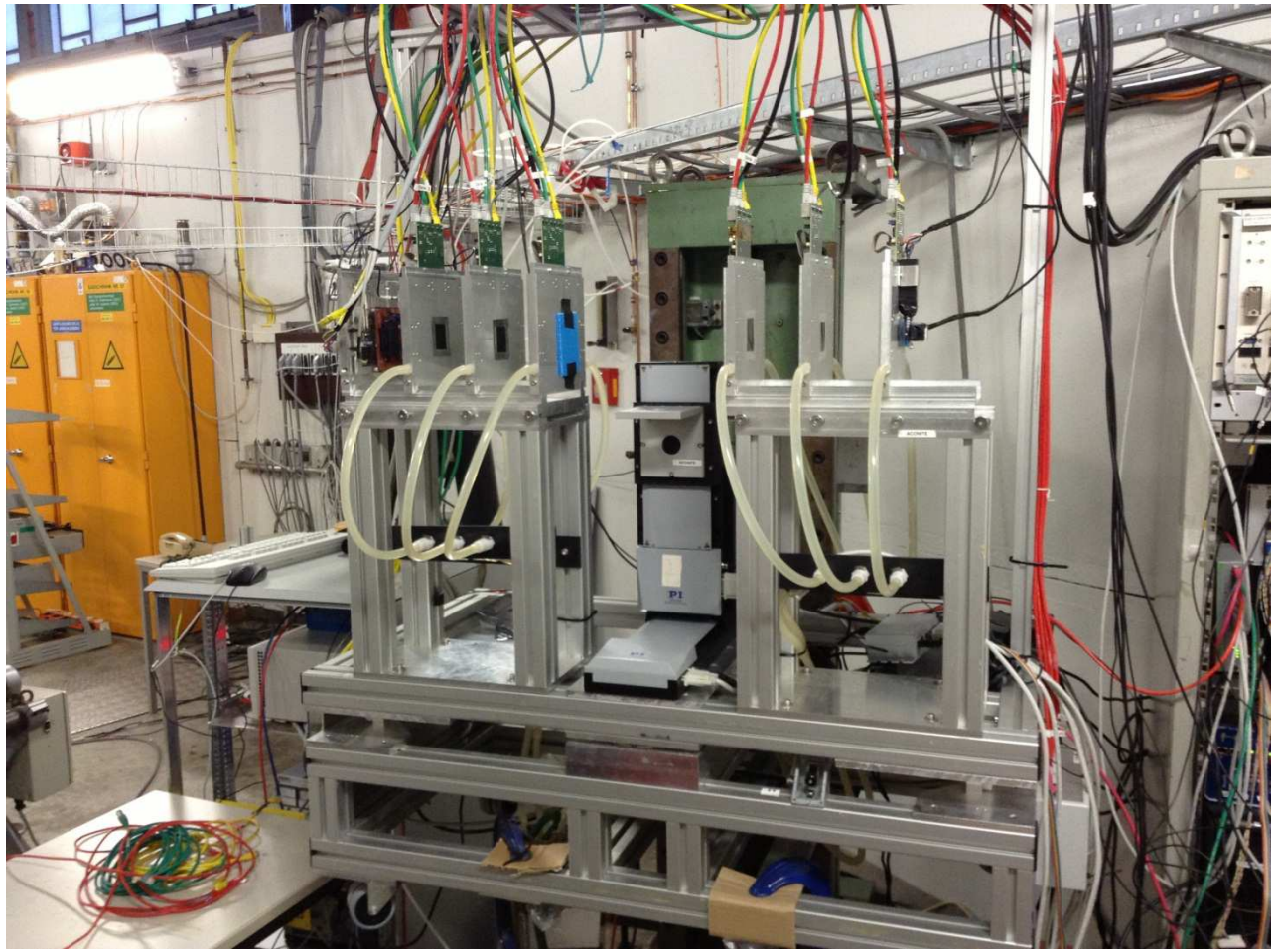


A few % of events include nuclear interactions in material.

Event Example



Pixel Telescope at DESY



DUT Interfaces

- Interfaces foreseen:
  - PSI46 digital ROC: phase 2 sensor design R&D
  - FE-I4B modules: Mu2e extinction monitor tests
  - VIPIC chip: vertically integrated sensor + ROC
- Other interfaces:
  - Interface via 50 pin 3M connector
  - Readout firmware in same design as strip readout
- Independent readout architecture
  - Strip readout provides accelerator clock and trigger signals
  - Events in strips and DUT matched by trigger number

DUT Interface

- Typical analysis:
  - Measure efficiency as a function of…
    - Angle with respect to beam axis
    - Dose delivered during irradiation
    - Bias voltage or DAC settings

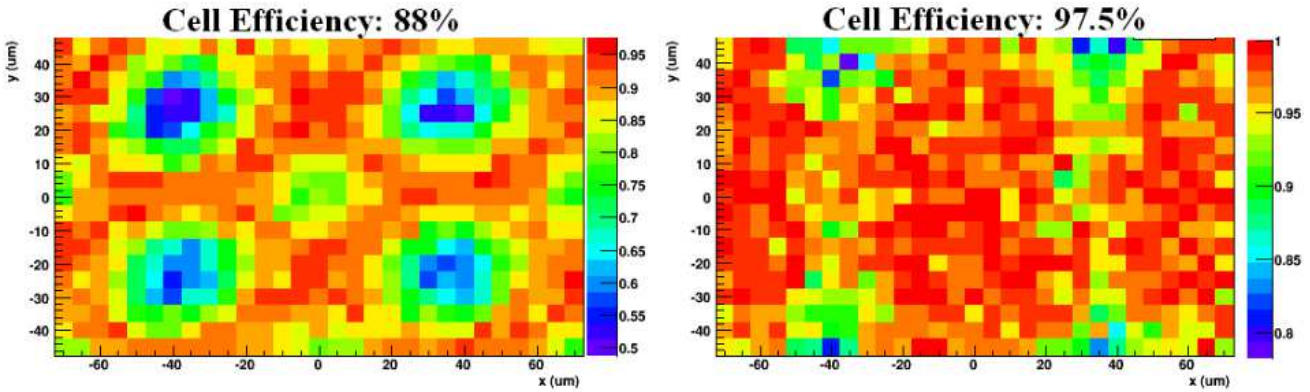


Figure 8. Hit efficiency of SINTEF 3D 4E sensor at 0 degree (left) and at 20 degrees (right) measured before irradiation in beam tests.

arXiv:1402.6384v2 [physics.ins-det] 30 Apr 2014

Summary

- Small scale experiment models many issues faced by large detector systems
- Useful examples of some solutions to common data acquisition issues
- New Test Infrastructures for Future Particle Physics Experiments and Upgrades