Recent advances in silicon photonics

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Outline

1. Silicon photonics: motivation

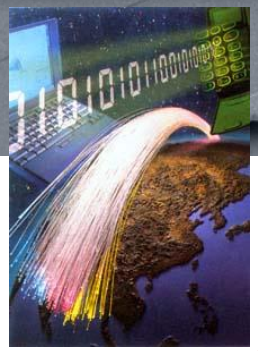
2. Optoelectronic devices

   - Photodetection
   - Optical modulation
   - Optical laser source

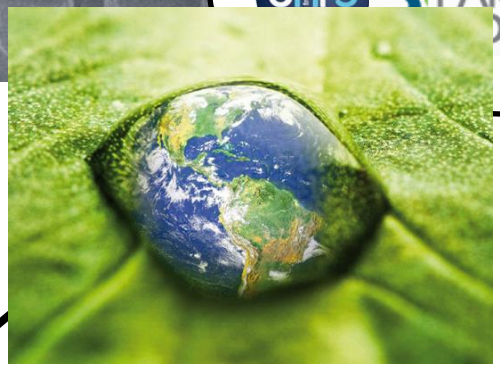
3. Electronic-photonic convergence

4. Conclusion

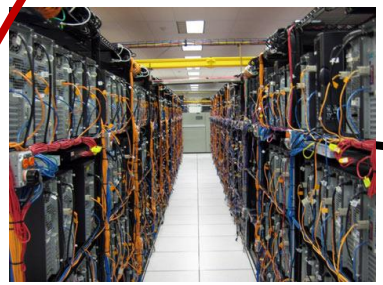
FTTH



Optical telecommunications



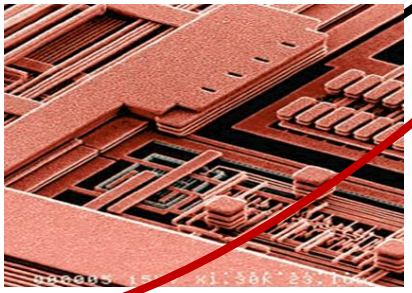
Environment



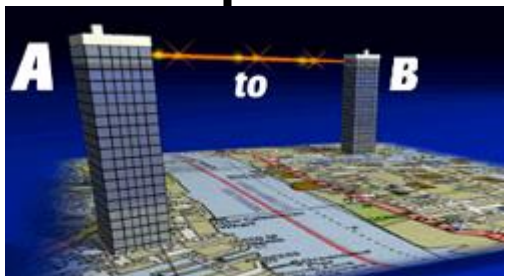
Data centers

Silicon photonics

Chemical/Biological sensors



Interconnects



Free space communications

Military

Global internet traffic

Source: L.Oxenlowe, Denmark

Courtesy: D. Moss, CUDOS, Australia

Google

Google maps Google earth

VIDEO!!!

Data centre web services

On-line games, File sharing

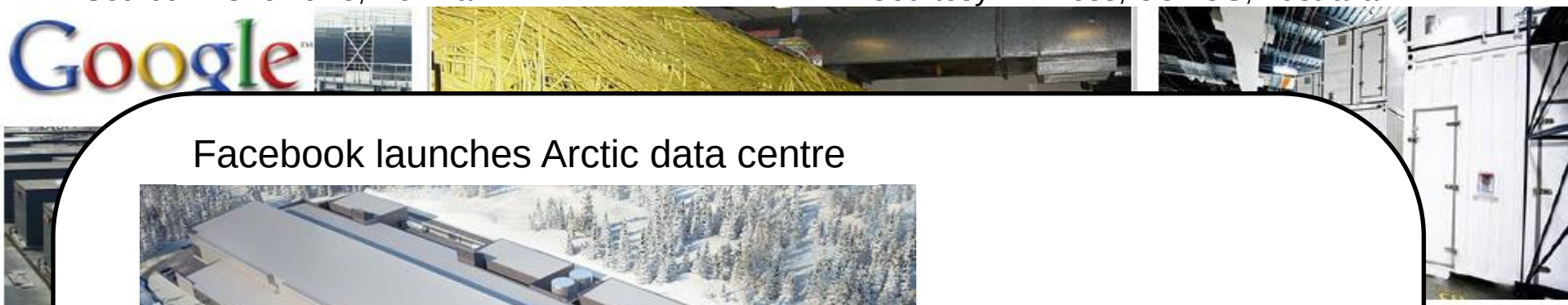
TV/audio juke box … more to come !!

1: E. Desurvire, J.Lightwave Technol., vol. 24, no. 12, (2006), "Capacity Demand…Next…Decades"

Data centers

Source: L.Oxenlowe, Denmark

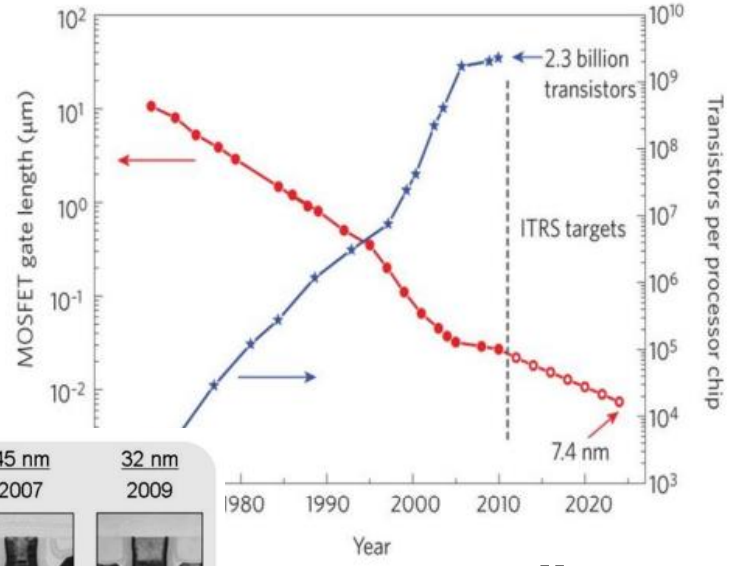
Courtesy: D. Moss, CUDOS, Australia



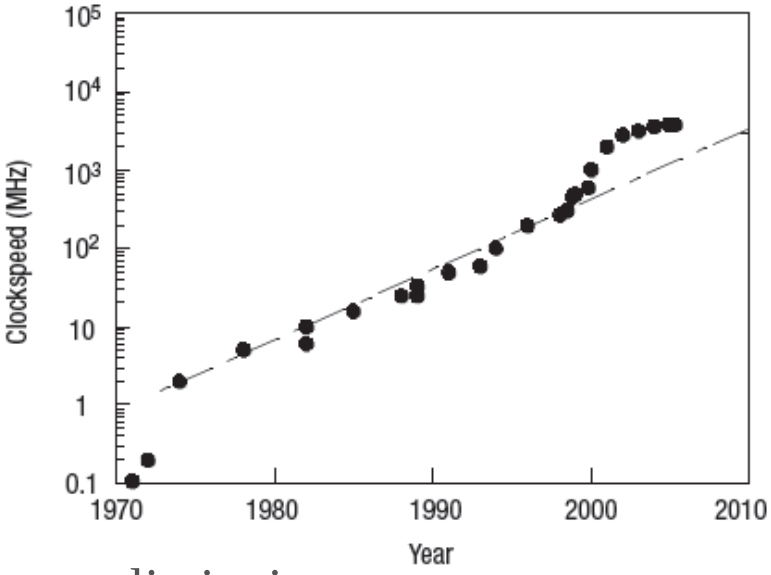
Facebook launches Arctic data centre

Integrated circuits

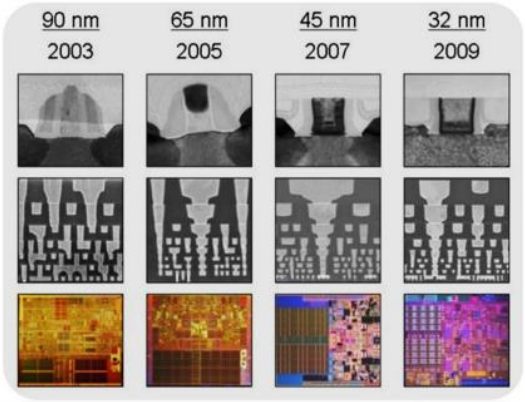
- Increase of integrated circuit complexity
  - √ Number of transistors
  - √ Frequency operation
  - √ Length and density of metallic interconnects



Source: ITRS and Intel



DA. Muller, Nature Mat. 4, 645, 2005



Metallic interconnect limitations

- RC delay
- Signal distortion
- Power consumption

To improve performances

Performance = Parallelism x Frequency

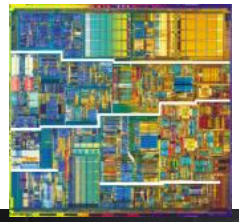
- Ne
  me
- Mo

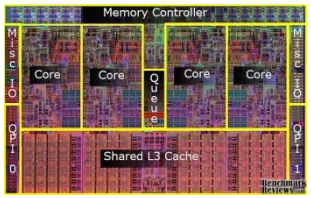
Use photonics at the chip scale to:

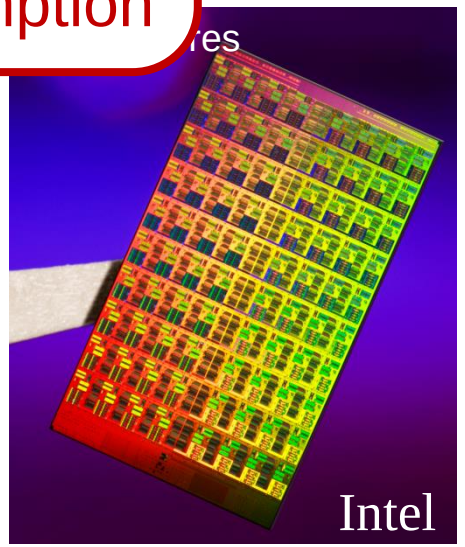
- Increase the data transmission
- Reduce the power consumption

connect
s

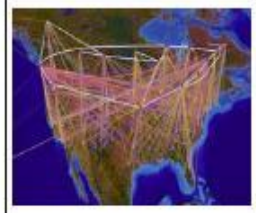
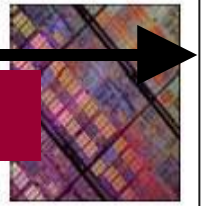
Example:







Optics vs Copper

	Internet, Wide Area Network	Local Area Network	Rack-to-Rack	Card-to-Card	On-Card	On- MCM	On-Chip
							
Distance	multi km	10 - 2000 m	30 cm	1 cm	0.1 - 0.2 m	5 - 100 mm	0.1 - 10 mm
Number of lines	1	1 – 10	~100	~100-1000	~1000	~10'000	~100'000

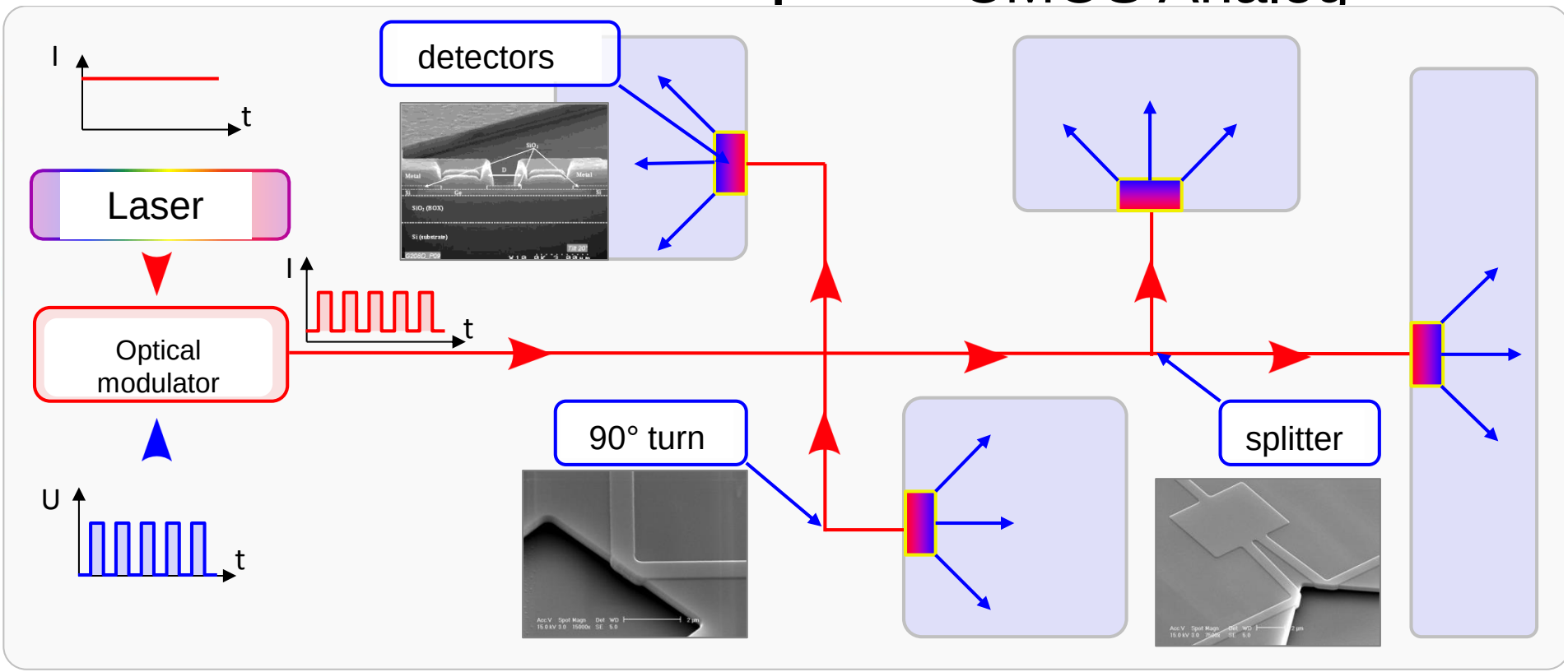
Copper

Photonics

Source: IBM

Towards at the end…

Photonics . CMOS Analog

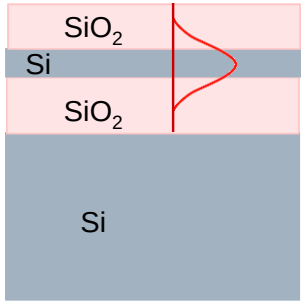


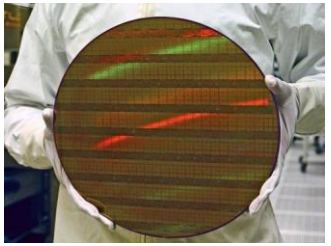
Silicon photonics

uxtera

Silicon for optics: Pro's and Cons

- Transparent in 1.3-1.6 µm region
  - √ Low loss waveguides
- Take advantage of CMOS platform
  - √ Mature technology
  - √ High production volume
- Low cost
- Silicon On Insulator (SOI) wafer
  - √ Natural optical waveguide
- High-index contrast (n_{Si}=3.5 – n_{SiO2}=1.5)
  - √ Strong light confinement
    - ➢ Small footprint (450nm x 220nm)





Higher refractive index contrast, smaller cores, tighter bends

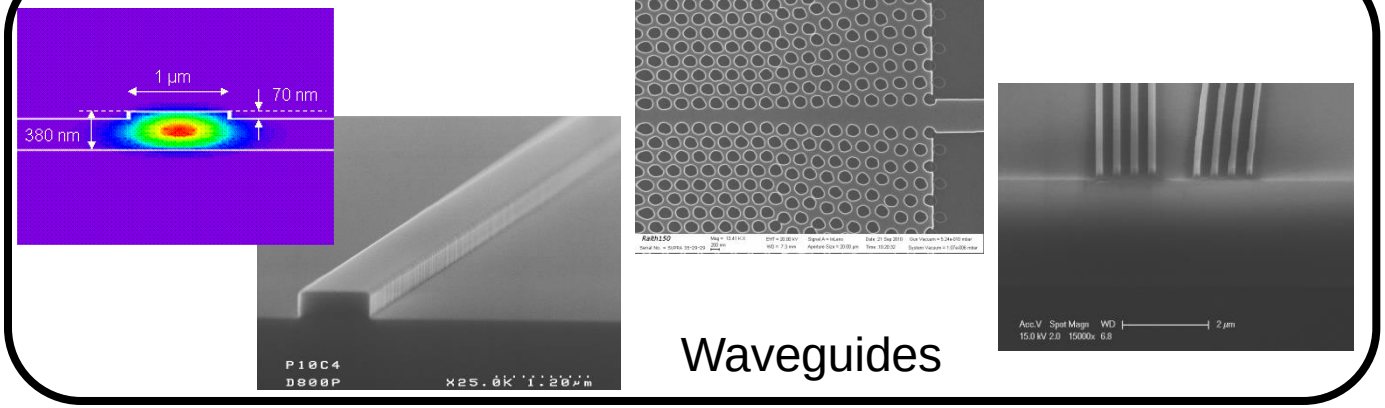
Silica on silicon

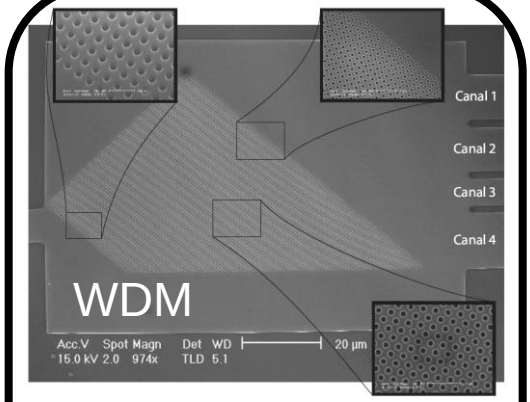
Contrast ~ 0.01 – 0.1
Mode diameter ~ 8µm
Bend radius ~ 5mm
Size ~ 10 cm^2

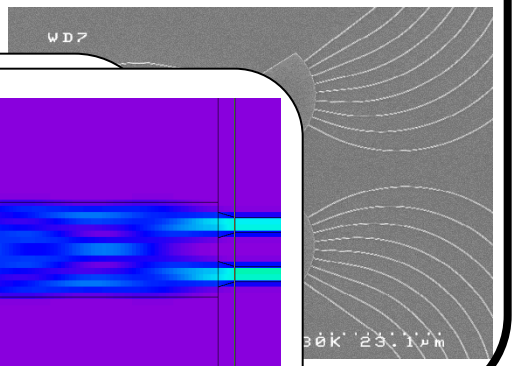
Downscaling of photonics

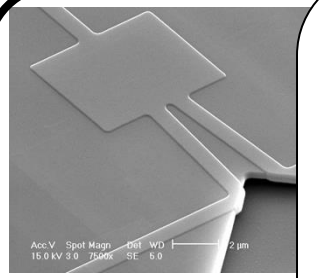
Source: Slide from Wim Bogaerts – Summer school 2011 St Andrews

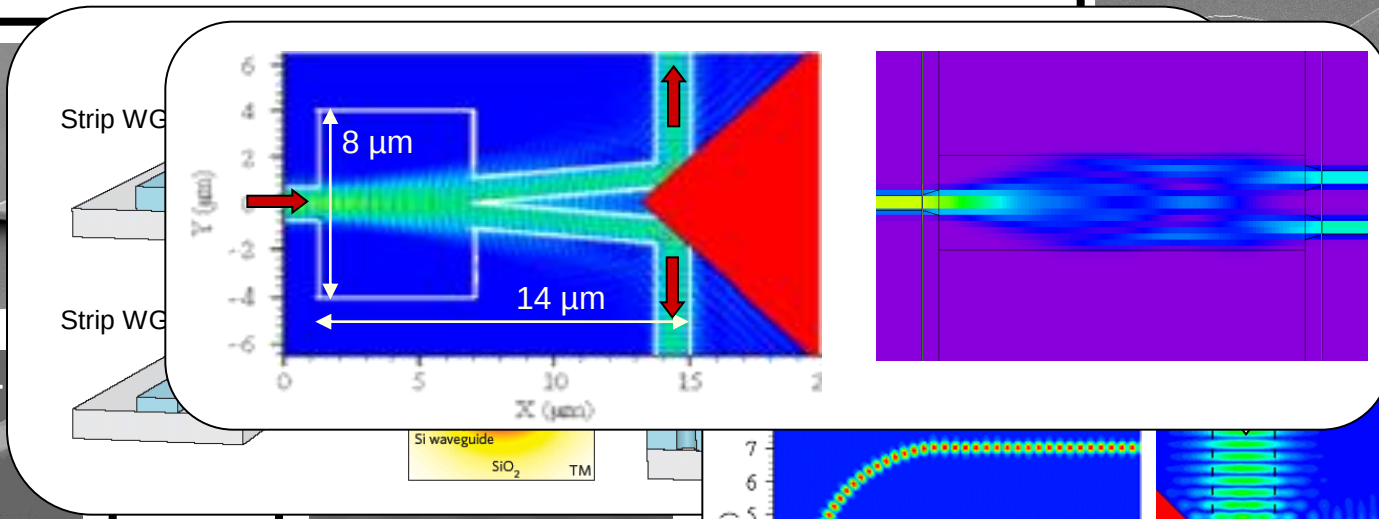
Passive photonic devices

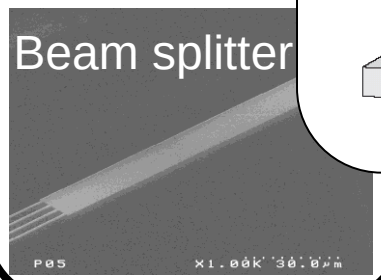


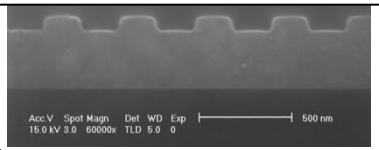


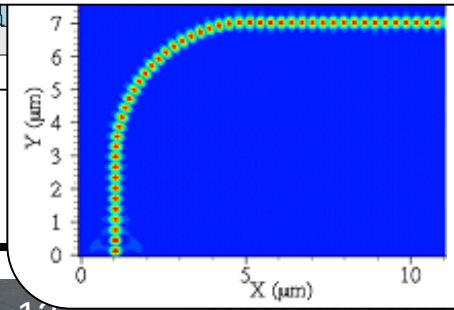


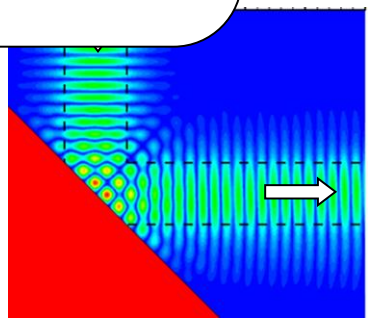








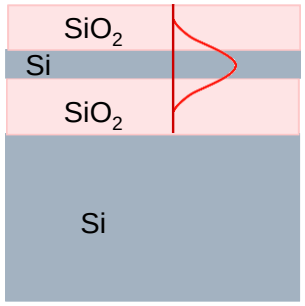


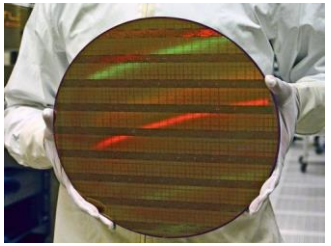


Silicon for optics: Pro's and Cons

- Transparent in 1.3-1.6 µm region
  - √ Low loss waveguides
- Take advantage of CMOS platform
  - √ Mature technology
  - √ High production volume
- Low cost
- Silicon On Insulator (SOI) wafer
  - √ Natural optical waveguide
- High-index contrast (n_{Si}=3.5 – n_{SiO2}=1.5)
  - √ Strong light confinement
    - ➢ Small footprint (450nm x 220nm)

- Indirect bandgap material
  - √ No or weak electro-optic effect
  - √ "Lacks" efficient light emission
    - ➢ No Si laser
- No detection in 1.3-1.6 µm region





Outline

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2. Optoelectronic devices

   - Photodetection
   - Optical modulation
   - Optical laser source

3. Electronic-photonic convergence

4. Conclusion

Germanium on silicon: Pros and Cons

- Absorption coefficient of pure Ge
  - $\alpha \approx 9000\ cm^{-1}$ at $\lambda = 1.3\mu m$

    $\Rightarrow L_{ABS}^{95\%} \approx 3.3\mu m$ (!)

    $\Rightarrow$ Low capacitance devices

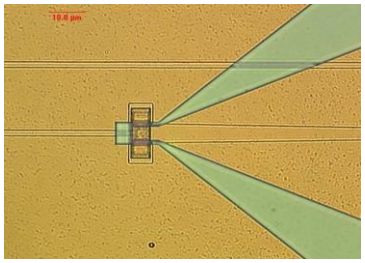
    $\Rightarrow$ High frequency operation
- High carrier mobility

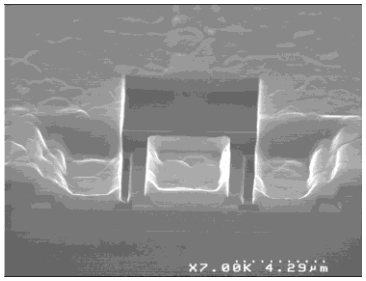
- Lattice misfit with Si of about 4.2%

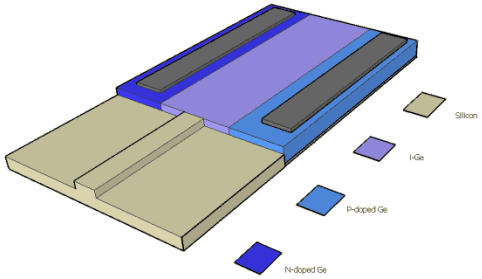
  $\Rightarrow$ specific growth strategies required (wafer-scale and localized)
- Low indirect bandgap: $E_G = 0.66eV$

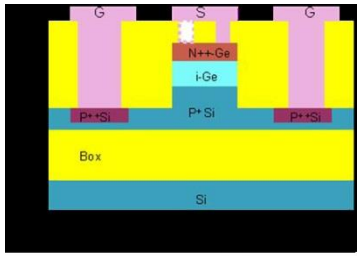
  $\Rightarrow$ high dark current for MSM devices

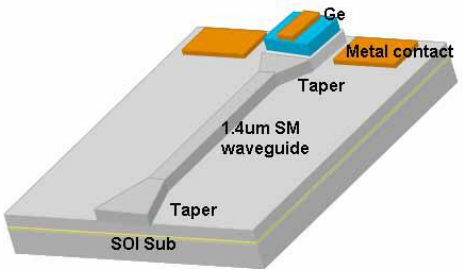
Ge Photodetectors

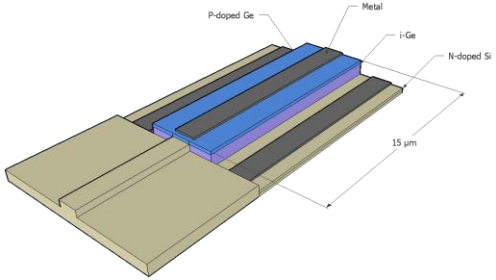


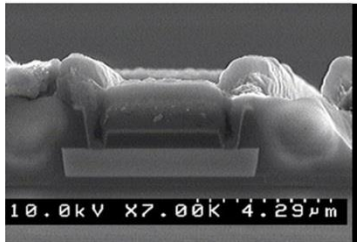


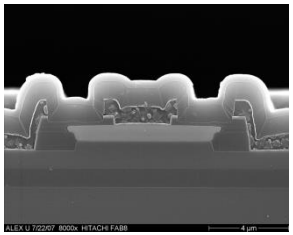










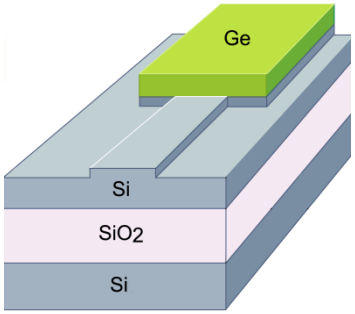


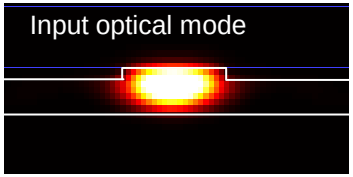
Europe: PSUD-IEF, CEA-Léti, Stuttgart Univ., Roma Univ. …

Asia: Tokyo Univ., A*Star, Petra, AIST, Chinese Academy of Sciences, …

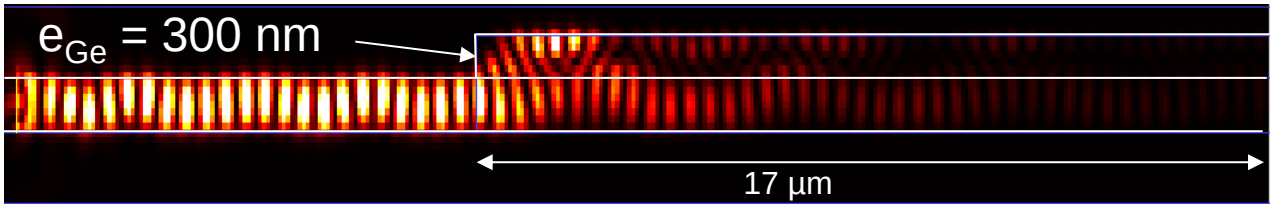
North America: Intel, MIT, IBM, Cornell, Luxtera, Ligthwire, Kortura, Oracle …

Ge photodetector: optical coupling

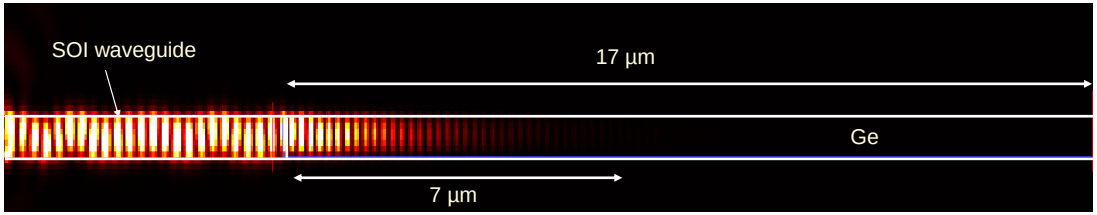


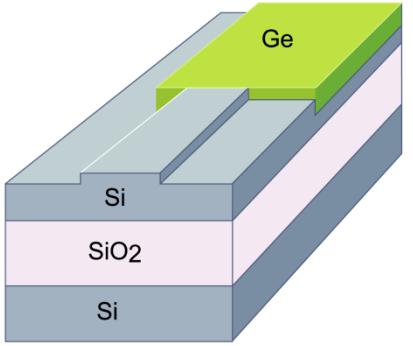


Vertical coupling



Butt coupling

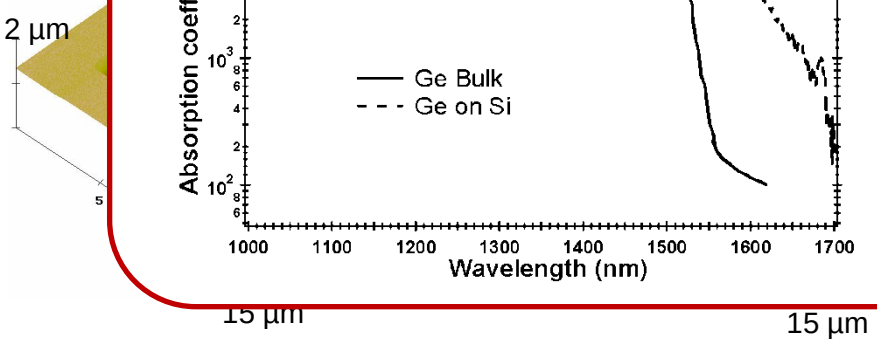




⇨ Short absorption length => Low capacitance
⇨ Light absorption is independent of Ge film thickness

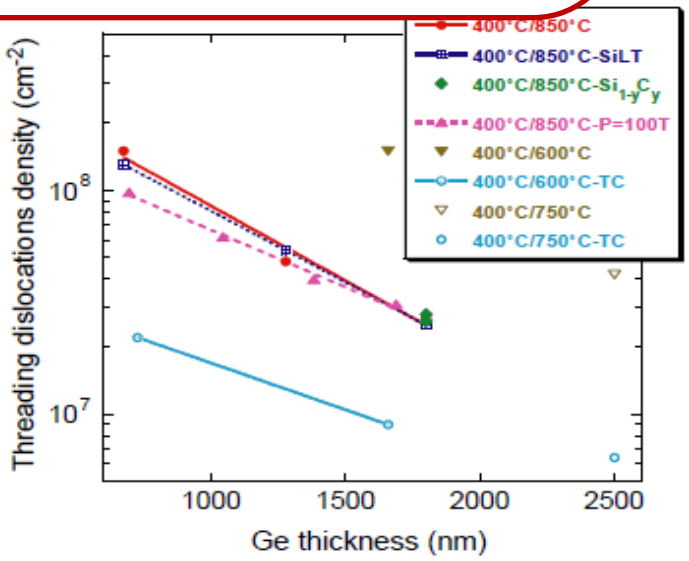
Device Fabrication: Ge Growth

- Two RPCVD steps to overcome lattice mismatch issue



- Optical absorption
  - √ Close to bulk values
  - √ Bandgap shrinkage (50 nm)
    - ➢ Tensile strain
    - ⇒ Absorption up to 1.6 µm

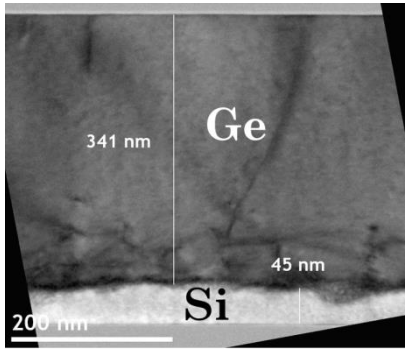
- Overgrowth of Ge
  - ➢ To avoid faceting inside the cavity
  - ➢ To reduce Threading Dislocation Density (TDD)

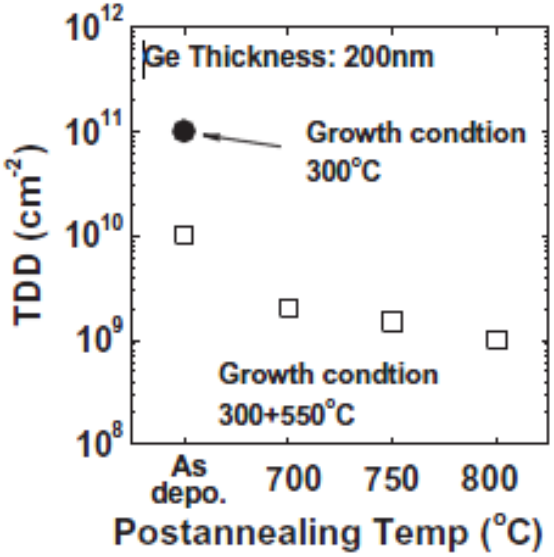


J.M. Hartmann et al., *J. Crystal Growth*, **274**, 90-99 (2005)

Device Fabrication: Ge Growth

- Post epitaxial thermal cycling to further reduce TDD in the Ge layer
- CMP step to remove protruded Ge
- SiO_2 encapsulation
- Ion implantation of Ge
  - √ N-type : Phosphorus
  - √ P-type : Boron
- Rapid Thermal Anneal





Y. Yamamoto et al., *Solid-State Electronics*, **60-1**, 2–6, (2011).

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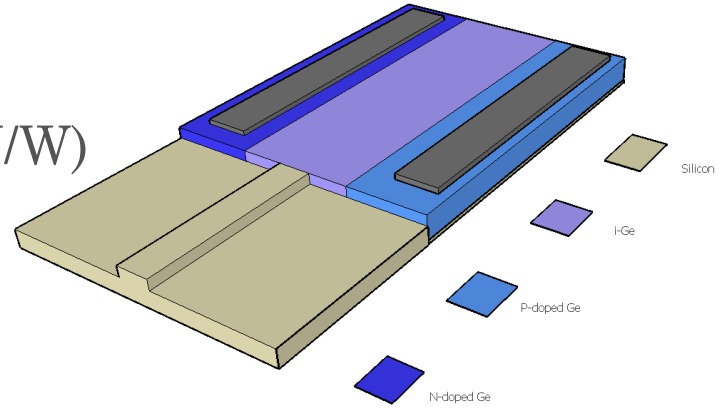
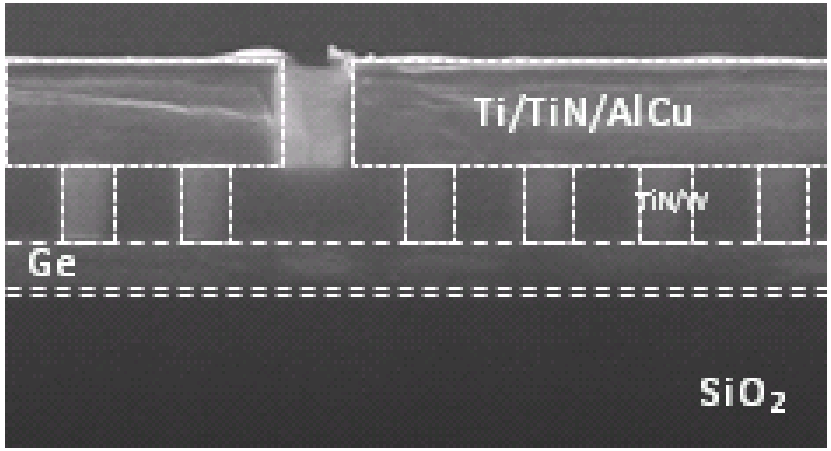
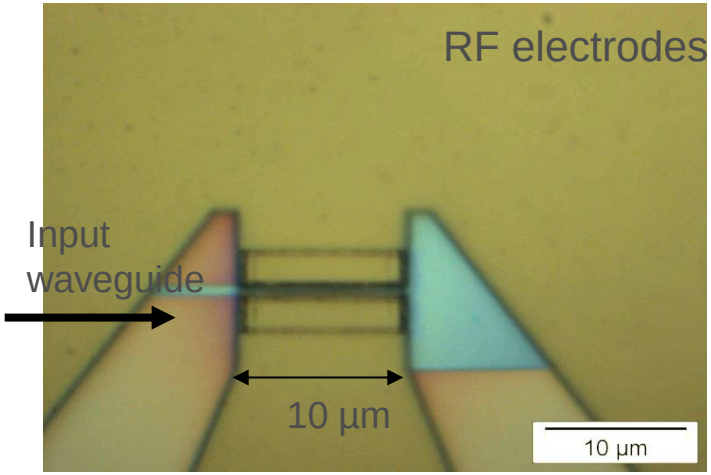
Device Fabrication: Contact and Metal

- Oxide encapsulation
- Planarization
- Contact definition
  - 0.4x0.4µm vias for metal filling (TiN/W)
  - Ti/TiN/AlCu pad defined by etching

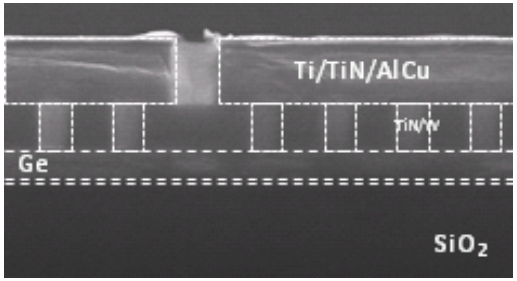
Lateral

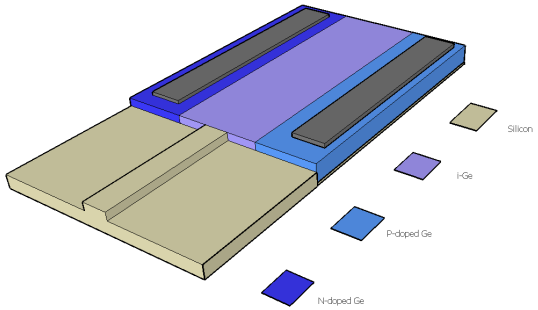


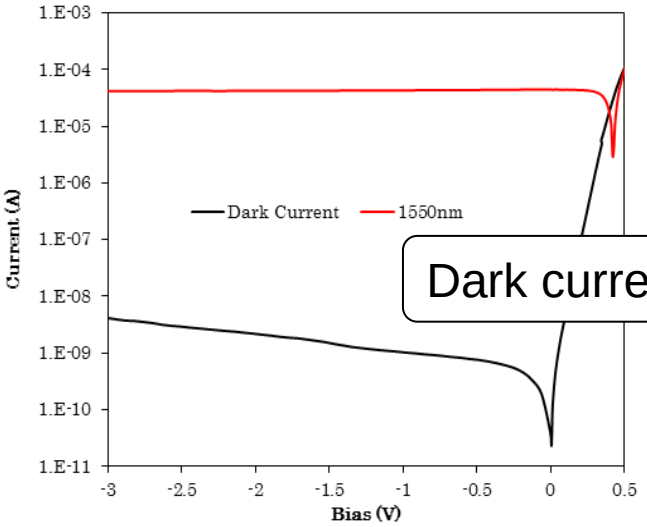




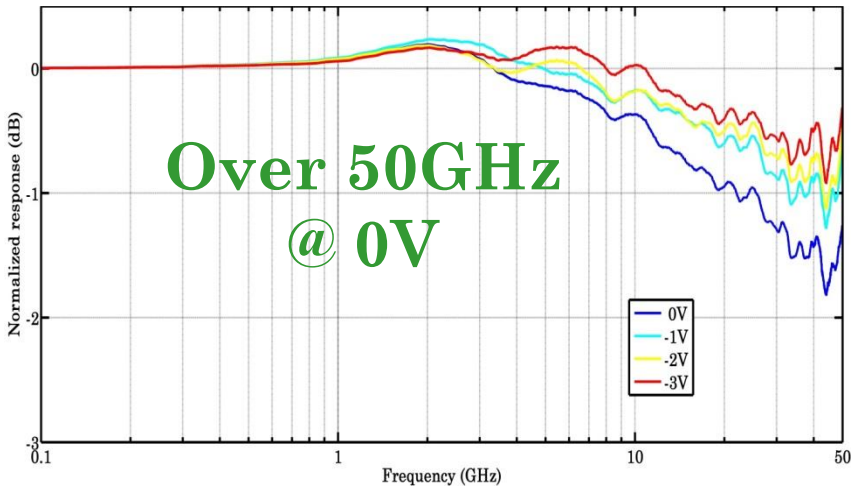
Ge waveguide photodetector



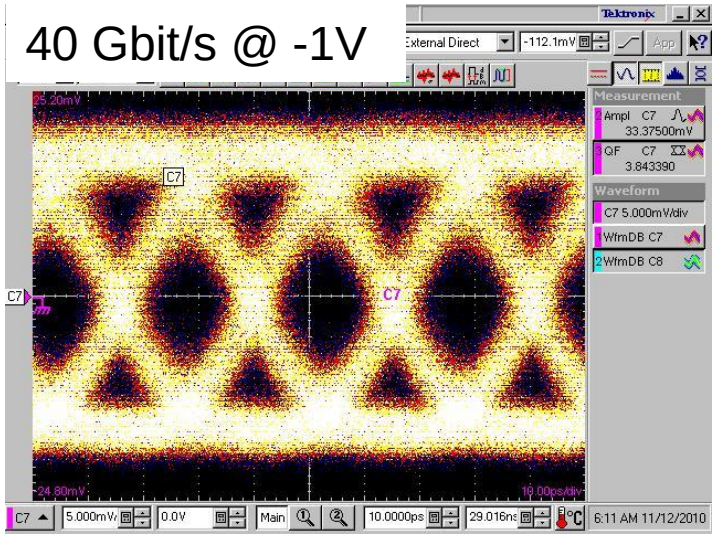




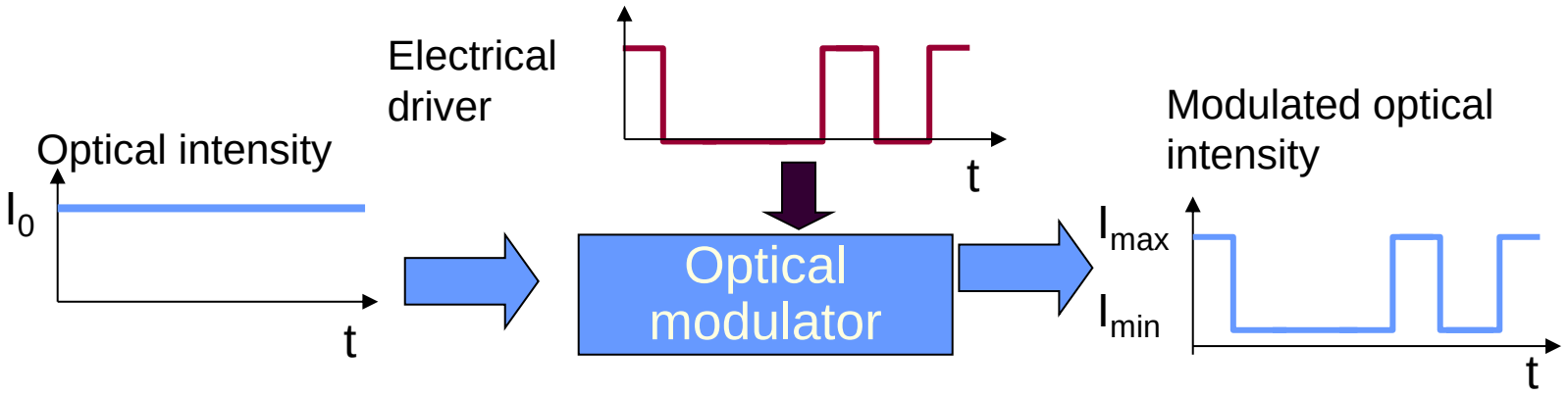
Dark current: ~1nA



40 Gbit/s @ -1V



Optical modulation in silicon



Electro-absorption

Absorption coefficient variation with electric field

Intensity modulation

Electro-refraction

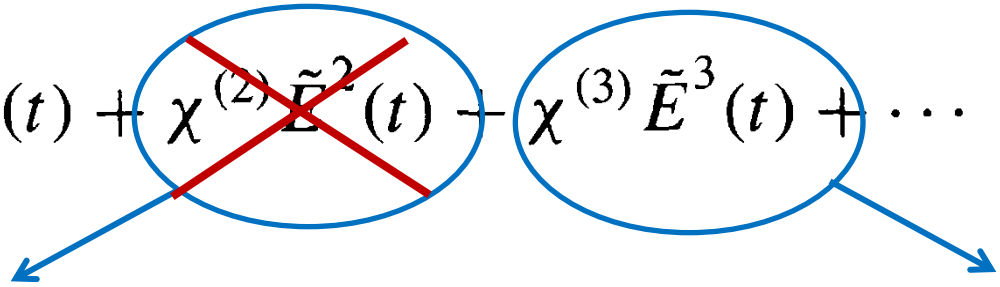
Refractive index variation with electric field

Phase modulation

Electro-optic effect

Nonlinear Polarization:

$$\tilde{P}(t) = \chi^{(1)}\tilde{E}(t) + \chi^{(2)}\tilde{E}^2(t) + \chi^{(3)}\tilde{E}^3(t) + \cdots$$



- √ **Pockels effect**:
  - ➢ Linear electro-optic effect
- √ Wavelength conversion
  - ➢ Second Harmonic Generation (SHG)

Silicon is a centro-symetric material !

- √ **Kerr effect**:
  - ➢ Nonlinear electro-optic effect
- √ Wavelength conversion
  - ➢ Four wave mixing (FWM)

Too weak to be used in modulation

$$n = n_0 + I * n_2$$

$$n_2^{Si} \sim 10^{-14}\,\mathrm{cm}^2/\mathrm{W} \quad >> \quad n_2^{glass} \sim 10^{-16}\,\mathrm{cm}^2/\mathrm{W}$$

Nonlinear optics in silicon

Nonlinear Polarization:

$$\tilde{P}(t) = \chi^{(1)}\tilde{E}(t) + \cancel{\chi^{(2)}\tilde{E}^2(t)} + \chi^{(3)}\tilde{E}^3(t) + \cdots$$

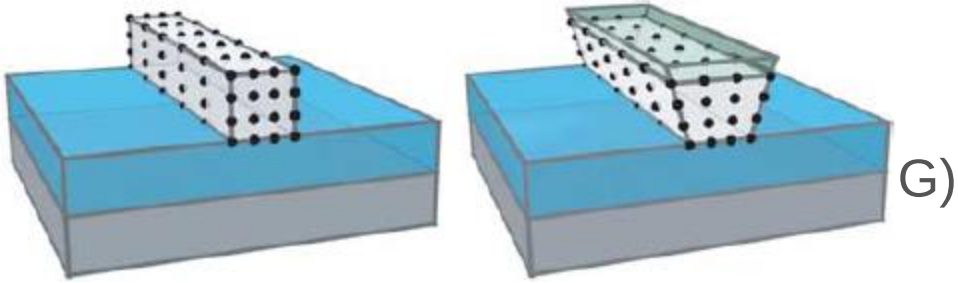
√ **Pockels effect**:

- Linear electro-... effect

Without straining layer

With straining layer

...ric material ...



√ \

G)

Break the symmetry of silicon crystal

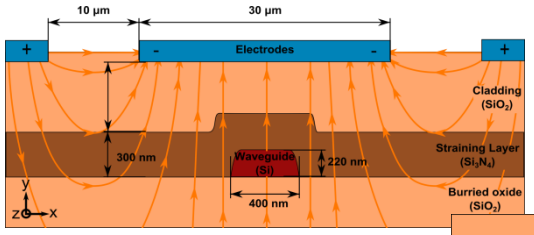
⇩

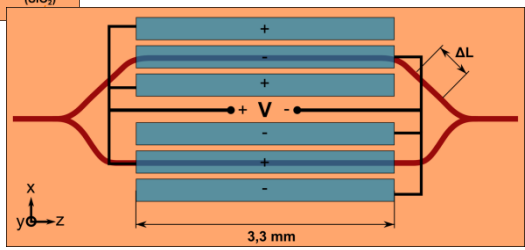
Strained silicon photonics

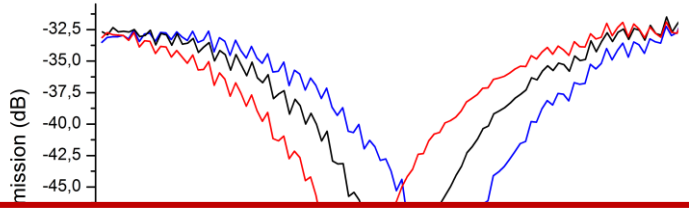
Mach-Zehnder modulator based on Pockels effect

- Pockel's effect:

$$n_{eff}(30\ \mathrm{V}) = (1.9 \pm 4) \times 10^{-5}$$

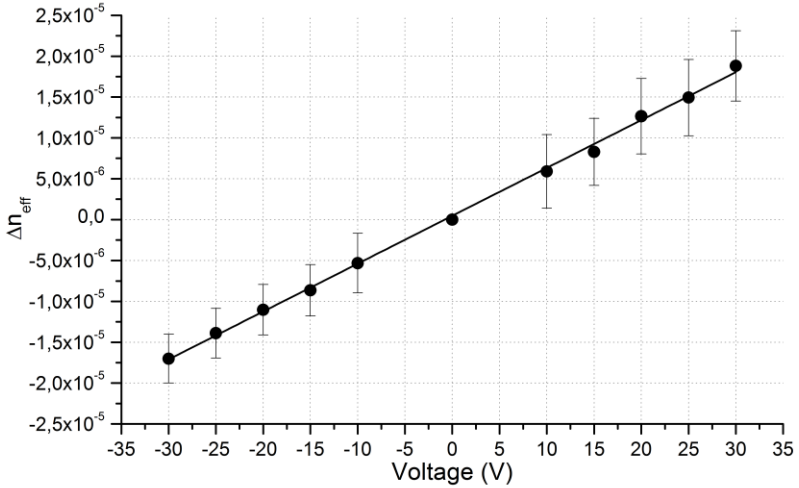






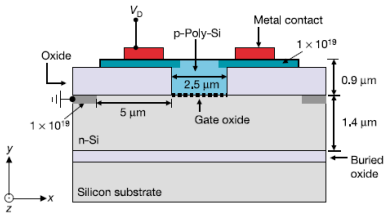
Still weak effect and high voltage BUT promising

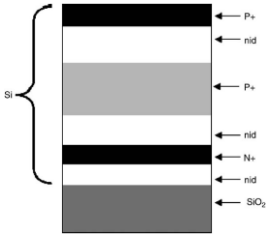
for the development of low power consumption devices

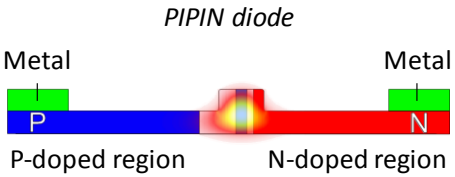


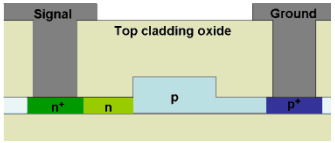
- ✓ Intrinsically high speed
- ✓ Field effect – no capacitance
  - ➢ Low power consumption
- ✓ Low bias swing
- ✓ Low insertion loss
  - ➢ No doped regions

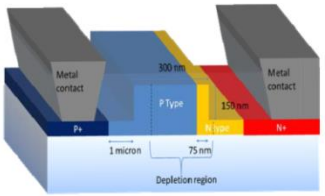
Plasma dispersion Si optical modulator



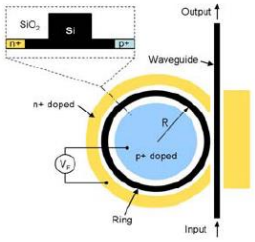


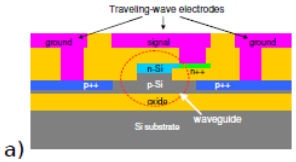


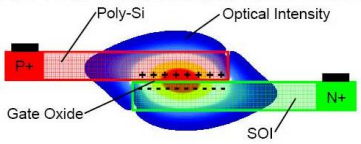


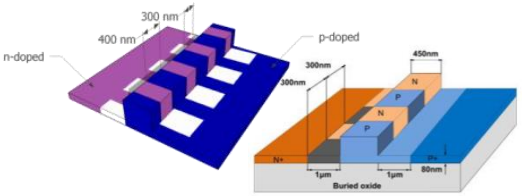


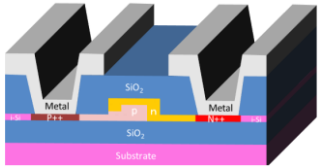
2004 2005 2006 2007 2008 2009 2010 2011 2012











Europe: Univ. Paris Sud, CEA Leti, Univ. of Southampton…

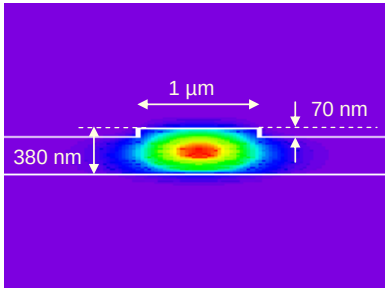
Asia: A*Star, Petra, AIST, Chinese Academy of Sciences, Samsung Electronics, Tokyo Institute of Technology …

North America: Intel, IBM, Cornell, Luxtera, Ligthwire, Kotura, Oracle …

Electro-refraction vs intensity variation

Electro-refraction effect:

- √ carrier density variation: accumulation, depletion, injection

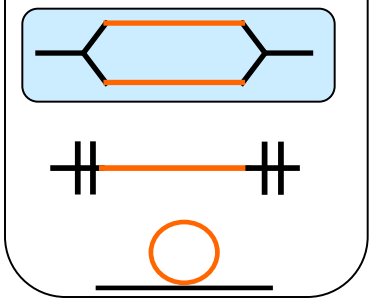


Refractive index variation

Effective index variation of the guided optical mode

Phase variation

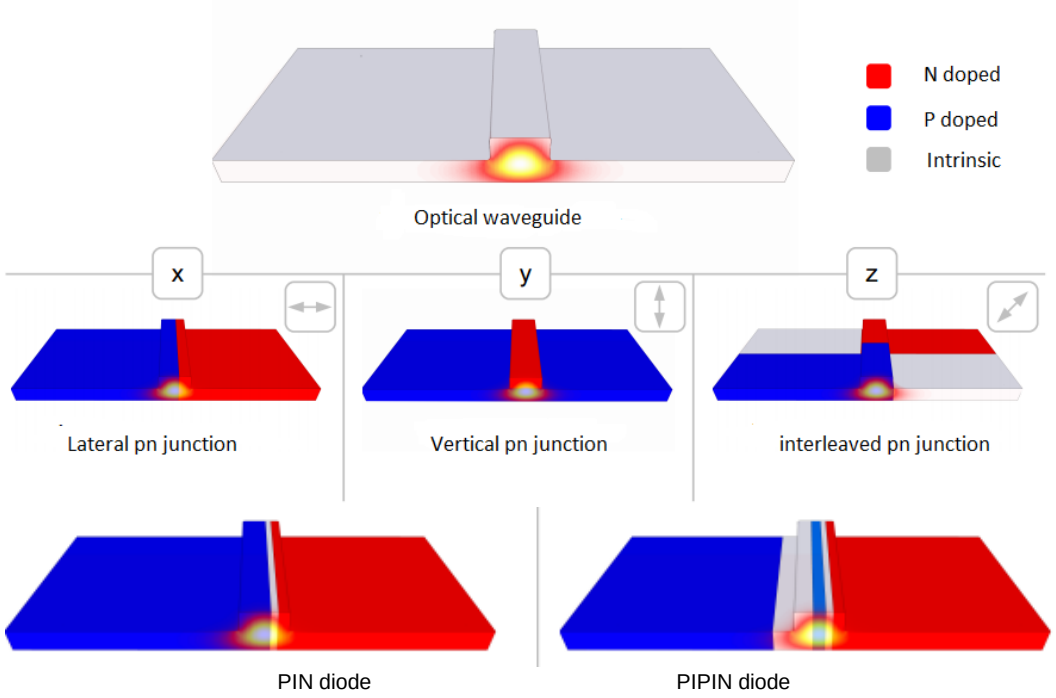
Interferometers



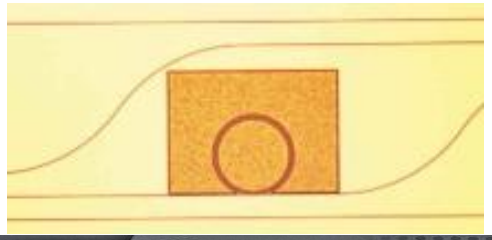
Optical intensity variation

Optical modulators

- Phase shifters:
  - PN diode
  - Interleaved PN diode
  - PIN diode
  - PIPIN diode
  - MOS capacitor

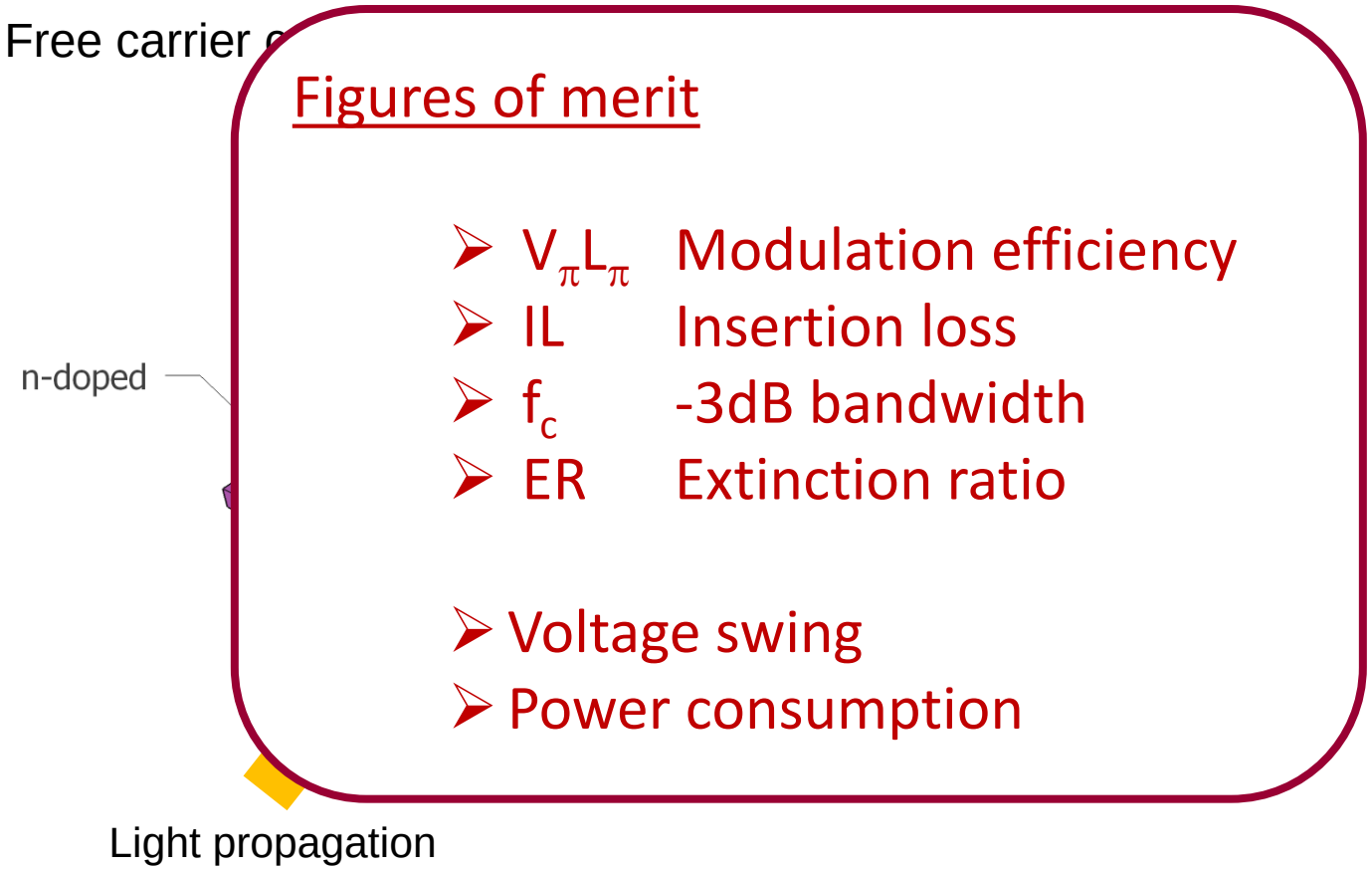


- Interferometers
  - Ring resonator
  - Mach-Zehnder
  - Photonic cristals



Silicon modulator design

Example: carrier depletion in interleaved pn diode



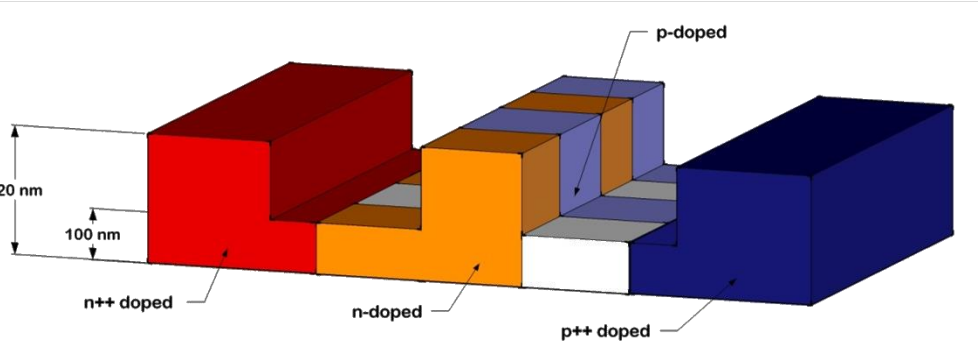
Figures of merit

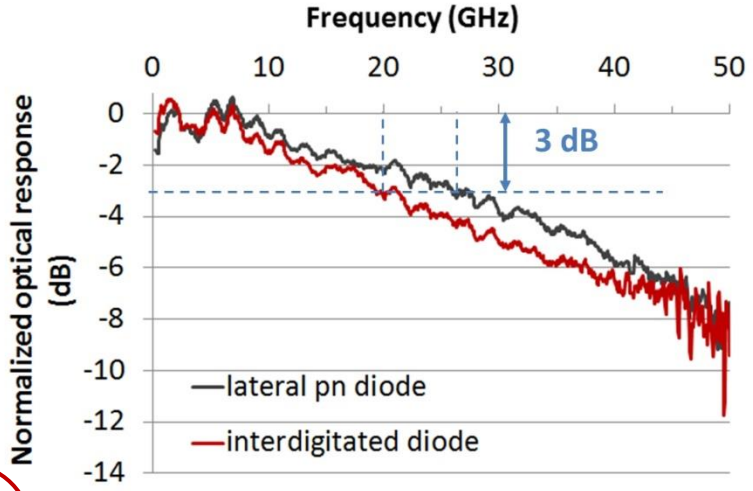
- $V_\pi L_\pi$ Modulation efficiency
- IL Insertion loss
- f_c -3dB bandwidth
- ER Extinction ratio

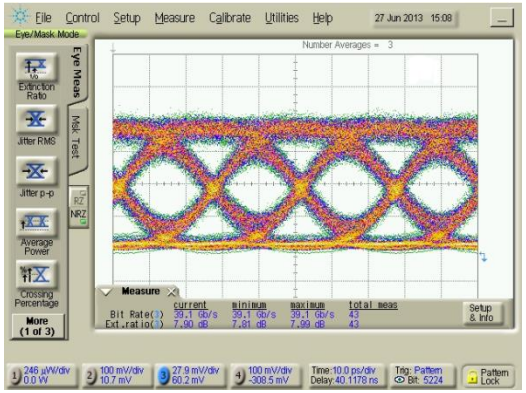
- Voltage swing
- Power consumption

Si modulators on 300-mm platform

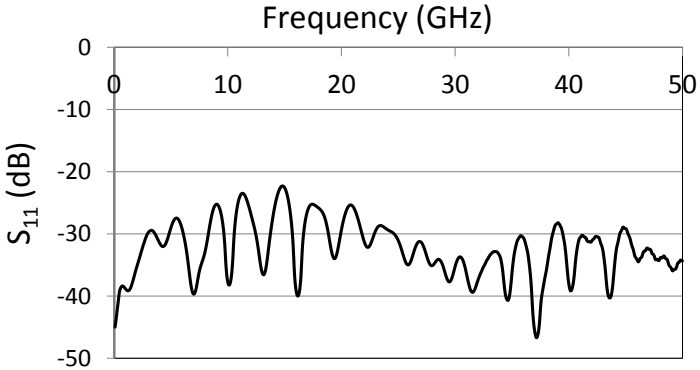
Geometry: 0,95mm long Mach-Zehnder modulator







- ✓ $V_\pi L_\pi$ ~2.2 V.cm
- ✓ Extinction ratio: 8 dB
- ✓ Insertion loss: 4 dB
- ✓ Frequency > 20 GHz
- ✓ S_{11} < 20 dB
- ✓ Data rate: 40 Gbit/s



D. Marris-Morini et al, Opt. Exp. (2013)

life.augmented

Silicon modulators

Short distance and high volume applications (electrical bottleneck)

Optical interconnects

Data-center

Main challenges:

- ✓ Driving voltage of modulator
- ✓ Compactness
- ✓ Power consumption

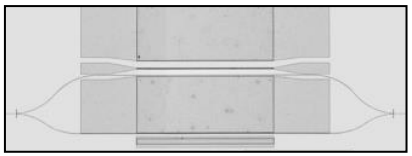
ITRS Roadmap: Optical interconnect

- (…) A large variety of CMOS compatible modulators have been proposed in the literature (…)
- "The primary challenges for optical interconnects at the present time are producing cost effective, low power components."

Power consumption

For emitters and short optical links:
~100 fJ/bit down to fJ/bit
(D.A.B. Miller, Opt Exp. , 2012)

Mach Zehnder modulators
~ 3 pJ/bit

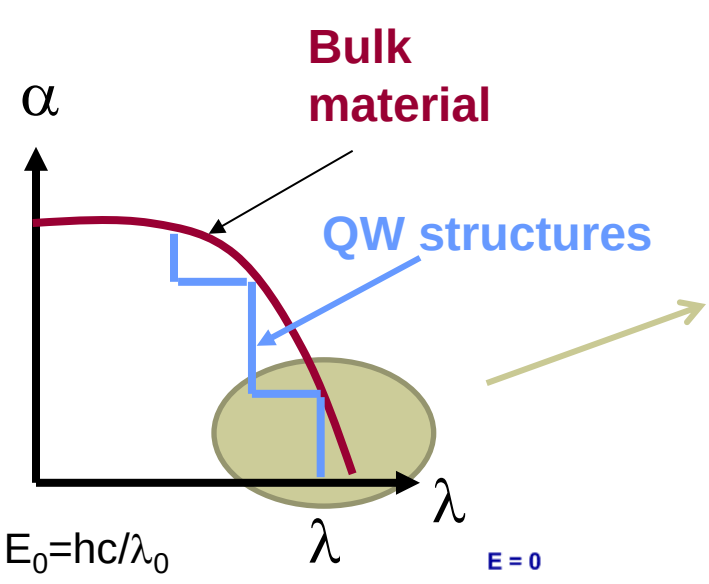


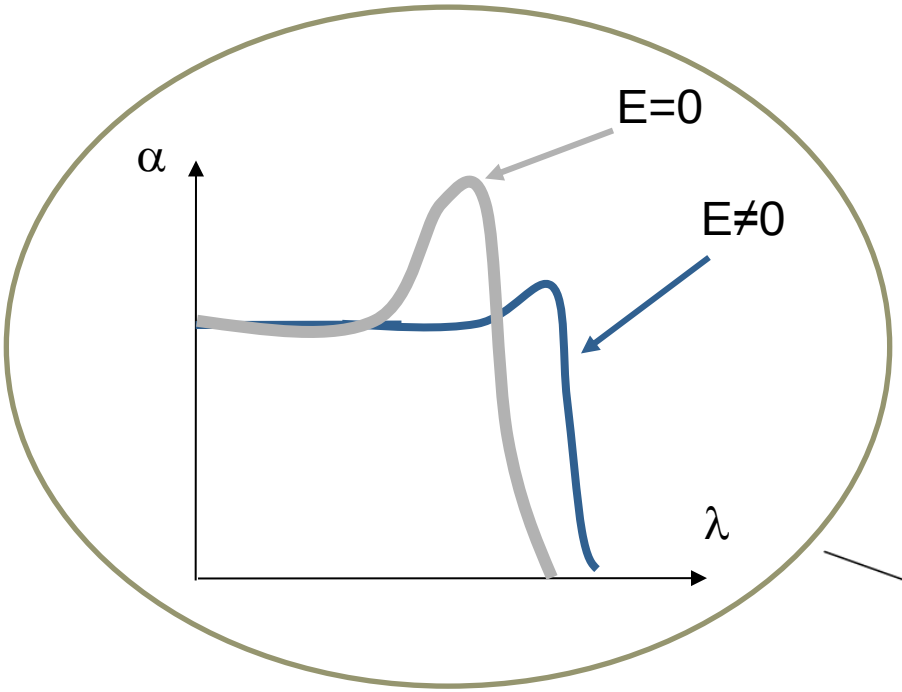
Ring resonator modulators
~ 0.5 to 1 pJ/bit

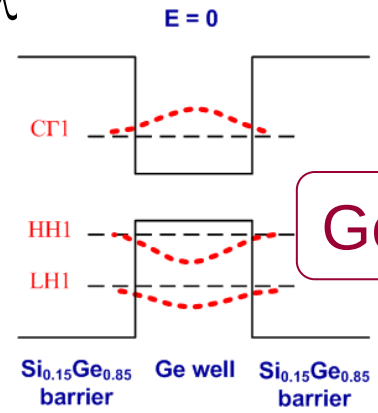
- Franz-Keldysh effect in bulk material
- Quantum Confined Stark Effect in quantum well

Electro-absorption

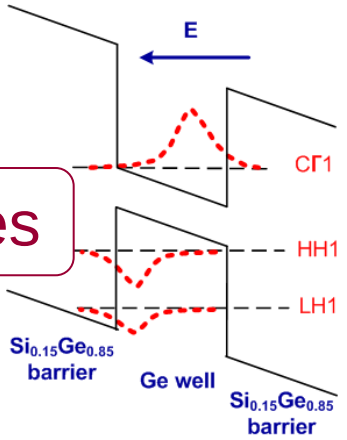
Electro-absorption modulator







Ge/SiGe quantum well structures



- Absorption edge in QW structures is more abrupt than in bulk material
- E_0 depends on the quantum well thickness
  - Adjustment of the wavelength is possible

Epitaxial growth by LEPECVD

- ✓ Growth of Ge/SiGe multiple quantum wells

LEPECVD

Low energy plasma enhanced chemical vapor deposition

Relaxed buffer graded from Si to $Si_{0.1}Ge_{0.9}$ buffer layer

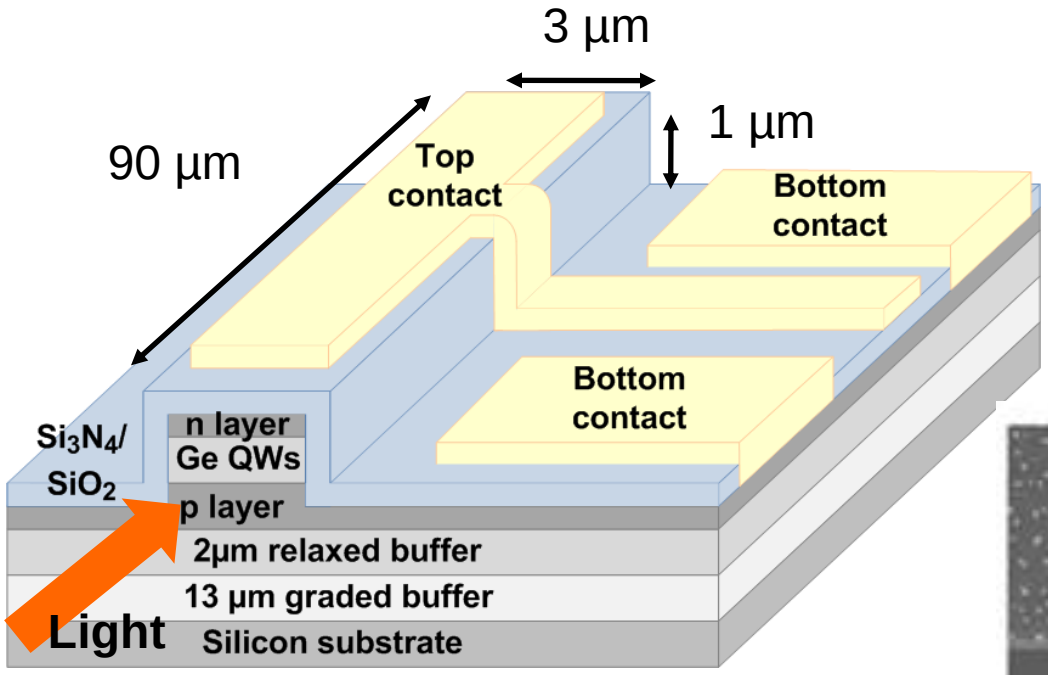
Si(100)

Low dislocation density
- Best device performance

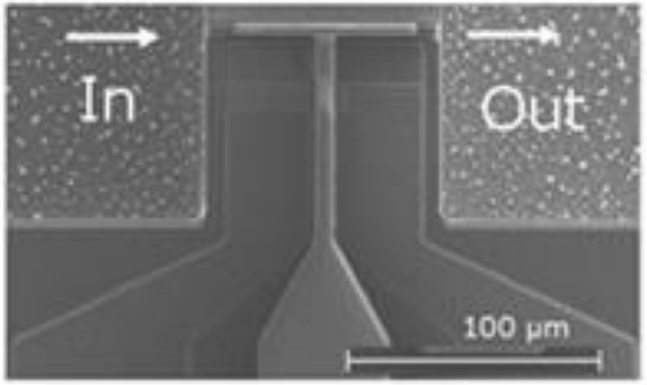
- ✓ Temperatures down to 400°C

L-NESS
Como, Italy

Electroabsorption modulator

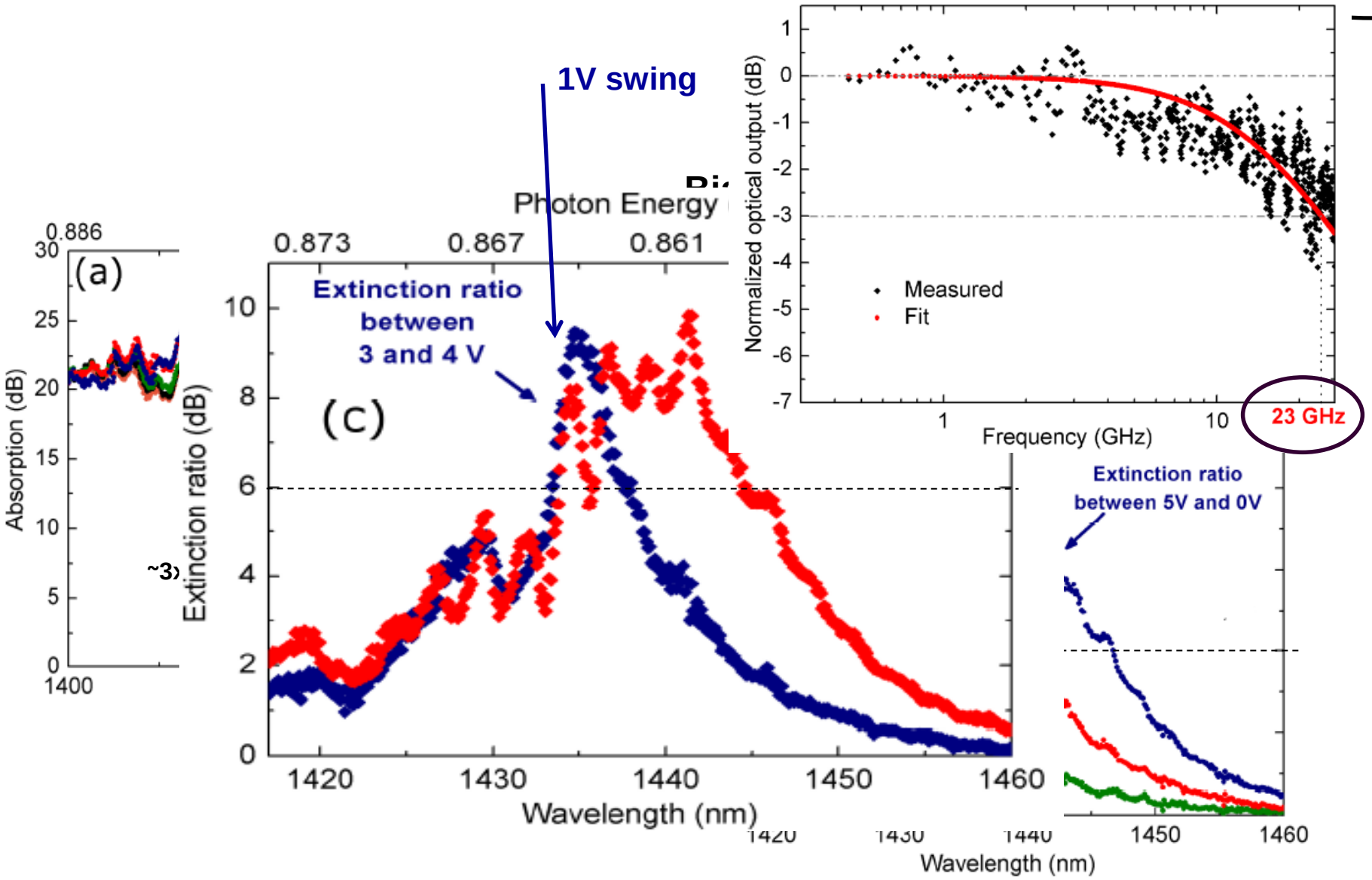


20 Ge/SiGe QW

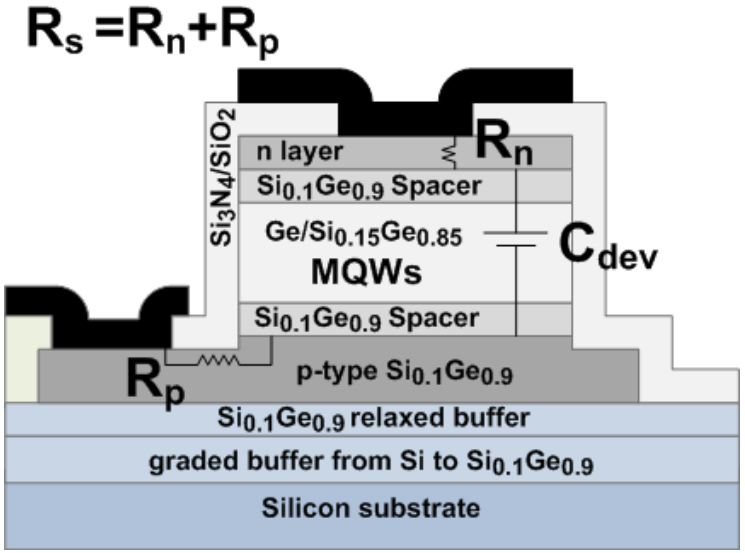


P. Chaisakul et al., Optics Express (2012).

Static performance: optical transmission



Energy consumption



Energy to charge the device

Energy/bit = 1/4 $(CV_{pp})^2$

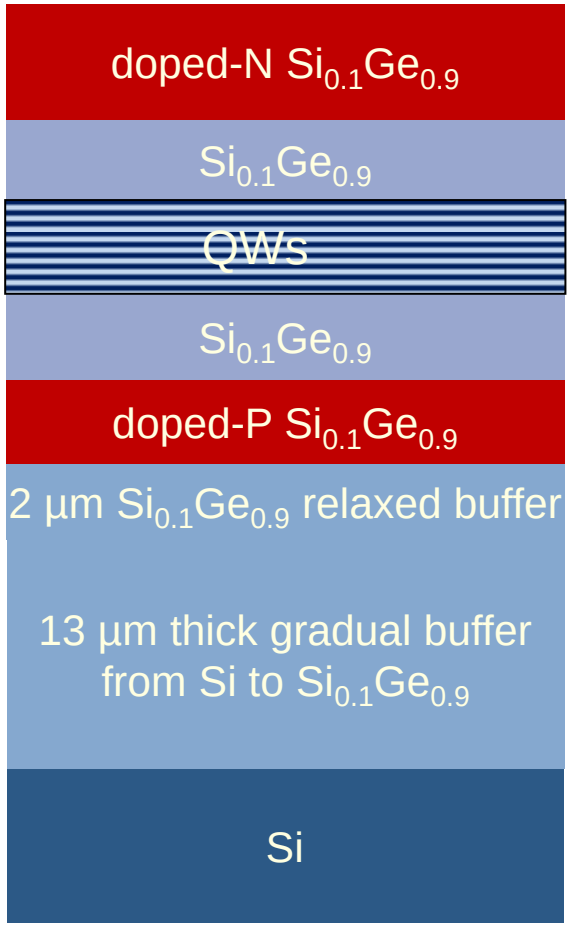
Energy dissipation of photocurrent

Energy/bit = 1/B $(I_{ph}V_{bias})$

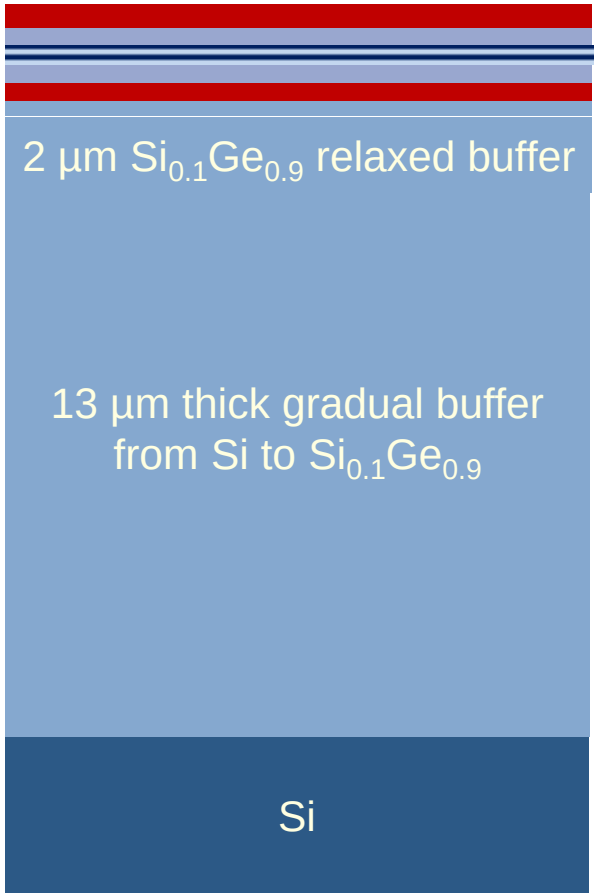
C ~ 62 fF ➡ Energy/bit = **70 fJ/bit**

(for a voltage swing of 1 V , 20 Gbps, 0.5 mW input power)

Integrated circuits based on Ge/SiGe QW ?



Schematic description

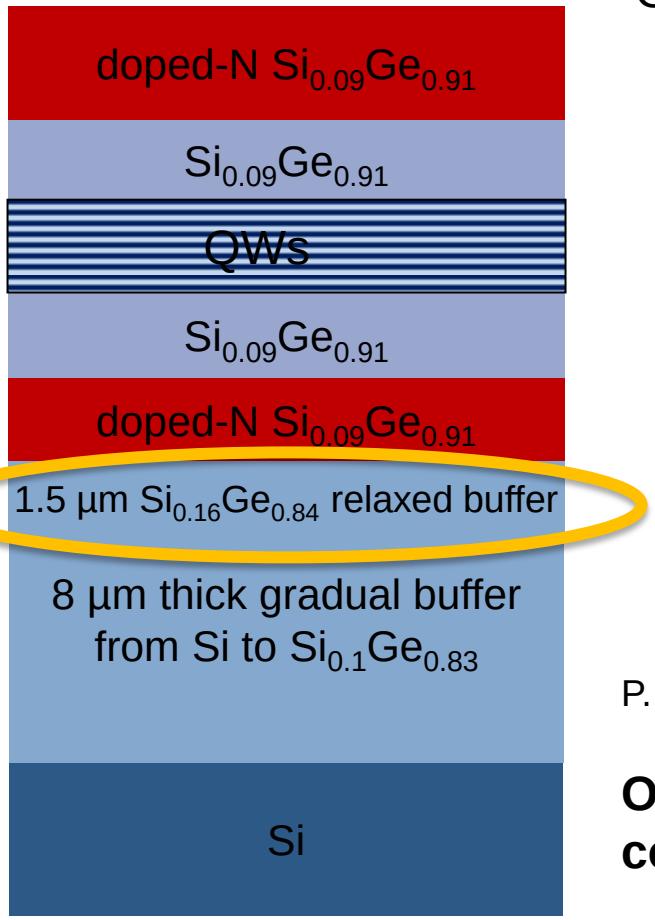


The real scale

Challenge: coupling the light from silicon to Ge/SiGe QW

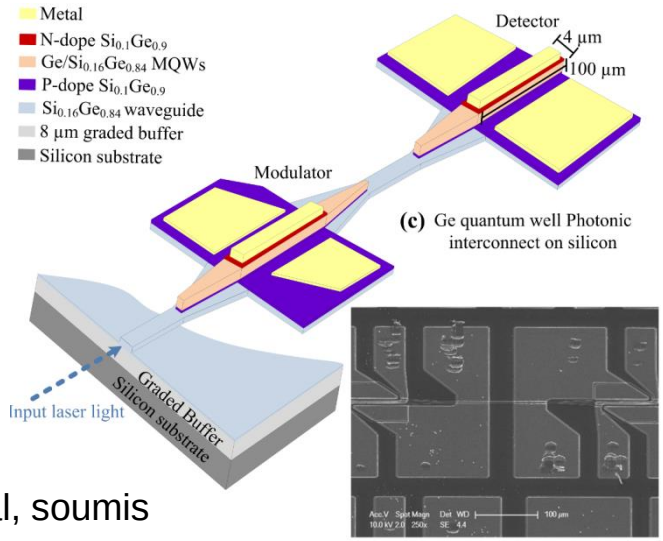
Integration on bulk silicon

1st option: waveguide in the relaxed SiGe layer (thanks to the graded buffer)

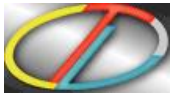


Ge concentration in the waveguide: trade-off between

- Strain compensation
- Optical loss



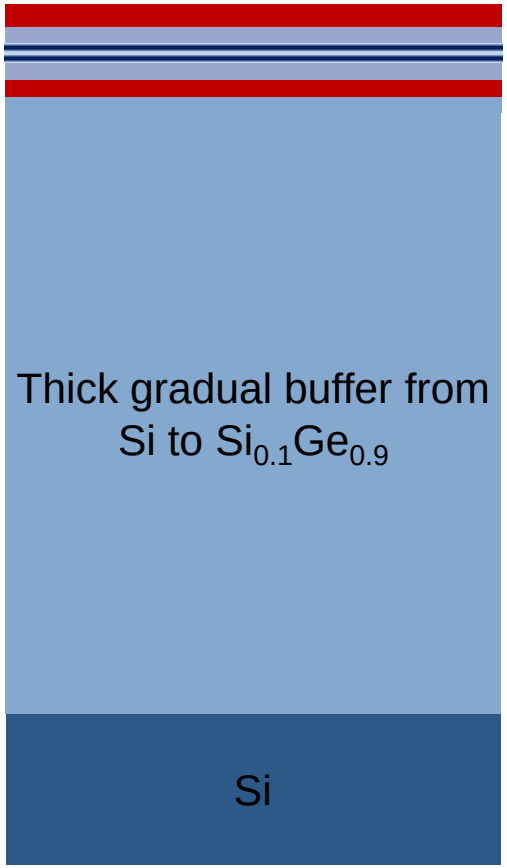
P. Chaisakul et al, soumis

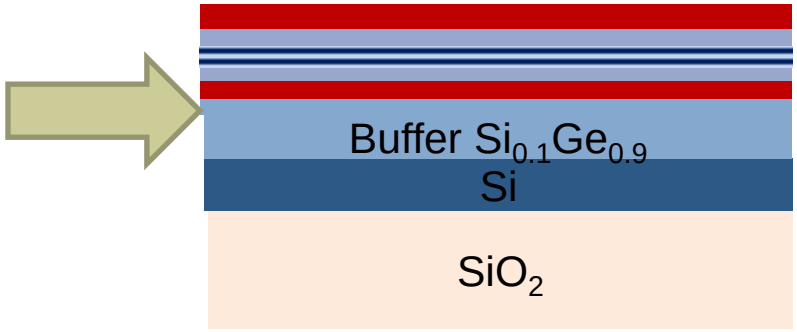


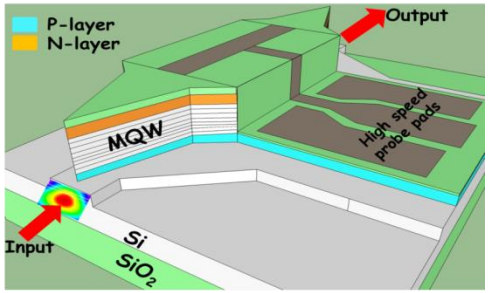
Optical loss of each device, including input/output coupling with $Si_{0.16}Ge_{0.84}$waveguide < 5dB

2nd option: decrease the thickness of the buffer layer

Challenge: keeping homogeneous and high quality layers

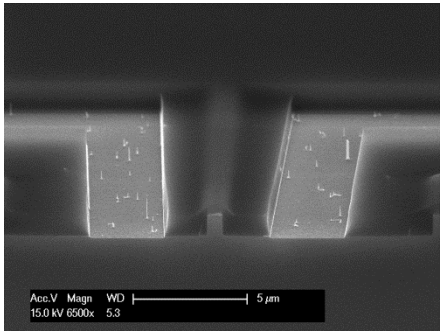






Ge/SiGe modulator integrated with SOI : estimated performance :
Extinction ratio = 7.7 dB, loss = 4 dB

M-S. Rouifed et al, soumis



Under fabrication

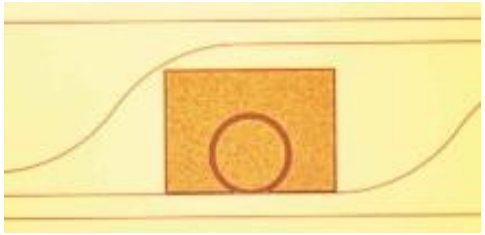
Power consumption evolution

Carrier depletion modulator MZi

Energy/bit ~ 5 pJ/bit

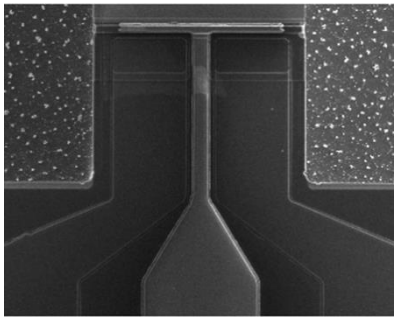
Ring resonator modulator

Energy/bit ~ 0.7 pJ/bit

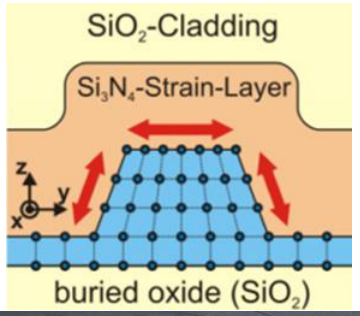


EA Ge/SiGe modulator

energy/bit ~ 0.07 pJ/bit



Strained modulator

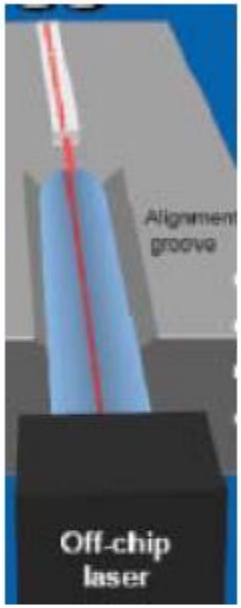


Ultra low power consumption modulator

energy/bit ~ few fJ/bit

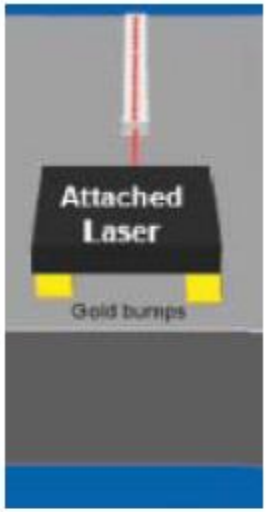
Laser on silicon

Off-chip laser
Fiber attachement & alignment
High coupling losses
Very expensive
Non-integrated



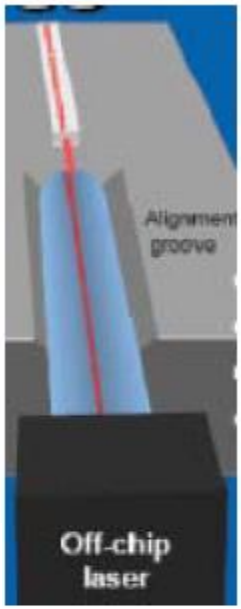
courtesy: Blas Garrido

Laser on silicon



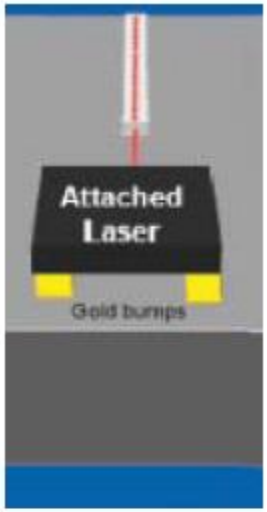
Attached laser
Tight alignment tolerances
Gold metal bonding
Expensive

Off-chip laser
Fiber attachement & alignment
High coupling losses
Very expensive
Non-integrated



courtesy: Blas Garrido

Laser on silicon



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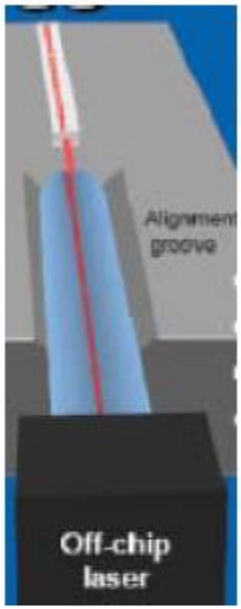
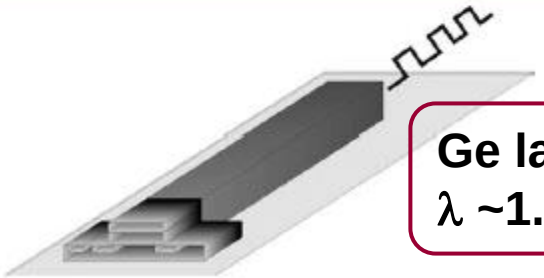


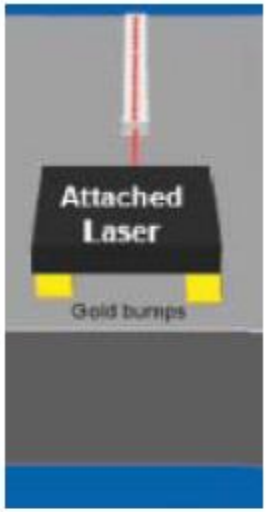
Monolithic laser Si compatible
Not any alignments
Highly integrable
Low cost
Electronic-photonic integration



Ge laser on Si
λ ~1.6µm

courtesy: Blas Garrido

Laser on silicon



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Expensive

Off-chip laser
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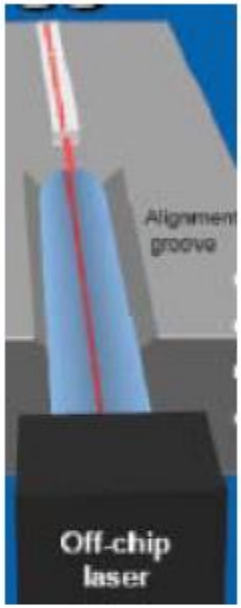
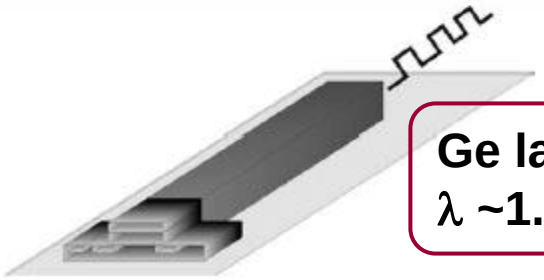
Non-integrated

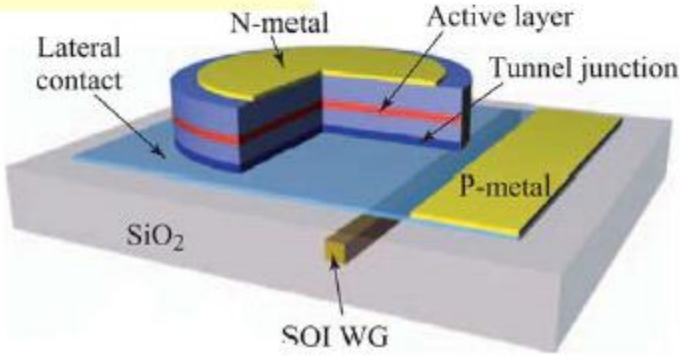


Monolithic laser Si compatible
Not any alignments
Highly integrable
Low cost
Electronic-photonic integration

Hybrid integrated laser
InP bonded laser to SOI CMOS
No alignment
Possibly to integrate
Moderate cost

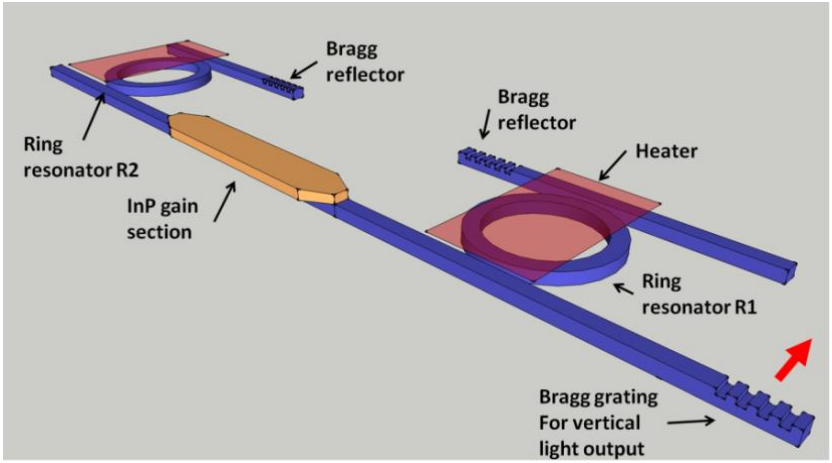


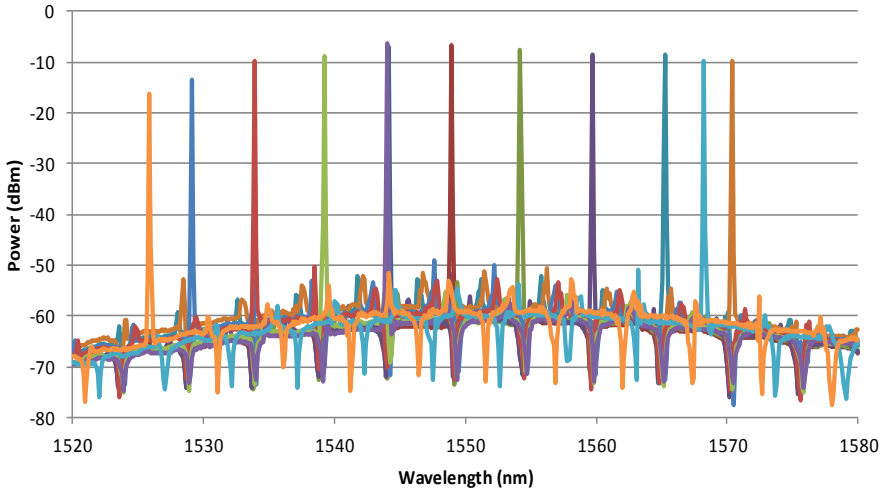
Ge laser on Si
λ ~1.6µm



courtesy: Blas Garrido

Tunable lasers





- 20 mA threshold at room temperature
- >45dB SMSR, tuning range 45nm

courtesy: G.H. Duan

Outline

1. Silicon photonics: motivation

2. Optoelectronic devices:

   - Photodetection
   - Optical modulation
   - Optical laser source

3. Electronic-photonic convergence

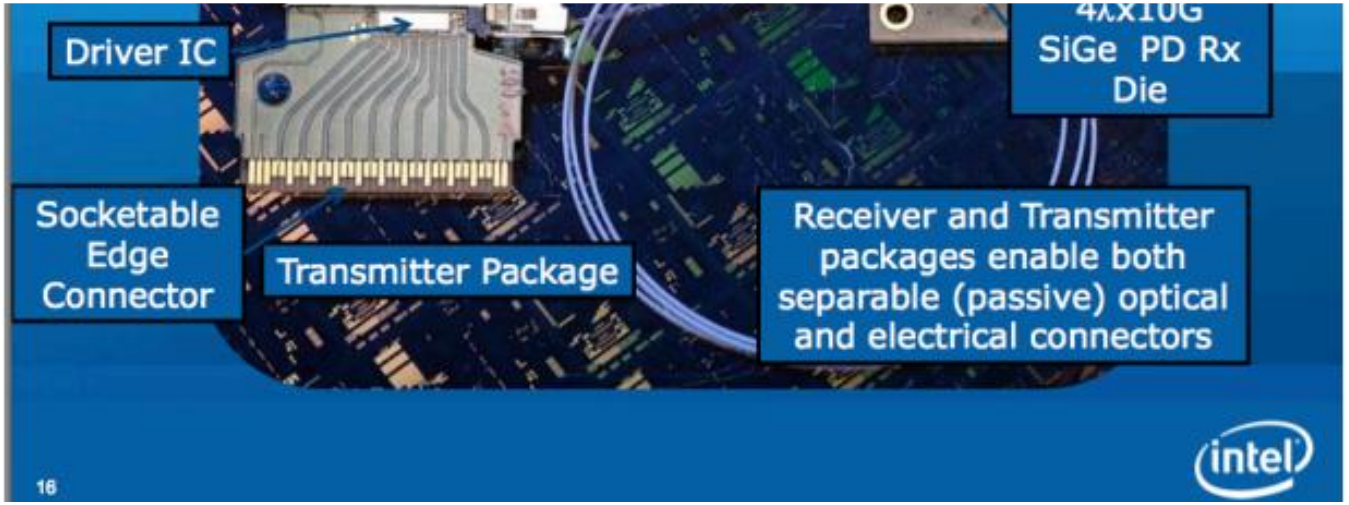
4. Conclusion

Option beta –

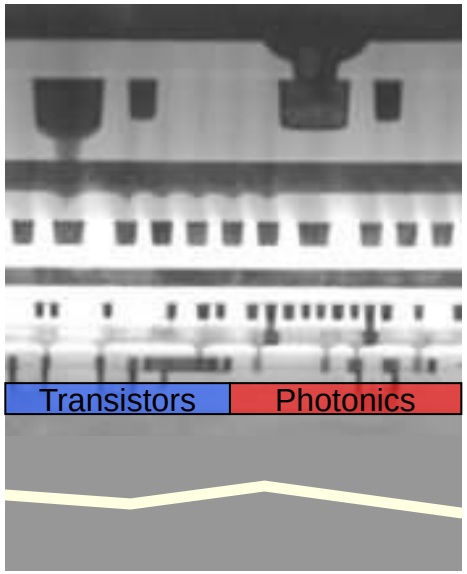
- Use wire-bonding to connect chips

Not a waferscale approach

Not compatible with micro-electronics packaging



Photonics-electronics integration



Front-end fabrication

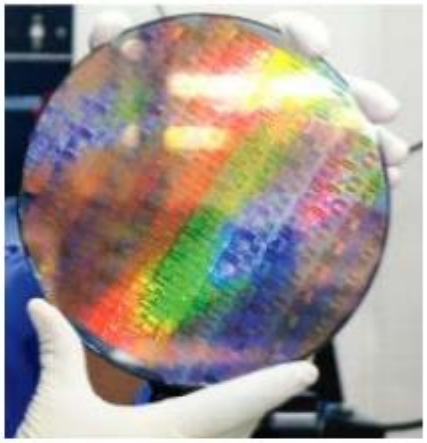
☺ Very low parasitics

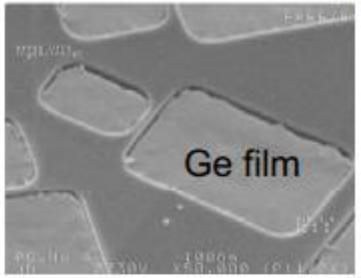
☹ Custom SOI, specific libraries

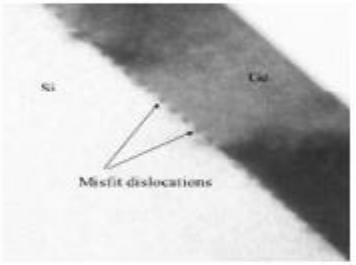
☹ process co-integration

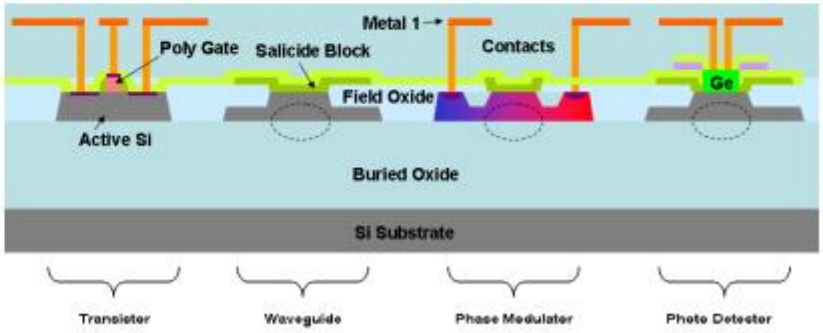
CMOS Photonics Process: LUX-G

- **LUX-G CMOS Process:**
  - 130 nm CMOS SOI Technology Platform (8") based on Freescale Semiconductor's HIP7SOI (PowerPC™ microprocessors and controllers)
  - Extensive library of photonic and electronic devices (including high-speed transistor models).
- **"Photonically-enabled" CMOS SOI process:**
  - Shallow trench etch: definition of waveguides and grating couplers
  - Selective Ge epitaxy for photo-detector integration
    - Low temperature growth of relaxed Ge films
    - Standard CMOS foundry toolset for Ge epitaxy (SiGe stressors, HBT)
    - After-salicidation approach:
      - No need for transistor protection
      - One contact module for all devices
- **LUX-G CMOS Process in manufacturing mode since 2008 (Maturity Level 3 at Freescale Semiconductor):**
  - All processes and tools standard and fully compatible with full flow SOI CMOS
  - Under change control and run by production team
  - Second of a kind (SOAK) fab tools verified in split lots
  - Process windowing experiments on split lots completed satisfactory
  - More than 1500 wafers (~ 61 lots) processed
- **Electronic and photonic device models:**
  - Based on material from different lots and process skews
  - Accurate transistor and interconnect models established
  - Results in improved circuit designs (e.g. power reduction) and high yields
- **Passed industry standard reliability qualification (JEDEC)**
  - Hot Carrier Injection, Negative Bias Thermal Instability, Time Dependent Dielectric Breakdown, Electromigration
  - Performed on nmos, pmos, sgo and dgo test structures from 3 different lots

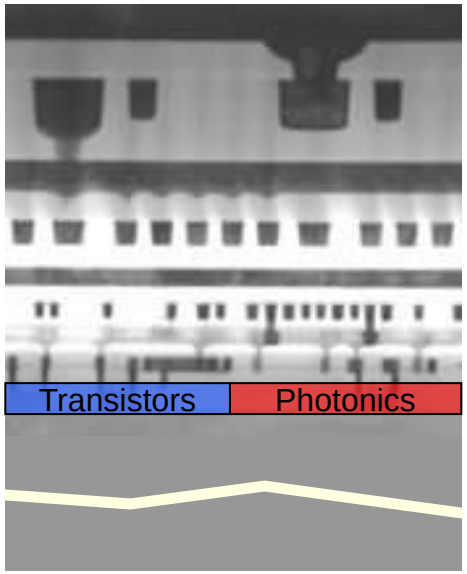








Photonics-electronics integration



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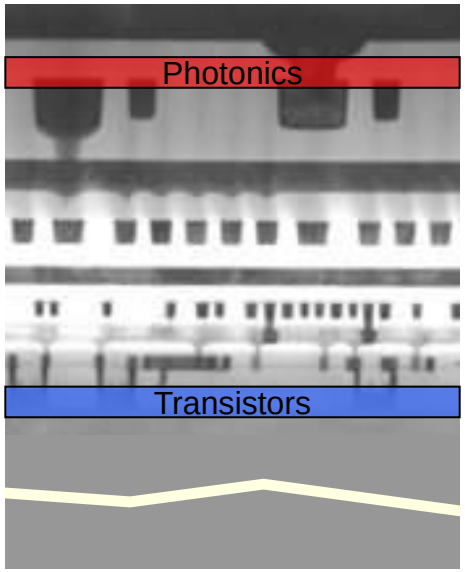


Back-end fabrication

☺ On top of CMOS or in metal layers

☺ Serial process

☹ Compound yield

☹ Thermal budget < 400C

MIT BEOL approach

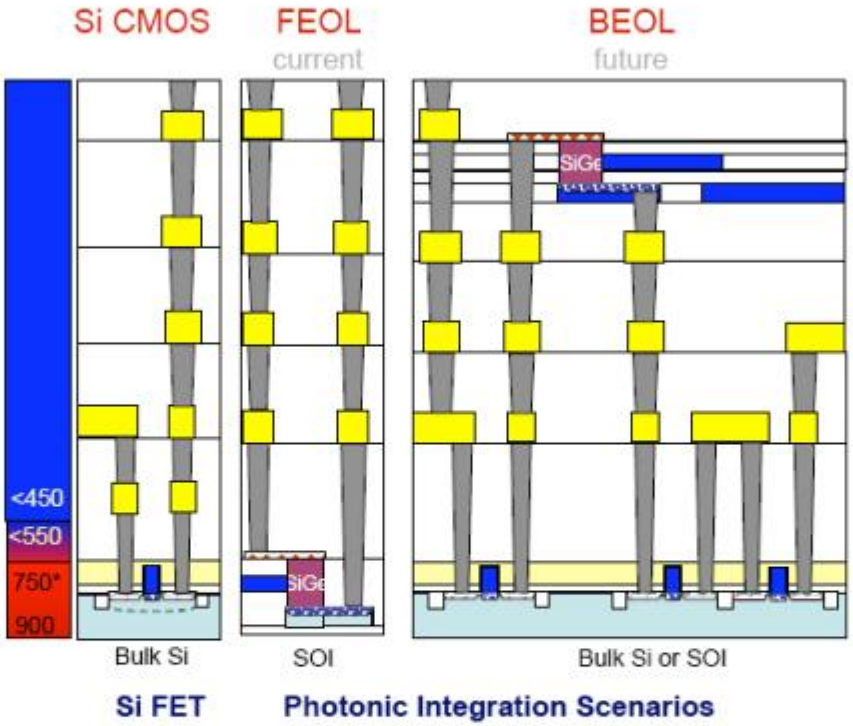
Target Areas for Integration

FEOL for current devices

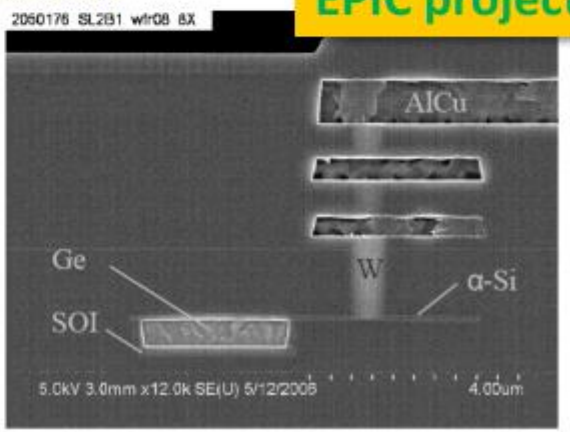
- Shared area with FET's
- Crystalline Si low loss WG's
- Temperature tolerant processing

BEOL for future device generations

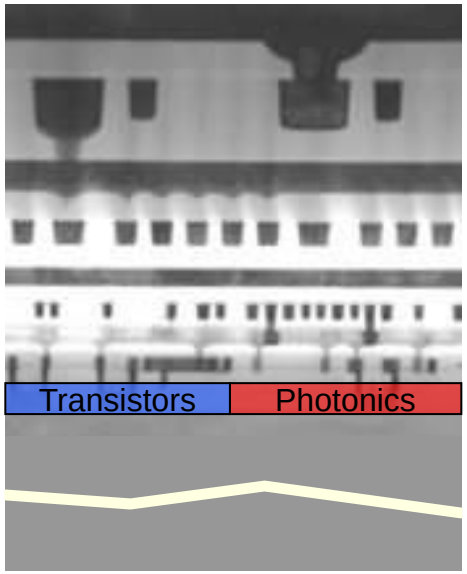
- T_{limit} < 450 °C
- Current research focus



EPIC project



Photonics-electronics integration



Front-end fabrication

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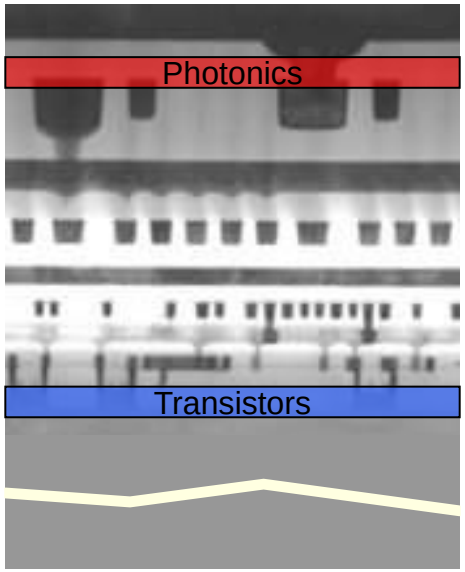

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☹ Compound yield
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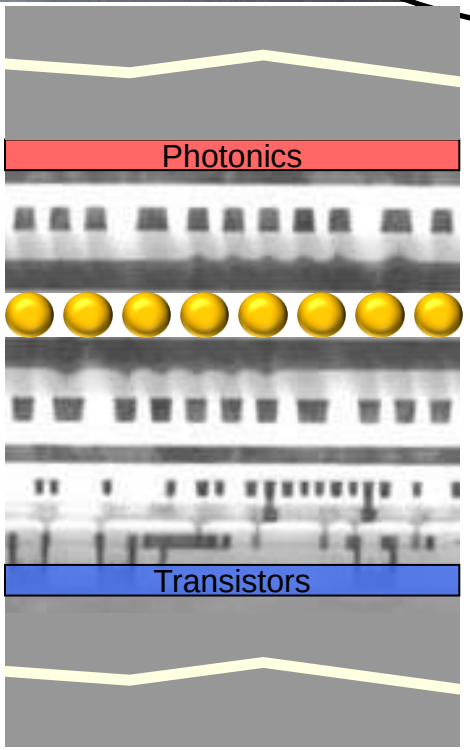
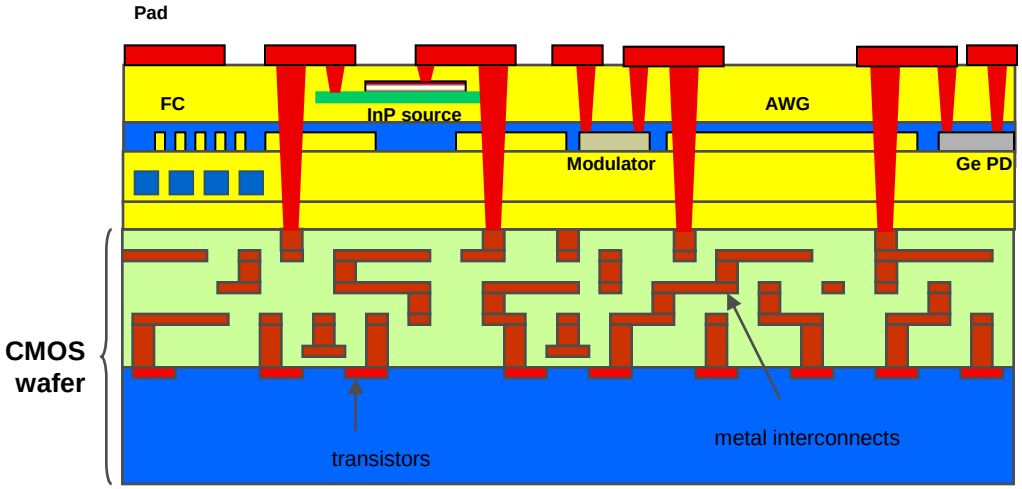


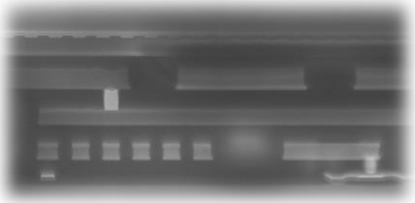
3D integration

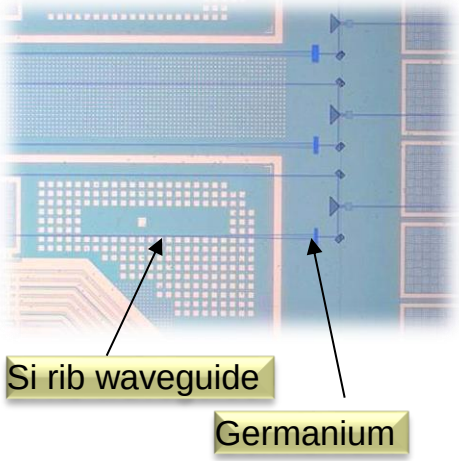
☺ Separate processes
☺ No change in CMOS Front-End
☺ No thermal budget!
☺ Other layers: MEMS, antennas
☹ Higher (but reasonable) parasitics

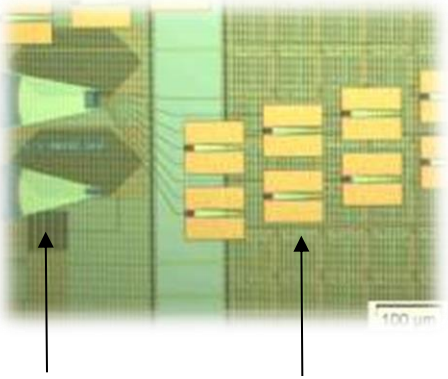
3D integration

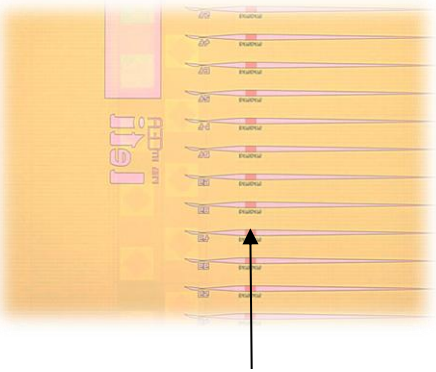


- 3D integration
- Not depending on the specific node used to produce the electronic wafer









Conclusion

- Photonic links may replace copper links, even for very short distances
  - √ Silicon photonics is more and more a mature technology with the demonstration of 40Gbit/s optoelectronic devices including optical modulators and photodetectors
  - √ Development of silicon photonics on 300mm platform
- Advances in electronic - photonic integrated circuits (EPIC)
- New trends:
  - √ Low power consumption optoelectronic devices

⇒ Ge/SiGe platform on silicon
⇒ Strained silicon photonics

Acknowledgements: Funding and collaborations

National Research Agency

SILVER, MICROS, GOSPEL, MASSTOR, ULTIMATE, Ca-Re-Lase, POSISLOT

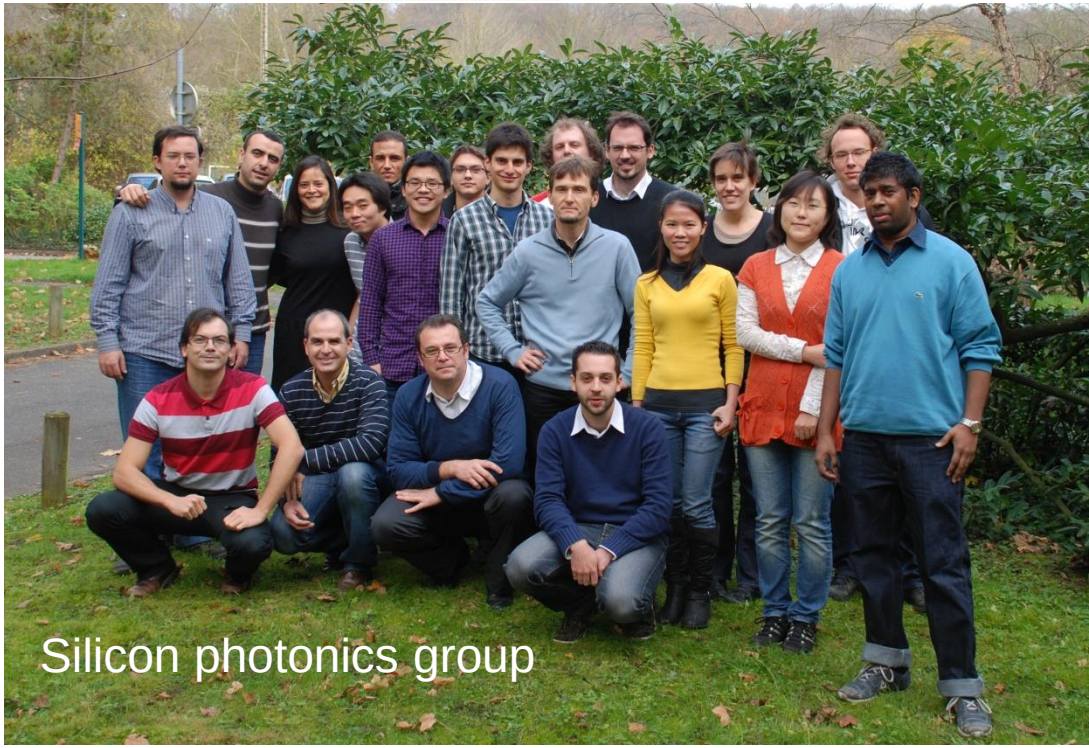
UNION EUROPEENNE

HELIOS
Photonics Electronics functional integration on CMOS

Plat4M
photonic libraries and technology for manufacturing

SASER
Safe and Secure European Routing

CARTOON
Carbon nanotube photonic devices on silicon


Silicon photonics group