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Introduction to Very Deep Sub Micron CMOS technologies: the 65nm CMOS process for mixed mode analog-digital circuits

Wednesday 16 July 2014 09:00 (1 hour)

Presentation type

Lecture

Summary

Future upgrades of detector systems for high energy physics experiments at high-luminosity colliders and for photon science at advanced X-ray sources set unprecedented and extremely challenging requirements to the readout electronics. In the case of pixel detectors, current designs of front-end microelectronic systems foresee the integration of very complex analog and digital functions inside small readout cells, and have to ensure the capability of handling huge data rates and of keeping adequate performance at extremely high radiation levels. The progress of industrial microelectronic technologies has to be exploited to the purpose of complying with these aggressive designs ideas for front-end integrated circuits at future experiments. Recently, the community of microelectronic designers has focused its activity on the 65 nm CMOS generation as a promising technology for these applications. This lecture provides a review of the potential advantages and challenges associated to the design of low noise, high speed and rad-hard mixed-signal circuits in such a process for pixel detectors in the fields of high energy physics and photon science.

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Session Classification: Second Morning Session