Preliminary simulation study of a Coincidence Avalanche Pixel Sensor

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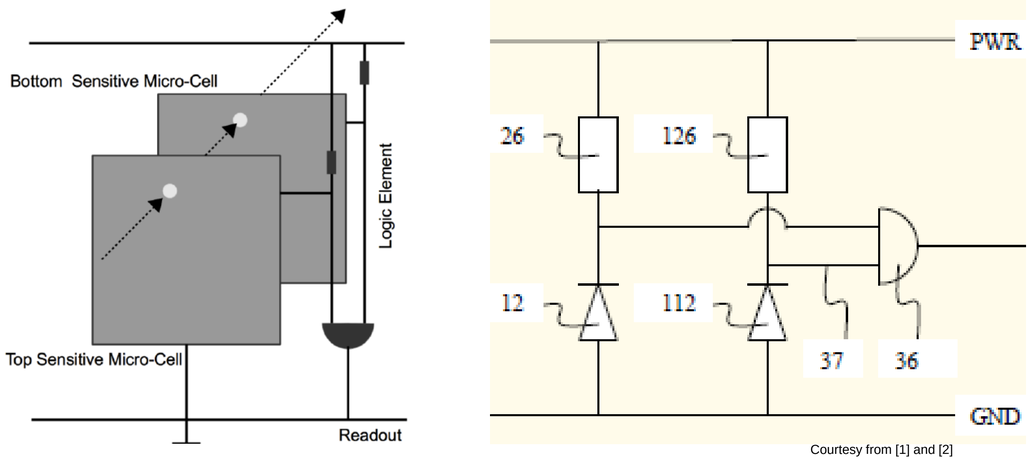
Introduction

The development and optimization of position sensitive detectors is of crucial importance in vertex tracking applications for HEP experiments, where material budget, very high spatial resolution and noise immunity are very important aspects. Besides the power dissipation of the Front-End Electronics (FEE) sitting on the detector has a strong impact as it may need cooling systems which are also material budget consuming. A number of R&Ds on new pixel technologies address all these issues under active development and competition. The focus is on new pixel sensor technologies, improvements of the associated FEE and services (cooling, cabling, etc.) material budget reduction. Among these R&D's, an innovative device based on silicon avalanche diodes and exploiting the concept of coincidence detection has been proposed for the first time in [1] and referred as "Avalanche Pixel Sensor" (APiX) and further developed [2]. This poster presents some specific simulation study related to Premature Edge Breakdwon prevention by adopting suitable designed guard rings besides other important considerations about the in-pixel read-out electronics

The coincidence detection



Courtesy from [1] and [2]

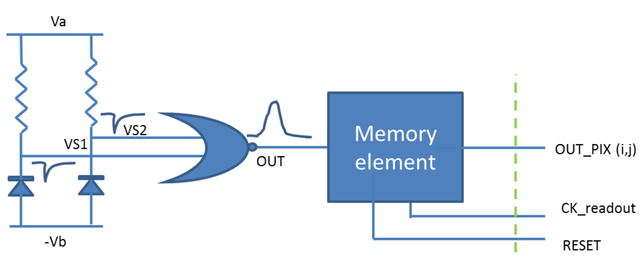
- The passage of an ionizing particle through the pair of vertically aligned cells triggers a breakdown process in each cell, producing two substantially coincident electrical signals
- The detection of a coincidence event allows discrimination of the signal produced by an incoming ionizing particle from background Ultra-Violet, Visible and Near-Infrared photons and thermal dark counts
- A fake coincidence may occur if a microcell is activated by a thermal generated electron or background photons and, within a certain coincidence window, the other cell is activated as well.
- The fake coincidence rate is given by the following:

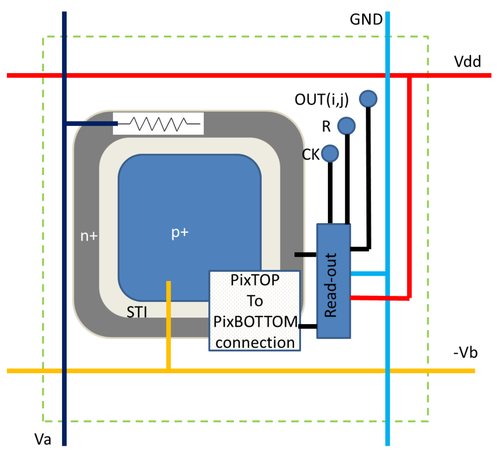
$$FCR_{APiX} = 2DCR'^2 A^2 \Delta t$$

where DCR' and A are the dark count rate per unit area and sensitive area of each avalanche diode respectively. Δt is the coincidence window.

DCR vs FCR				
Technology	*DCR' (T=25°C)*	*Area*	*DCR*	*FCR*
Hamamatsu [3]	$0.1\frac{Hz}{\mu m^2}$	50x50 μm^2	250Hz	1.25mHz
Commercial CMOS 130nm [4]	$320\frac{Hz}{\mu m^2}$	50x50 μm^2	800kHz	12.8kHz

In-pixel electronics



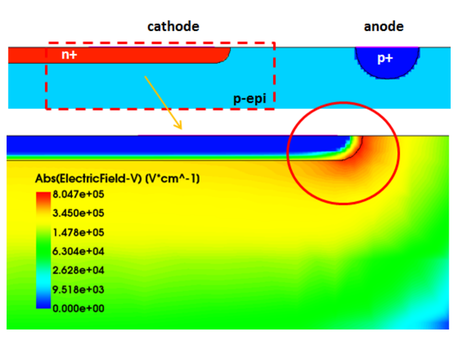


- 3D pixel: two vertically aligned avalanche cells have to be interconnected by using a 3D technology
- Minimal and simple quenching and in-pixel read-out circuits to maximize the detector fill factor.
- In pixel signal distribution and fast read-out (40 MHz per pixel) is challenging

Avalanche diode design

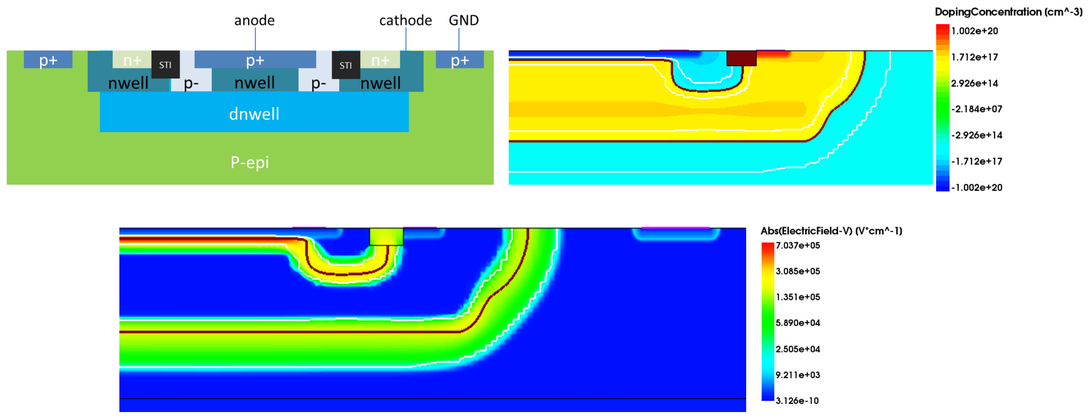
Main challenges in the design of avalanche diodes by using a commercial CMOS technology not optimized for detector design:

- Premature edge breakdown (PEB) prevention by adopting a proper guard-ring
- Guard-ring must not impact too much on the detector fill factor
- Dark count rate, afterpulsing and pixel-to-pixel cross-talk have to be minimized by exploiting different CMOS solutions



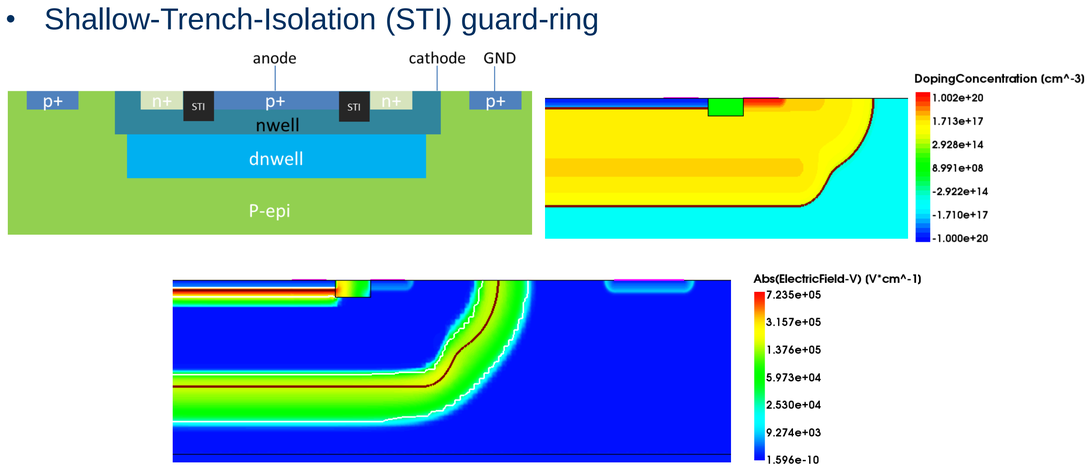
Guard-ring TCAD simulations with Synopsys Sentaurus for Premature Edge Breakdown (PEB) prevention

- P- guard-ring



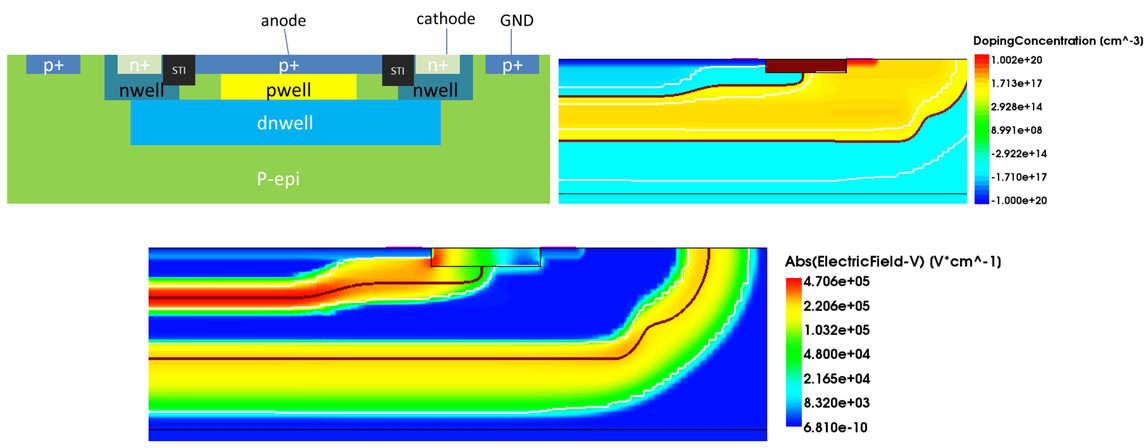
✓ PEB is prevented by surrounding the p+/nwell junction with pwell regions
❑ STI is placed far enough from the multiplication region thanks to a STI blocking layer at the expense of a reduced fill factor in order to avoid dark count degradation due to defects at the Si/STI interface
❖ The diode is formed by a highly doped p+ region and a nwell which may enhance band-to-band tunneling processes and therefore dark counts

- Shallow-Trench-Isolation (STI) guard-ring



✓ PEB is prevented and the multiplication region is properly confined inside the STI ring. In this way the detector fill factor is optimized.
❖ Defects at the Si/STI interface represent an additional source of dark current generation. Therefore the dark count rate may consequently result enhanced in this guard-ring implementation.
❖ The diode is formed by a highly doped p+ region and a nwell which may enhance band-to-band tunneling processes and therefore dark counts

- P-epi guard-ring in a buried pwell/dnwell junction



✓ PEB is prevented
✓ The diode is formed by a pwell and a deep nwell which should result in a low probability of band-to-band tunneling and therefore a lower dark count rate.
❑ STI is placed far enough from the multiplication region thanks to a STI blocking layer at the expense of a reduced fill factor in order to avoid dark count degradation due to defects at the Si/STI interface

Conclusion

- The impact of guard-ring design as well as band-to-band tunneling due to high doping profiles in deep sub-micrometer technology on dark count rate enhancement is on-going
- In parallel, an in-pixel read-out electronics design is in progress

References

[1] V. Saveliev, "Avalanche Pixel Sensor and Related Methods", US Patent. 8,269,181 (2012)
[2] N. D'Ascenzo, P.S. Marrocchesi, S. Moon, F. Morsani, L.Ratti, V. Saveliev, A. Savoy Navarro and Q. Xie, "Silicon Avalanche Pixel Sensor for High Precision Tracking" 13th Topical Seminar on Innovative Particle and Radiation Detectors IPRD13
[3] http://www.hamamatsu.com/eu/en/product/category/3100/4004/4113/S12571-010C/index.html
[4] C. Niclass, M. Gersbach, R. Henderson, L. Grant, E. Charbon, "A single photonavalanche diode implemented in 130-nm CMOS technology", IEEE J. Sel. Top.Quant. Electron. 13 (2007) 863–869.

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