Trends and Strategies for Triggering in HEP experiments

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Introduction & objectives

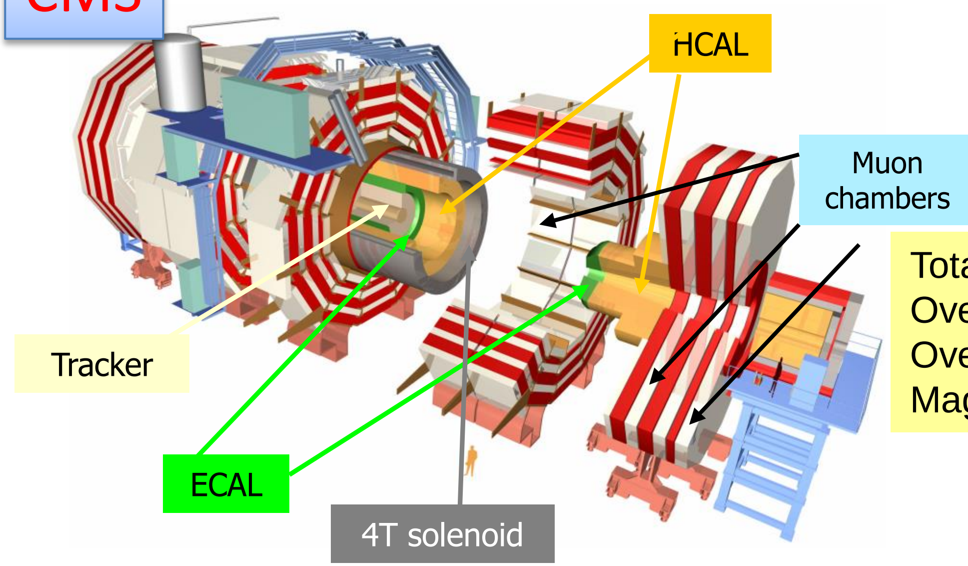
- Subject proposed by organisers
  - with a request to compare ATLAS, CMS and LHCb strategies
- Part 1: Review the current triggers
  - with only brief descriptions of the experiments
  - broadly similar approaches, with subtle differences
- Part 2: Describe the plans for the future at HL-LHC
  - experiments diverge significantly from each other
- I hope to answer: In what way, and why?
- Warning:
  - I need to assume some familiarity with some of the material to cover such a big subject. I hope not too much…
- Thanks for slides from other sources which I try to acknowledge!

The experiments in a nutshell

- ATLAS and CMS are General Purpose LHC experiments
  - similar overall designs, but some important differences in philosophy
- CMS – cylindrical 4T 6m diameter solenoid magnet
  - contains silicon tracker, crystal ECAL, brass-scintillator HCAL, +…
  - gaseous muon system in iron yoke return magnetic field
- ATLAS – vast toroidal open magnet system for muons
  - inner tracking detector in 2T B-field: silicon and TRTs
  - LAr and scintillator-tile calorimeters, gaseous muon detectors
- LHCb - a dedicated forward spectrometer at LHC
  - narrower range of objectives, esp B-physics, CP violation, rare decays
    - particle ID using Cerenkovs
  - very different layout to GPDs in some important respects
  - scintillator calorimetry, gas detectors in muon system

LHC Detectors

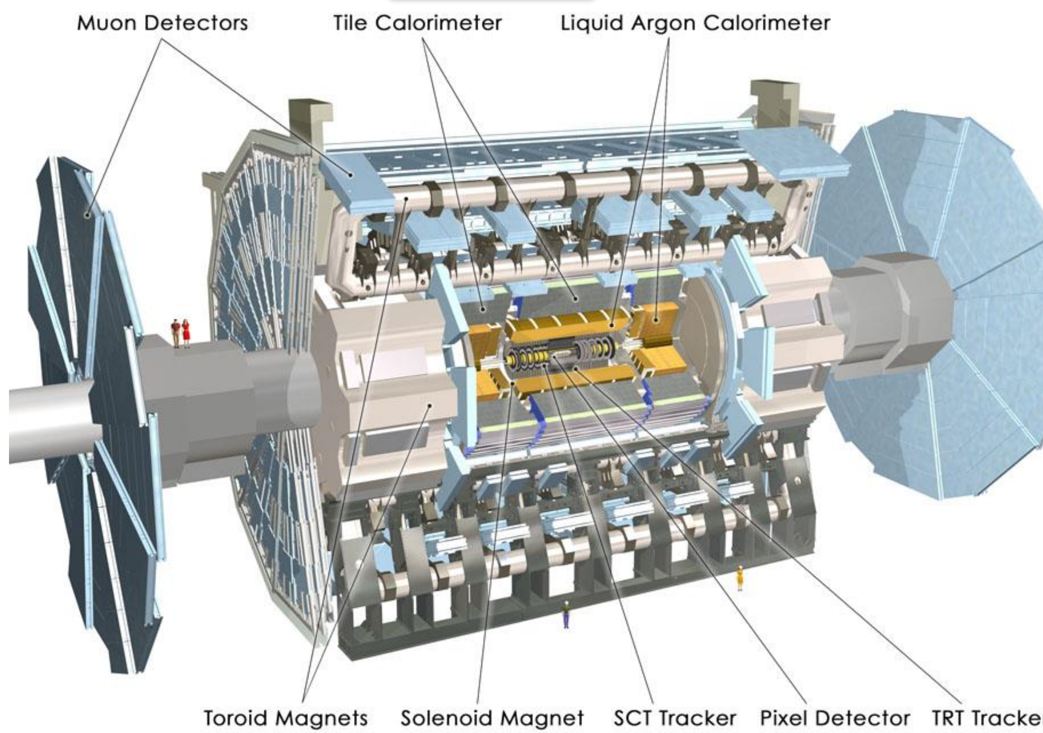
CMS



Total weight 12,500 t
Overall diameter 15 m
Overall length 22 m
Magnetic field 4 T

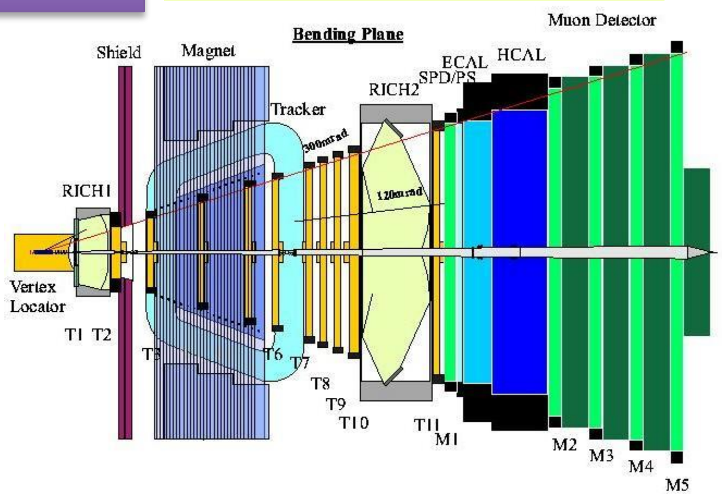
ATLAS

Total weight 7,000 t
Overall diameter 25 m
Overall length 44 m
Solenoid B field 2 T



LHCb

Overall length 20 m
Integral B field 4 Tm



Detectors & trigger

- ATLAS & CMS – similar physics goals and detector requirements
  - similar angular coverage
  - emphasise leptons, down to low p_T for wide range of physics
  - electronics deeply embedded inside the experiment, with little access
  - run at maximum machine luminosity with high efficiency
  - μs: open geometry with large lever arm & little material (ATLAS)
  - detectors embedded in magnet yoke, lower volume & more scattering (CMS)
  - Calorimeters: LAr with long electron drift time (ATLAS)
  - scintillators with fast charge collection ~ 1BX (CMS)
- LHCb - to capture high statistics modest luminosity is sufficient
  - many final states with muons, $e/\gamma/\pi^0$ with high p_T from B decay

Basic problem

- Reduce event rate so that next stage of processing can be done
  - keep repeating until rate is low enough
  - then store data for full analysis (at leisure!)
- Sounds like a simple problem?
  - what is raw event rate?
  - how long is available to make decision?
  - how long is available for processing data?
  - what is the rate reduction to be achieved?
- Event rate determined by total pp cross-section
  - at $L = 10^{34}\ cm^{-2}s^{-1}$ => ~20 events per 40 MHz bunch crossing in CMS & ATLAS
    - there may also be signal remnants from earlier crossings
    - in LHCb luminosity is lower to aim for <N> ~ 1 event per crossing
- Rate at which data can be stored ~100 Hz (1990s) – few kHz (today)

Trigger levels

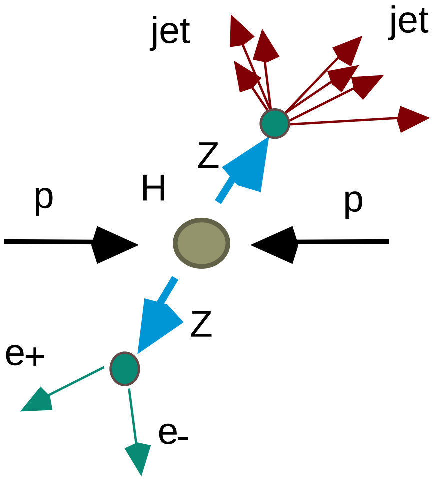
- Not feasible to go from raw event rate to storage rate in one step
  - data volume is large
  - data are not physics quantities (E, p, x, y, z, vectors…): convert & calibrate
  - algorithms for decisions may be complex
  - multiple overlapping events must be distinguished
  - processing speed and number of processors are finite
  - there are (not small) overheads from data transmission delays: t ~ L/c
  - data must be temporarily stored **locally** until event decision is made
- LHC solution – multi-level trigger
  - L1: fast hardware decision constrained by on-detector electronics
    - pipeline memory sizes, power for digitisation, precision of variables
  - L2: possible intermediate decision in hardware
  - L3: maximal event processing before storage
    - not usually with full offline precision

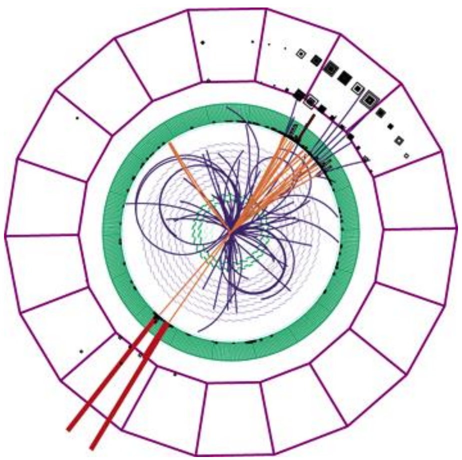
Trigger requirements

- High – as possible - efficiency for the most interesting events
  - should not introduce bias
- Large (enough) rate reduction
  - but can pass unwanted (with hindsight) events as BW permits
- Fast decision
  - to match hardware constraints, mainly at FE
- Deadtime free
  - to maximise good data, and $\varepsilon^N << 1$
- Flexible enough to adapt to changing experimental conditions
  - physics programme also evolves and typical early focus is on limited number of searches
- (affordable in $ & W)

Triggering

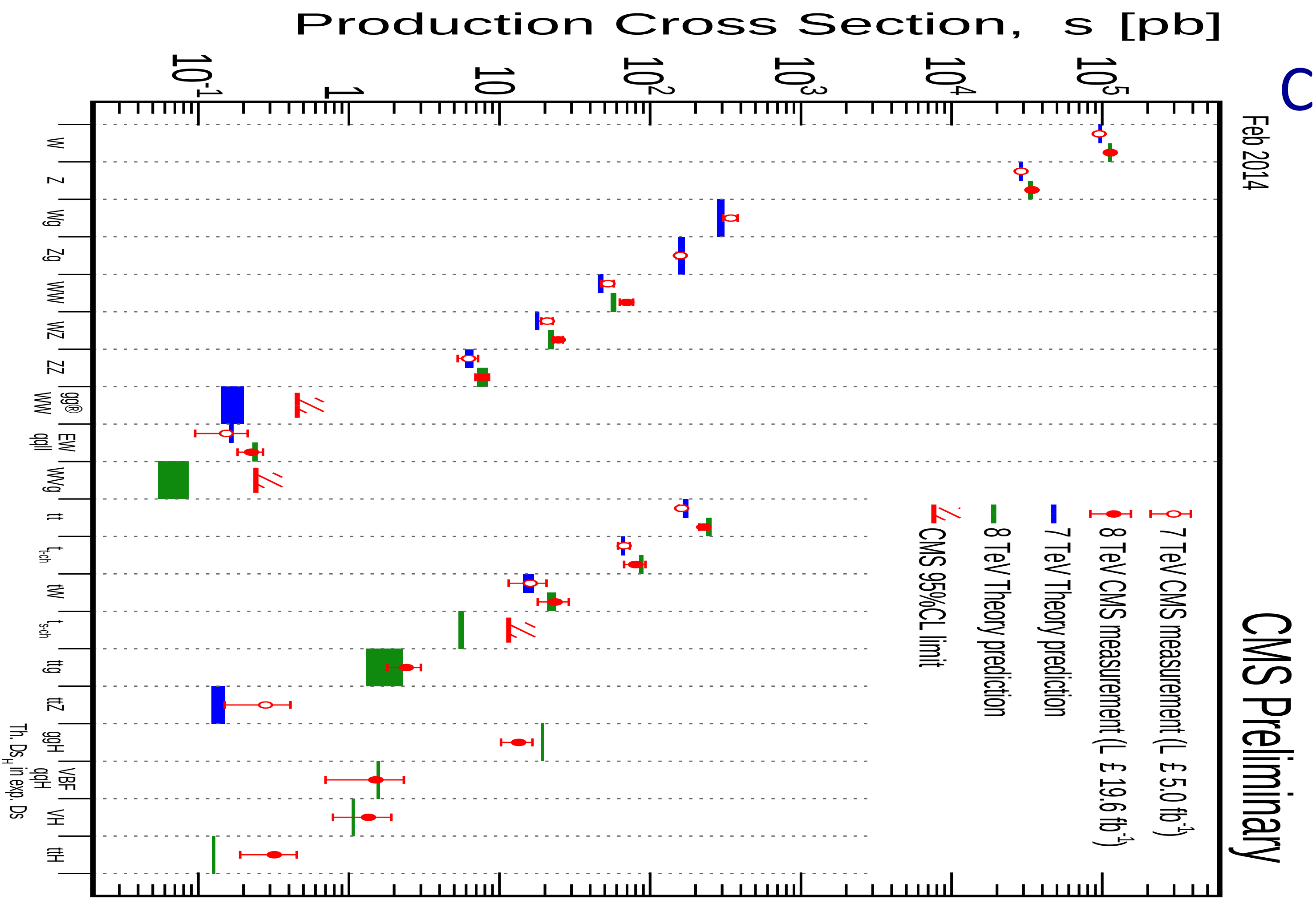
- Primary physics signatures in the detector are combinations of:
  - Candidates for energetic electron(s) and photons (ECAL)
  - Candidates for μ(s) (muon system)
  - Hadronic jets (ECAL/HCAL)
- Vital not to reject interesting events
  - very wide range of cross-sections, many very small
- Fast Level-1 decision in custom hardware
  - Higher level selection in software





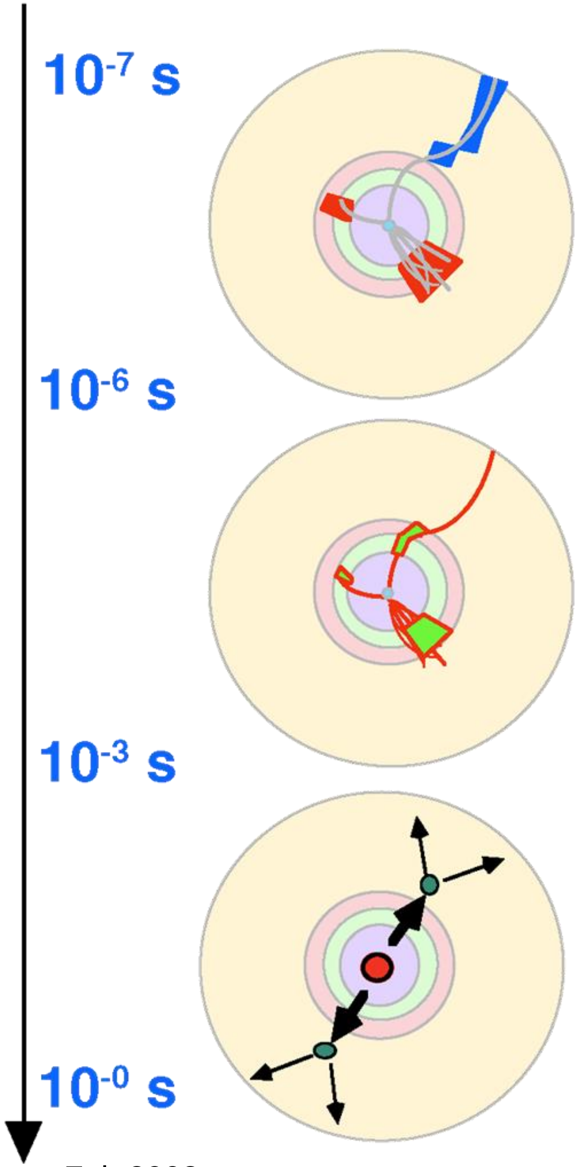
- Tracker not part of L1 trigger
  - Data volume enormous
  - Technically was not feasible for LHC

Cross-sections



- $\sigma_{b\bar{b}} = (75.3 \pm 14.1)\ \mu b$ [Phys.Lett. B694 (2010)]
  ⇠ 0.2% of events contain bb in acceptance
- $\sigma_{c\bar{c}} = (1419 \pm 134)\ \mu b$ [Nucl. Phys. B871 (2013)]
  ⇠ 4% of events contain $c\bar{c}$ in acceptance

LHC Trigger Levels



Collision rate 10^9 Hz

Channel data sampling at 40 MHz

Level-1 selected events 10^5 Hz

Particle identification (High p_T e, μ, jets, missing E_T)

- Local pattern recognition
- Energy evaluation on prompt macro-granular information

Level-2 selected events 10^3 Hz

Clean particle signature (Z, W, ..)

- Finer granularity precise measurement
- Kinematics. effective mass cuts and event topology
- Track reconstruction and detector matching

Level-3 events to tape 10..100 Hz

Physics process identification

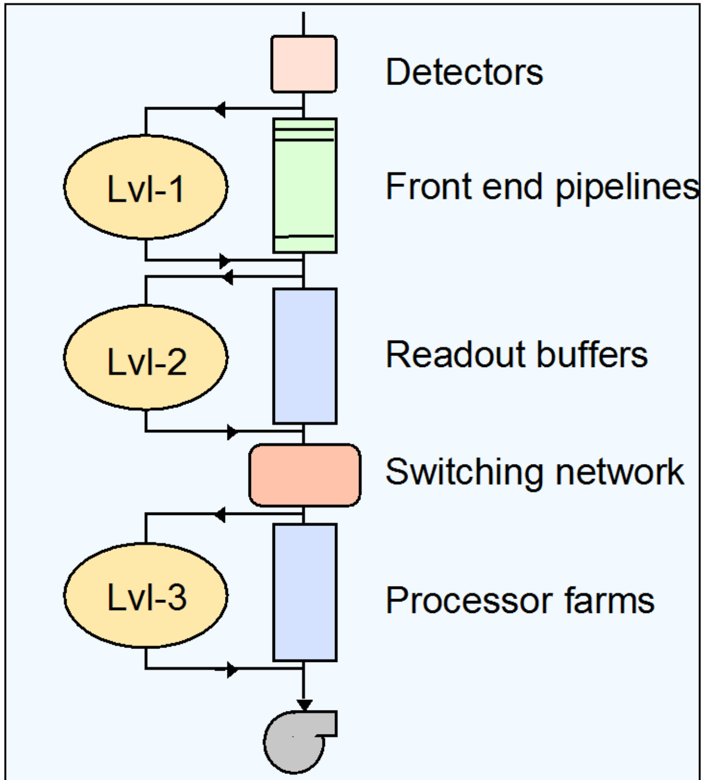
- Event reconstruction and analysis

Online Selection Flow in pp

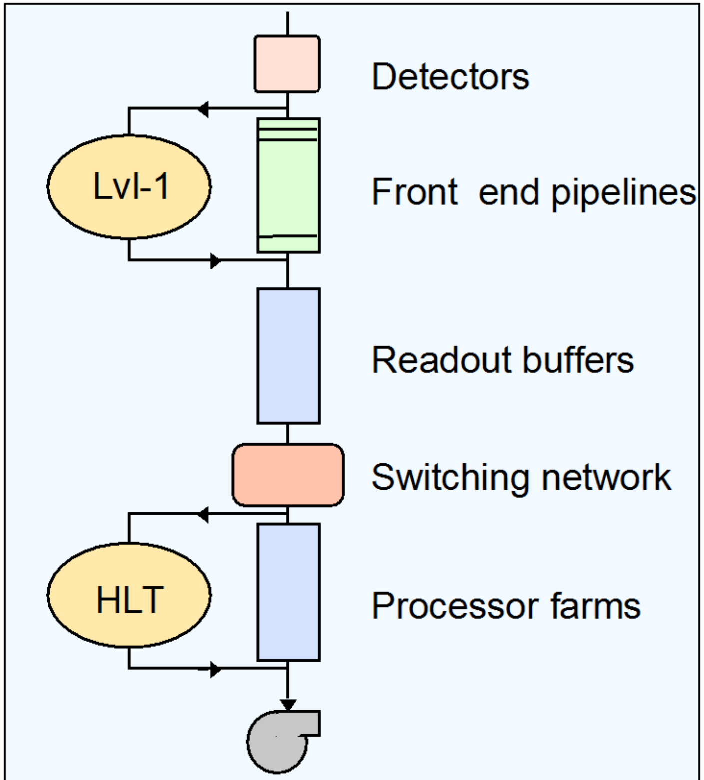
- Level-1 trigger: reduce 40 MHz to 10^5 Hz
  - This step is always there
  - Upstream: still need to get to 10^2 Hz; in 1 or 2 extra steps

LHCb call this L0

LHC GPD target



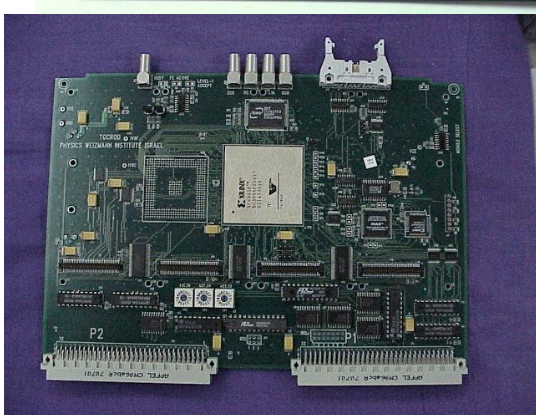
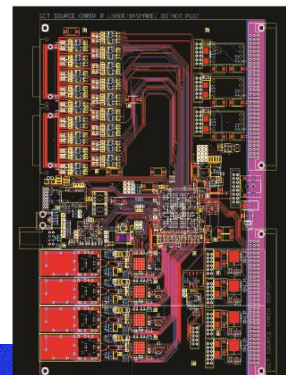
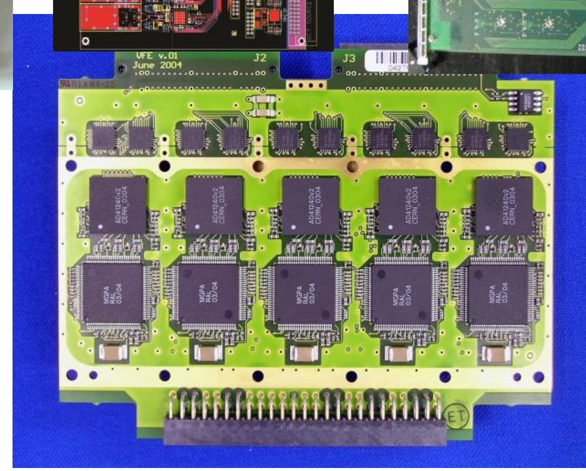
"Traditional": 3 physical levels

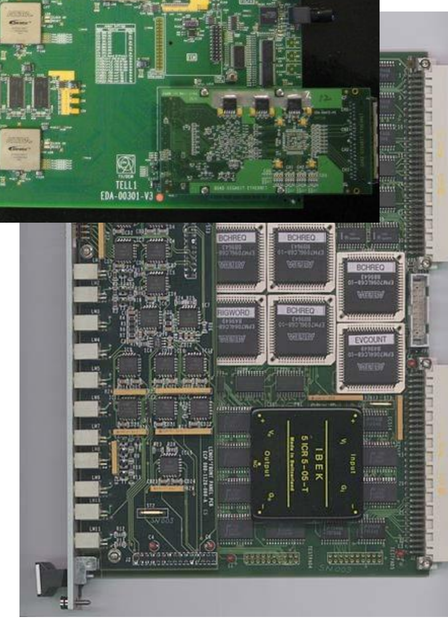


CMS: 2 physical levels

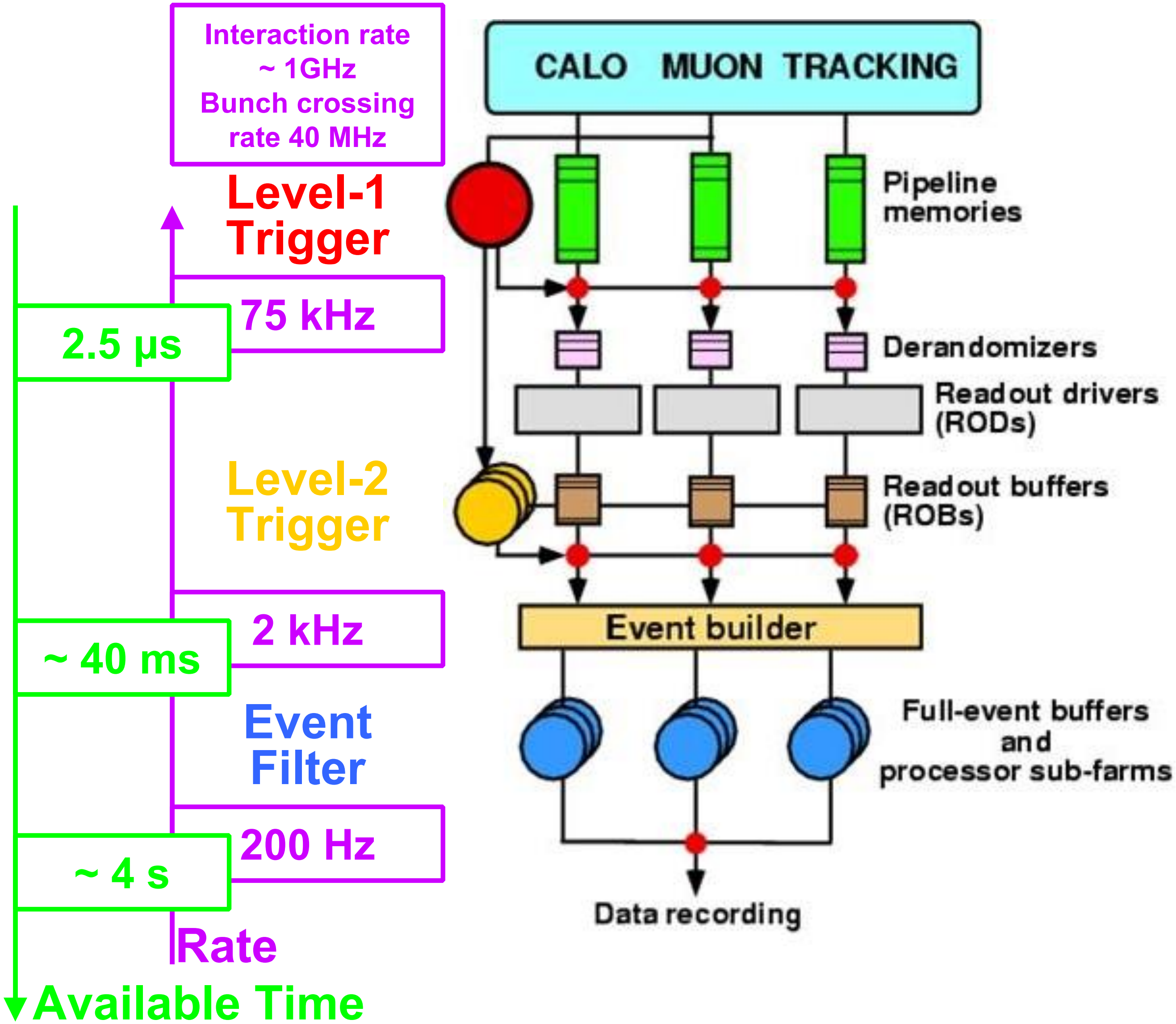
L1 processing hardware

- Processing hardware based on ASICs and FPGAs
  - ideally flexible but constrained by objectives and technology performance
    - evolves with time
  - aim for pipelined, parallel computations



ATLAS Trigger/DAQ System



Level-1 Trigger:
Electronics + Firmware

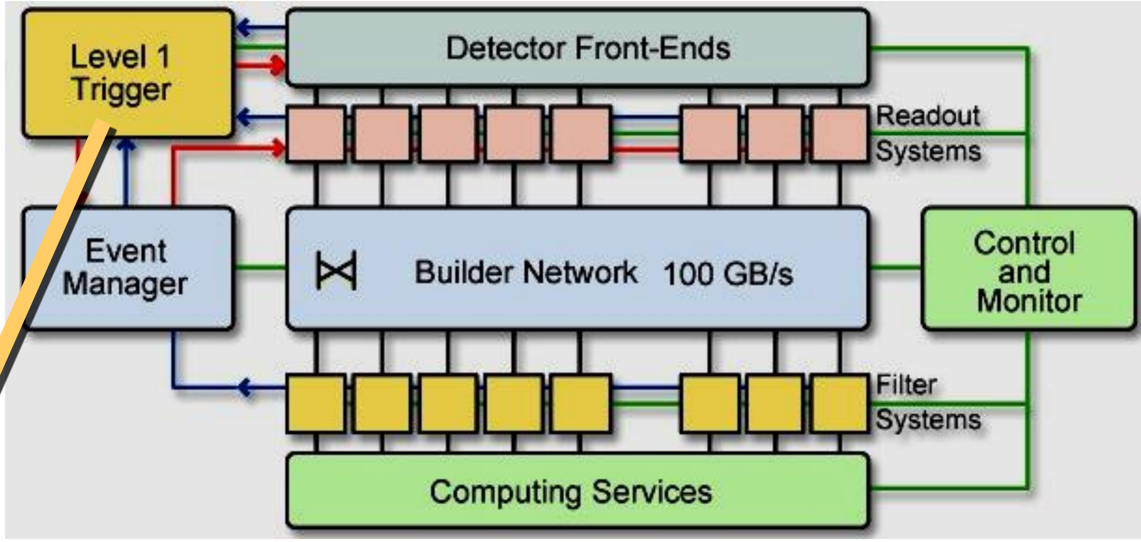
Level-2 Trigger

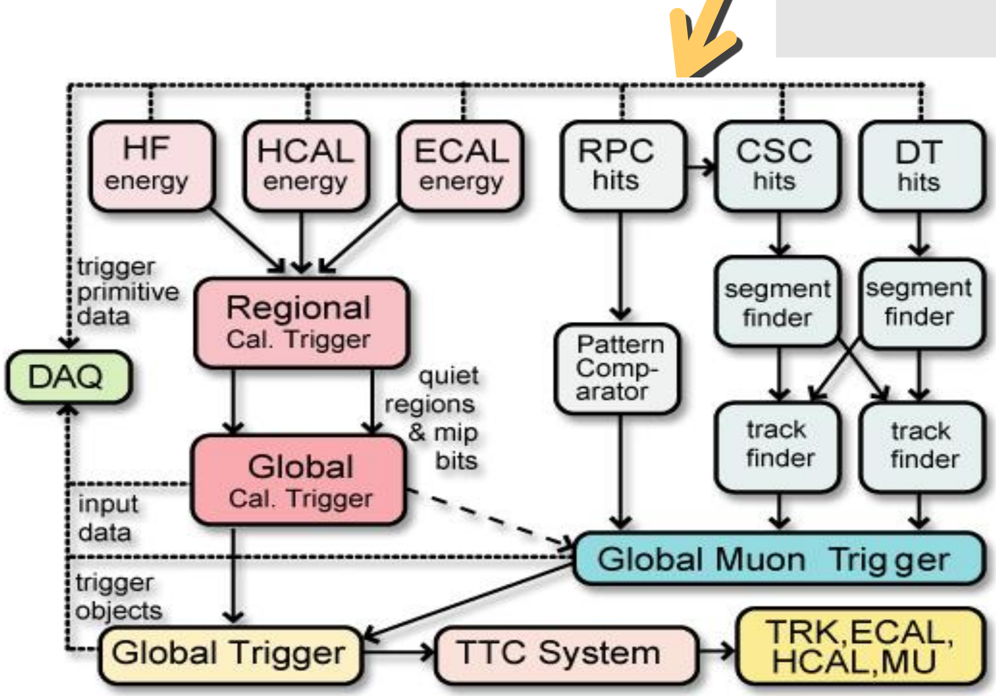
+ Event Filter:

- L2 trigger processes data from Regions of Interest to limit data transfers before final trigger decision

CMS Level-1 Trigger & DAQ

- L1 trigger initiates transfer of event data from detector to HLT
  - Readout Systems
  - Filter Systems
- No intermediate trigger stage





L1 Trigger:
- Highly distributed
- Both on detector and off detector
- Large variance in technology
- Trigger based on calorimeter and muon systems (no Si-Tracker)
- It is reasonably programmable

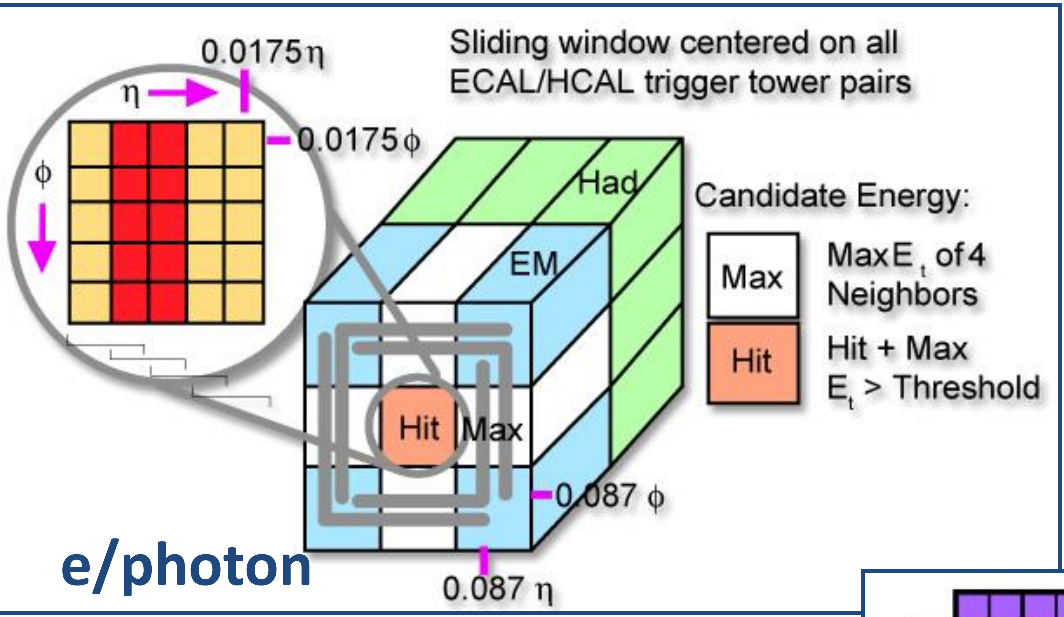
Issues for trigger (1)

- L0/L1 latency - determined by FE electronics technology
  - ASIC pipelines in trackers, calorimeters 128 - 256 BX
    - longer lengths now feasible but 10-20μs practical limit
  - Processing time depends on cable delays, TOF & experiment geometry
- Bunch crossing association
  - fast response sensors or more complex processing
    - even more complex with increasing pileup
  - synchronisation of detectors and data links
    - clock quality and distribution
- Bandwidth requirements
  - speed of links (<1 Gbps 1990s, >10 Gbps today)
  - volume of data : no of channels and no bits
  - data routing, error correction & decoding, serialisation/deserialisation

Issues for trigger (2)

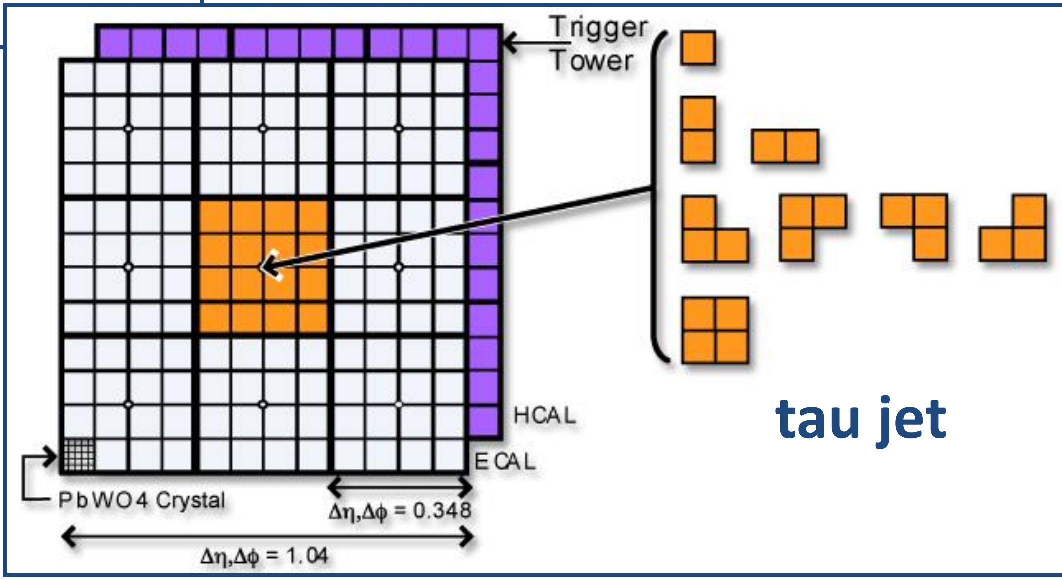
- Event processing challenges
  - Boundaries and size of objects (jets cf e/γ)
    - transferring and sharing data between boards, remaining synchronised
  - Simple, efficient and effective algorithms
    - Finding tracks in complex geometries or large overlapping calorimeter objects
  - Capacity of processing nodes (IO, storage, board complexity, size)
    - limits imposed by technology
  - Architecture: regional or global, handling of overlaps and data sharing
  - Internal structure & hierarchy
    - typically several types of processing in parallel, with different latencies
    - global decision on best, possibly overlapping objects required
- In short: a complex problem with many variables
  - unlikely that experiments will find identical solutions
  - decisions on practical implementation subject to law of unintended consequence

Calorimeter Algorithms

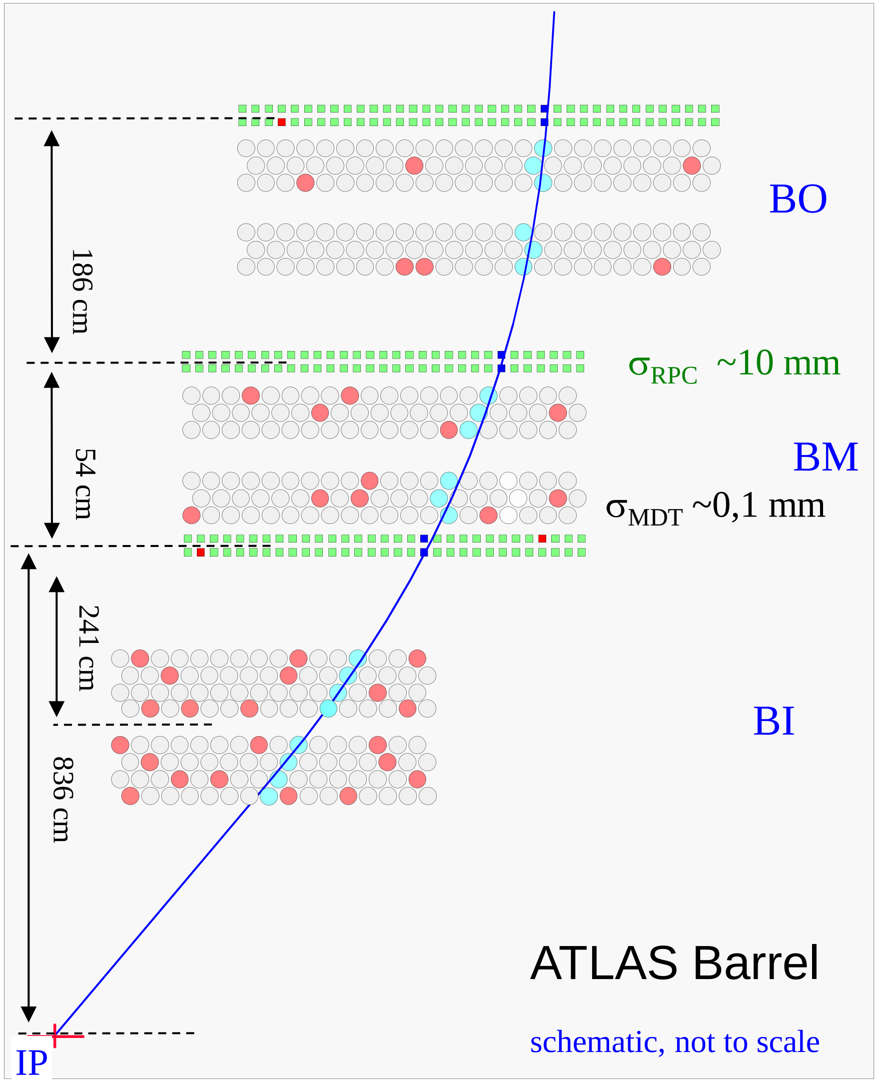


- Electron/photon
  - Large deposition of energy in small region, well separated from neighbour
  - pileup worsens the separation for lower p_T objects

- jets
  - hadrons – large, likely overlapping objects
  - τ - isolated irregular, narrow energy deposits
  - simulations identify likely patterns to accept or veto

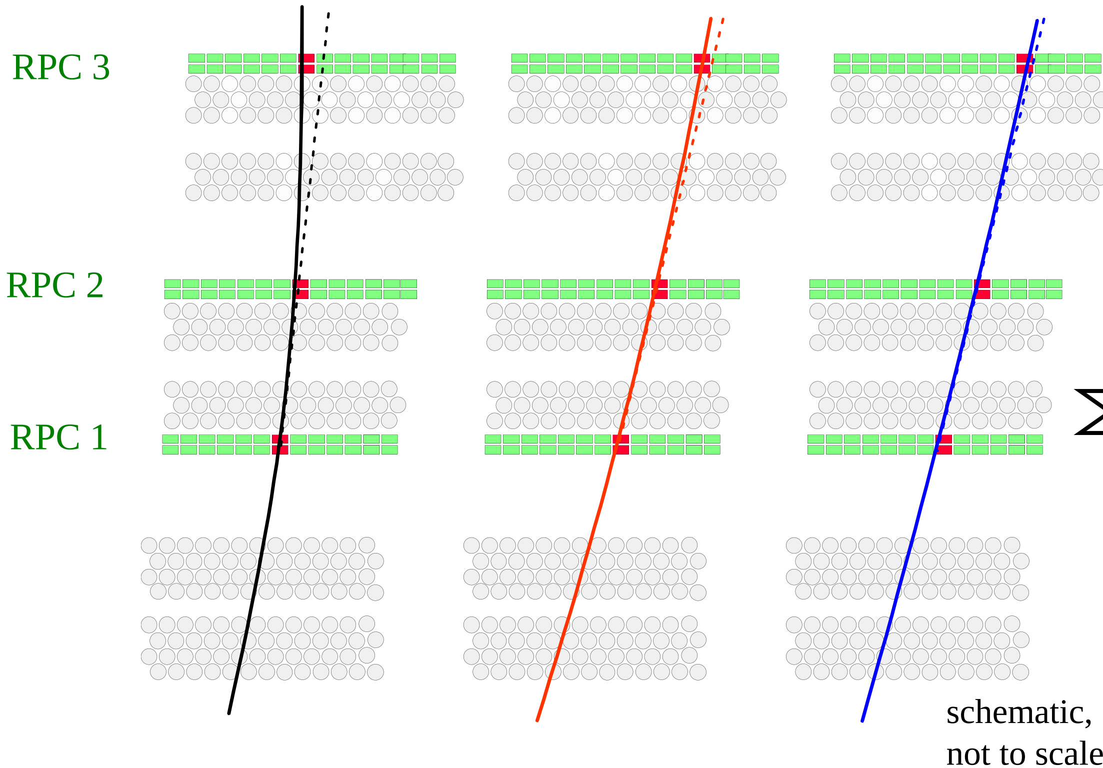


Muon triggers

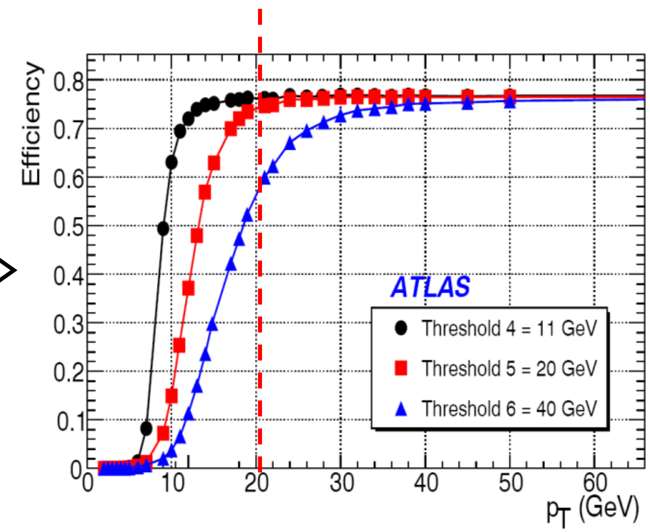


- Find penetrating tracks originating from collision region
  - Strongly dependent on geometry and detector response
  - typically combine fast response (RPC) with higher spatial resolution (DT)
  - challenges increase with occupancy and event pileup

The problem of RPC granularity and single muon L1 rate



← RPC strip width ~30mm



	p_T = 10 GeV	p_T = 20 GeV	p_T = 40 GeV
$\sigma_\mu > p_T$:	734 nb	47 nb	3 nb
actual trig. rate	110 kHz	24 kHz	11 kHz

High-p_T muons are a clear signature for interesting physics !

<u>However:</u> the present L1-trigger system has insufficient spatial resolution to tag muons above 10 GeV

1, 2, 3… levels?

- Not feasible to achieve sufficient data reduction in single step
  - mostly still the case today
  - 100 kHz was GPD target, 1 MHz for LHCb
    - but now feasible to increase the L0/L1 rate from technology progress
- When decisions were made on L2, two points of view
  - (custom) hardware processors needed to reduce data volume in ~50ms
  - sufficient computing power would evolve to avoid intermediate level
    - this proved to be correct, partly because of long LHC construction time
- ATLAS and CMS therefore diverged, with future implications
  - CMS must always store data on-detector until L1 decision
    - hardware trigger latency limited by shortest buffer length
    - transfer large data volume quickly to HLT = large BW
  - ATLAS can transfer selected data to L2 buffers
    - potentially much longer trigger latency possible
    - much smaller fraction of data, but more complexity

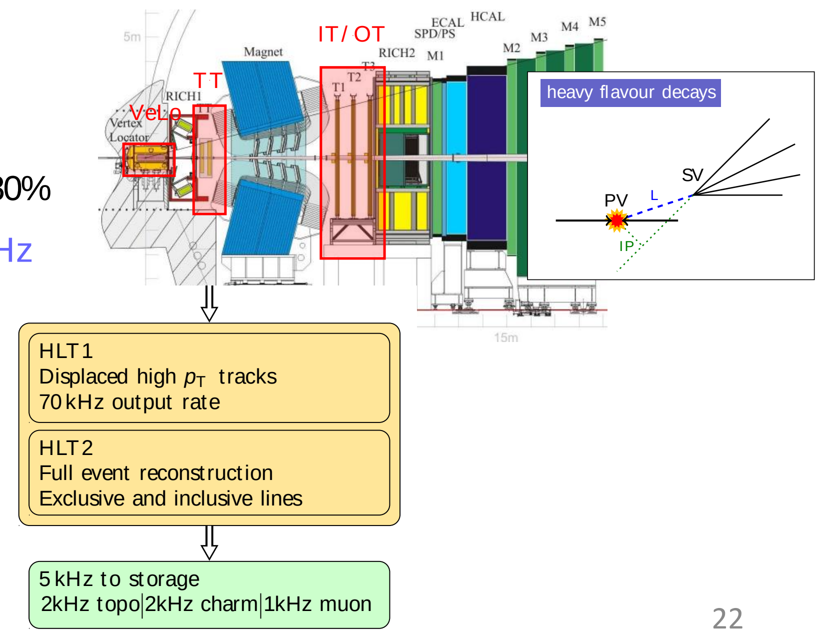
Special case of LHCb

- LHCb can read out entire detector faster than GPDs
  - the detector is much smaller (e.g. tracking ~0.5M chan)
  - then process events in HLT for storage at 5 kHz, event size ~0.1 MB
- 1 MHz is sufficient to allow HLT time to make selection
  - to avoid excessive HLT processing time include pileup veto
    - allows to increase <N_{coll}/BX>, and increase L, thus statistics

Status of the LHCb trigger

HLT1: Add tracking information

- Select high E_T hadrons, $e^{\pm}$, γ, threshold $E_T > 2.5 - 3.5$ GeV
- Efficiency hadronic B-decays ⇠ 50%, radiative B-decays ⇠ 80%
- L0 hadron rate ⇠ 450 kHz, L0 $e^{\pm}/\gamma$ rate ⇠ 150 kHz
- Momentum resolution $\Delta p/p$ ⇠ 20%
- Single muon $p_T > 1.5$ GeV, dimuon $p_{T,1} p_{T,2} > (1.3\,\text{GeV})^2$
- Efficiency typically ⇠ 90% for dimuon channels
- L0 muon rate ⇠ 400 kHz



C. Langenbruch (CERN), EPS 2013 | The LHCb trigger system

Overview of the LHCb L0 trigger

- <u>**Composed of four custom processors:**</u>
  - L0 Calorimeter trigger
  - L0 Muon trigger
  - L0 Pile-Up system

  And

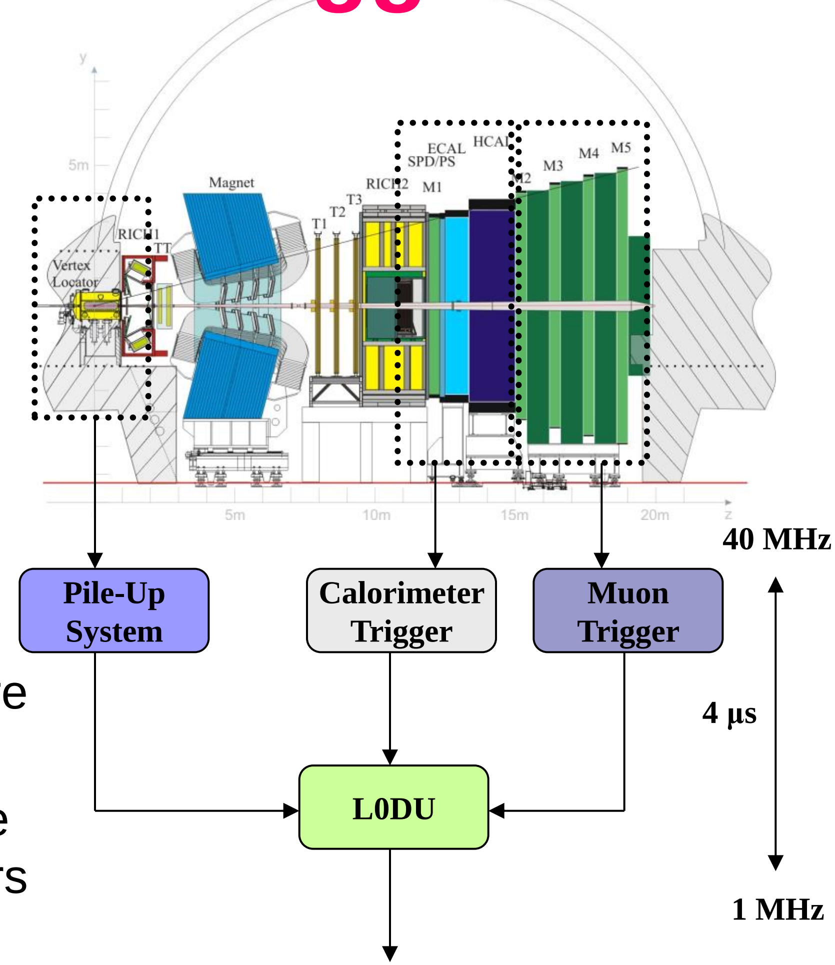
  The Level 0 Decision Unit (L0DU)

- Reduce the data flow down to 1 MHz for the next trigger level

- System fully synchronous, pipeline architecture
  => each event is processed

  => a decision is produced every 25 ns and the system is able to generate consecutive triggers

- **A physics algorithm is applied to select events** and to deliver the L0DU decision



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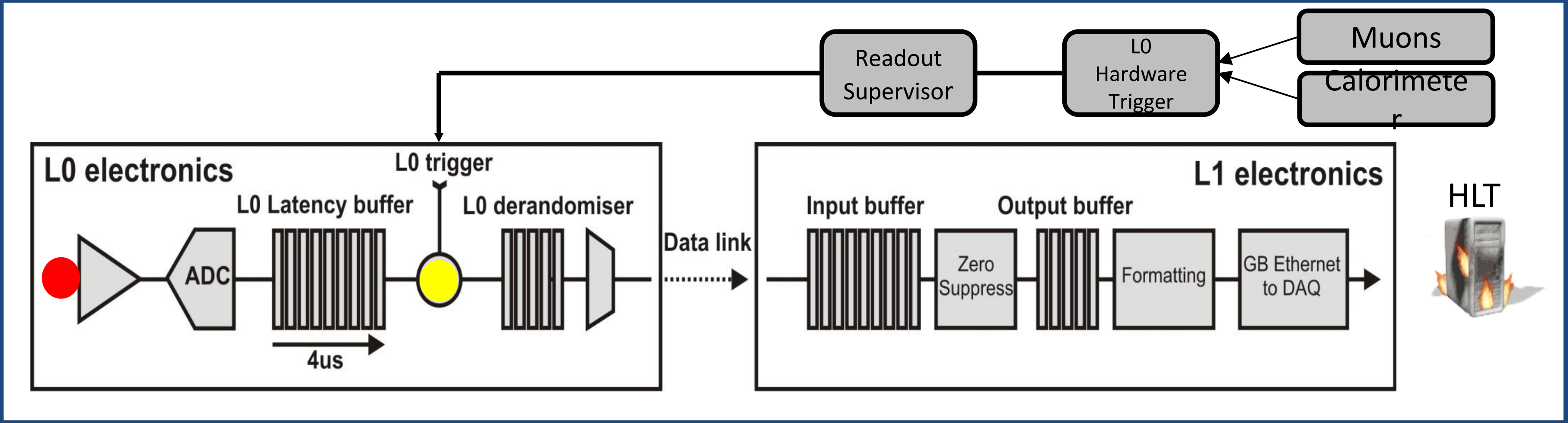
Existing readout system

Bunch crossing rate	40 MHz *
L0 trigger rate	1 MHz average
L0 trigger latency	4 μs fixed (160 BXs)
Event readout time	900 ns
Event rate to DAQ	1 MHz



Summary

- Many ways to solve the same problem
  - choices to be made are not simple
  - have implications for data handling and processing
  - and impact on future plans, as we shall see

Part 2

The Future

Trigger upgrades

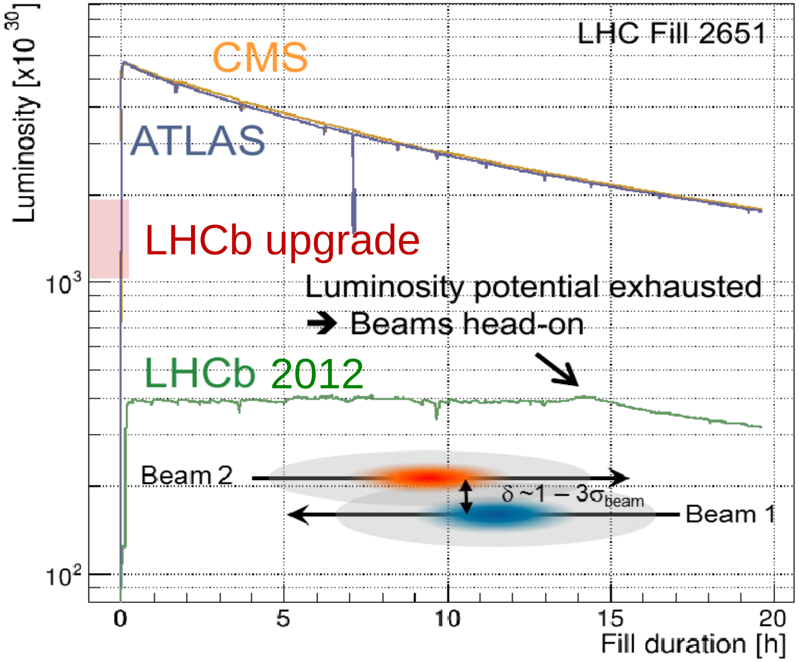
- All the experiments wish to profit from the increased HL-LHC luminosity to carry out high statistics studies
  - there will be significant changes to the detectors
  - technology has evolved considerably since experiments were built
  - but conditions will be more challenging

- Start with the simplest case: LHCb
  - presently single level (L0) hardware trigger
  - but small data volume per event and relatively simple geometry
  - increase data taking rate by a factor ~5
- Proposed solution
  - dispense with hardware trigger
  - pass all detector data to fast processors for event selection

Can this be done by other experiments too?

How to increase LHCb statistics significantly

2012 running conditions



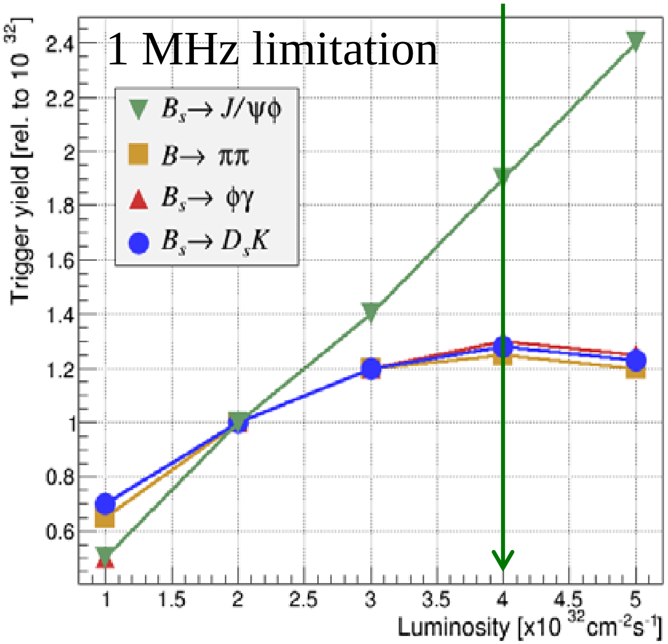
← $1\text{-}2\cdot10^{33}$ $cm^{-2}s^{-1}$

← ~ $4\cdot10^{32}$ $cm^{-2}s^{-1}$

up to LS2 (2018)

- levelled luminosity of ~ $4\cdot10^{32}$ $cm^{-2}s^{-1}$
- pile-up ~ 1
- record ~ 3-5 kHz

LHCb 2012



LHCb upgrade

post LS2 (2020)

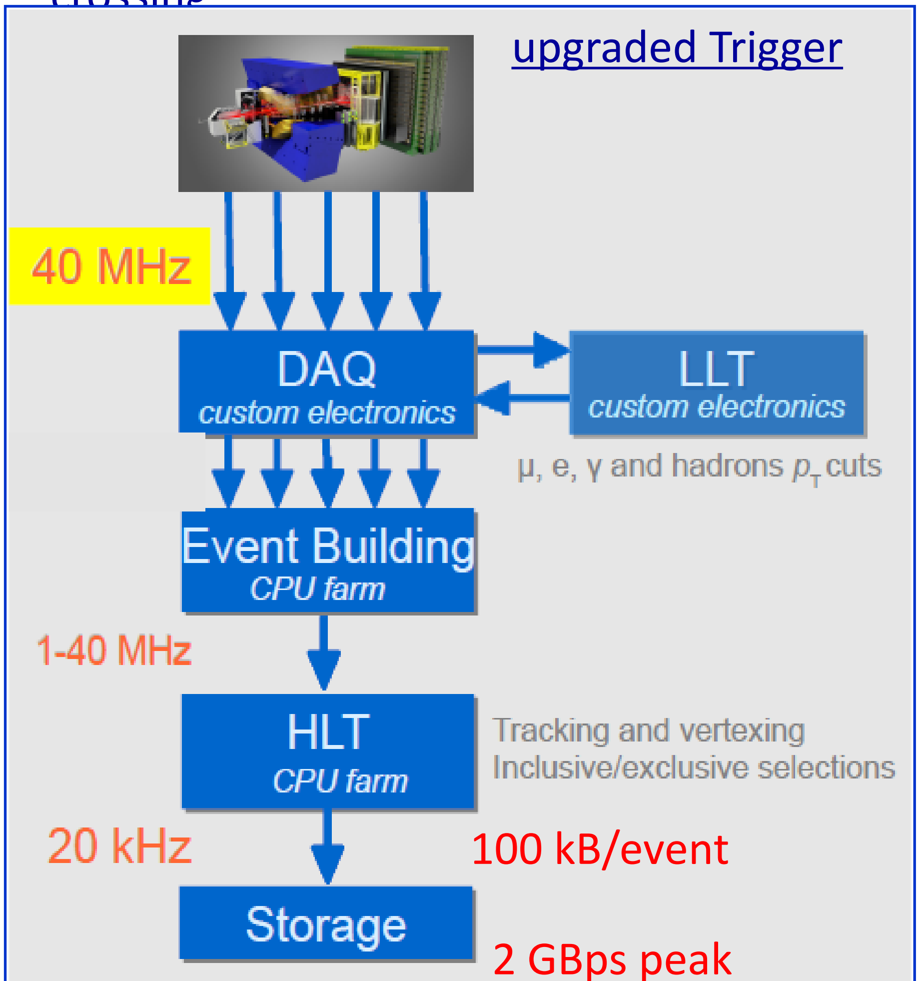
- levelled luminosity $1\text{-}2\cdot10^{33}$ $cm^{-2}s^{-1}$
- pile-up ~ 5
- record ~ 20 kHz

Trigger upgrade

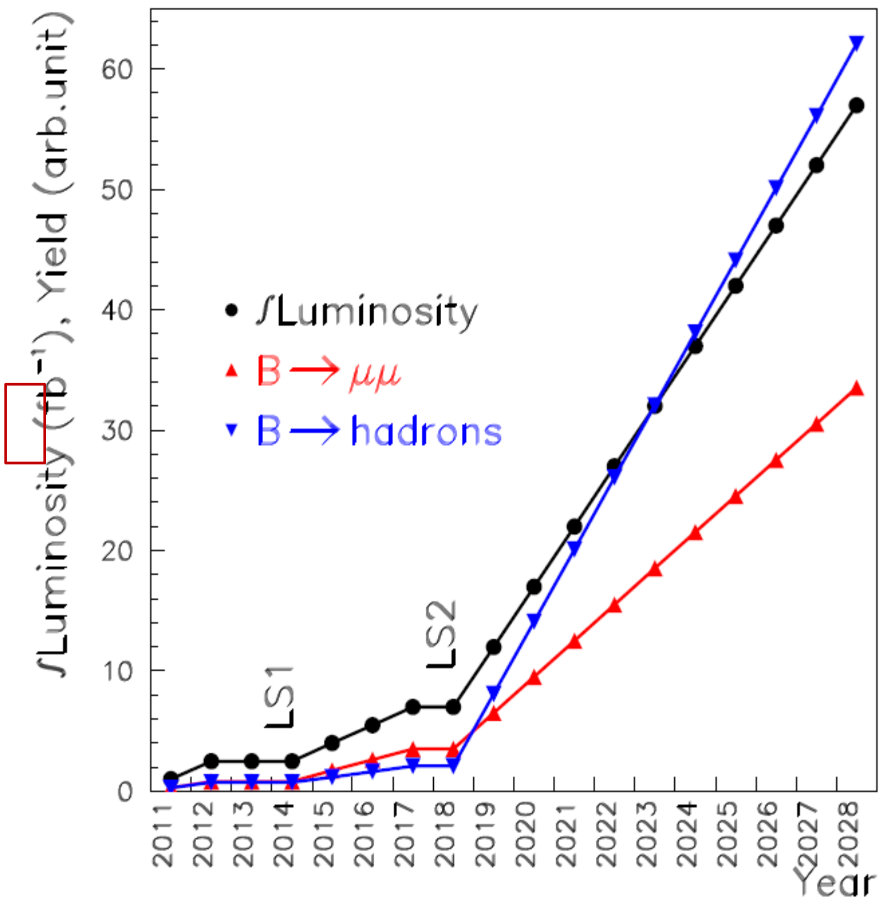
run an efficient and selective software trigger with access to the full detector information at every 25 ns bunch crossing

→

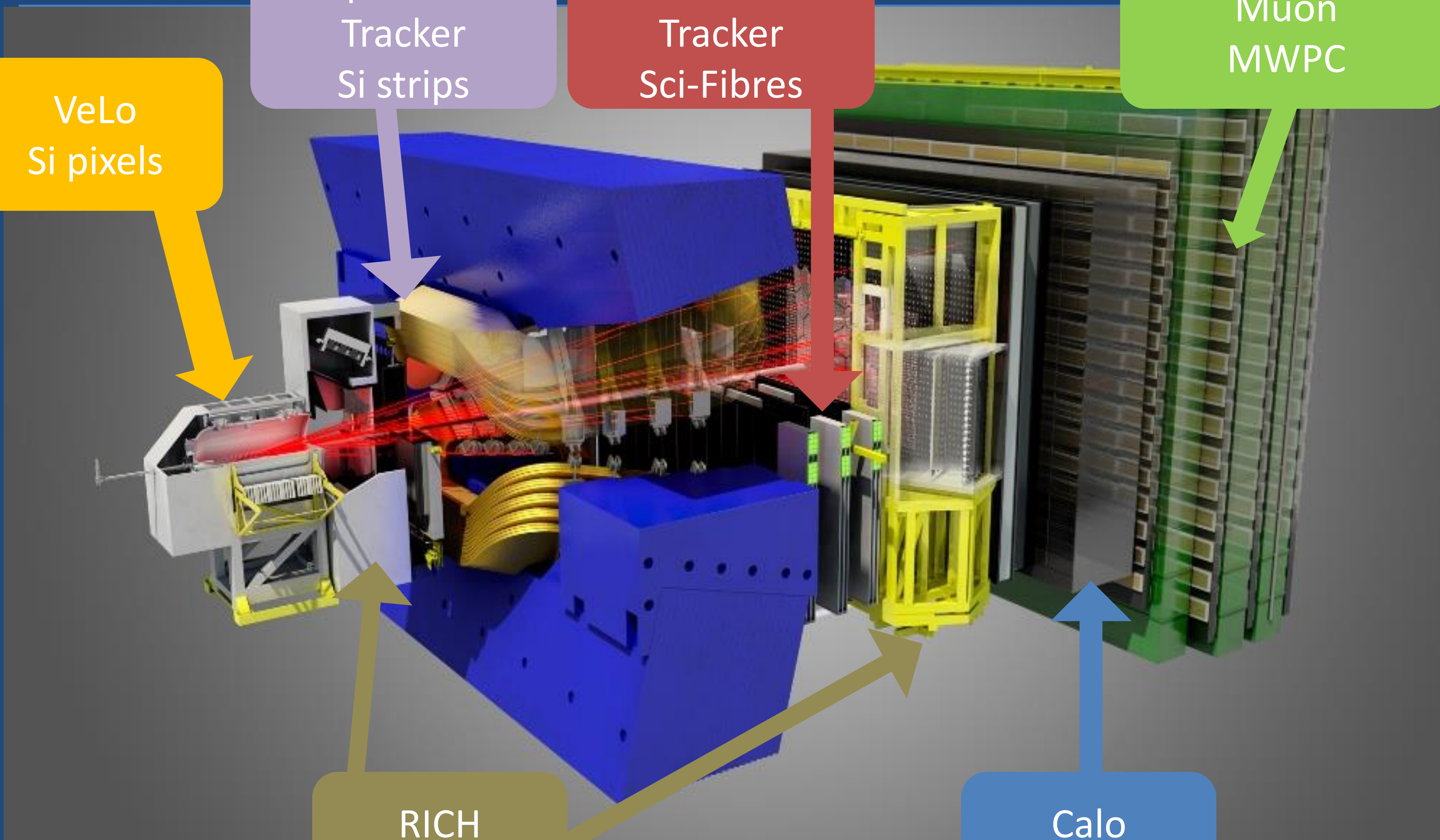
increase luminosity and signal yields



effect on luminosity and signal yields

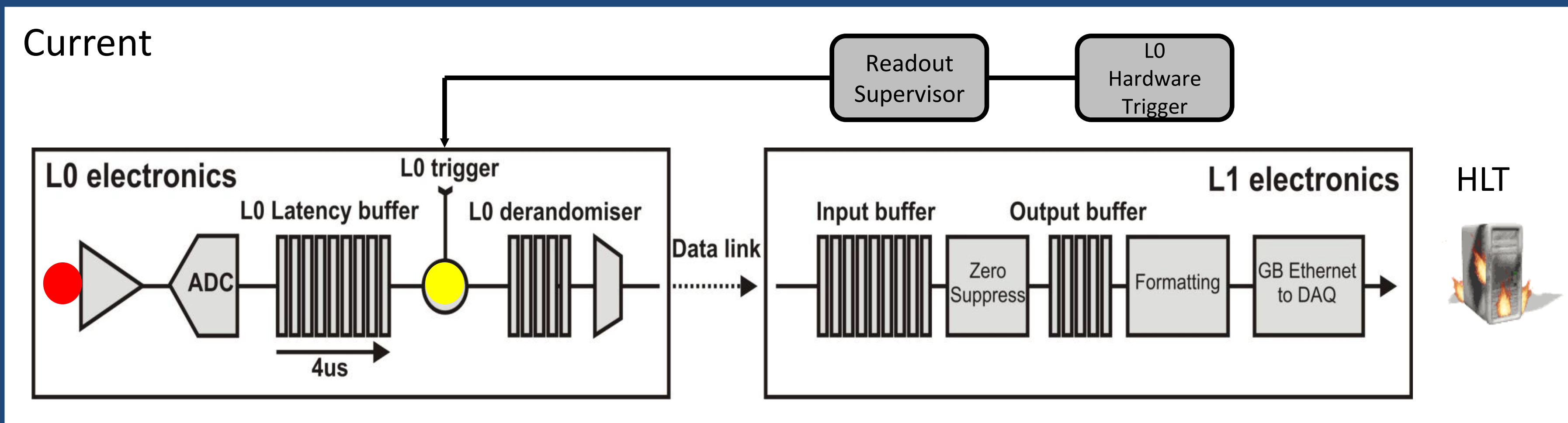


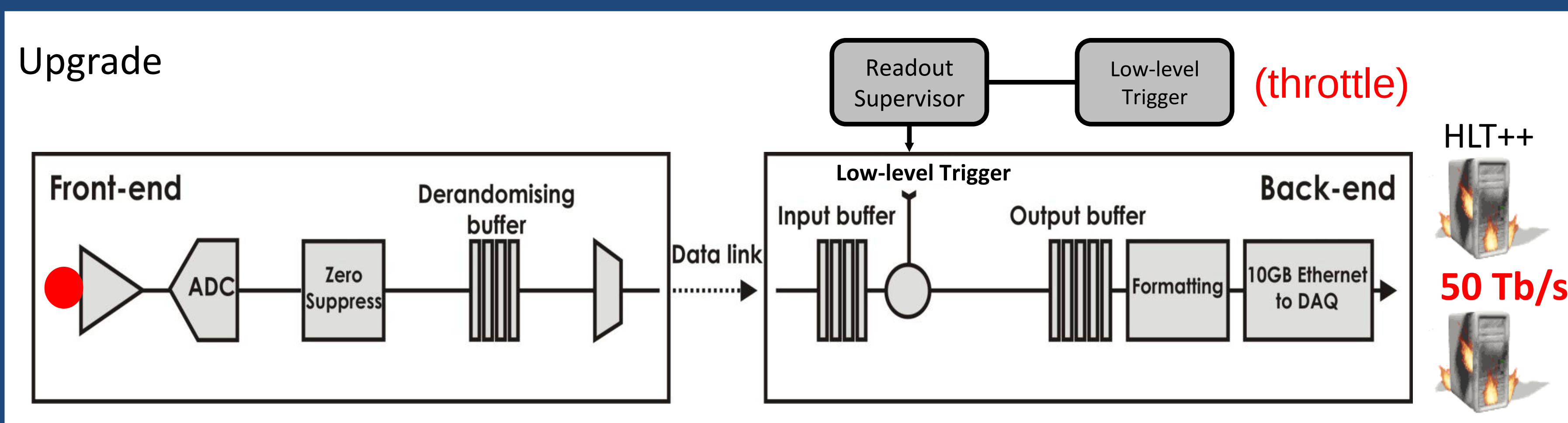
LHCb tomorrow



Upgrade architecture

No ‘front-end’ trigger, Event rate to DAQ nominally 40 MHz

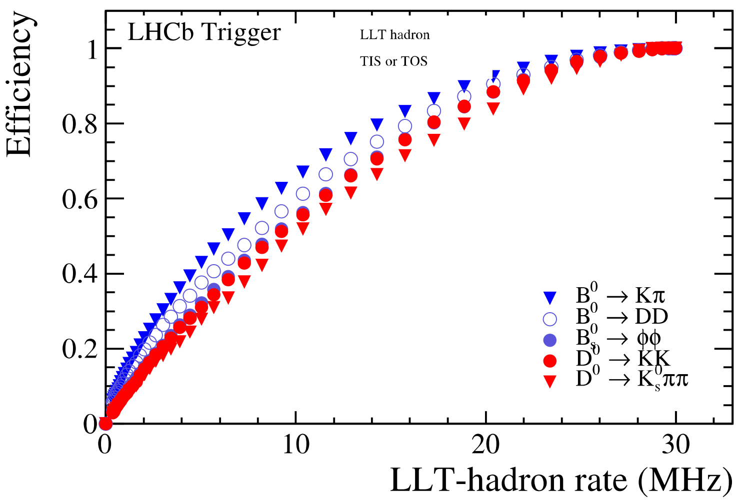


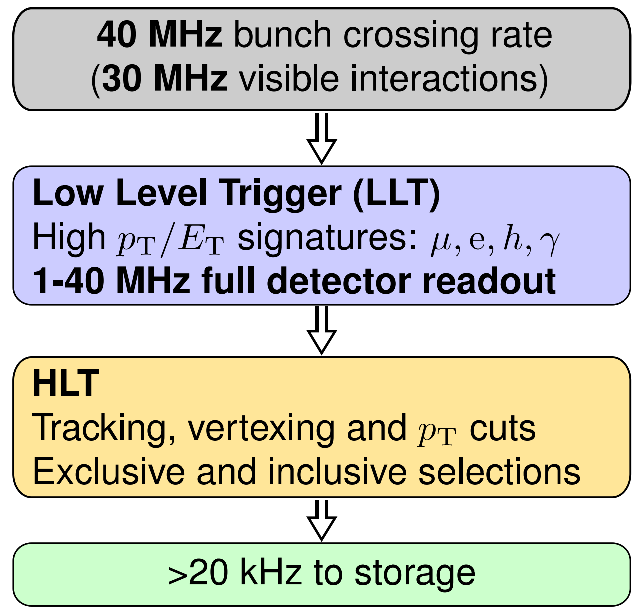


The Upgrade Trigger

TDR in preparation

- At $\mathcal{L} = 2 \times 10^{33}$ cm^{-2} s^{-1}, 1 MHz readout becomes a bottleneck:
  - Saturation problem: at increased lumi signal less well separated in L0.





- Readout upgraded to 40 MHz: Full readout of 30 MHz Visible pp interactions
  - L0-hardware trigger removed, software Low-Level Trigger (LLT) as replacement
  - Acts as 'handbrake' during commissioning, $1 - 40$ MHz scaleable output rate

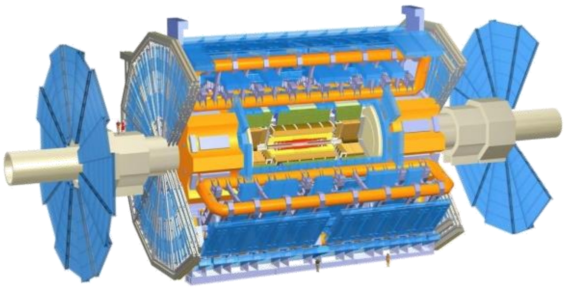
offline quality tracking at 30 MHz is possible in software

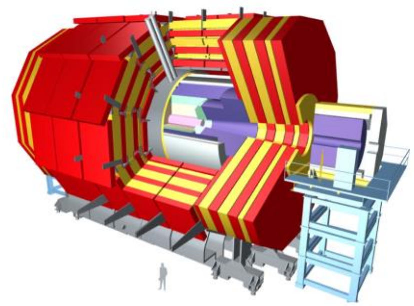
ATLAS & CMS

GPDs: scope of detector upgrades

- Most sub-detectors are foreseen to survive to 3000 fb^{-1}
  - with on-going maintenance and refurbishment where possible
- Trackers must be completely replaced
  - radiation damage limits their lifetimes to <500 fb^{-1}
- New tracker readout systems are therefore essential
  - based on more modern technologies, which improve performance
    - though to meet even greater challenges – radiation, occupancy, precision
  - all sub-system readout systems must remain compatible
    - some constraints on tracker changes, and modifications to others
- Triggers must also be substantially upgraded
  - designed for 10^{34} $cm^{-2}s^{-1}$, $\langle N_{ev} \rangle \sim 25$
  - with safety factors – but exploited to maximise acceptance

ATLAS & CMS @ Run 4 (2025)





	ATLAS		CMS
Level 1	Level 1	0.5 – 1 MHz	Level 1
HLT	HLT		HLT
Rate to storage	5-10 kHz, 2MB/event		10 kHz, 4MB/event
Storage	Storage		Storage
Peak output	10-20 GB/s	← PEAK OUTPUT →	40 GB/s

Hardware triggers retained
- but with much higher rate

Why?

Preserve low trigger thresholds

BW is still insufficient to transmit all data off detector at 40 MHz

Why?

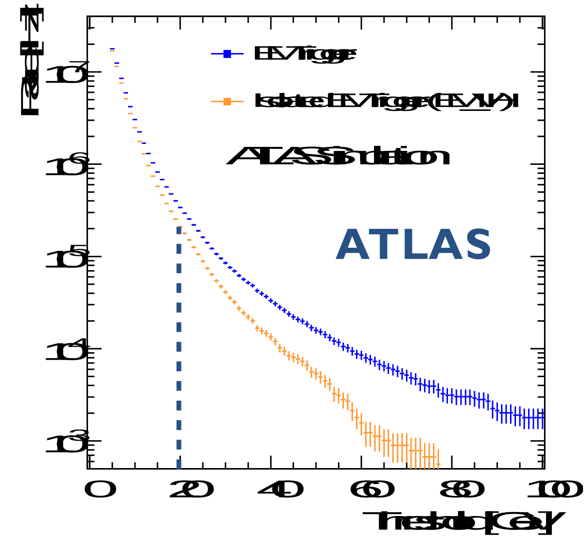
New issues for trigger

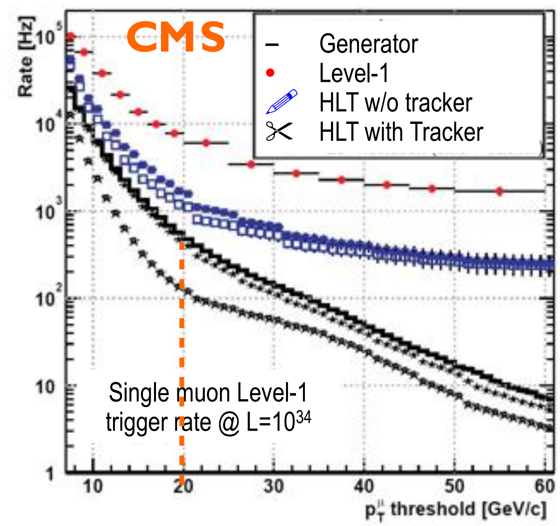
- $L \sim 5 \times 10^{34}$ $cm^{-2}s^{-1}$ (levelled) => N_{ev}/BX ~ 140 - 200
- Calorimeters
  - isolation of e/γ/τ degraded by pile-up from π^0 γs and hadrons
  - many more jets, which overlap
- Muon systems
  - increased combinatorial fakes, enhanced by MS (CMS)
- Outcome: much higher rate of L1 triggers
  - usual response is to increase thresholds, which risks physics
  - even worse - raising thresholds does not look effective
- Options to mitigate
  - increase L1 accept rate – and improve performance of HLTs
  - seek new input data to help the trigger decision
    - but only modest improvements expected from gains in μ & Calo systems

New Trigger Schemes Required

- Choice of trigger has direct impact on tracker design
- Tracker input to Level-1 trigger
  - μ, e and jet rates would exceed 100 kHz at high luminosity
  - Increasing thresholds would affect physics performance
    - Muons: increased background rates from accidental coincidences
    - Electrons/photons: reduced QCD rejection at fixed efficiency from isolation

- Add tracking information at Level-1
  - Move part of High Level Trigger reconstruction into Level-1
  - Challenge: squeeze data processing into a few micro seconds





Improvements To Current Triggers

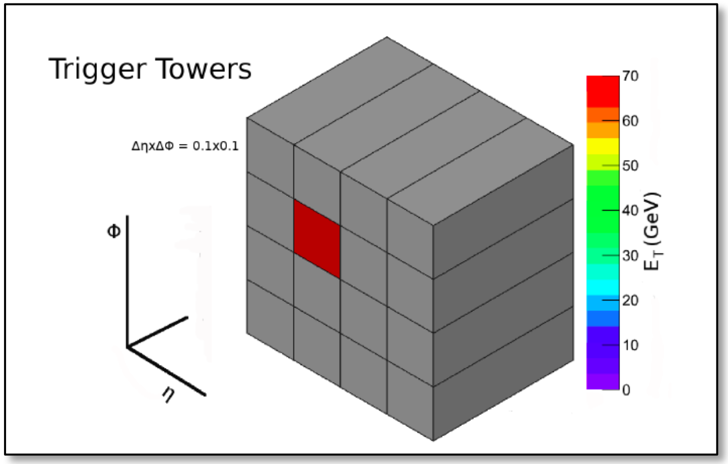
extract further information, where possible, from μ & Calo trigger data

Examples

ATLAS Level-1 calorimeter trigger

Run-1 calorimeter trigger input:
Trigger Towers $\Delta\eta \times \Delta\phi = 0.1 \times 0.1$

- Used to calculate core energy, isolation



Run-1 trigger menu
at L_{inst}=3 x 10^{34} $cm^{-2}s^{-1}$

⇩

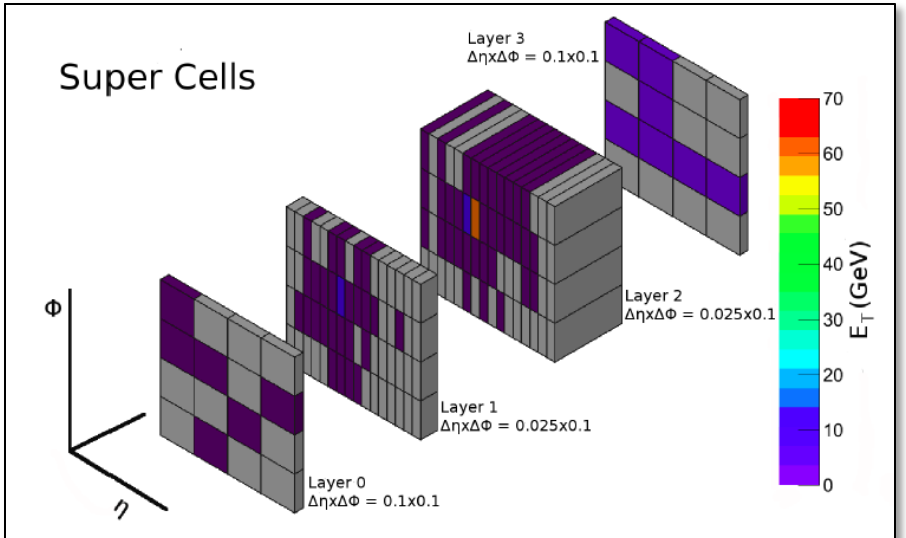
Total rate for EM triggers would be 270 kHz!
(Total L1 bandwidth is 100kHz)

⇨

maintain lower thresholds at an acceptable rate

↑

Provide better granularity and better energy resolution

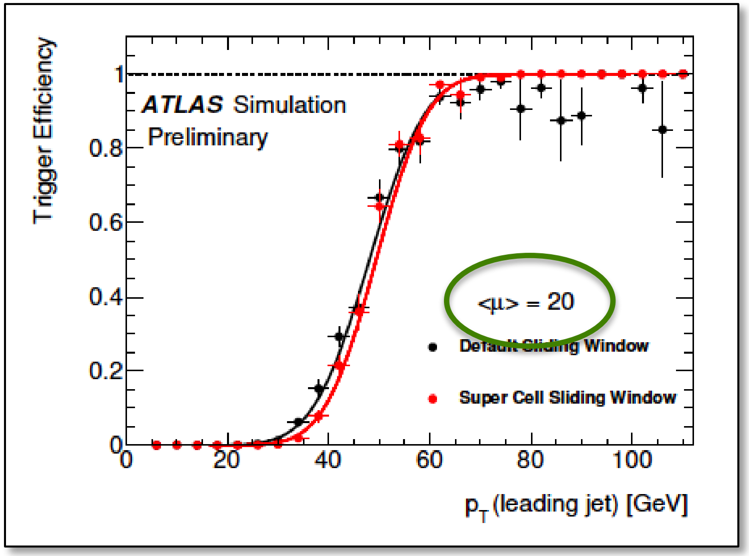


(b)

Complemented by new L1Calo trigger processors eFEX and jFEX

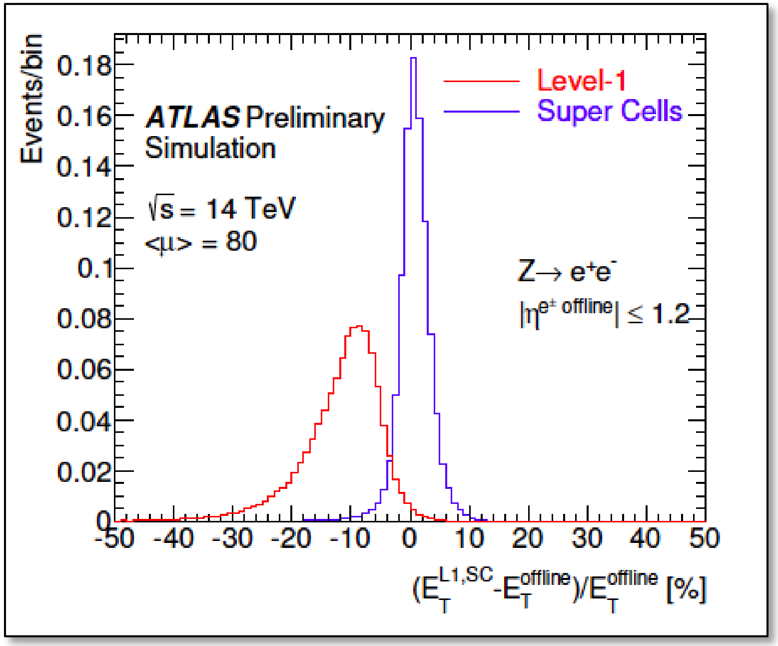
ATLAS Level-1 calorimeter trigger

Trigger eff. vs jet p_T



Significant degradation of the turn-on curve with pile up (<μ>=80)

- requiring much higher offline threshold (black curve)
- recovered through introduction of super-cells (red curve)



EM Triggers

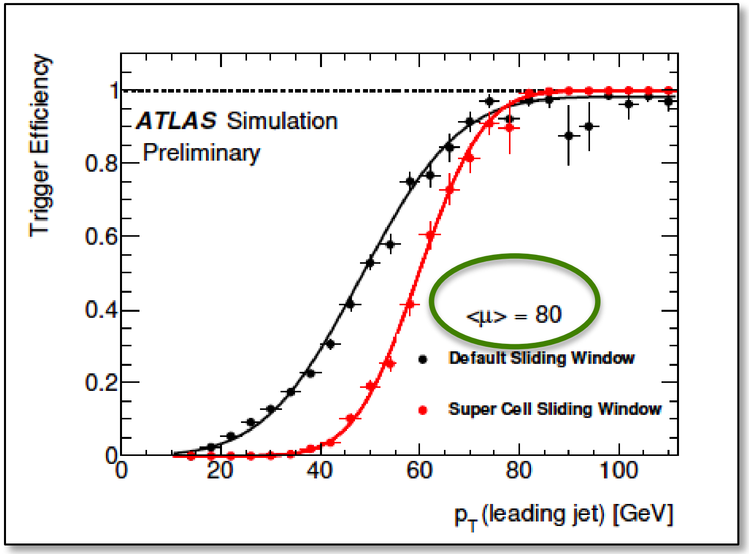
- Better shower shape discrimination
  → lower EM threshold by ~ 7 GeV at same rate
- In addition significantly improved resolution
  → lower EM threshold by another few GeV at same rate

Topological triggering

- Will feed calorimeter trigger input to L1 topological processor (already in Phase-0)

ATLAS Level-1 calorimeter trigger

Trigger eff. vs jet p_T



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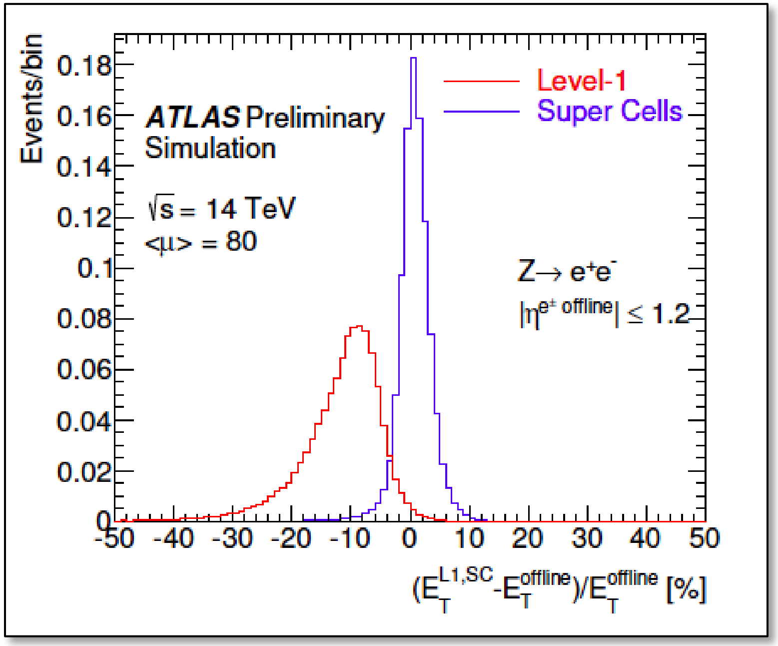

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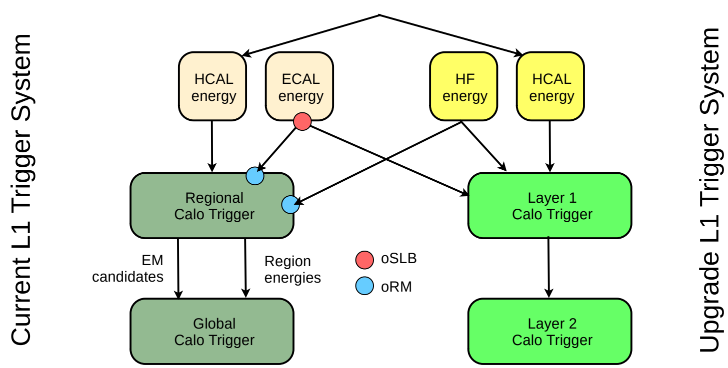
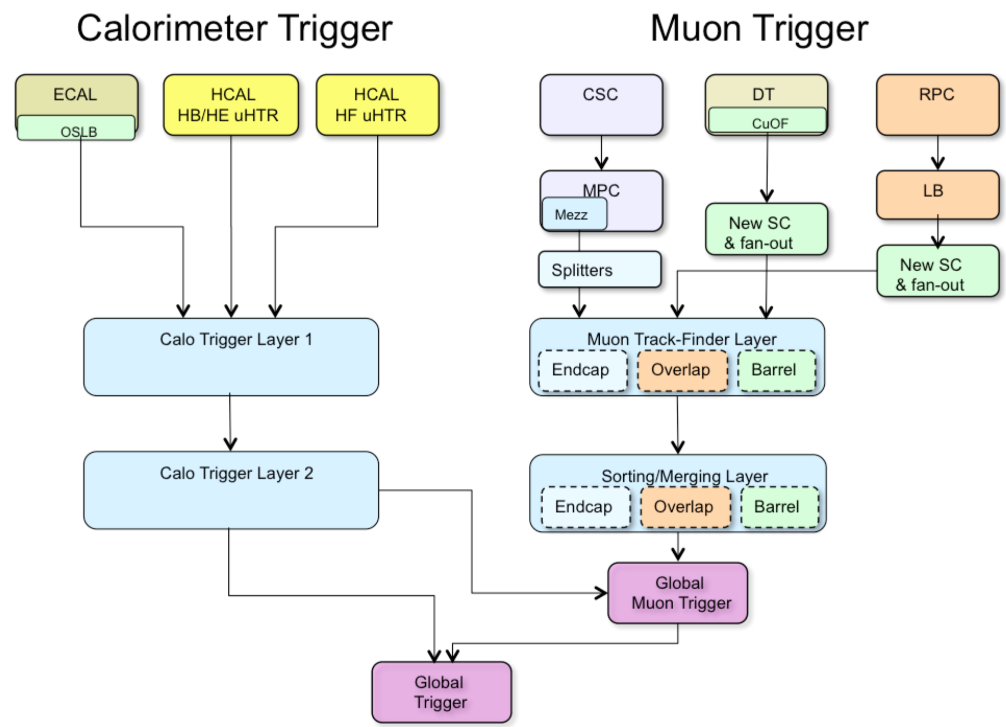
CMS Phase 1 Upgrade of L1 Trigger

- Hardware based on powerful FPGAs and high bandwidth optics
  - Calorimeter, Muon and Global triggers built with few board types, all using Virtex 7 FPGA
  - Improved algorithms for PU mitigation and isolation
  - Trigger inputs split during LS1 to commission new trigger in parallel to operating system



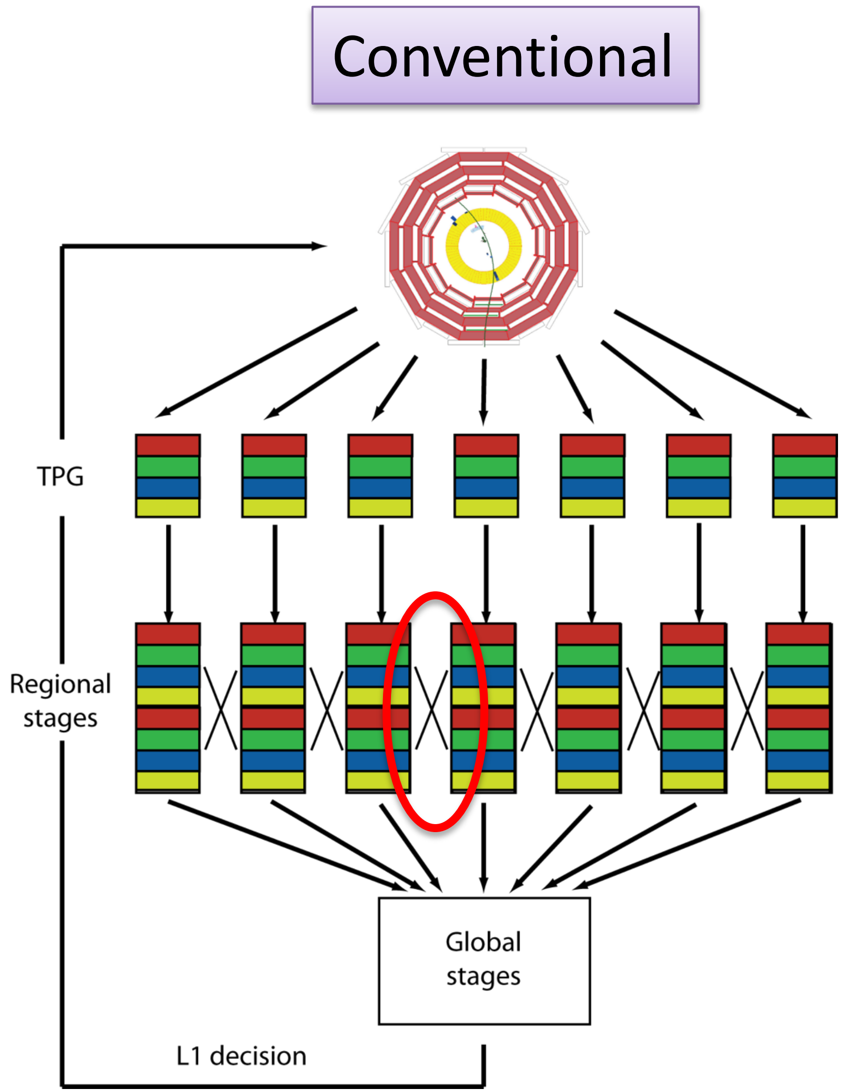
Optical splitting for parallel commissioning, calorimeter trigger

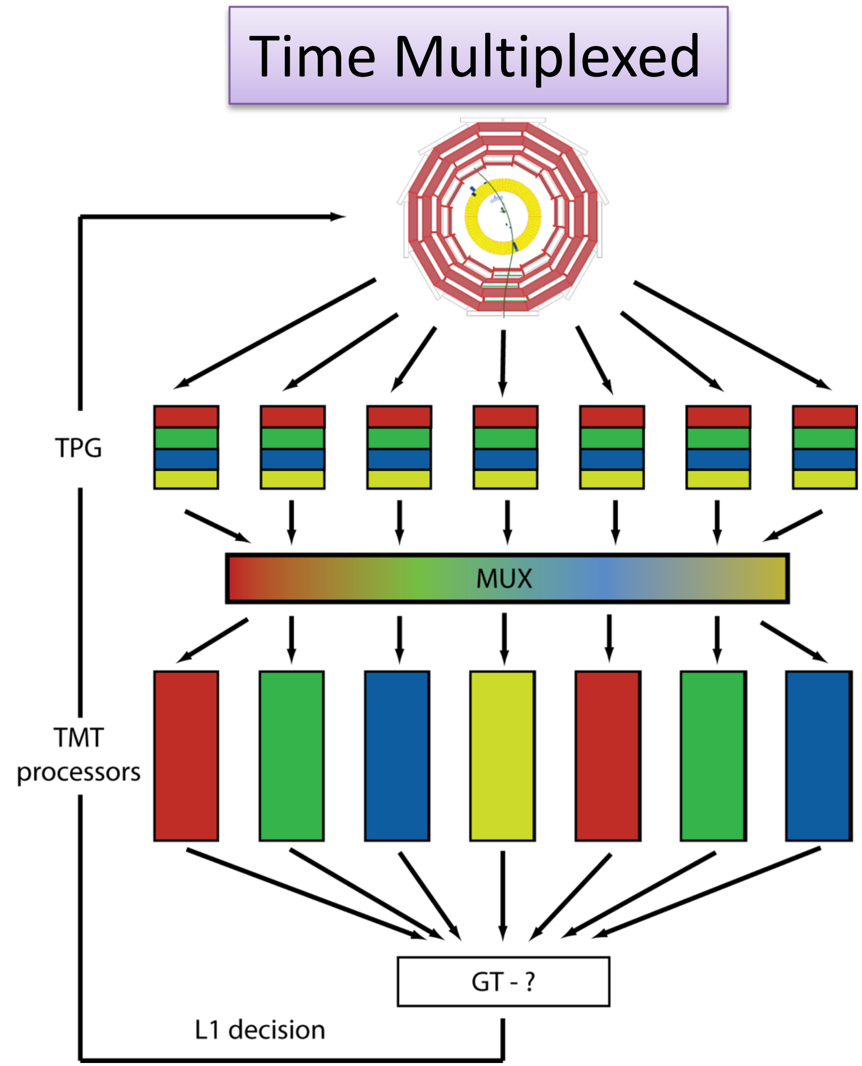


Level 1 Trigger Upgrade

transmit greater granularity calorimeter information = more bits

New Trigger Architecture





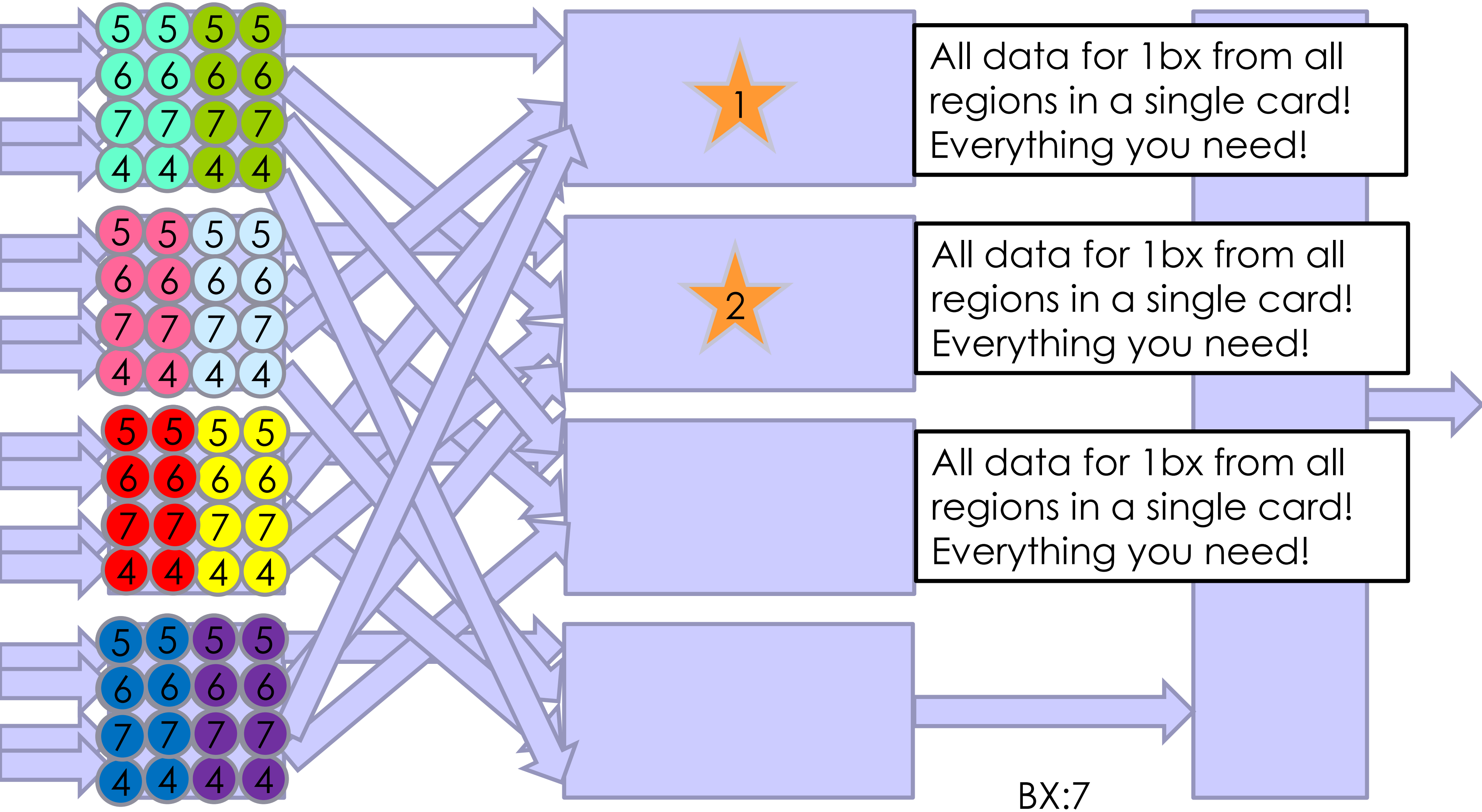
What Is A Time Multiplexed Trigger?

- Multiple sources send to single destination for complete event processing
  - as used, eg, in CMS High Level Trigger

- Requires two layers with passive switching network between them
  - can be "simple" optical fibre network
  - could involve data processing at both layers
  - could also be data organisation and formatting at Layer 1, followed by data transmission to Layer 2, with event processing at Layer 2

  - illustration on next slide

Time-multiplexing

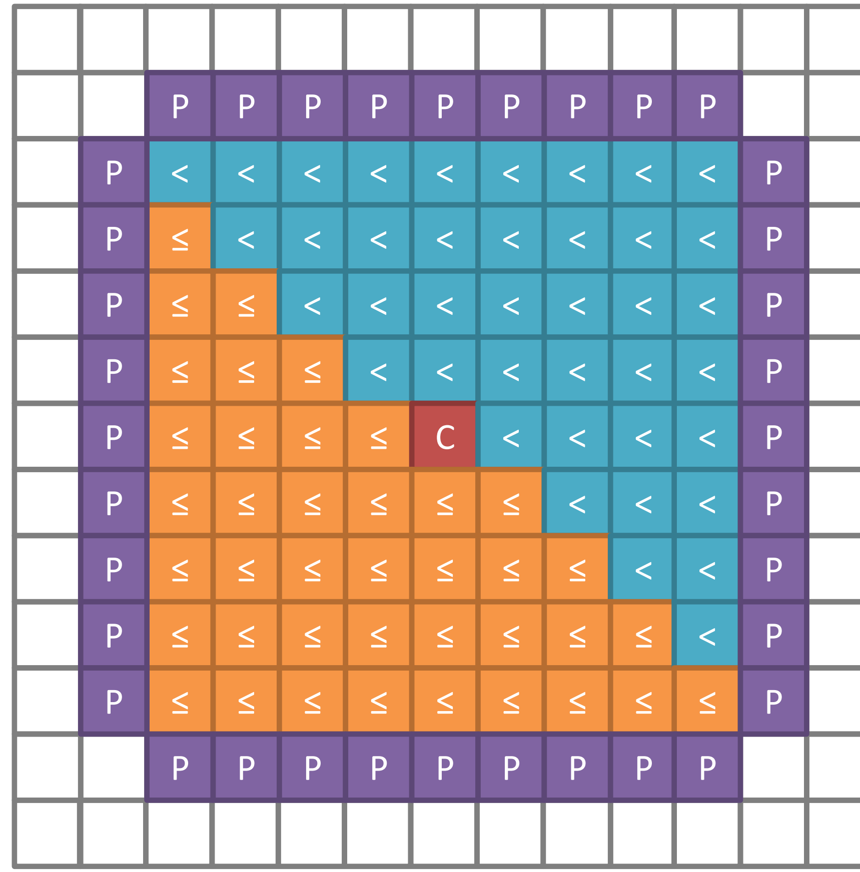


Advantages of TMT

- "All" the data arrive at a single place for processing
  - in ideal case avoids boundaries and sharing between processors
  - however, does not preclude sub-division of detector into regions
- Architecture is naturally matched to FPGA processing
  - parallel streams with pipelined steps at data link speed
- Single type of processor, possibly for both layers
  - L1= PP: Pre-Processor L2 = MP: Main Processor
- One or two nodes can validate an entire trigger
  - spare nodes can be used for redundancy, or algorithm development
- Many conventional algorithms explode in a large FPGA
  - timing constraints or routing congestion for 2D algorithms
- Synchronisation is required only in a single node
  - not across entire trigger

TMT jet algorithm

- Jets
  - 9 × 9 sum of trigger towers at every site
  - Fully asymmetric jet veto calculation
  - Local ("Donut") or Global pile-up estimation
  - Full overlap filtering
  - Pile-up subtraction
  - Pipelined sort of candidates in ϕ
  - Accumulating pipelined sort of candidates in η
- Ring sums
  - Scalar and Vector ("Missing") ET
  - Scalar and Vector ("Missing") HT



9 × 9 jet at tower-level resolution

50% LUT utilization <u>INCLUDING</u> links , buffers, control, DAQ, etc.
Runs at 240 MHz

HL-LHC CMS Trigger

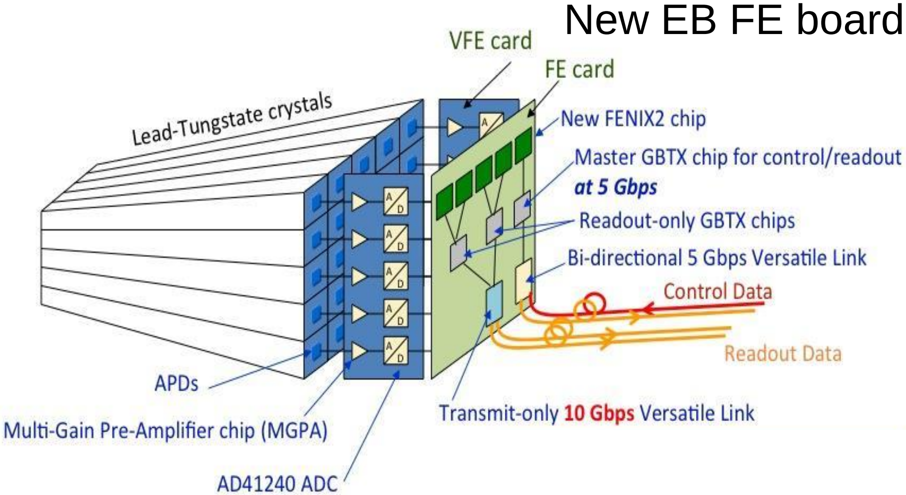
- L1-trigger to build on the Phase 1 architecture
  - outer tracker information available to all trigger objects
  - increased granularity (EB at crystal level)
  - operate up to 1 MHz

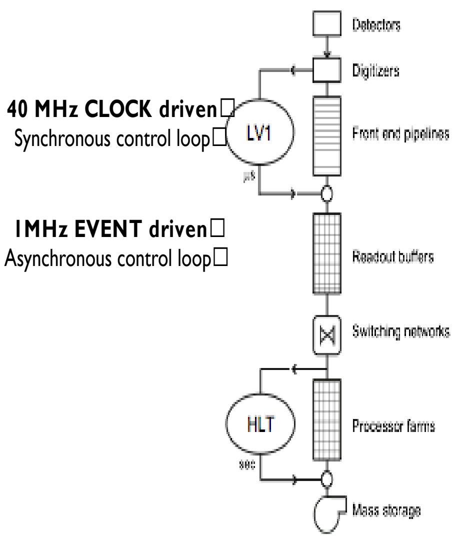
- Match leptons with tracks
- Improved isolation of e, γ, μ, τ
- Vertex association to reduce effect of pileup in multiple object triggers

- Replacement of ECAL Barrel FEE
  - Allow 10 μs latency at L1

- Upgrade HLT and DAQ to handle 1 MHz into HLT and 10 kHz out

New EB FE board





HLT to profit from "Moore's Law" for CPUs, networks, and storage

Track-based Triggers

How will the data be processed?

See also Stefano Mersi - Friday

Tracker challenges and constraints

- Trackers are sub-detectors with largest channel count
  - so data volume is VERY large
    - leave remaining technical challenges for other lecturers
- Issues
  - how can the data be transmitted from the tracker to L1 pre-processors?
  - once arrived, what can be done with it?
  - once reconstructed, how can it be applied to the trigger decision?
  - the solution should be compatible with existing trigger architecture
- Conclusions to date
  - reconstruction of tracks will be required
    - individual points or track segments are not sufficient
  - ATLAS: transmit limited data from RoI, guided by L0 trigger from Calo/μ
  - CMS: suppress low p_T hit data from detector to reduce data volume

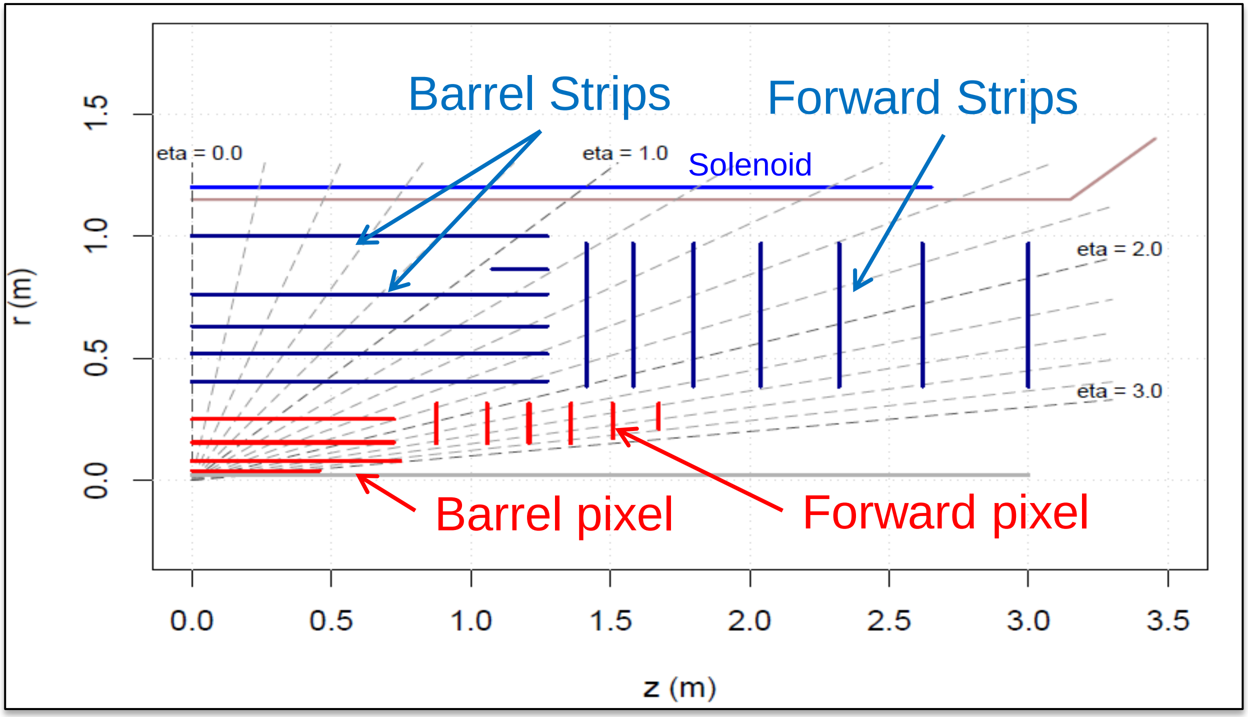
T Wengler
ECFA workshop

ATLAS New Tracker (LS3)

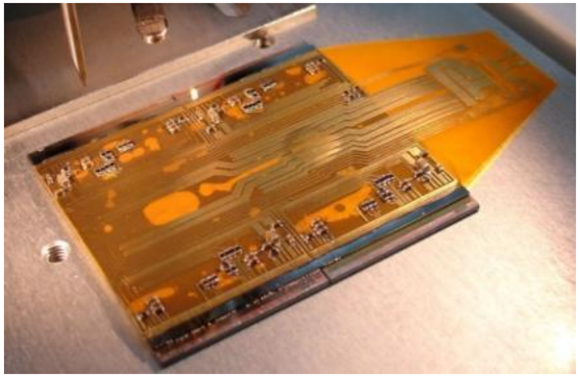
- Limiting factors at HL-LHC
  - Bandwidth saturation
  - High occupancies
  - Radiation damage

Microstrip Stave Prototype

New (all Si) ATLAS Inner Tracker for HL-LHC



Quad Pixel Module Prototype



New 130nm ASICs

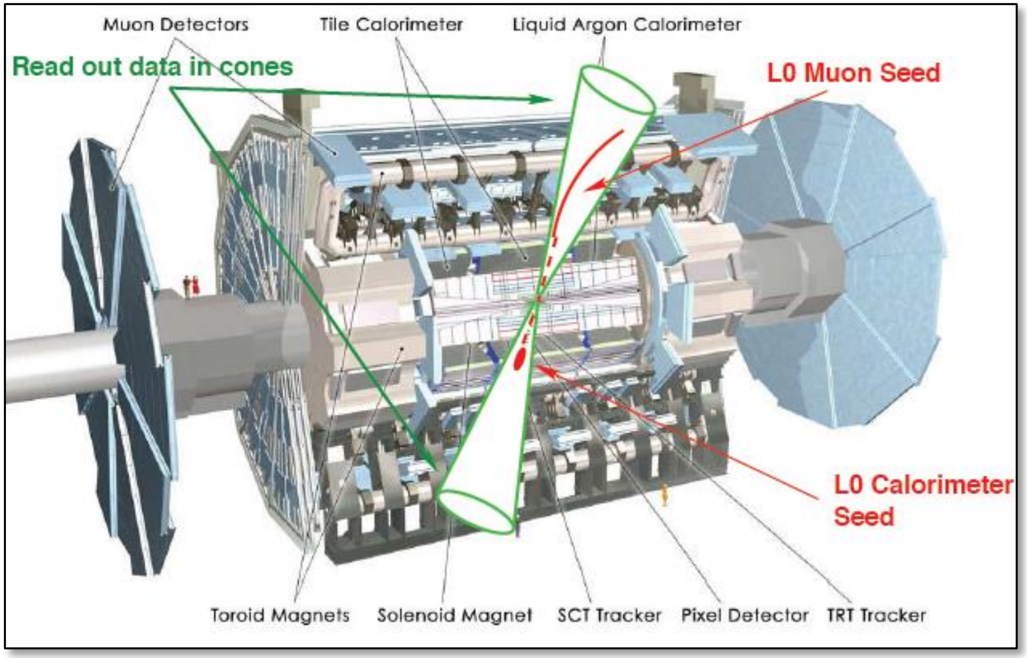
- incorporates L0/L1 logic

Sensors compatible with 256 channel ASIC

L1 Track Trigger

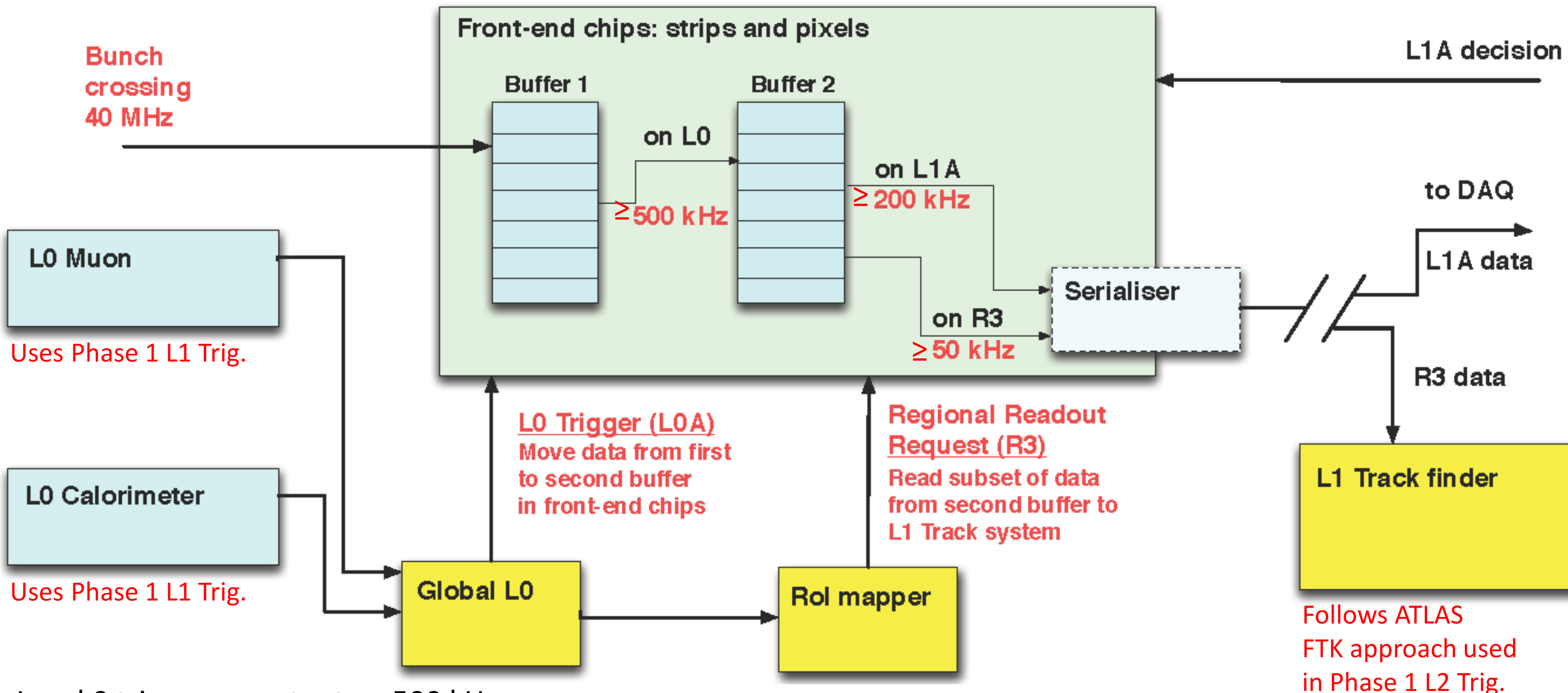
- Adding tracking information at Level-1 (L1)
  - Move part of High Level Trigger (HLT) reconstruction into L1
  - Goal: keep thresholds on p_T of triggering leptons and L1 trigger rates low

- Triggering sequence
  - L0 trigger (Calo/Muon) reduces rate within ~6 µs to ≳ 500 kHz and defines RoIs
  - L1 track trigger extracts tracking info inside RoIs from detector FEs



- Challenge
  - Finish processing within the latency constraints

ATLAS "Double buffer" readout



- Level 0 trigger accept rate ≥ 500 kHz
  - On an L0 accept, copy data from primary to secondary buffer
  - Identify "Regions" in detector (1-10% of the detector on each L0 accept) like L1 RoI
  - Generate "Regional Readout Request" (R3) - modules in "Region" read out subset of their data
- On an L1 accept (≥ 200 kHz), all modules read out event from Secondary buffer
- Since only ~10% of the detector (the "Regions") will be read out on the Level 0 accept, R3 request rate for any specific part of the detector will be ≥ 50 kHz

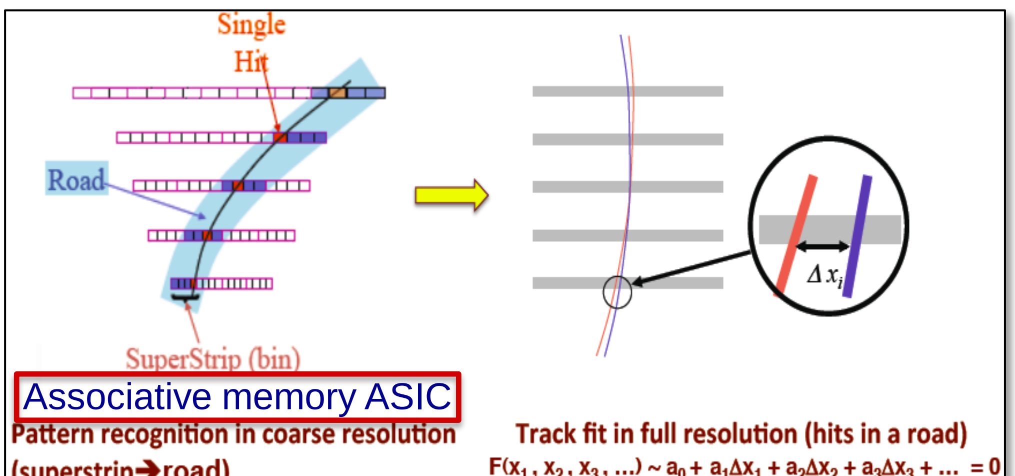
ATLAS Fast TracK Trigger (FTK)

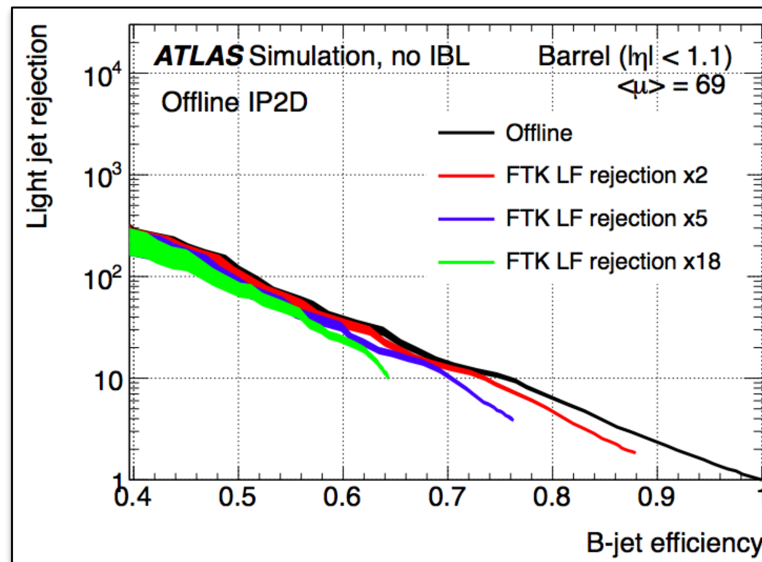
- Dedicated, hardware-based track finder
  - Runs after L1, on duplicated Si-detector read-out links
  - Provides tracking input for L2 for the full event
    - not feasible with software tracking at L2
  - Finds and fits tracks (~ 25 μs) in the ID silicon layers at an “offline precision”

- Processing performed in two steps

hit pattern matching to pre-stored patterns (coarse)

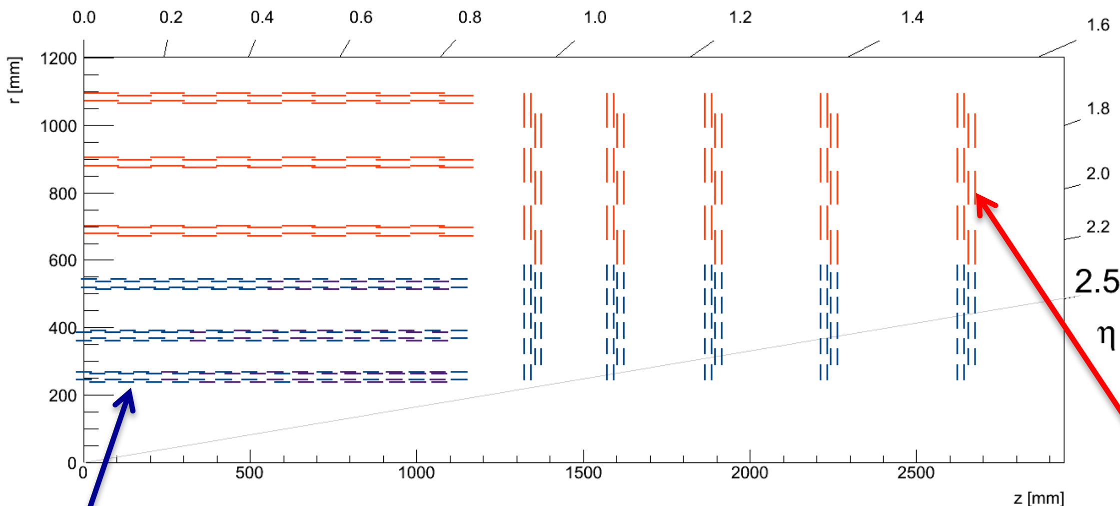
subsequent linear fitting in FPGAs (precise)

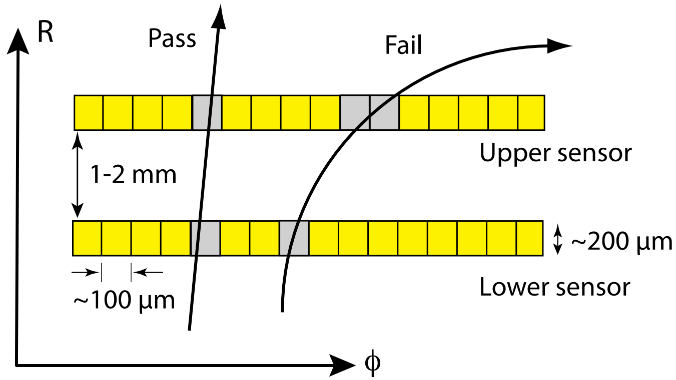




Light jet rejection using FTK compared to offline reconstruction
(further improved by addition of IBL)

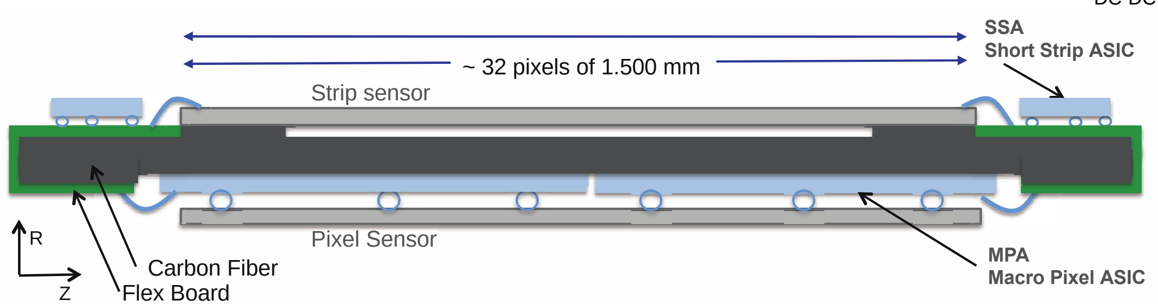
CMS Phase II Outer Tracker design

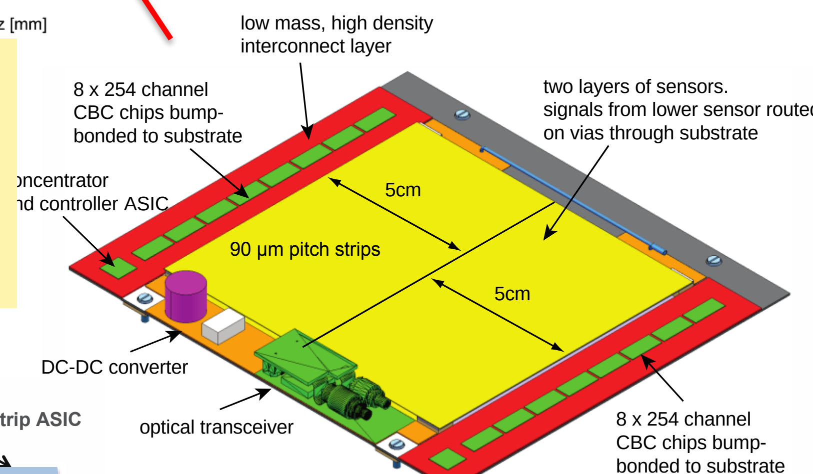




- ~15000 modules transmitting
  - p_T-stubs to L1 trigger @ 40 MHz
  - full hit data to HLT @ 0.5-1 MHz

~7100 PS-modules

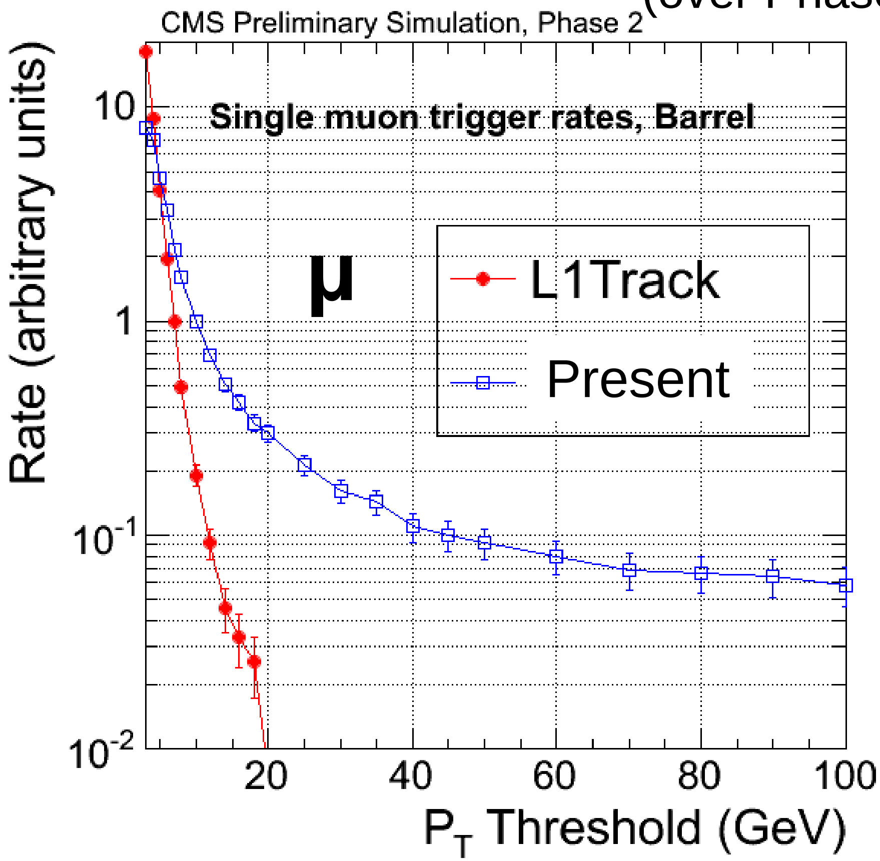


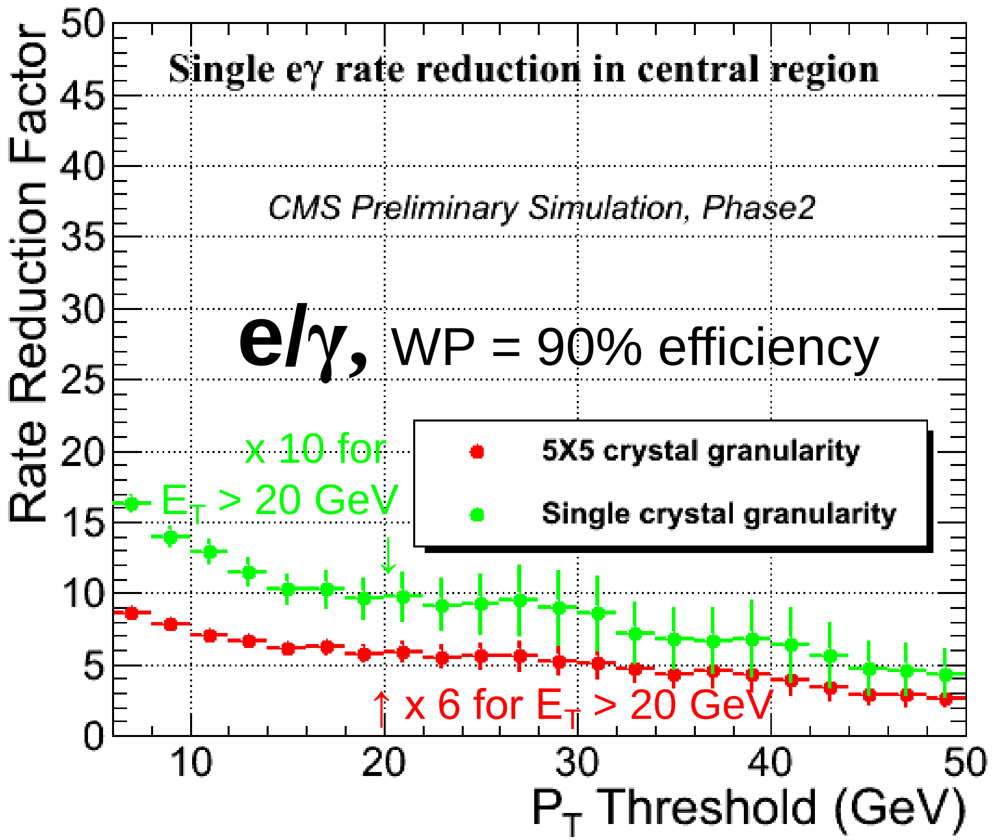


~8400 2S-modules

CMS Gains for μ, e Triggers

(over Phase 1 Trigger, |η| < 1)





Matching Drift Tube trigger primitives with L1Tracks: **large rate reduction:**

Removes flattening at high P_t

Rate reduction by matching L1 e/γ to L1Track stubs for | η | < 1.

Red: with current (5x5 xtal) L1Cal granularity.

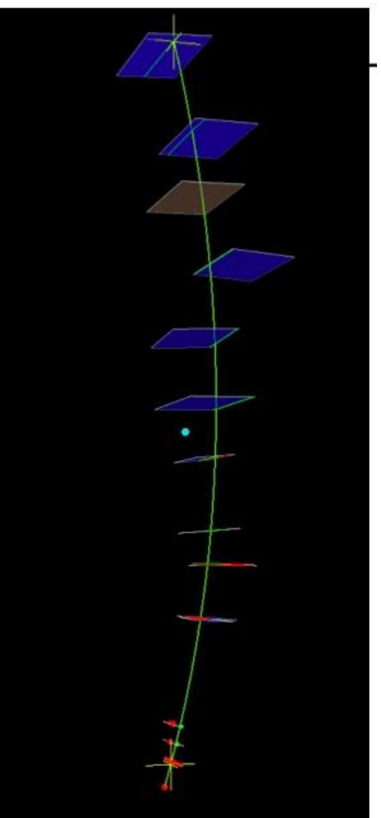
Green : using single crystal-level position resolution improves matching

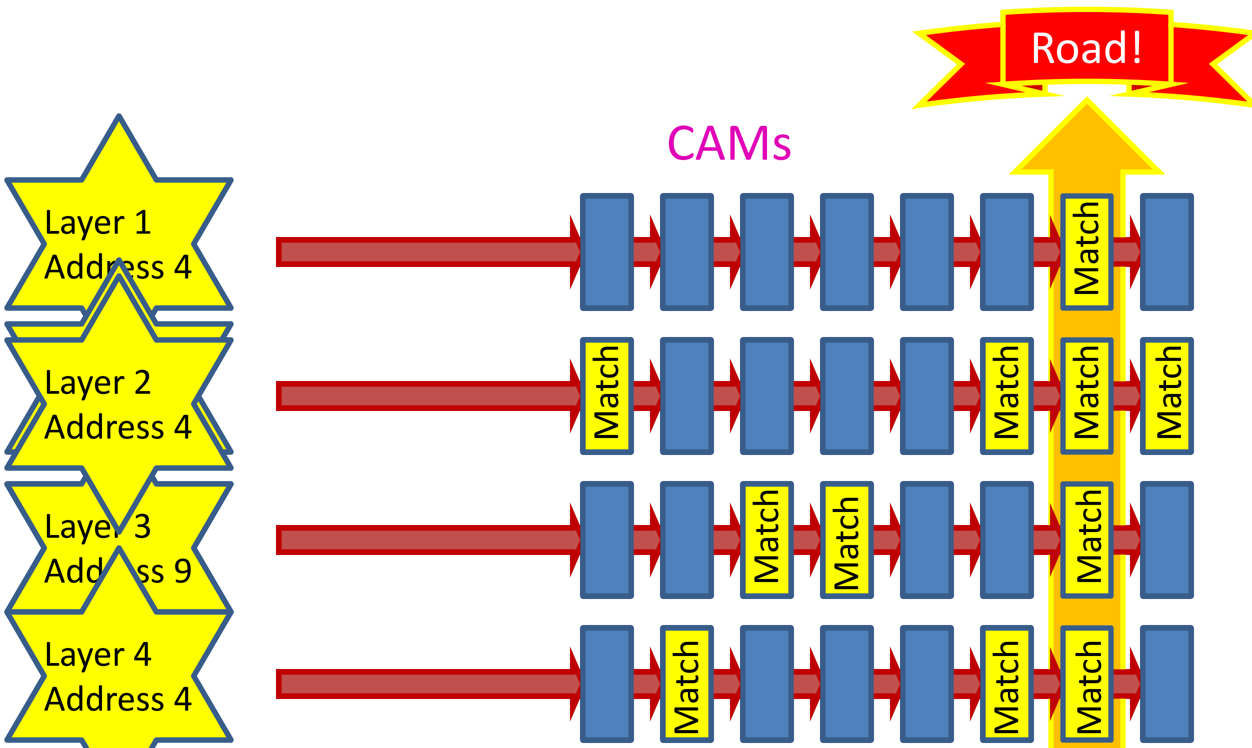
T. Liu

The AM approach

- Pattern Recognition Associative Memory
  - Based on *CAM cells to match and majority logic to associate* hits in different detector layers to a set of pre-determined hit patterns (simple working unit, yet massively parallel)
  - *Pattern Recognition finishes right after all hits arrive (fast data delivery important)*
  - *Potentially good approach for L1 application (require custom ASIC)*

A PR engine naturally handles a given region: divide & conquer

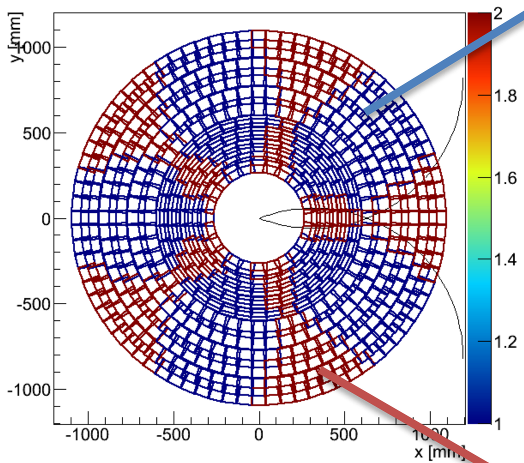




Linearized track fitting can follow each road found (FPGA implementation)

Time Multiplexed Track Trigger

- Still too much data to transmit to a single module
  - sub-divide tracker into slices, with data shared between processors



from non-shared modules

68 FE links
3.2Gbps per link

4 bidirectional DAQ links
10Gbps per link

Layer 1
Pre-Processor

to one TR

24 TRG links
10Gbps per link

from shared (boundary) modules

68 FE links
3.2Gbps per link

4 bidirectional DAQ links
10Gbps per link

Layer 1
Pre-Processor

to two TRs -
24 TRG links
to each

48 TRG links
10Gbps per link

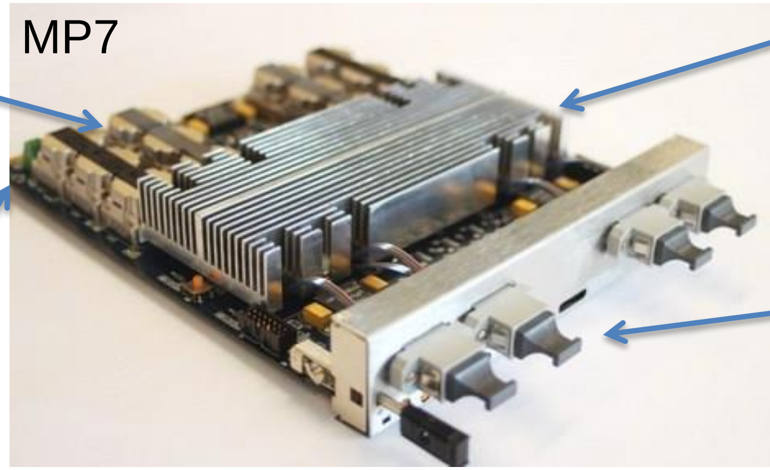
4 DAQ links per PP/FED allows a maximum bandwidth of 40Gbps (~588Mbps available per tracker module)

M Pesaresi

Demonstrator for TM track trigger:
using hardware & expertise developed for L1 calorimeter trigger upgrade

miniPOD 12 channel
parallel optics
12.5 Gbps per link

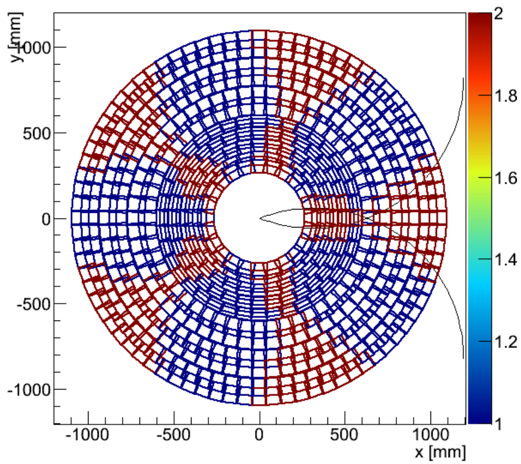
µTCA format



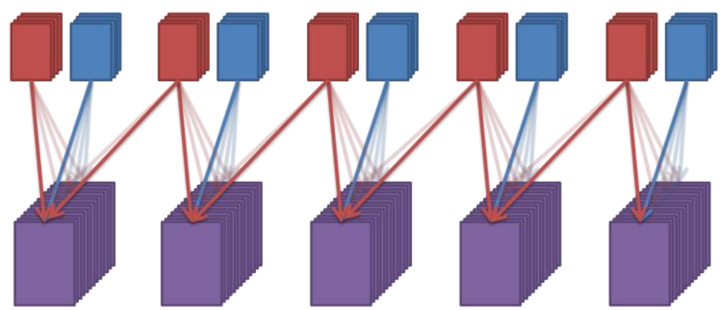
Xilinx Virtex-7 FPGA

72 input / 72 output optical links
=> 0.9Tb/s total bandwidth

example implementation:
divide tracker up into 5 regions in phi



processors (purple) build tracks in the FPGA
or data can be forwarded to AM ASICs



~230 Layer 1 - PreProcessors
- input data from tracker
- output trigger data is formatted & time multiplexed

120 Main Processors
- each receive data over 24BX
- each processes one phi sector per event

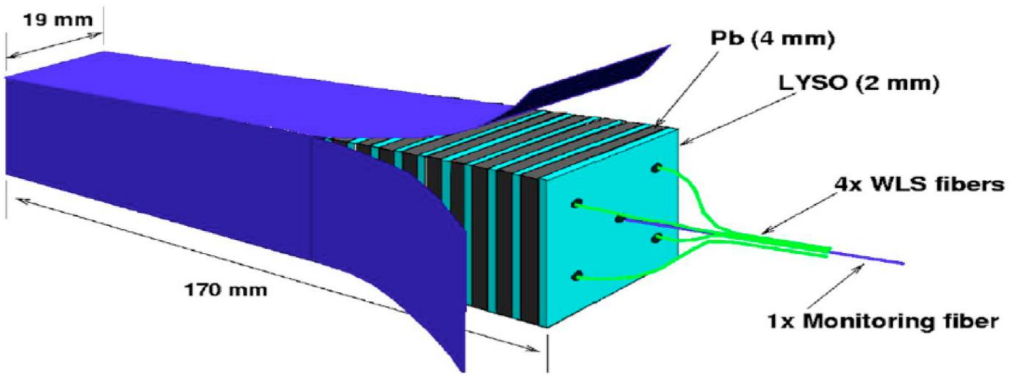
Summary

- Detector design and present architectures impose constraints on future triggers
- LHCb
  - small data volumes and simple geometry make it now feasible to read out all the data for event selection in CPU
- ATLAS and CMS
  - new trigger strategies are needed to preserve wide physics programme
  - extra information from tracking should be deployed at L1 but too much data to read it all out
  - either
  - L0 trigger + processing to find all tracks in seeded, limited region (ATLAS)
  - or
  - suppress low p_T hits in L1 data to find higher p_T tracks in entire detector (CMS)

BACKUP MATERIAL

Possible further CMS challenge

- Endcap Calorimeters – require replacement because of radiation damage
  - Build EE towers in eg. Shashlik design (crystal scintillator: LYSO, CeF)
  - Rebuild HE with more fibers, rad-hard scintillators



  - OR Particle Flow Calorimeter (PFCAL) – following work of CALICE
    - fine transverse & longitudinal segmentation to measure shower topology using silicon pads

- Either solution will require solution for triggering