Signal Processing for Large area tracking system based on Silicon strips
&
Real time Track Triggering: Technological challenges

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CERN
18 July 2014

Purpose of the lesson

1) Keep audience awake for ~ 2h
2) Introduce the basics of F.E. signal processing for strip detectors
3) Point to some good old friends audience might encounter
4) Introduce novel approaches in detector design

Outline of the lesson

- Silicon strip tracking detectors
- Front-end signal processing
- Examples of detector design
- Real-time tracking

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- Silicon strip tracking detectors
- Front-end signal processing
- Examples of detector design
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More “didactic”

More “informing”

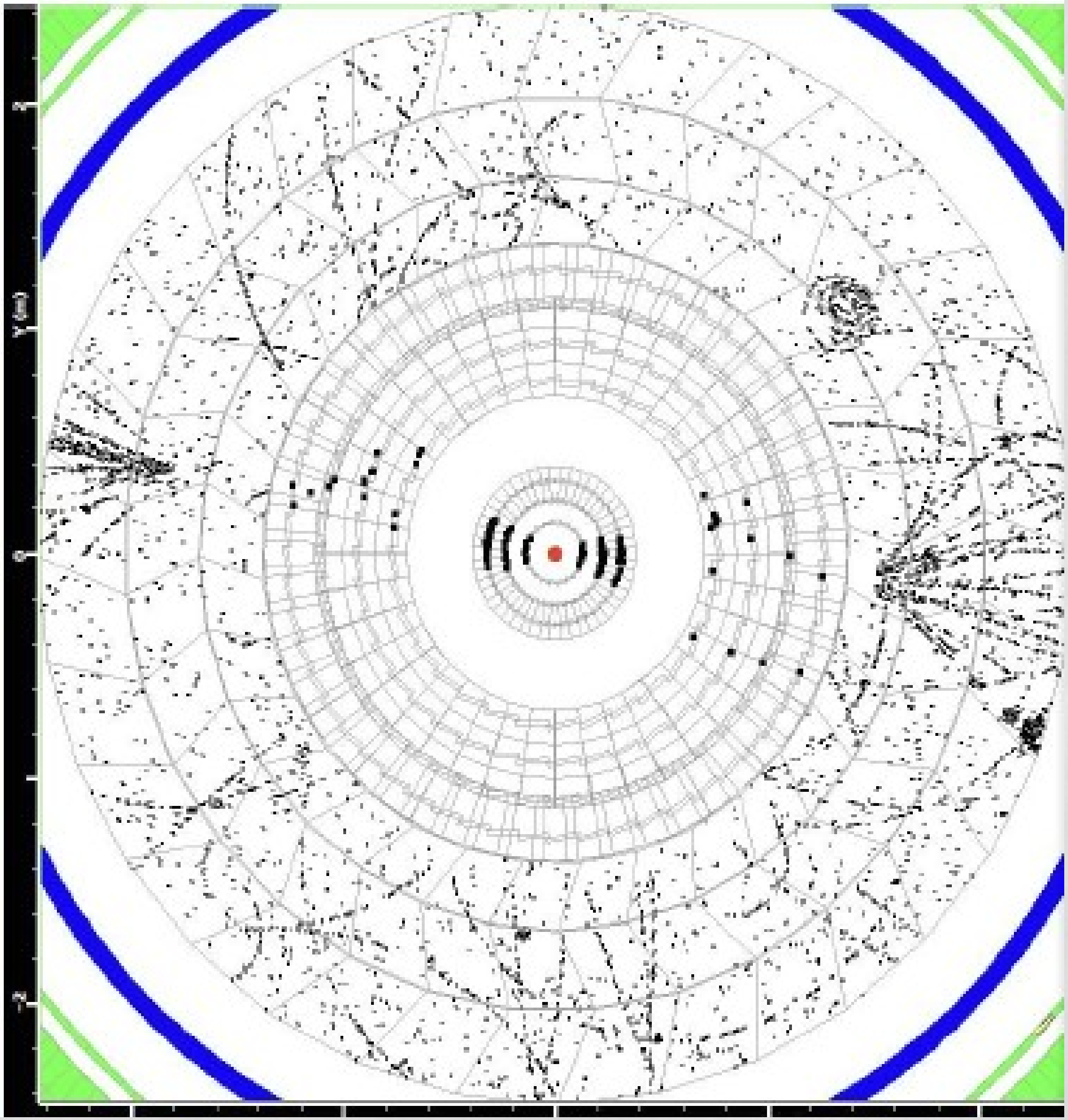
Outline of the lesson

- ➡ Silicon strip tracking detectors
- Front-end signal processing
- Examples of detector design
- Real-time tracking

Tracking detectors

- Goal: measure momentum & energy of each product of collision – identify each particle
- Trackers: used in HEP experiments to reconstruct “track” of **charged** particles
- Set of single measurement point: (x,y,z) or rather (r,φ,z)
- (Typically) solenoid magnetic field

… plus: “do not disturb!”



Does it ring a bell?

$$q\vec{v}\times\vec{B}$$

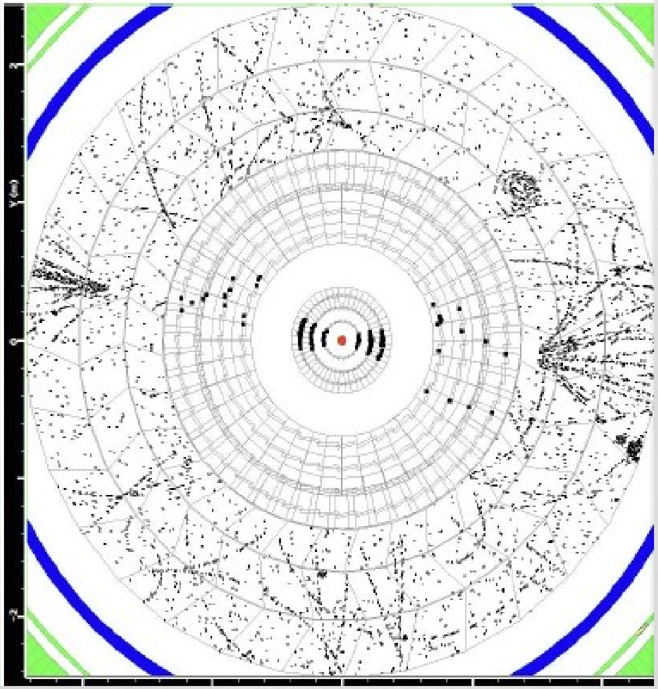
Tracking detectors

Curvature radius proportional to p_T

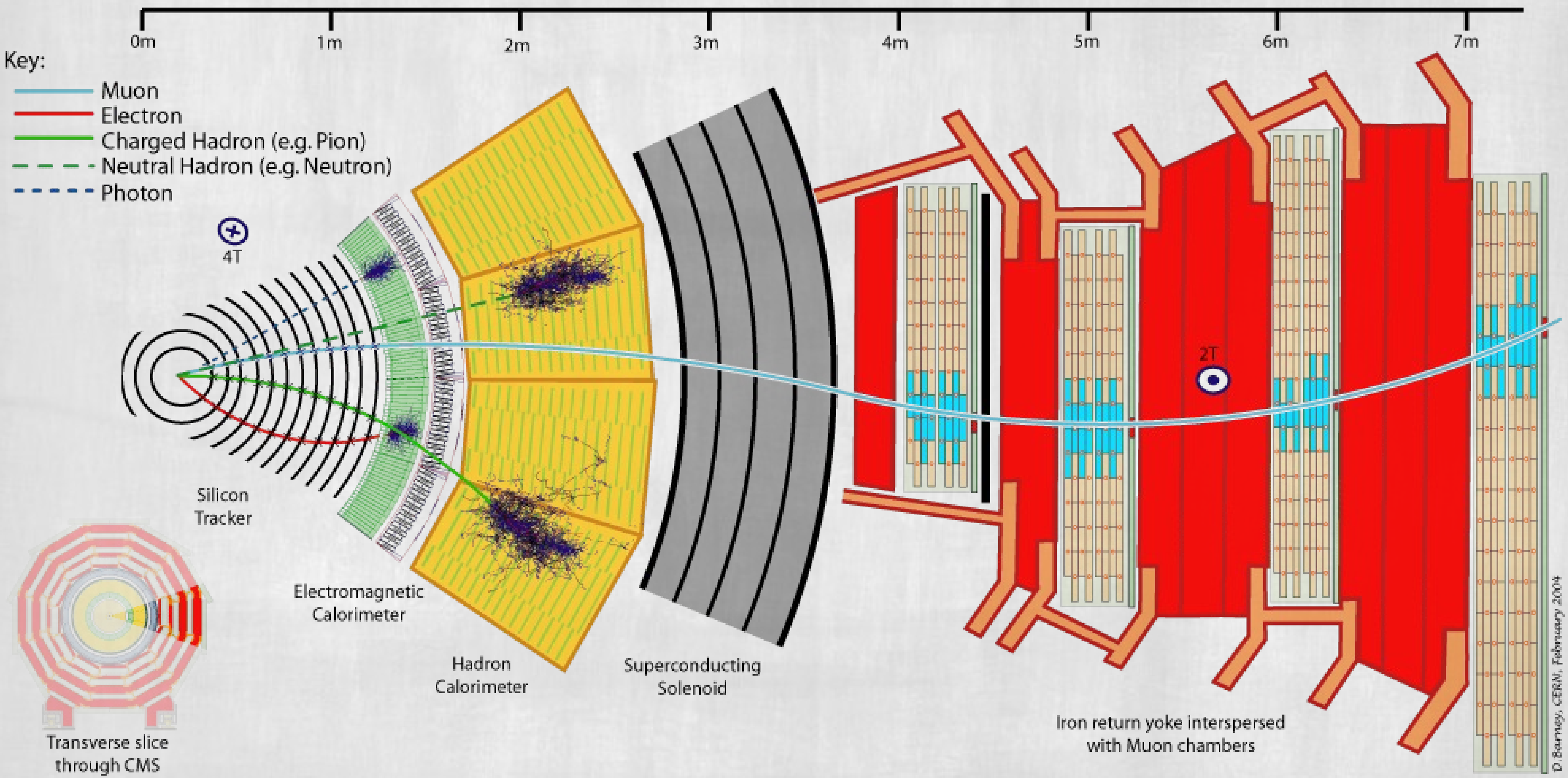
$p_T = 0.3\ z\ B\ R$ GeV/(T×m)

Track => p_T, θ => p_Z

Additional information on energy E from other detectors (calorimeters, muon detectors) to identify the particle



A slice of CMS

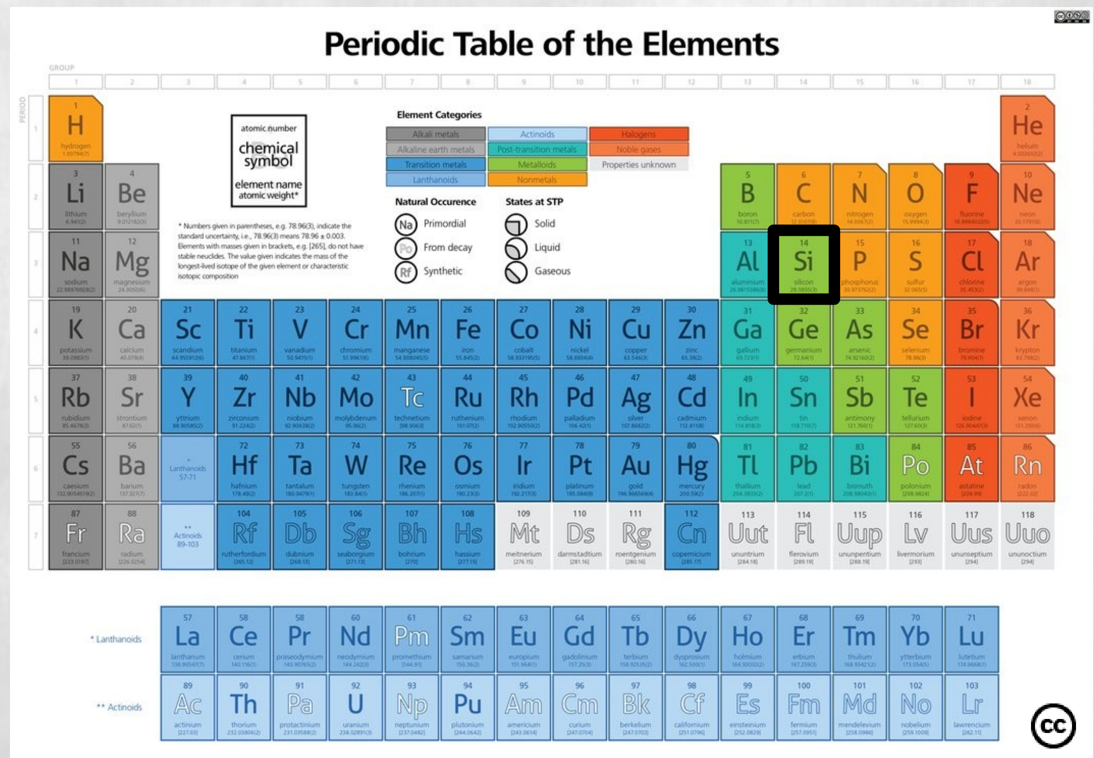


Tracking: why silicon

- Advantages w.r.t. competitors
  - Large signal: 24'000 pairs/300 μm
  - Fast signal: O(10 ns)
  - High rate: no "recovery time" like gas detectors
  - Resolution: down to few μm (feature size + S/N)
  - Light (low Z), but...

    X_0 = 9.36 cm

    300 μm = 0.32% X_0



http://fiveless.deviantart.com/art/Periodic-Table-of-the-Elements-147350318

- Disadvantages
  - ... heavy-ish

    Front-end + services needed

    Will come back on this

    - Typical 1% X_0 per layer
  - At colliders: material in active volume

Tracking: why silicon

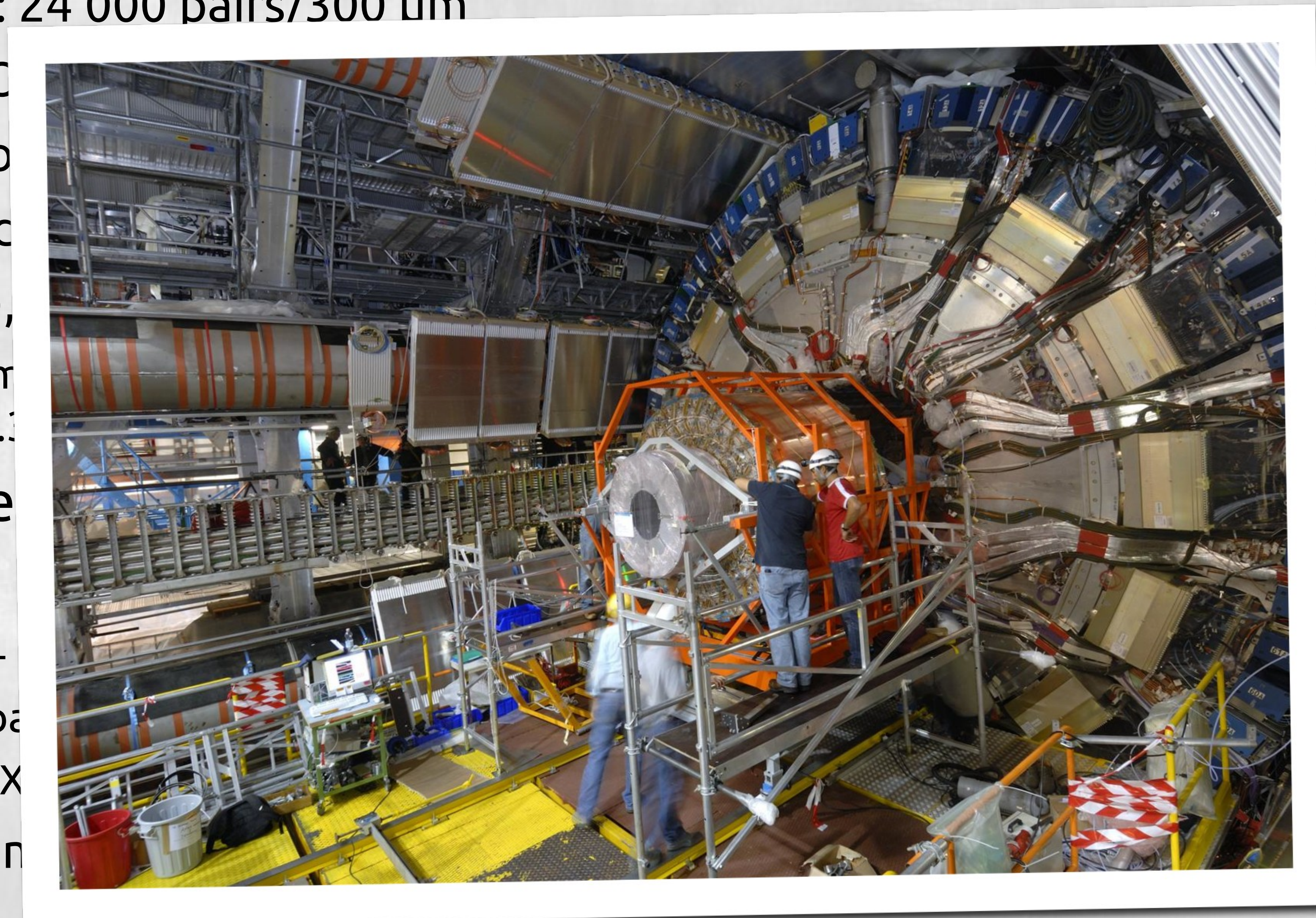
- Advantages w.r.t. competitors
  - Large signal: 24'000 pairs/300 μm
  - Fast signal: C
  - High rate: no
  - Resolution: c
  - Light (low Z),

    $X_0 = 9.36$ cm

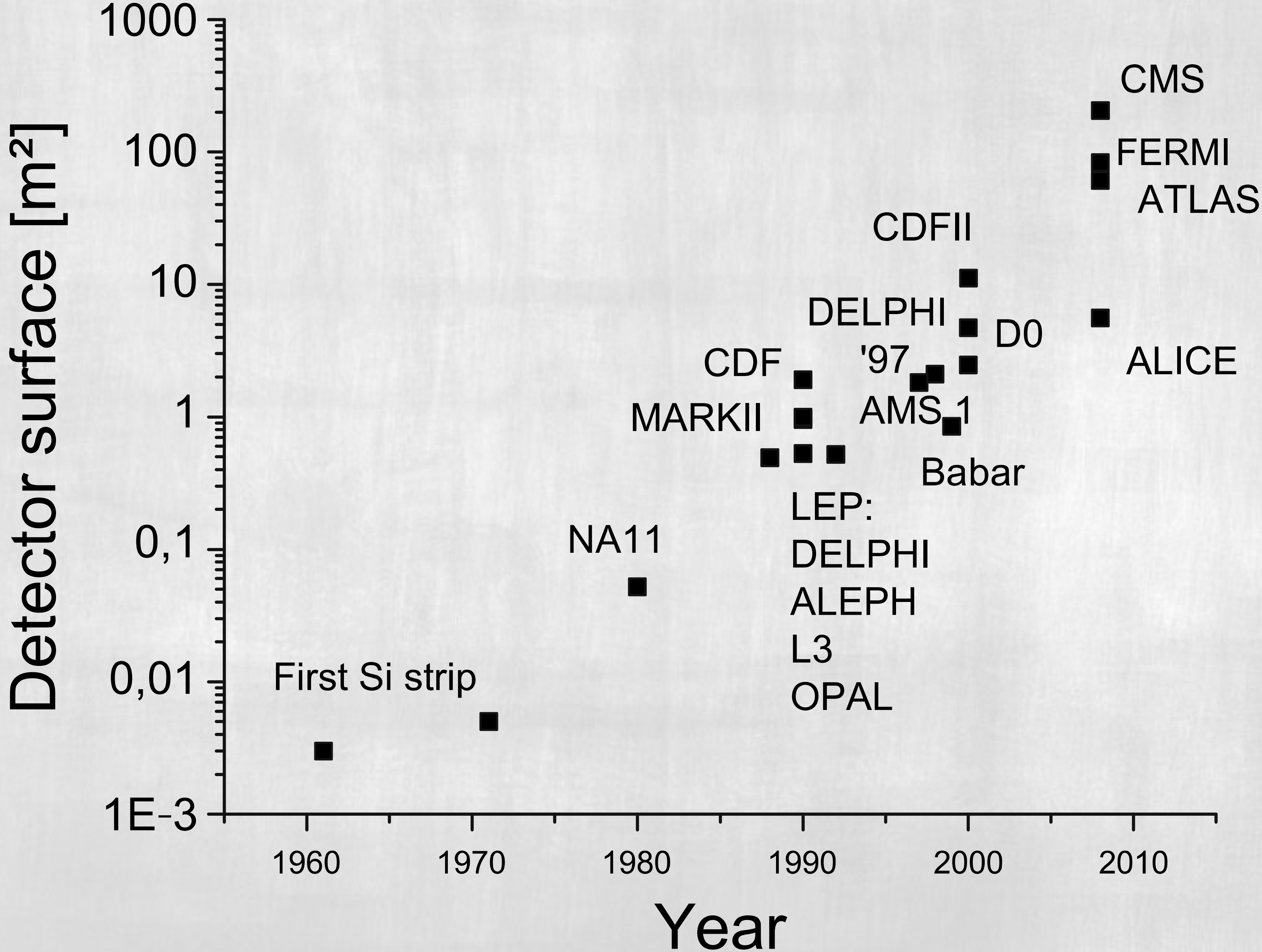
    300 μm = 0.3
- Disadvantage
  - … heavy-ish

    Front-end +

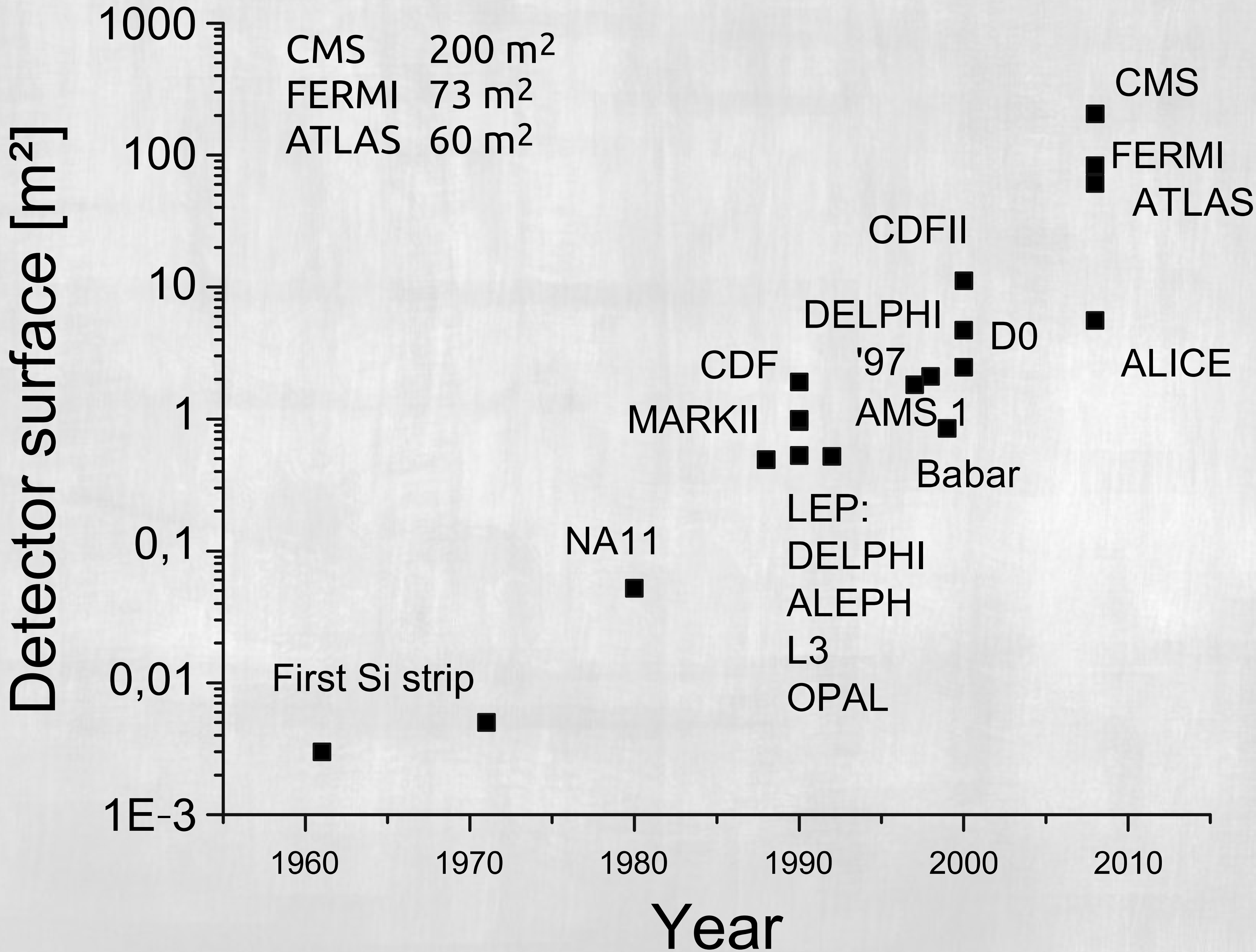
    Will come ba
    - Typical 1% X
  - At colliders: n
    volume



Evolution of silicon detectors

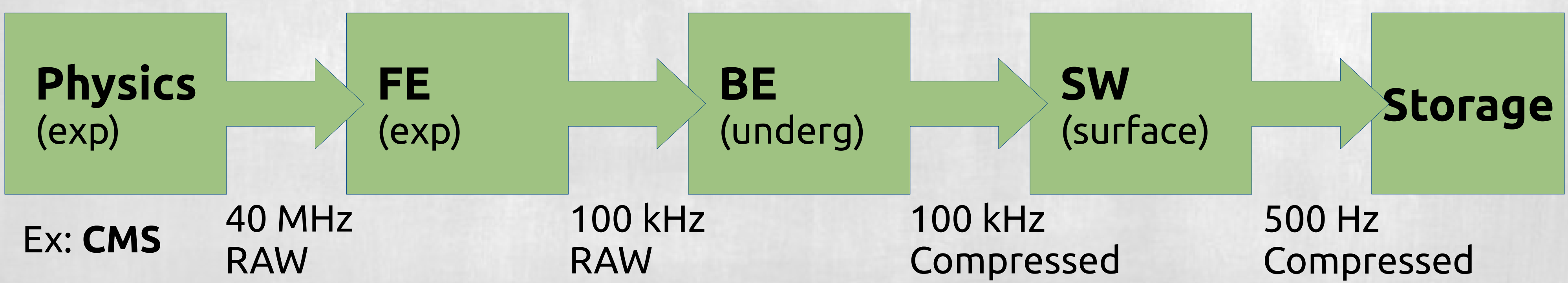


Evolution of silicon detectors



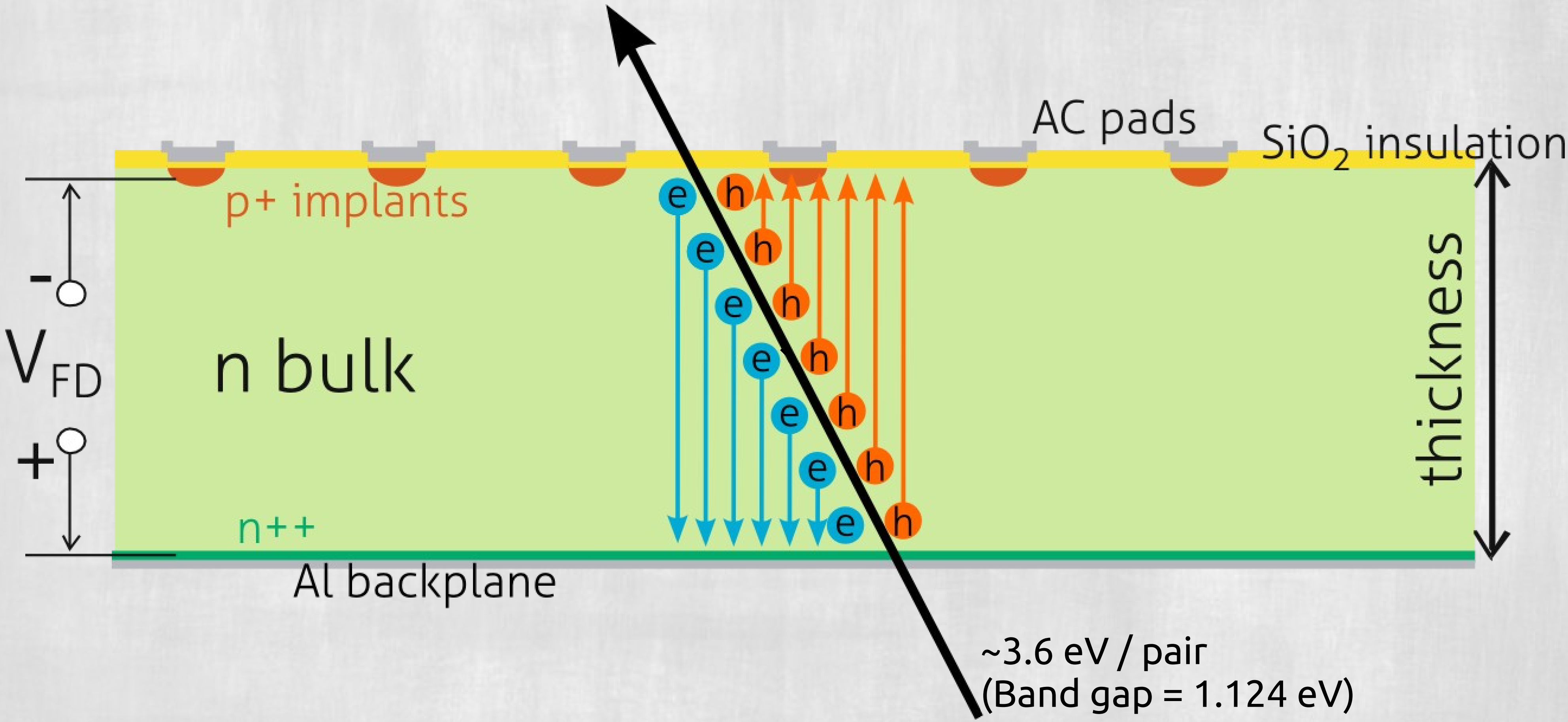
Silicon strips in collider experiments

- Fine-grained granularity (many channels)
- Large collision frequency
  - TeV: → 1.7 MHz
  - LHC: → 40 MHz
- Cannot possibly store all data → selection of interesting events is mandatory
- Reducing data in F-E: more power to F-E processing
- Reducing data in B-E: more power to data links
- Front-end constraint: material/power!



Silicon as a detector

Working principle: array of p-n diodes (reverse biased)

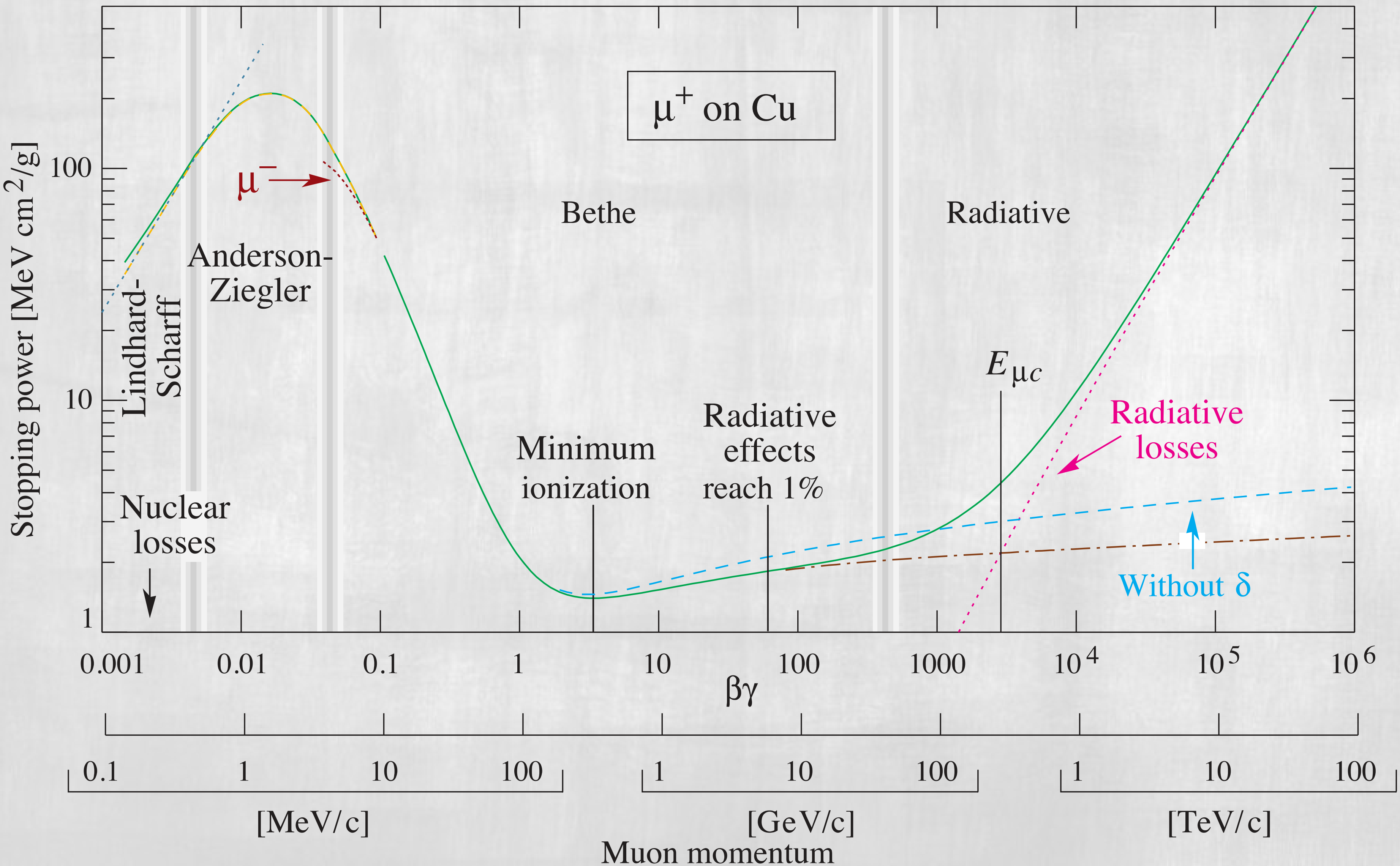


F. Hartmann: Evolution of Silicon Sensor Technology in Particle Physics, Springer

Silicon as a detector

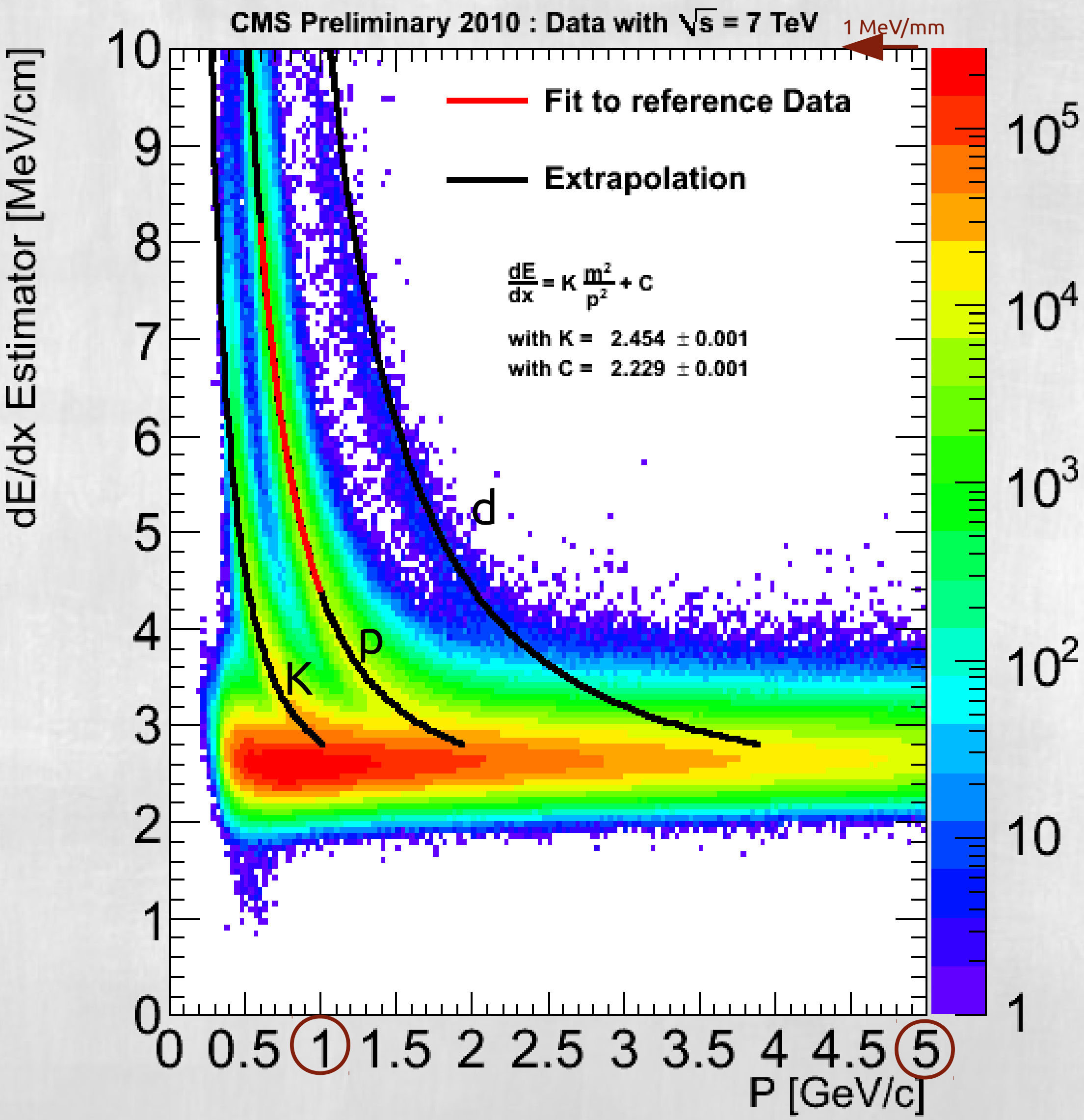
Energy loss

http://pdg.lbl.gov/2013/figures/figures.html



Particle identification

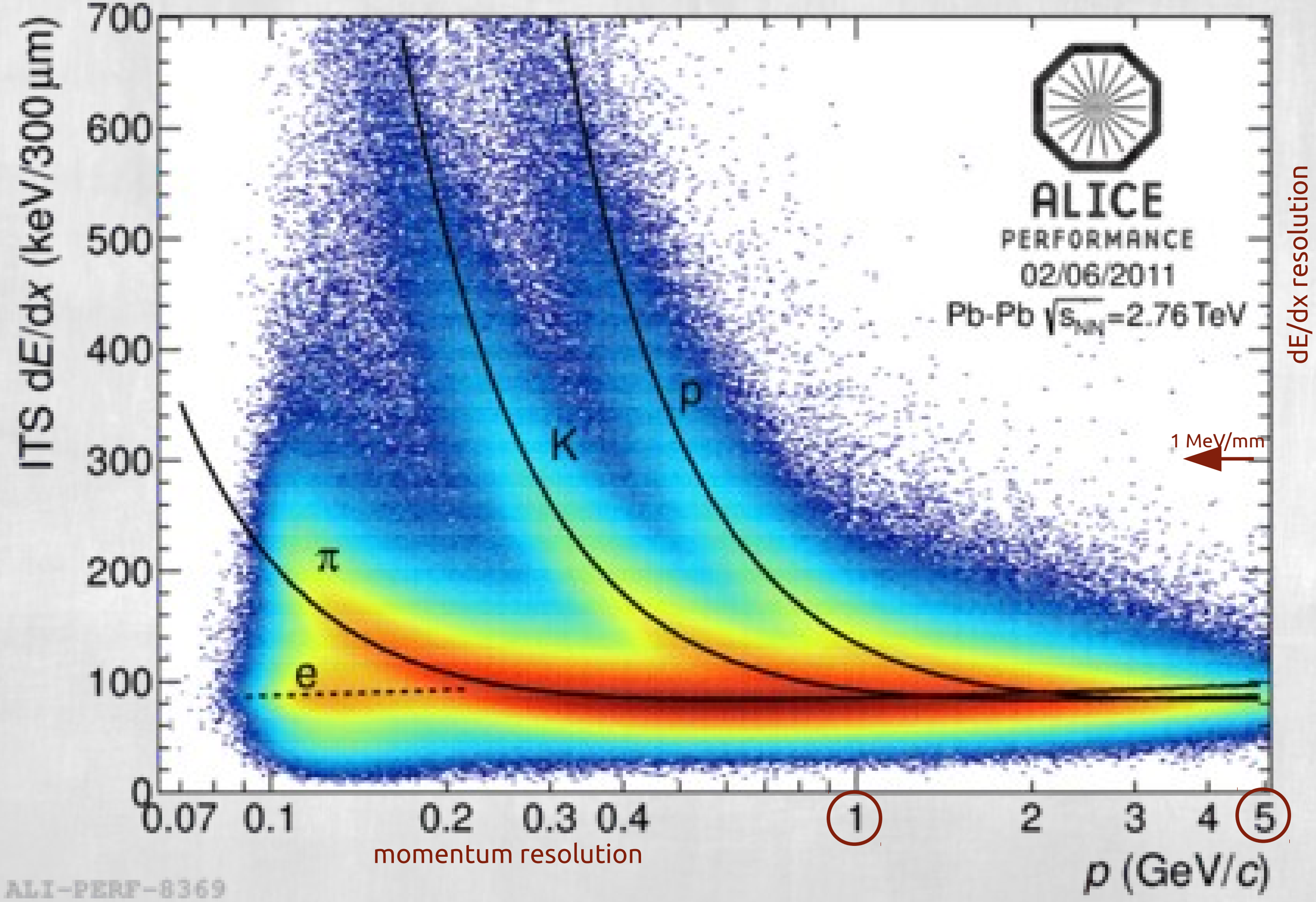
… by reading the signal amplitude



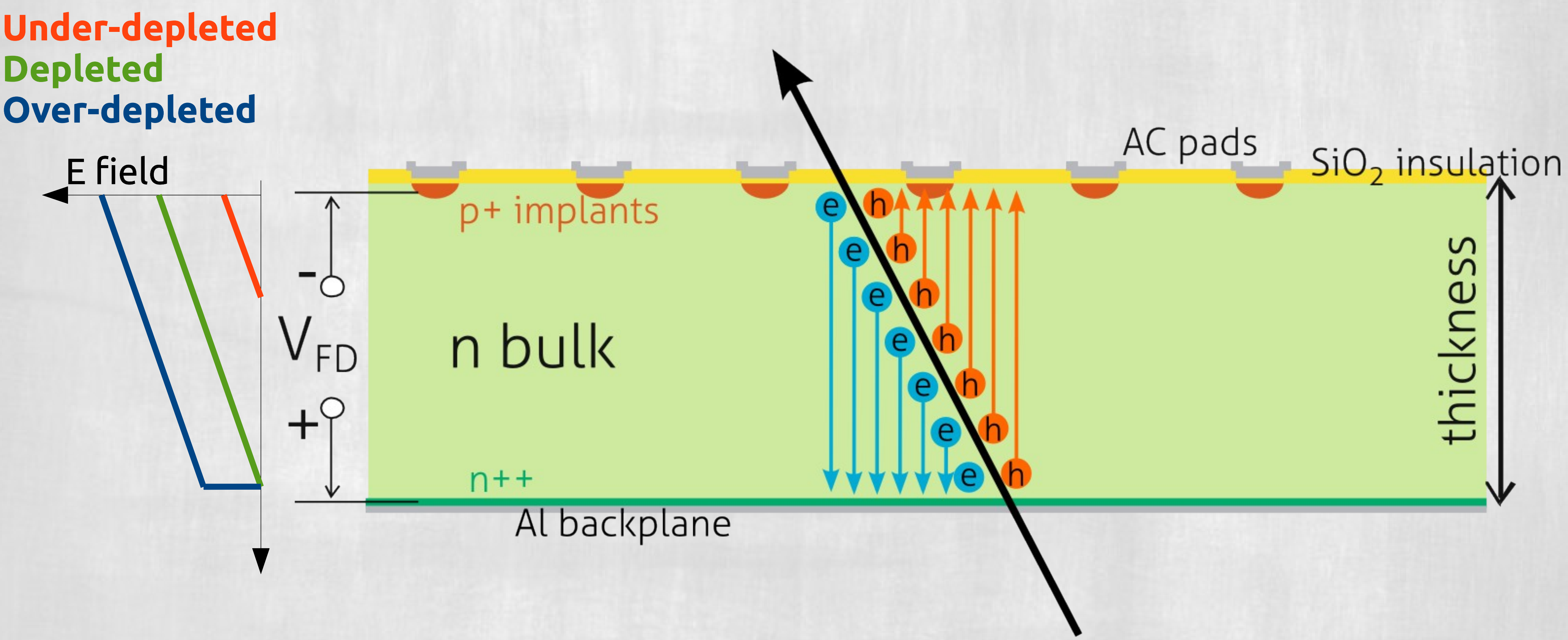
Particle identification

… by reading the signal amplitude ("go ask Alice…")

Silicon Drift Detector +
Silicon µStrip Detector



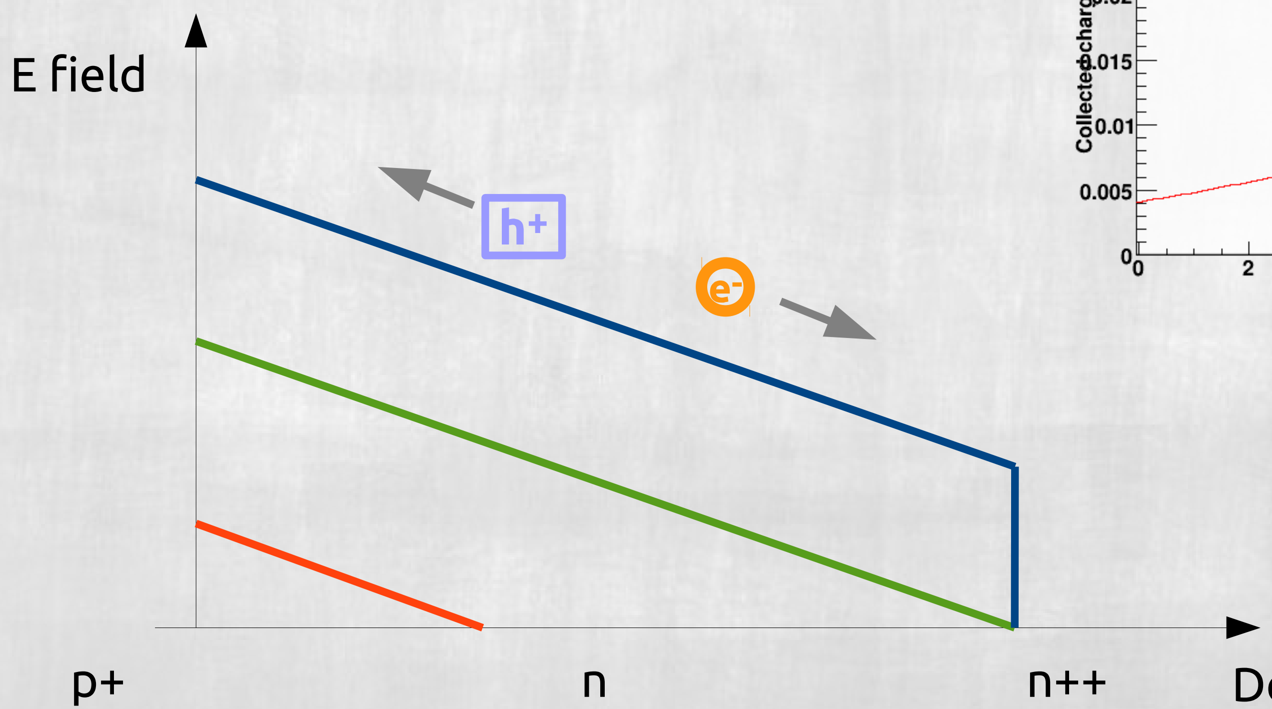
Sensor characteristics: depletion

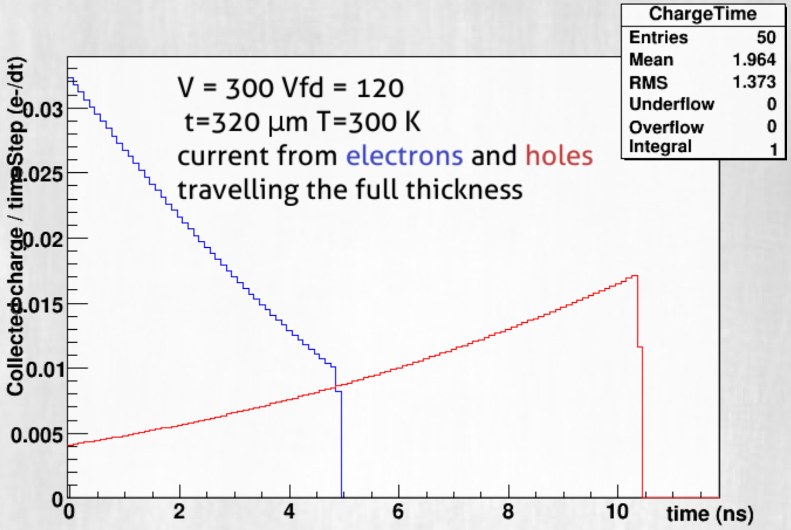


Sensor characteristics: depletion

Shockley–Ramo theorem [1,2]: $i = q\frac{\vec{E}\cdot\vec{v}}{V_0}$

Or, alternatively: $Q = \frac{q}{V_0}\int \vec{E}\cdot d\vec{s}$





Under-depleted
Depleted
Over-depleted

[1] Shockley, W. (1938). "Currents to Conductors Induced by a Moving Point Charge". Journal of Applied Physics 9 (10): 635
[2] Ramo, S. (1939). "Currents Induced by Electron Motion". Proceedings of the IRE 27 (9): 584–585

Sensor characteristics: mobility

Linear approximation $\vec{v} = \mu \vec{E}$

with μ = mobility of charge carrier

Why can we use this approximation?

Sensor characteristics: mobility

Linear approximation $\vec{v} = \mu \vec{E}$

with μ = mobility of charge carrier

charge carrier scattering on lattice defects:
"viscous" approximation

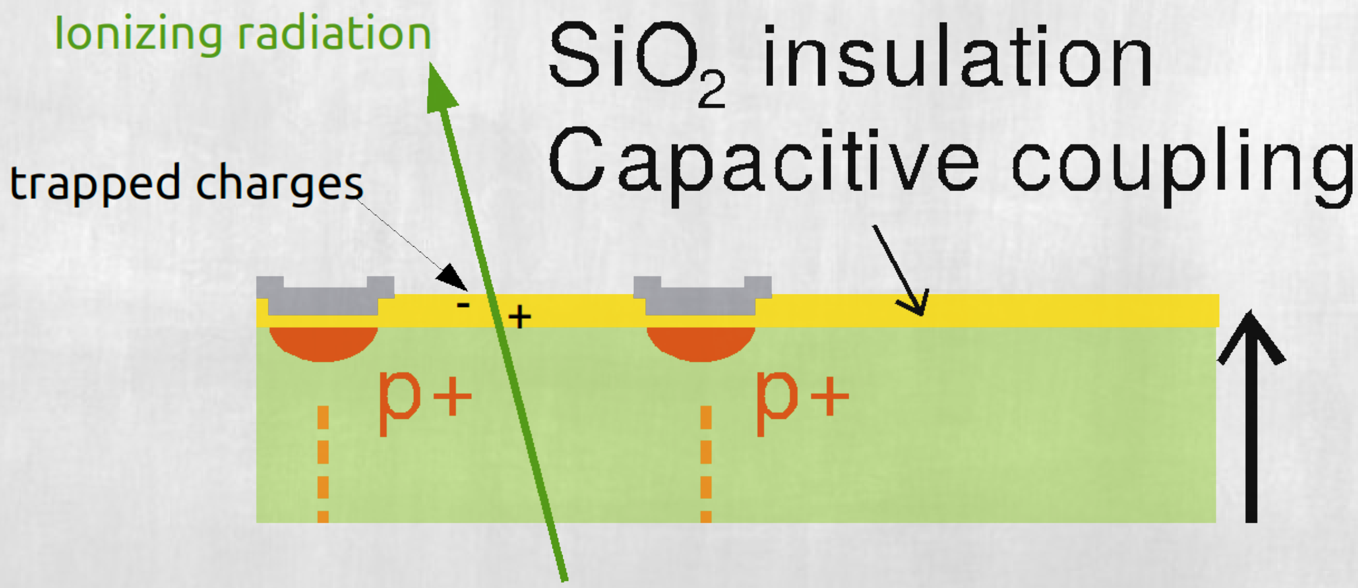
Mobility of charge carriers:

$\mu_e = 1350\ cm^2\ V^{-1}\ s^{-1}$

$\mu_h = 450\ cm^2\ V^{-1}\ s^{-1}$

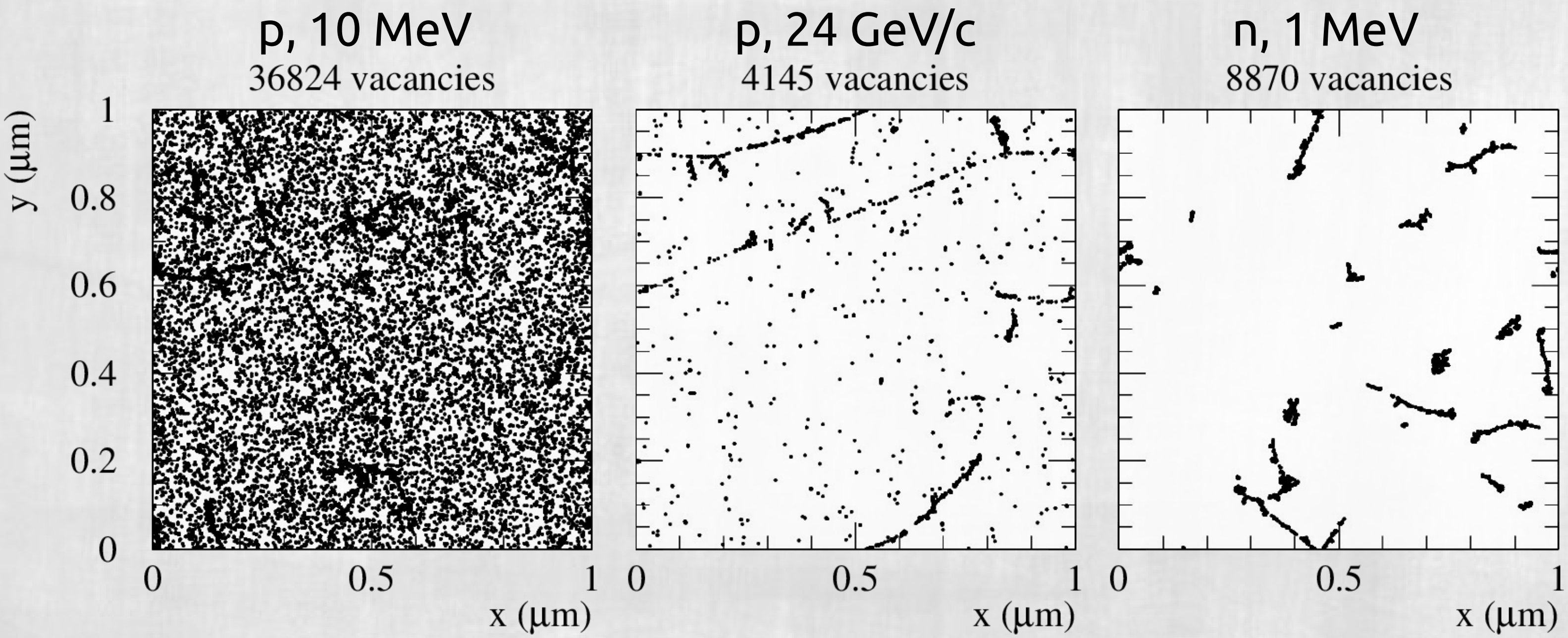
Radiation damage

- Surface damage (charge accumulation)
  - Ionizing radiation, measured in rad, Gy
  - Typical LHC dose (60 cm → 20cm) 1 MGy → 10 MGy
  - Mostly relevant for Front-End electronics



Radiation damage

- Bulk damage (current+trapping)
  - Non Ionizing Energy Loss (Hamburg model)
  - More relevant for sensors
  - Measured in 1MeV-n-eq (according to scaling of current)



Non-ionizing interaction between incident radiation and silicon lattice creates defects: additional levels inside the band-gap

Mika Huhtinen
Simulation of non-ionising energy loss and defect formation in silicon
ROSE/TN/2001-02

Radiation damage

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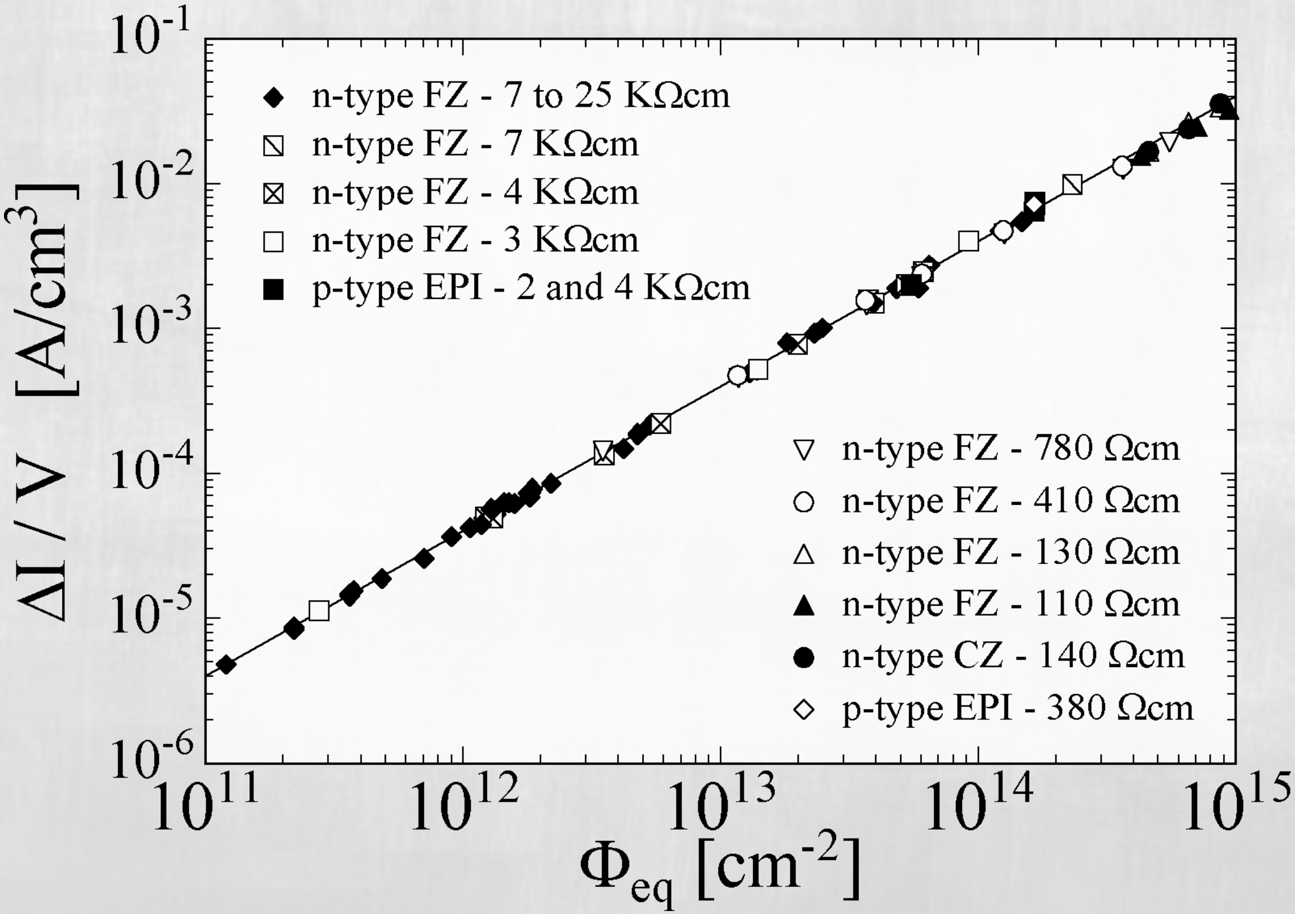
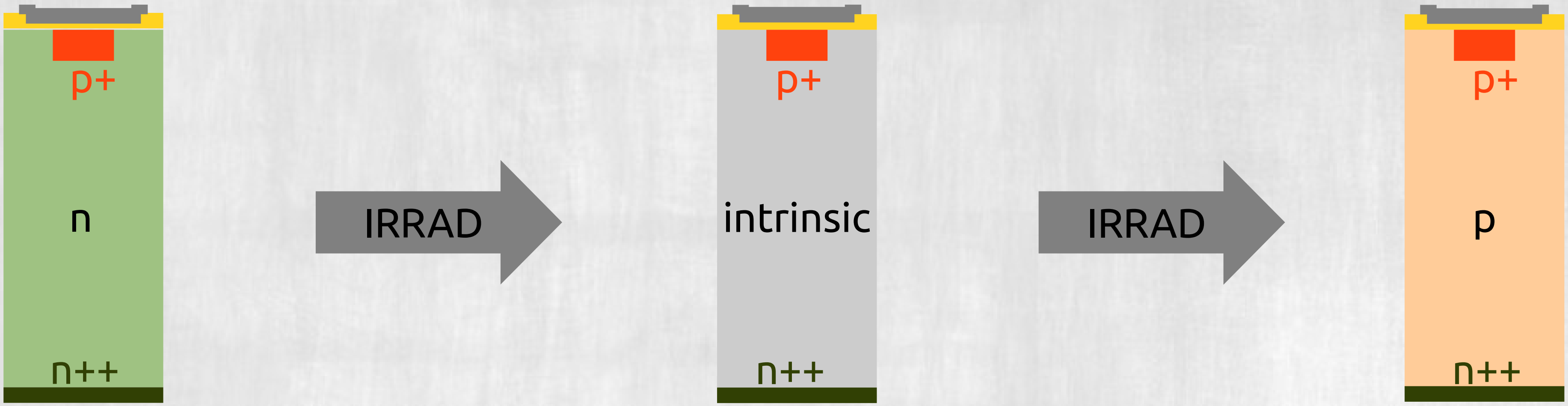


Michael Moll
Ph.D. thesis
https://mmoll.web.cern.ch/mmoll/thesis/

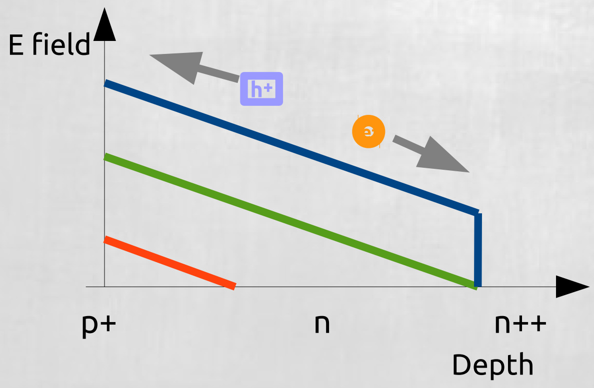
Radiation damage for p-on-n

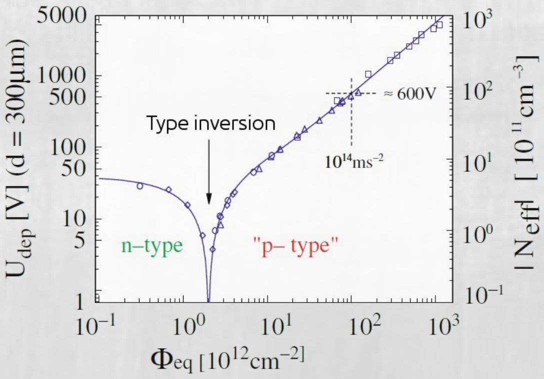
Defects introduced by radiation act as acceptors

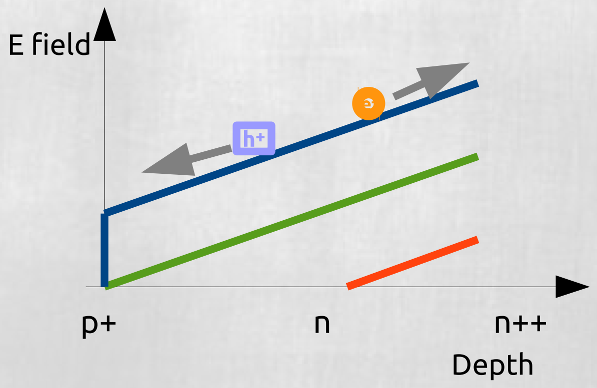


After irradiation:

- same signal polarity
- no signal if not fully depleted

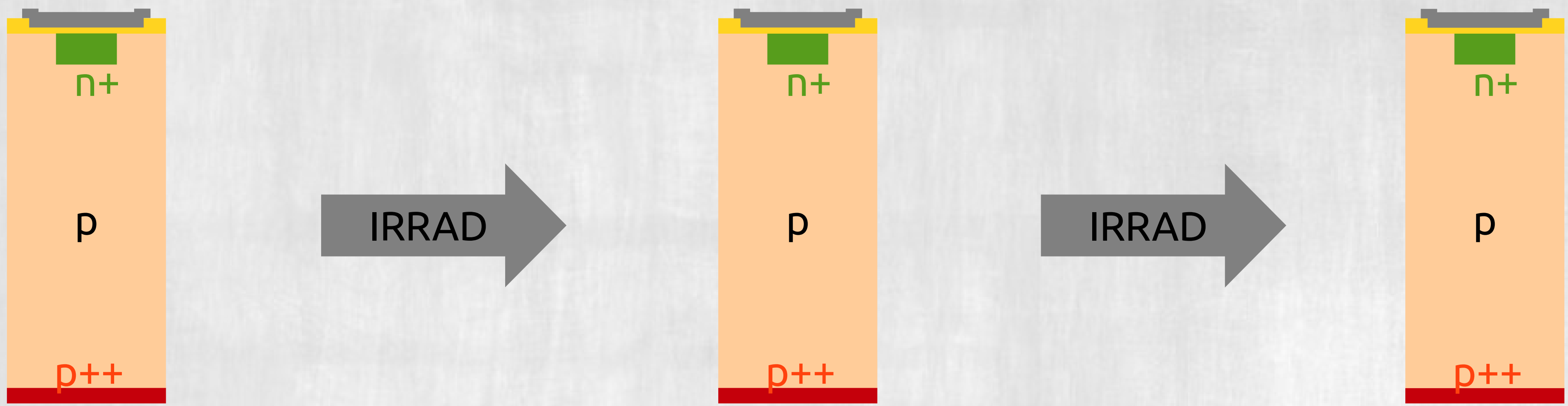


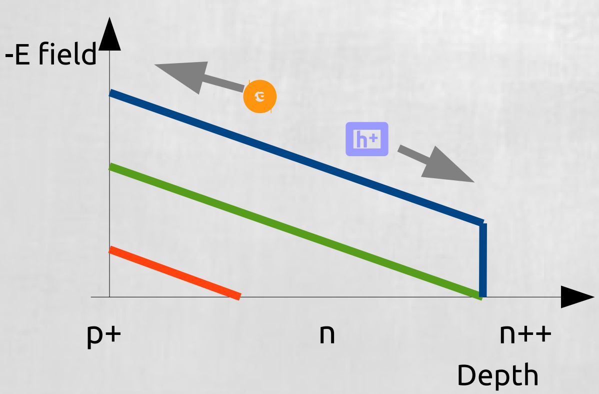




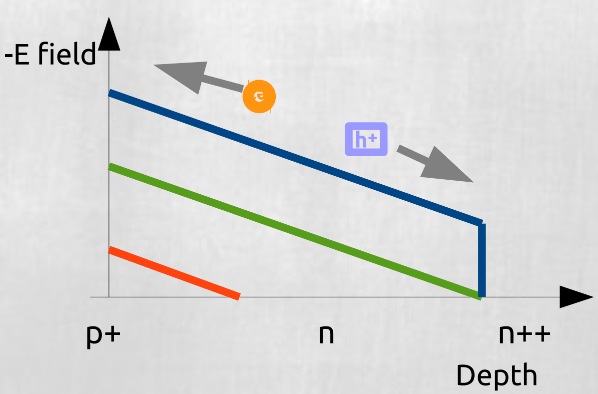
Radiation damage for n-on-p

No type inversion





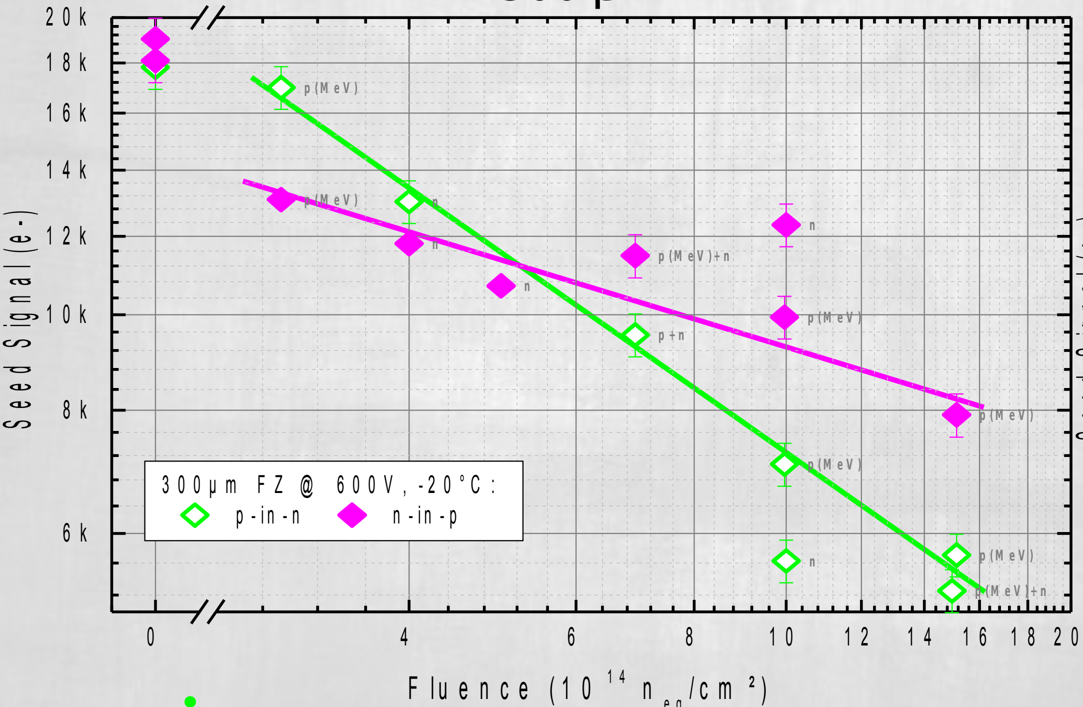
After irradiation:
- always collect signal even if not fully depleted



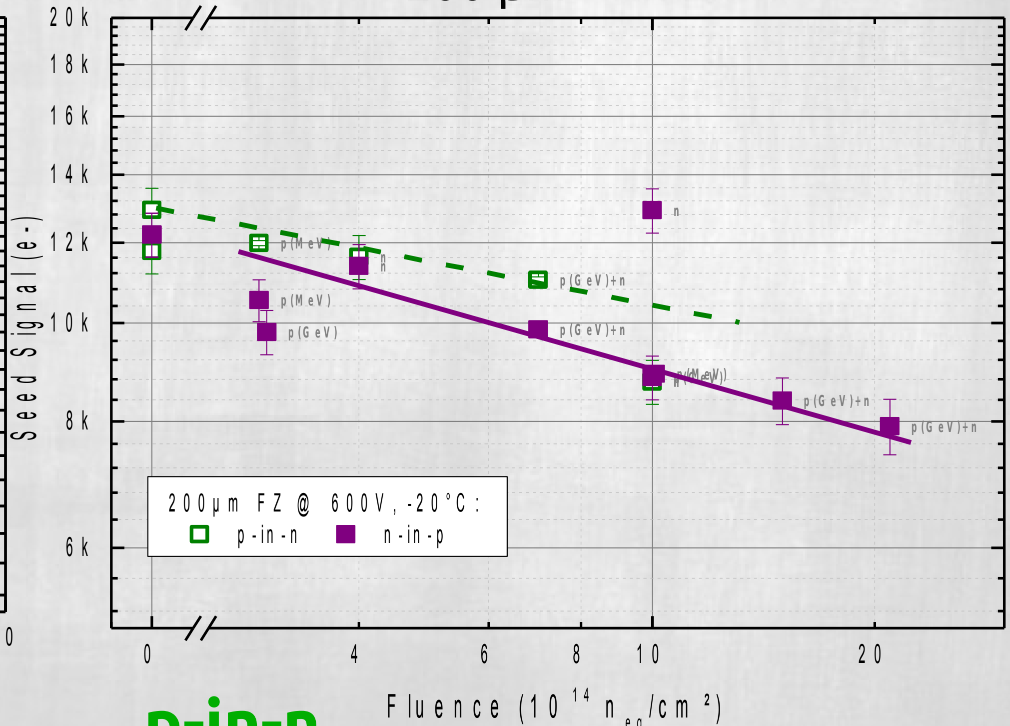
Signal degradation with irradiation

- Full depletion voltage increase ⇒ operating in partial depletion
- Bulk defects created ⇒ charge carriers trapping

300 μm



200 μm



p-in-n
n-in-p

p-in-n
n-in-p

Signal polarity

- Note:
  - The front-end electronics input polarity must match the one of sensor's signal
  - To make the electronics compatible with both sensor polarities, an additional *inverter* stage is needed (which draws a little extra power and adds a little extra noise)

Outline of the lesson

~~Silicon strip tracking detectors~~

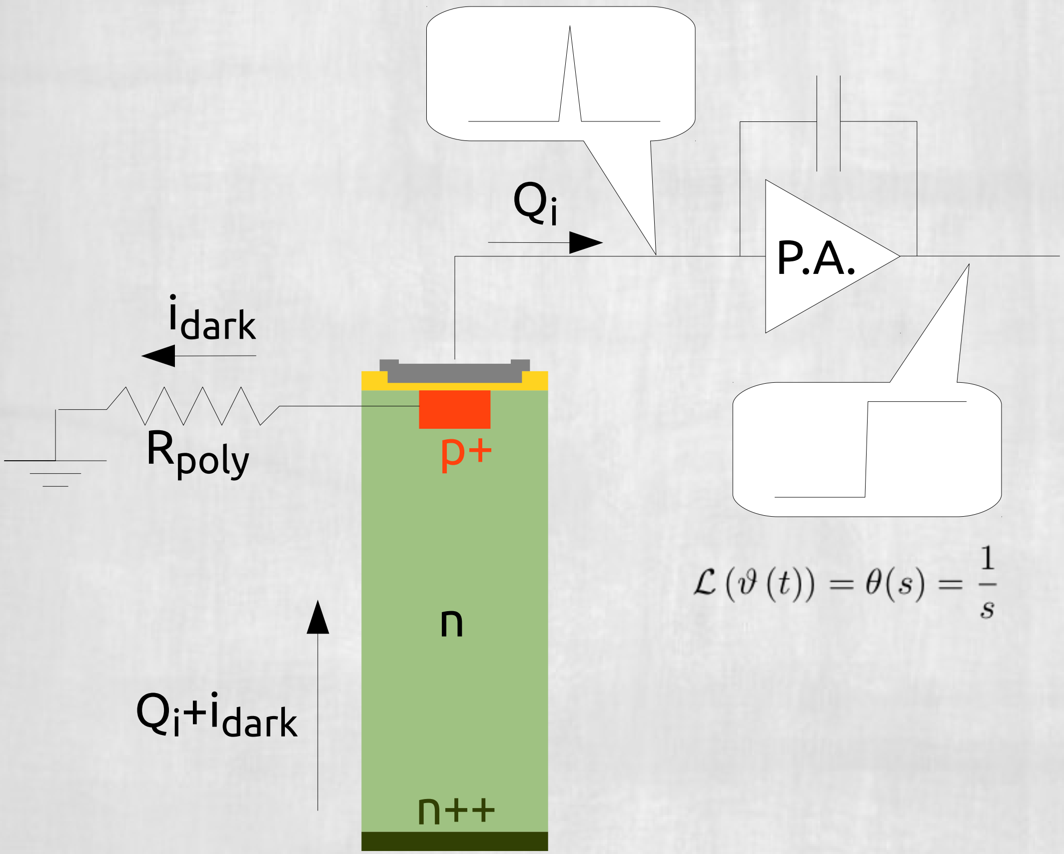
➡ Front-end signal processing

Examples of detector design

Real-time tracking

Front-end typical (analogue)

Small signal (ke-): amplification needed



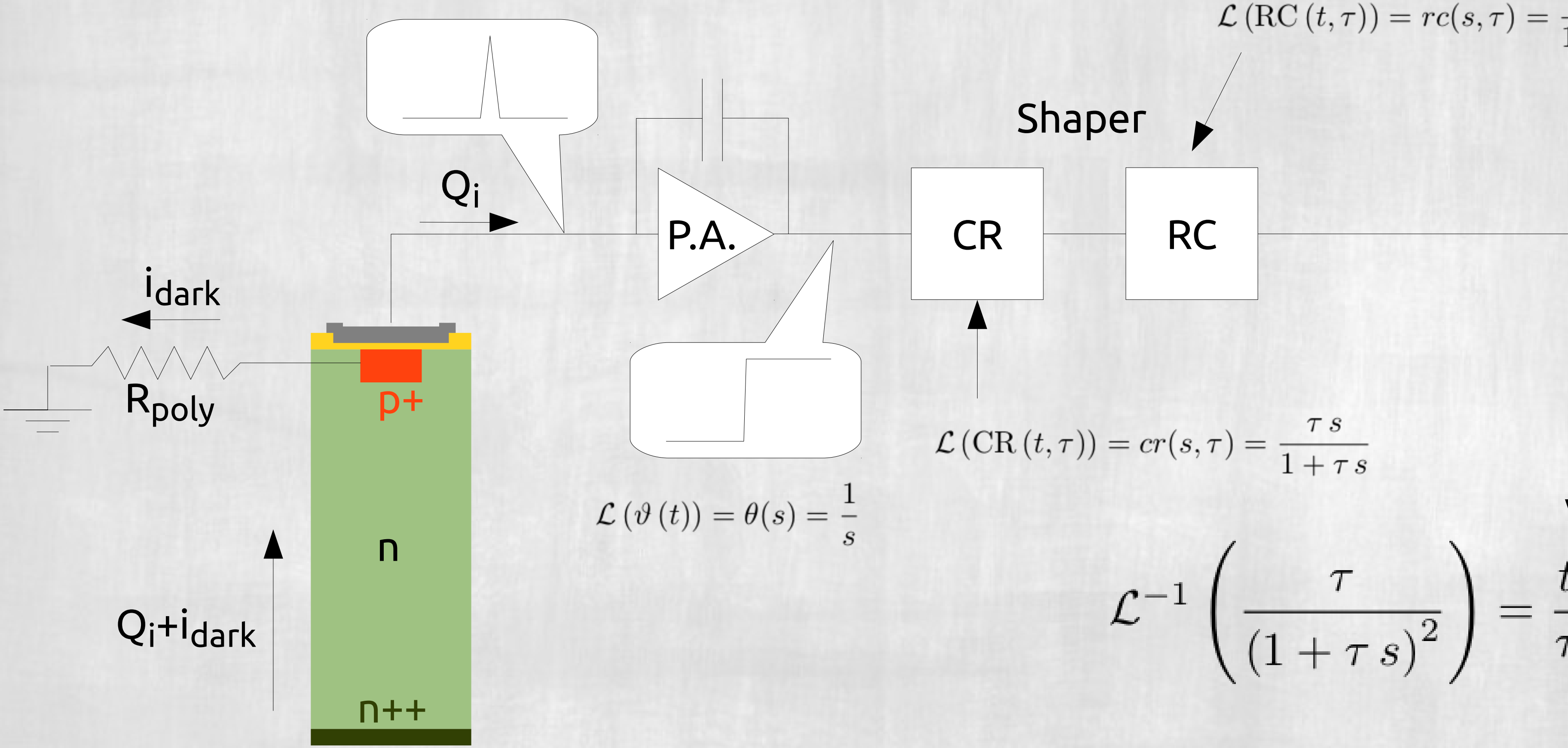
$$\mathcal{L}\left(\vartheta\left(t\right)\right) = \theta(s) = \frac{1}{s}$$

Front-end typical (analogue)

Small signal (ke-): amplification needed

Well-defined sampling time: shaping (amplitude proportional to input charge)

$$\mathcal{L}\left(\mathrm{RC}\left(t,\tau\right)\right) = rc(s,\tau) = \frac{1}{1+\tau\, s}$$



$$\mathcal{L}\left(\mathrm{CR}\left(t,\tau\right)\right) = cr(s,\tau) = \frac{\tau\, s}{1+\tau\, s}$$

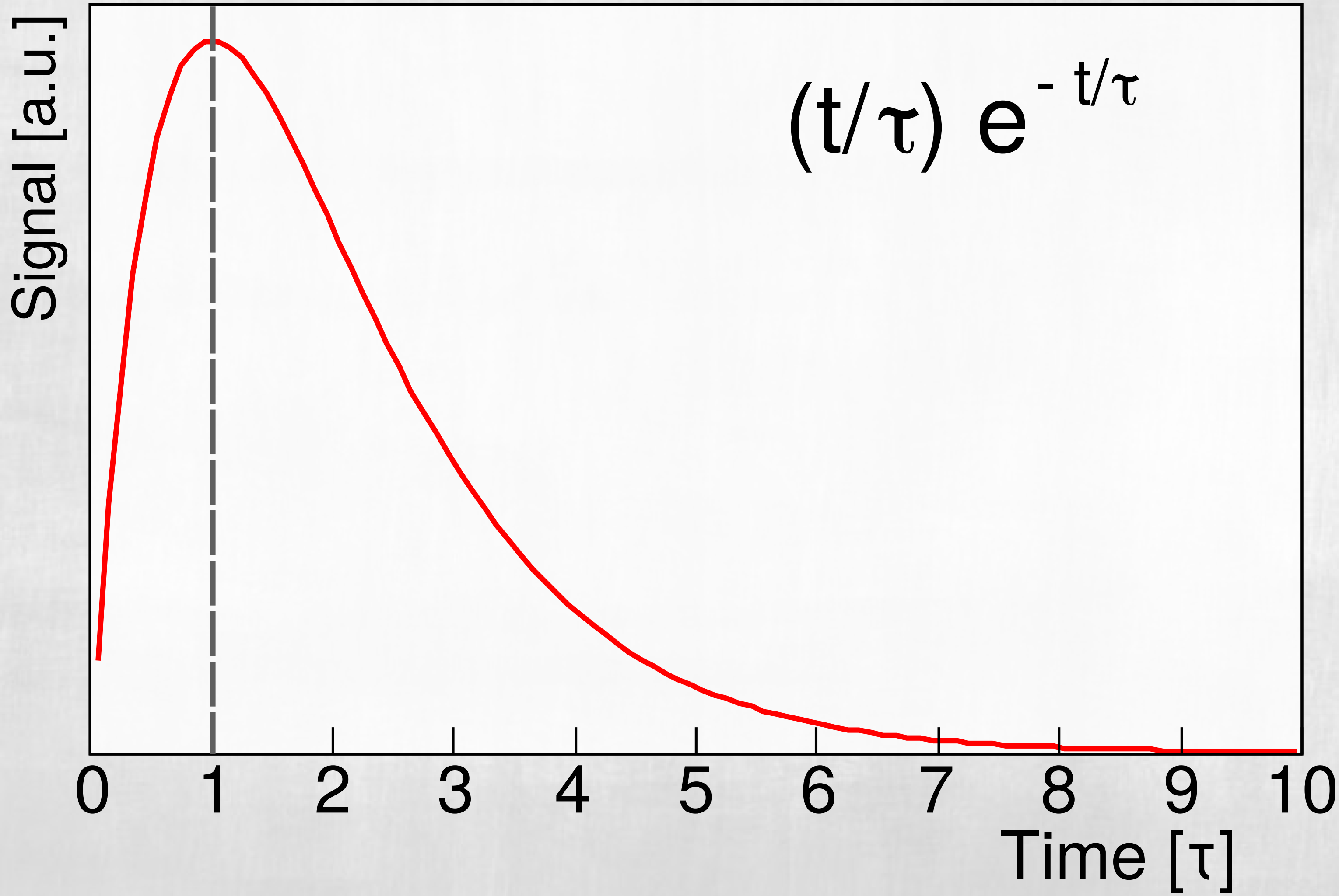
$$\mathcal{L}\left(\vartheta\left(t\right)\right) = \theta(s) = \frac{1}{s}$$

$$\mathcal{L}^{-1}\left(\frac{\tau}{\left(1+\tau\, s\right)^2}\right) = \frac{t}{\tau}\, e^{-\frac{t}{\tau}}$$

τ Shaper >> T signal (not always true...)
τ Shaper ≈ BX (for colliders)

Front-end typical (analogue)

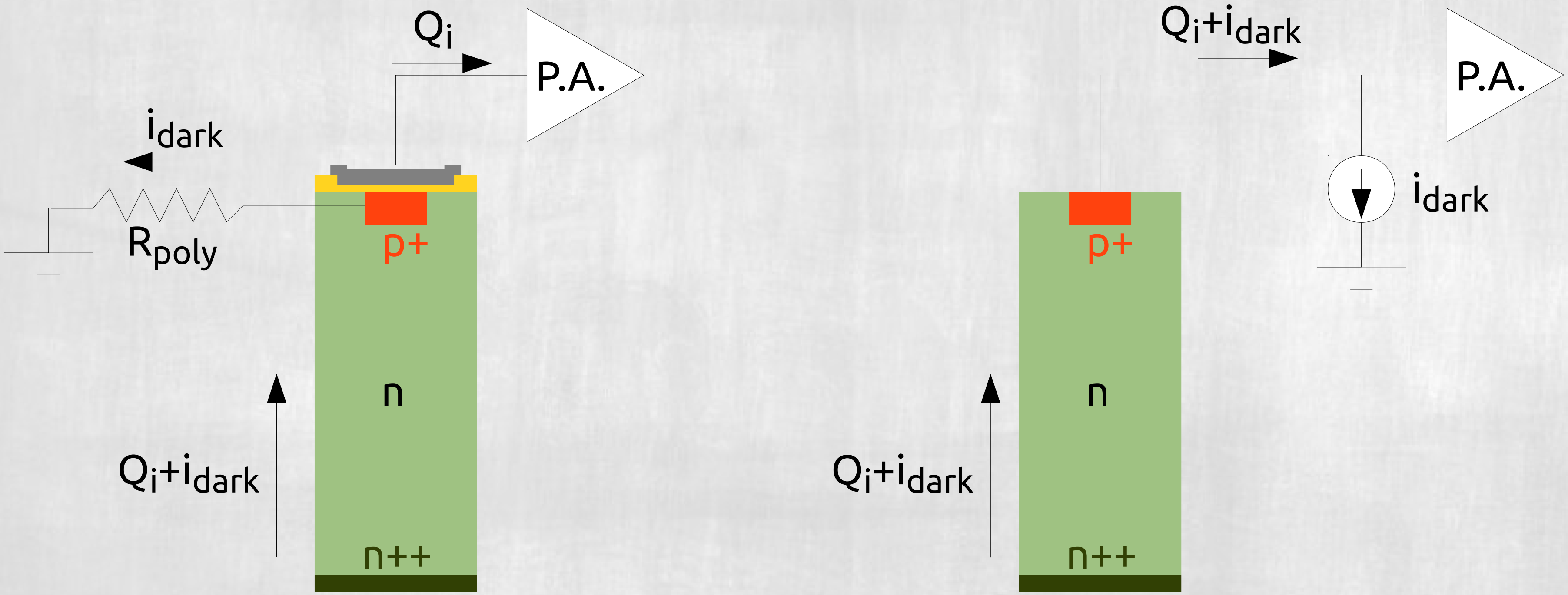
Time response of shaper to a preamp θ(t) signal



Front-end typical (analogue)

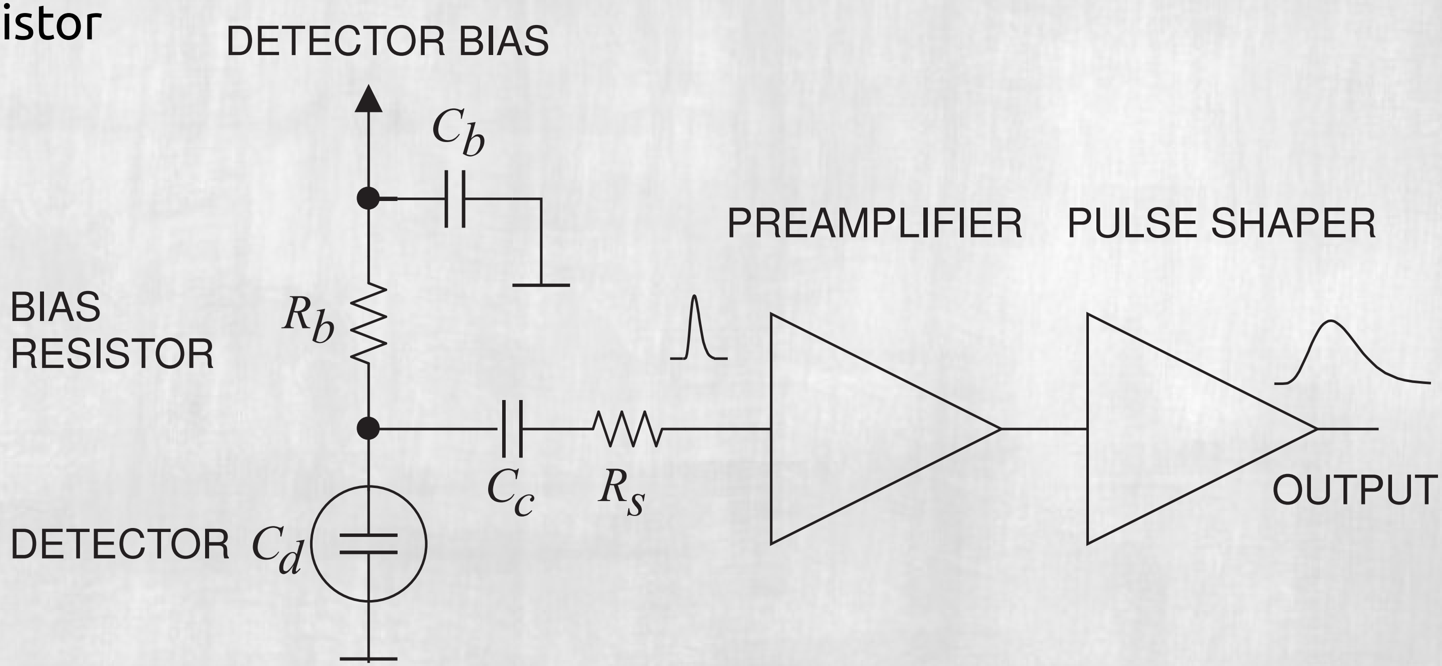
AC-coupled: requires additional sensor production steps

DC-coupled: additional signal processing to compensate dark current



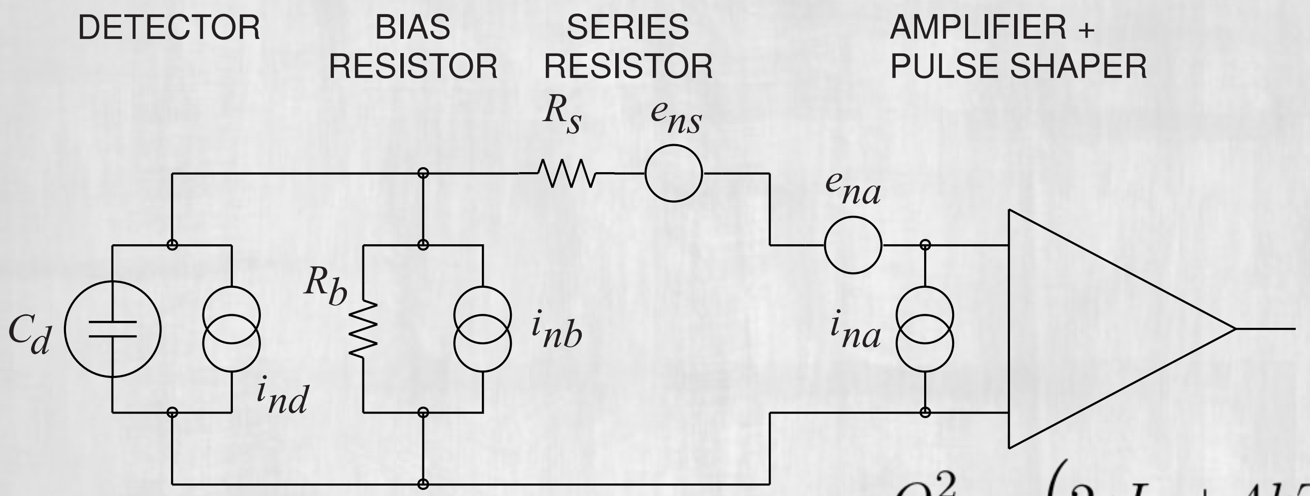
Front-end noise

- Noise typically measured as ENC (*equivalent noise charge)*
- Most important noise contributions:
  - Leakage current
  - Detector capacitance
  - Detector parallel resistor
  - Detector series resistor



http://journals.aps.org/prd/abstract/10.1103/PhysRevD.86.010001 (aka PDG)
For Italian readers: http://hep.fi.infn.it/POGGI/rum7.pdf

Front-end noise



$$Q_n^2 = \left(2eI_d + 4kT/R_b + i_{na}^2\right)F_iT_S$$
$$+ \left(4kTR_s + e_{na}^2\right)F_vC_d^2/T_S + F_{vf}A_fC_d^2$$

Q_n noise [input signal equivalent]
T_s = τ = shaping time can be optimized to minimise noise
I_d detector leakage current
T temperature
C_d input capacitance (i.e. strip)

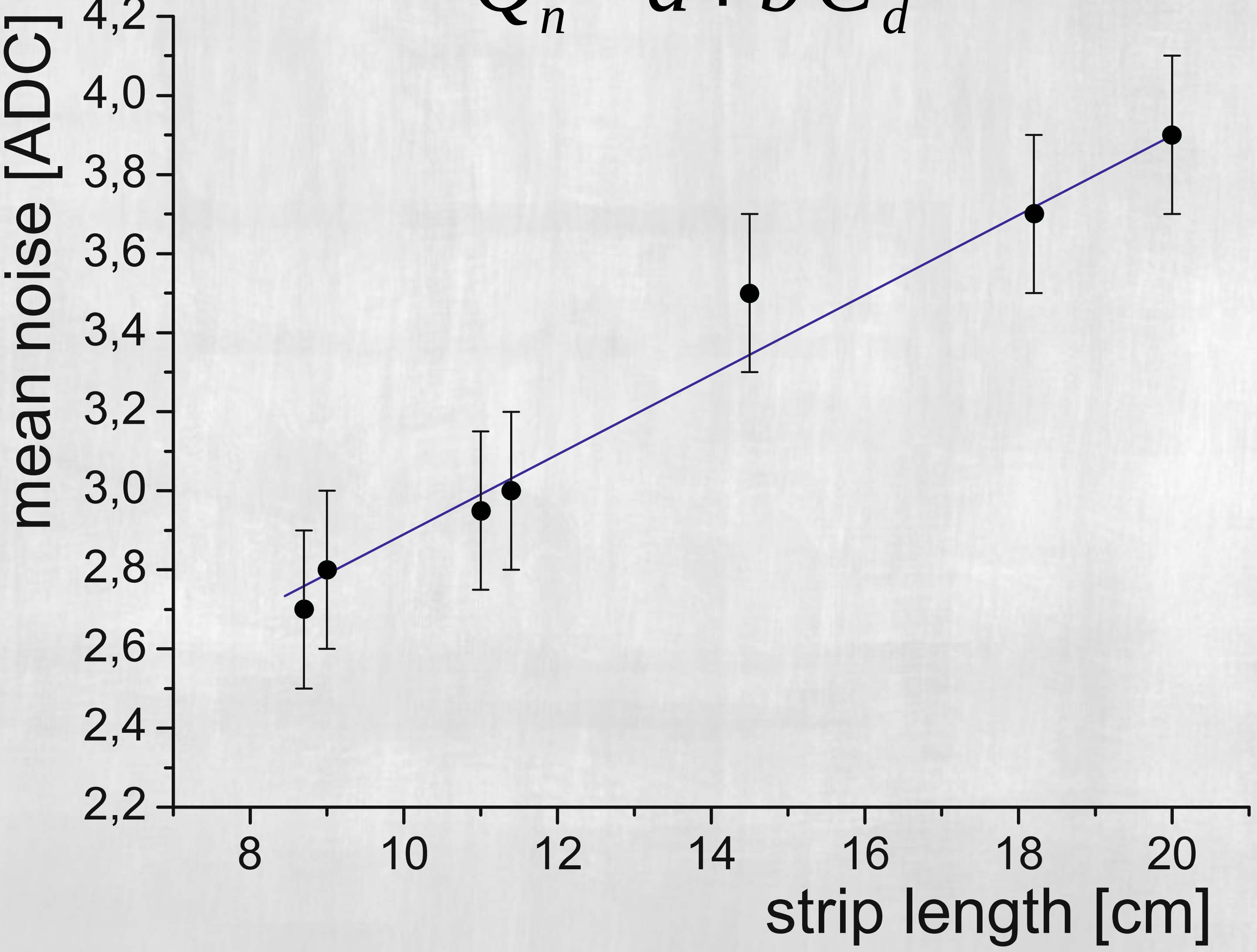
Once noise sources and T_S fixed

$$Q_n^2 = k_0^2 + (k_1 C_d)^2 + (k_2 I_d)^2$$
$$Q_n \simeq a + b\,C_d$$

http://journals.aps.org/prd/abstract/10.1103/PhysRevD.86.010001 (aka PDG)
For Italian readers: http://hep.fi.infn.it/POGGI/rum7.pdf

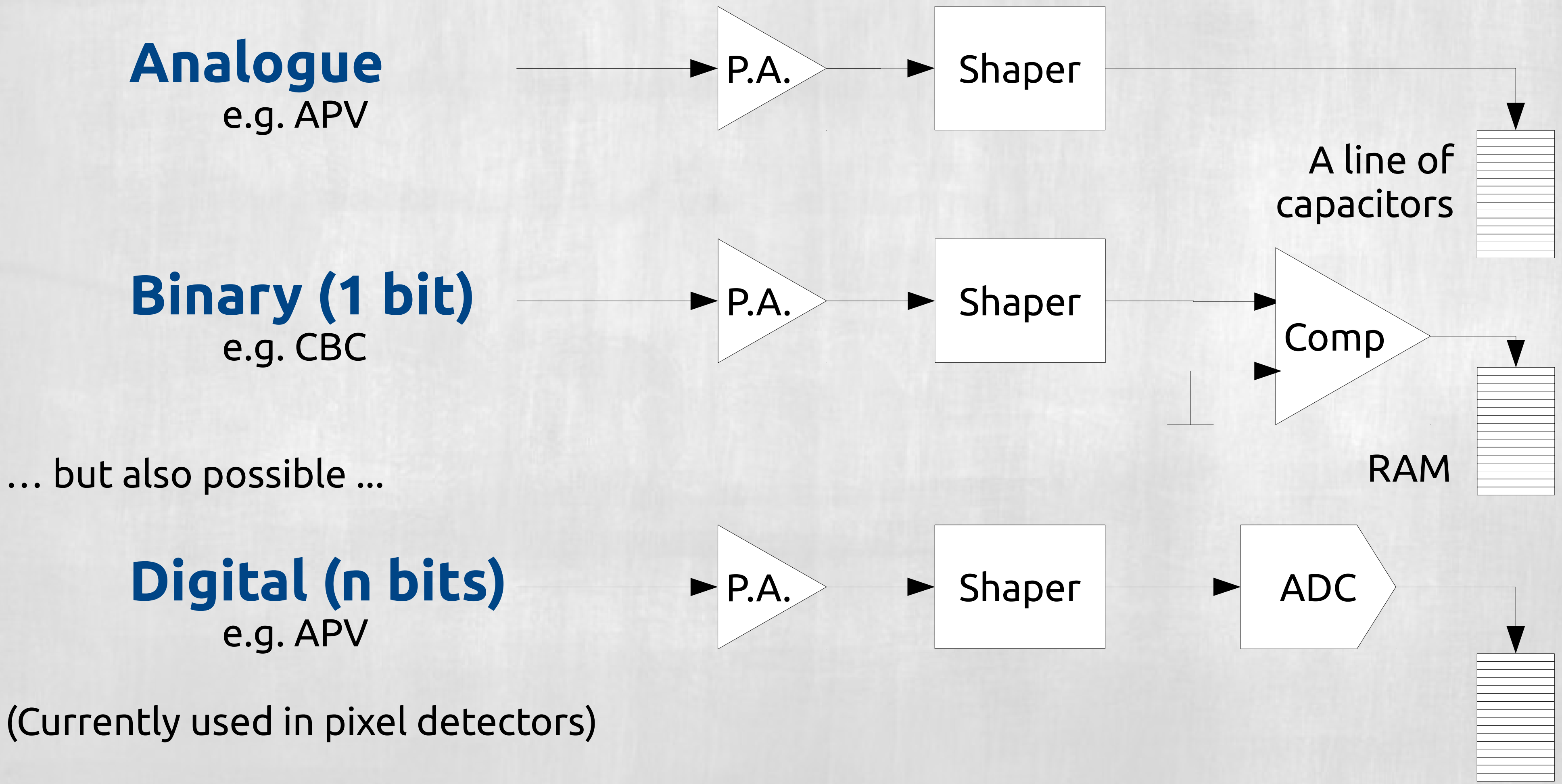
Front-end noise (CMS example)

$$Q_n \simeq a + b\,C_d$$

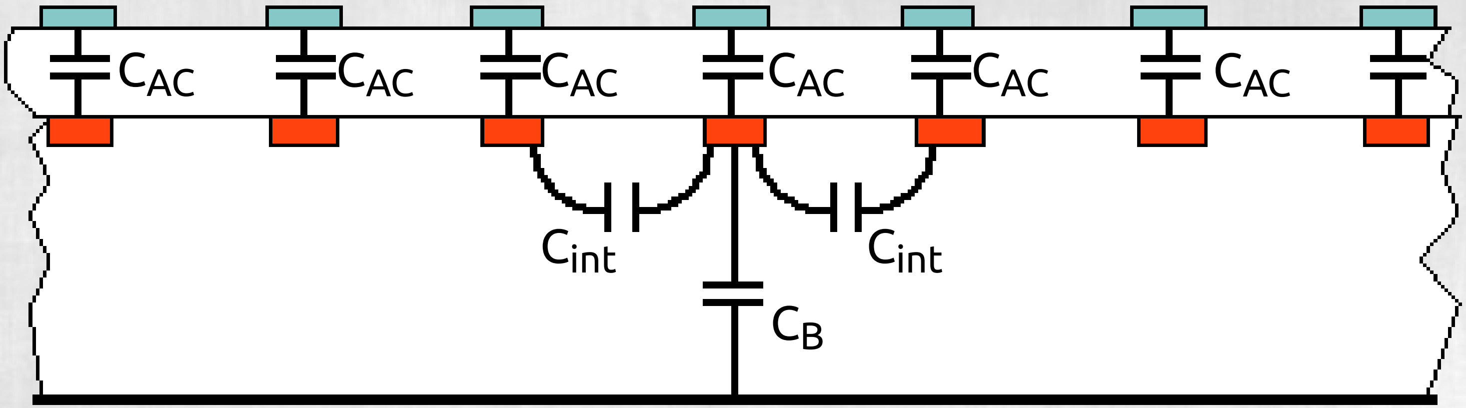


Front-end signal output

- Not all data can be shipped:
- Wait for external trigger: pipeline needed



Capacitances

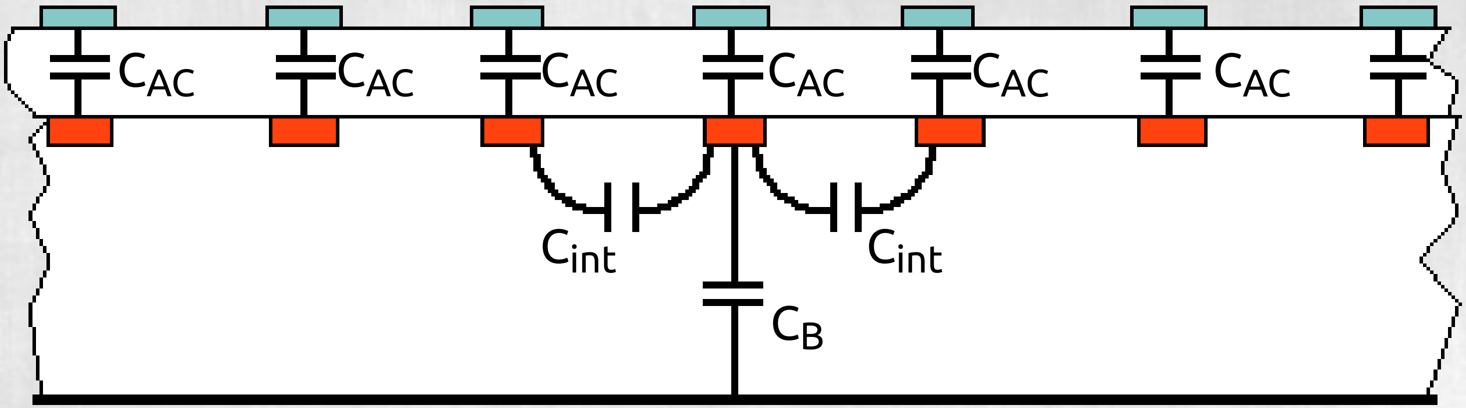


Main capacitances in strip sensors

- C_{AC}: coupling capacitance
- C_{int}: inter-strip capacitance (also 2nd neighbours)
  Grows with shrinking pitch
- C_B: back-plane capacitance
  Grows with thinning sensors

Note: C_{AC} in series with others...

Front-end typical (analogue)



Side note: noise anti-correlation between adjacent strips...

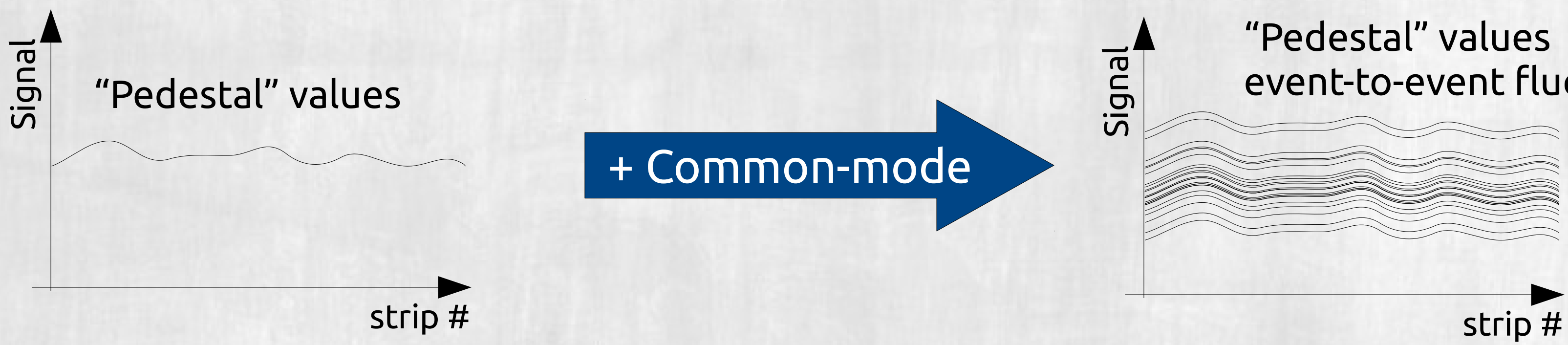
...why?

Check your answer here...:
Correlated Noise In Silicon Strip Detector Readout.
G. Lutz MPI-PAE-EXP-EL-173, Feb 1987
Published in NIM A309: 545-551,1991

Front-end typical (analogue)

More sizeable effect positive strip-to-strip signal correlation, a.k.a. Common-Mode-Noise, due to

- RF signal picked-up by the front-ends through the strips
- Voltage fluctuations from HV bias line appropriately not filtered
- Voltage fluctuations from power supplies appropriately not filtered
- Internal fluctuation of Vref (e.g. due to the activity of the front-end logic)
- …



Effect seen in analogue data

- Signal baseline fluctuation
  (remedy available: subtract signal median) WHY median? :-)

Effect seen in digital data

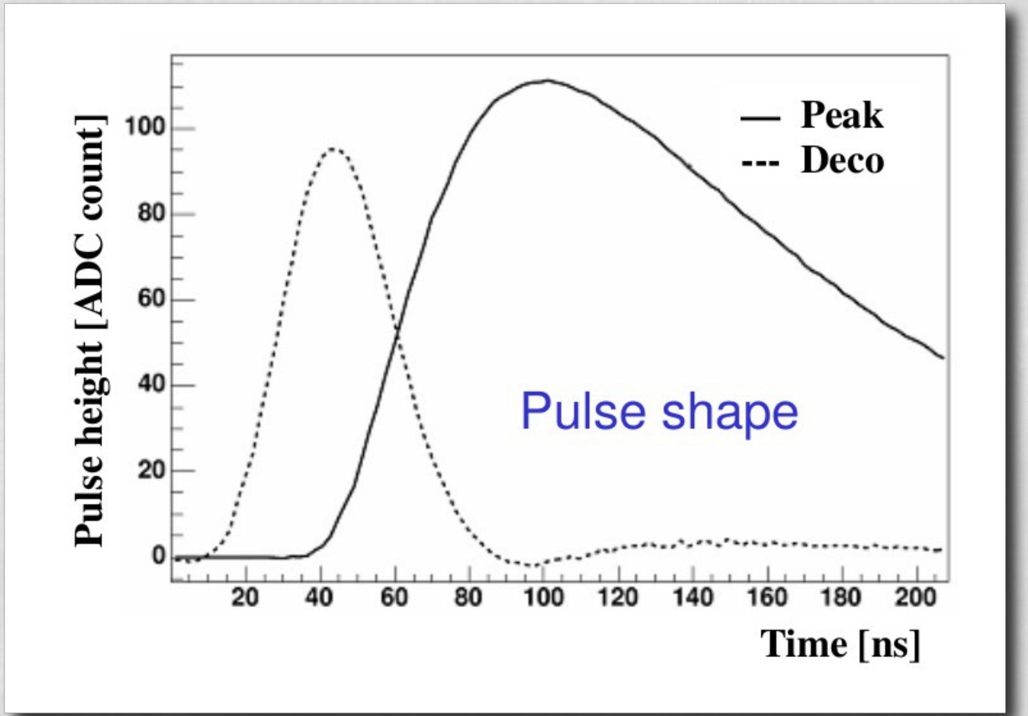
- Correlation between hit probability of different strips
- Broad distribution in hit counting (extreme: some events all fire, some other none)

L. Feld et al, *Measurement of common mode noise in binary read-out systems*, NIM A487 (2002) 557-564

Front-end signal output

If $\tau > T_{BX}$, then need to identify/remove pile-up

- To separate hits from previous BX analogue signal can be treated to have an effective faster shaping time
- Input (**peak** mode) signal must be correctly shaped as (CR)(RC) ⇒ $(t/\tau)\exp[-t/\tau]$
- Appropriate linear combination of three samples ⇒ **deconvolution** mode
- Currently used in CMS's front-ends (APV)



S. Gadomski et al,
The deconvolution method of fast pulse shaping at hadron colliers,
NIM A320 (1992) 217-227

Outline of the lesson

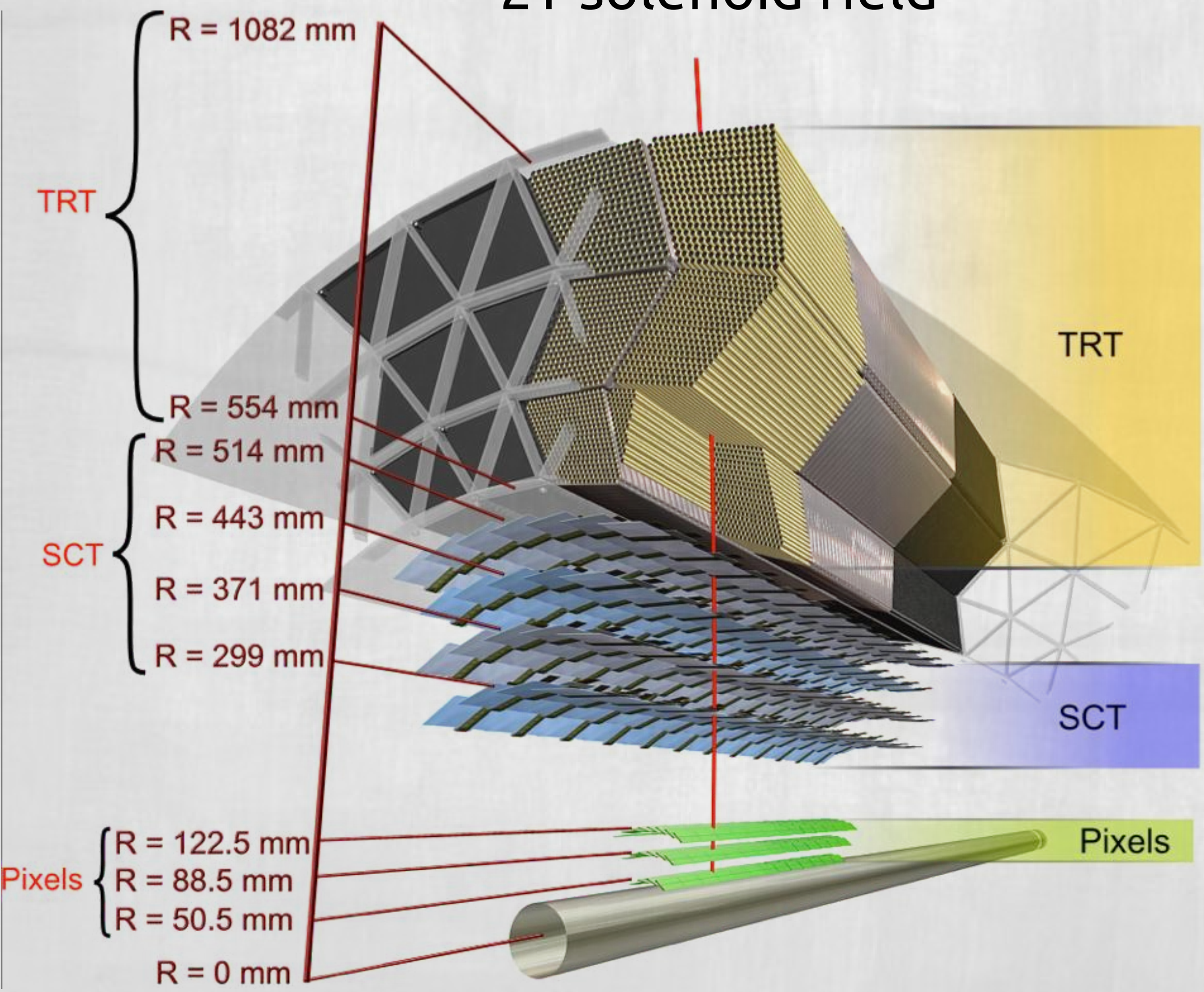
- ~~Silicon strip tracking detectors~~
- ~~Front-end signal processing~~
- ➡ Examples of detector design
- Real-time tracking

Current silicon strip front-end chips

ATLAS	CMS
ABCD chip	APV25 chip
250 nm technology	250 nm technology
AC coupled	AC coupled
128 channels	128 channels
Binary zero suppressed	Analogue raw
Positive signals (p-type strips)	Both input polarities
25 ns peaking time	50 ns peaking time [+ deco]
Token ring readout	2-chip time MUX
ENC < 1500 e^-	246 e^- + C_D×36 e^-/pF < 1000 e^-

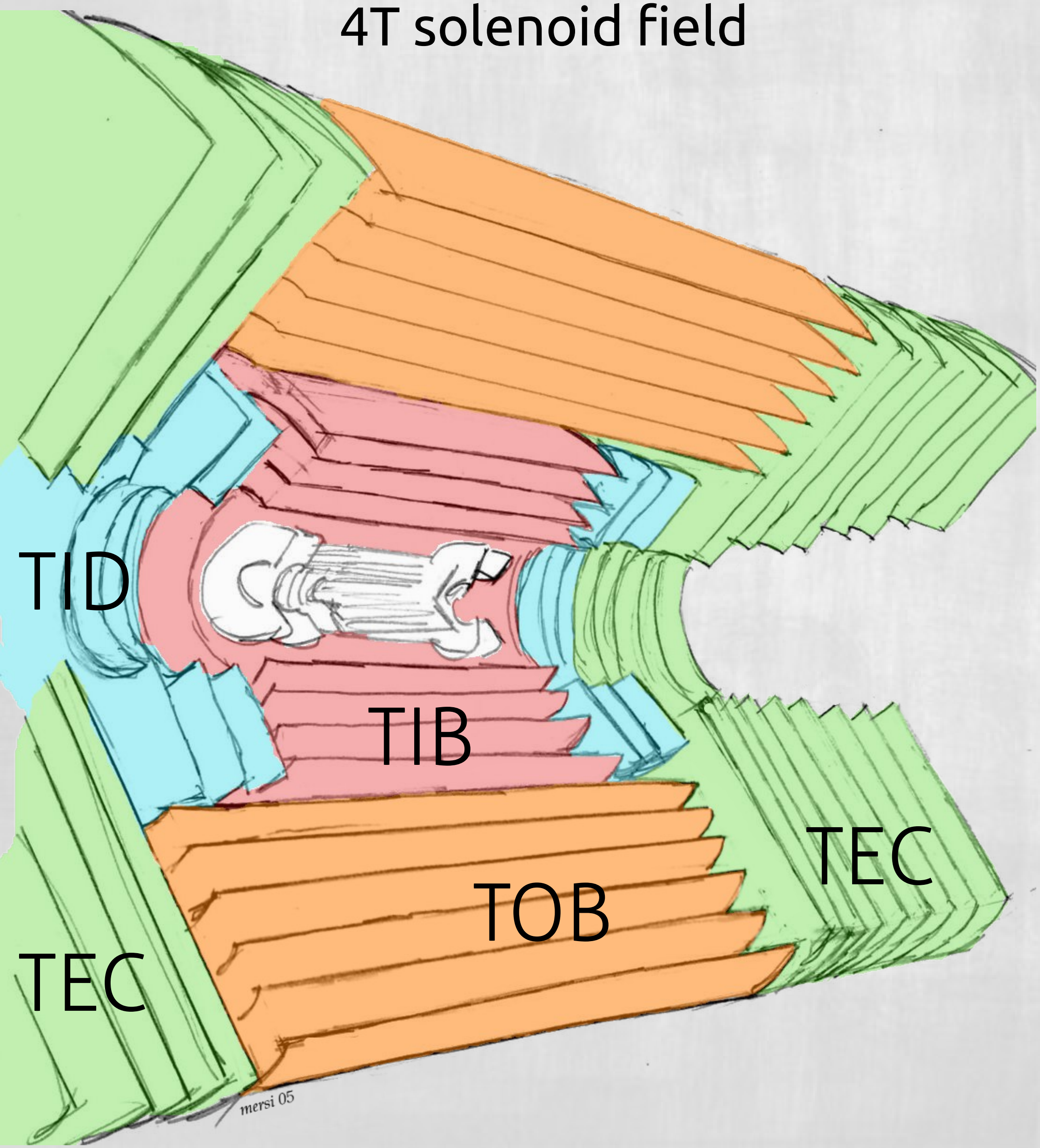
Current ATLAS tracker

2T solenoid field



	Pixel	SCT	TRT
barrel layers	3	4	72
end-cap layers	2*3	2*9	2*160
# hits / track	3	8	~30
element size [μm]	50x400	80	4 mm
resolution [μm]	10x115	17x580	130
channels	$8*10^7$	$6.3*10^6$	$3.5*10^5$

Current CMS tracker



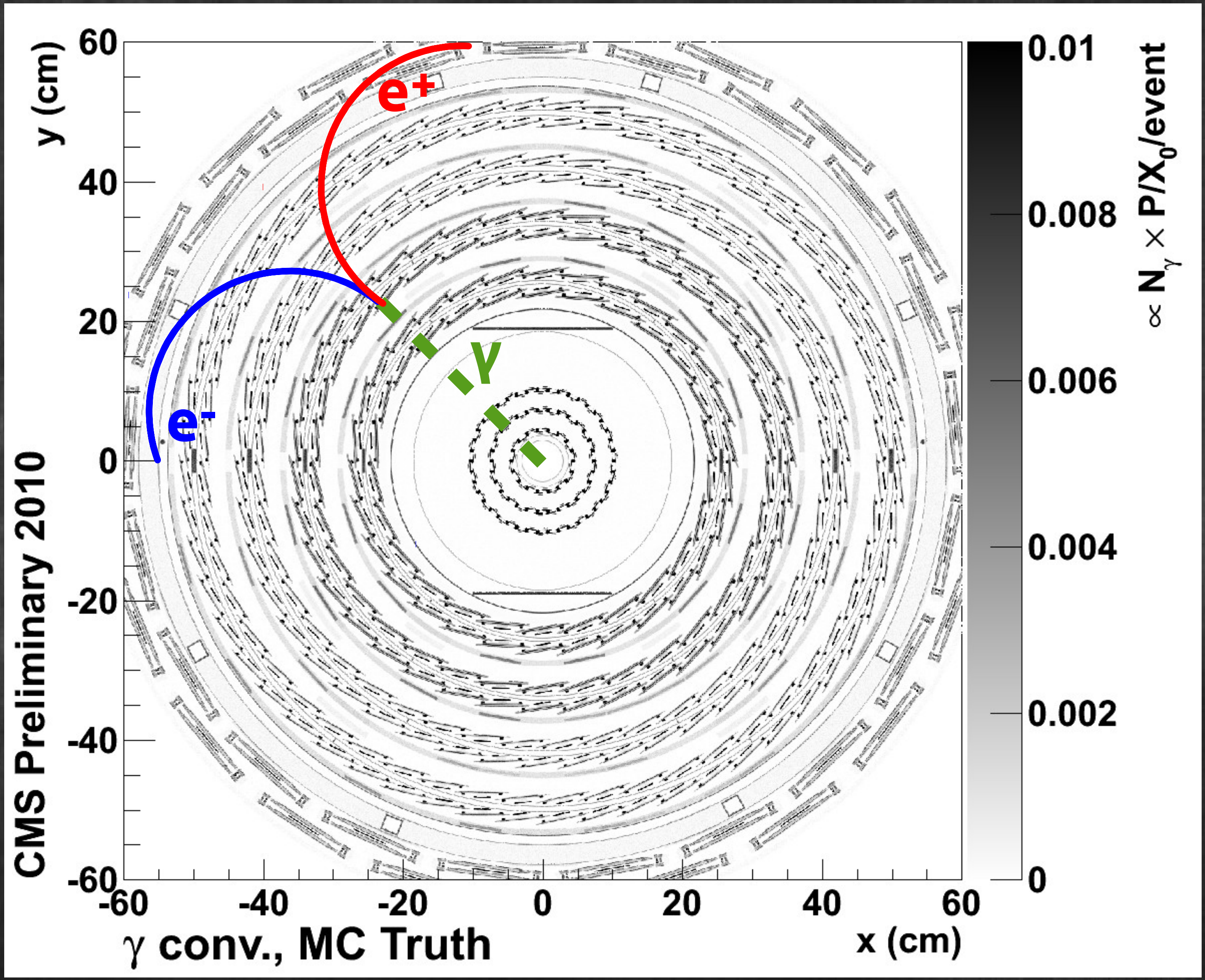
Volume	23 m^3
Active area	200 m^2
Modules	15'148
Front-end chips	72'784
Read-out channels	9'316'352
Bonds	24'000'000
Optical channels	36'392

Intermezzo on material budget

Material photon tomography

What you know

Gamma conversion
(pair production)

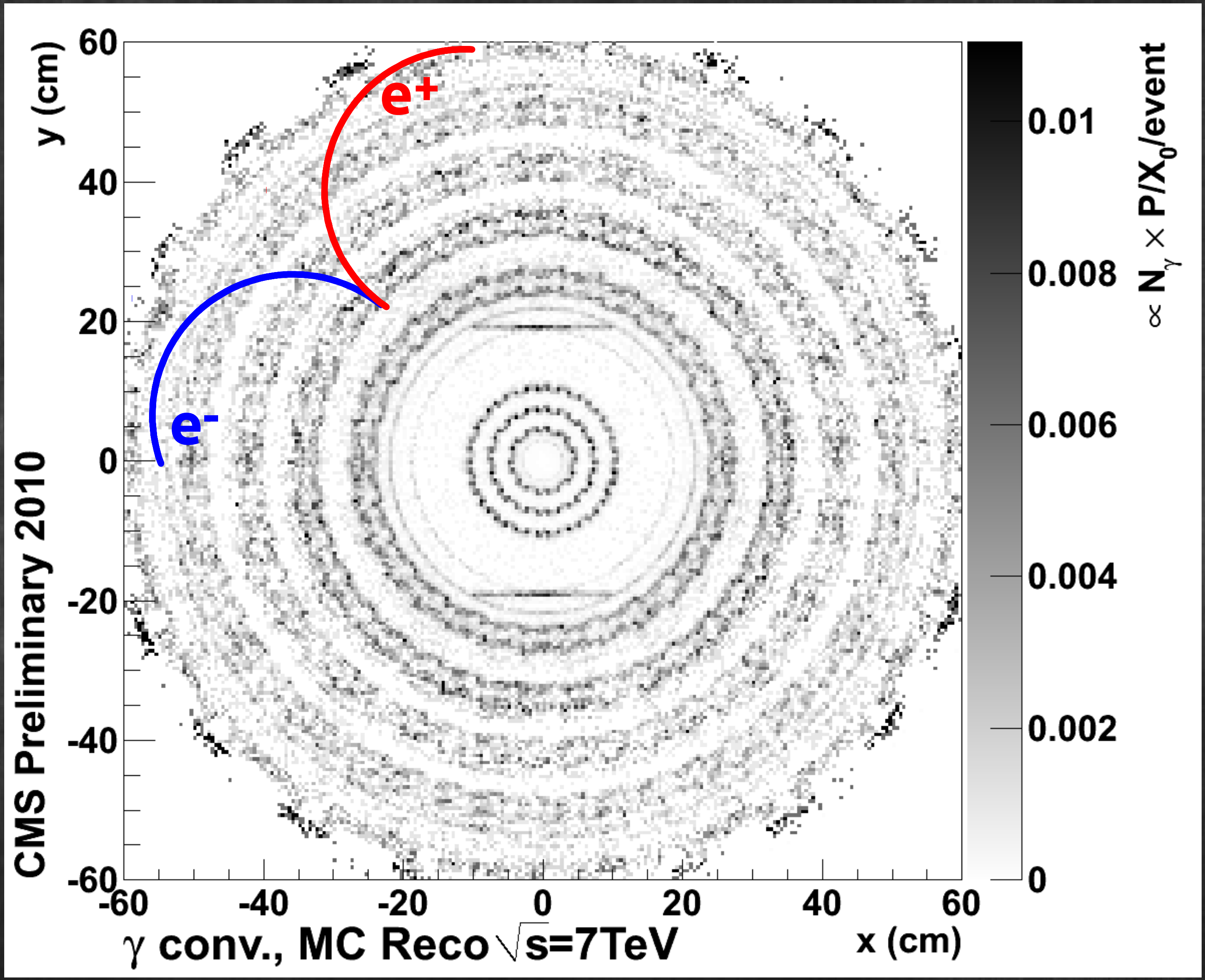


CMS-PAS-TRK-10-003

Material photon tomography

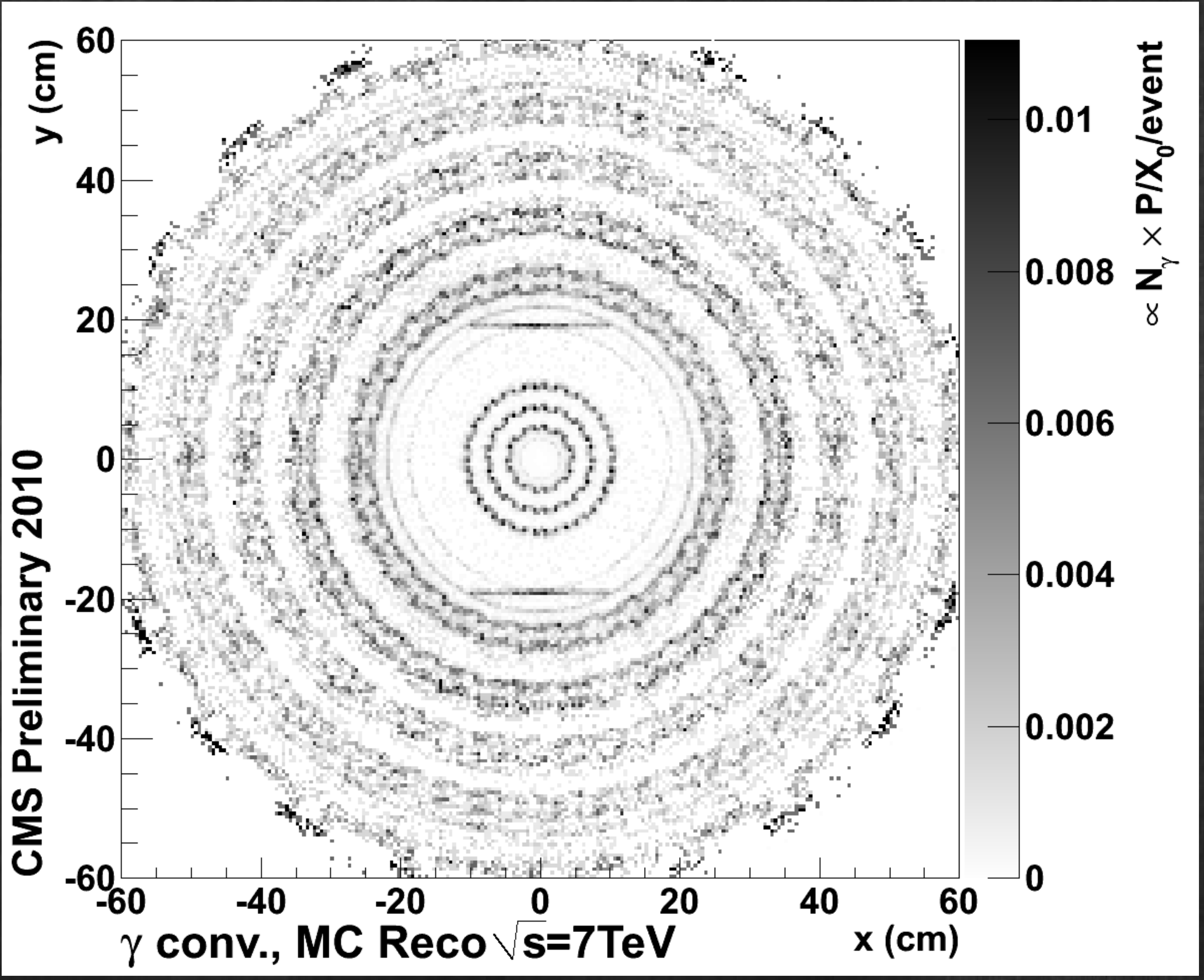
What you expect to see (MC)

Using γ conversion to reconstruct material position



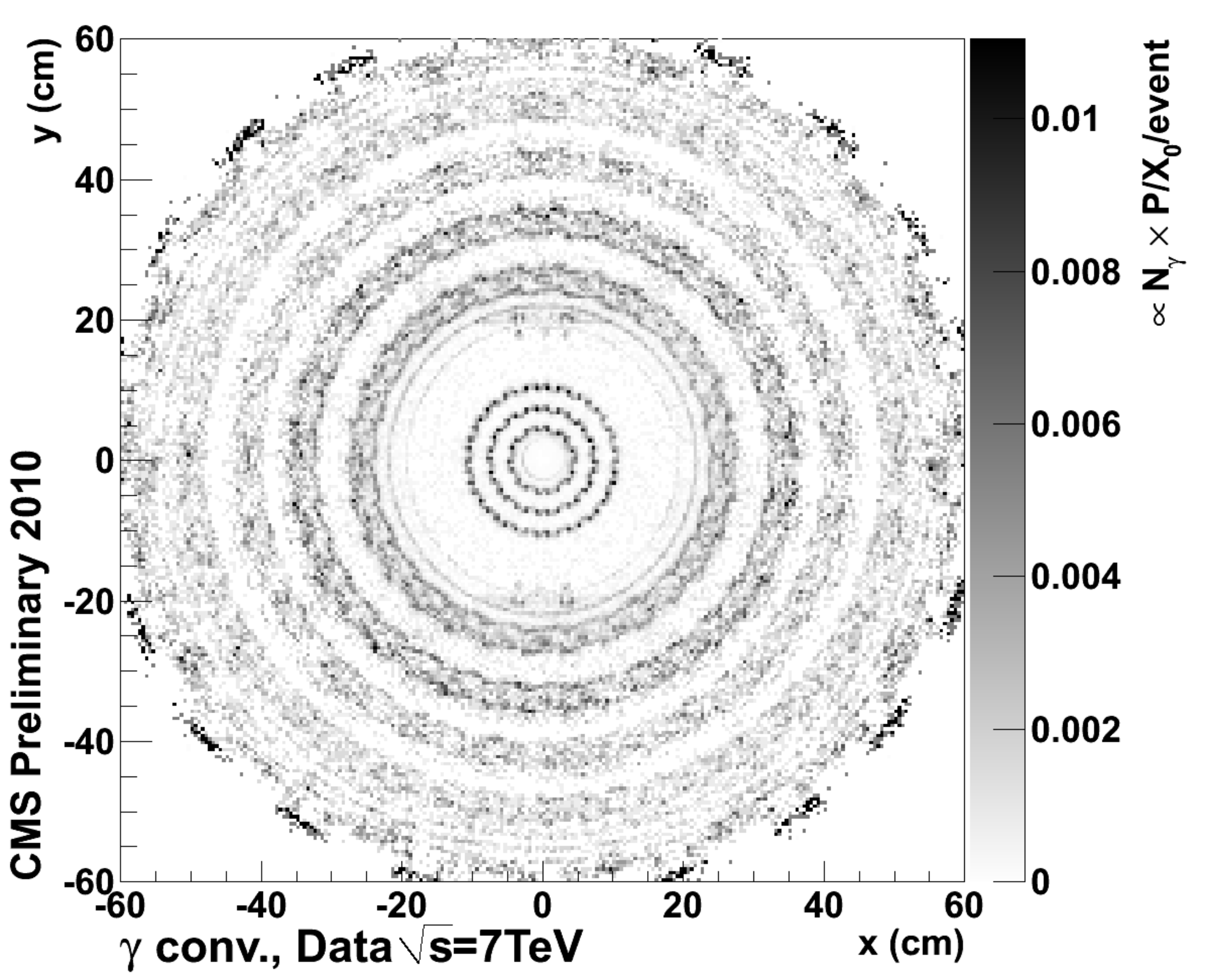
Material photon tomography

What you expect to see (MC)

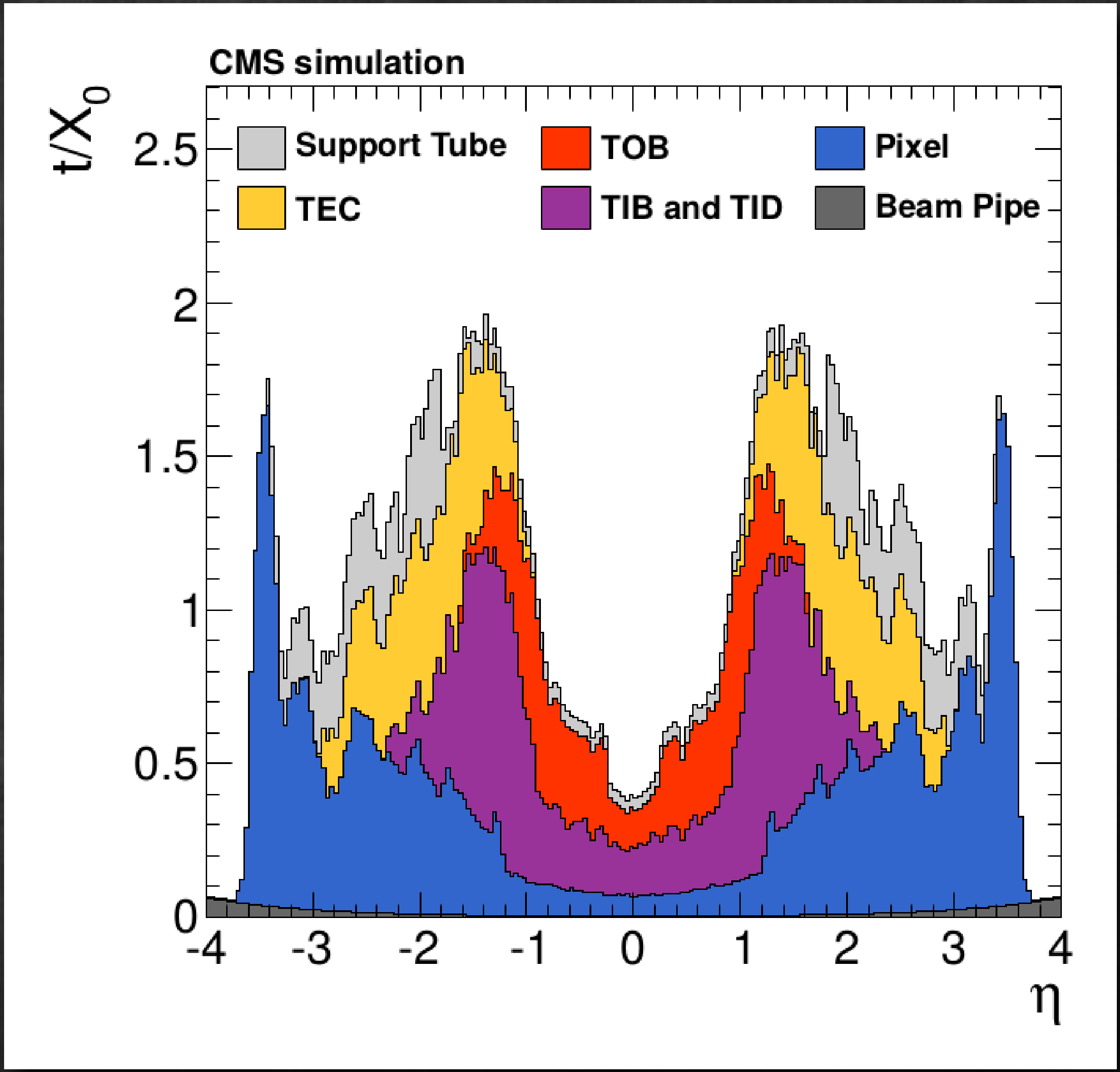


Material photon tomography

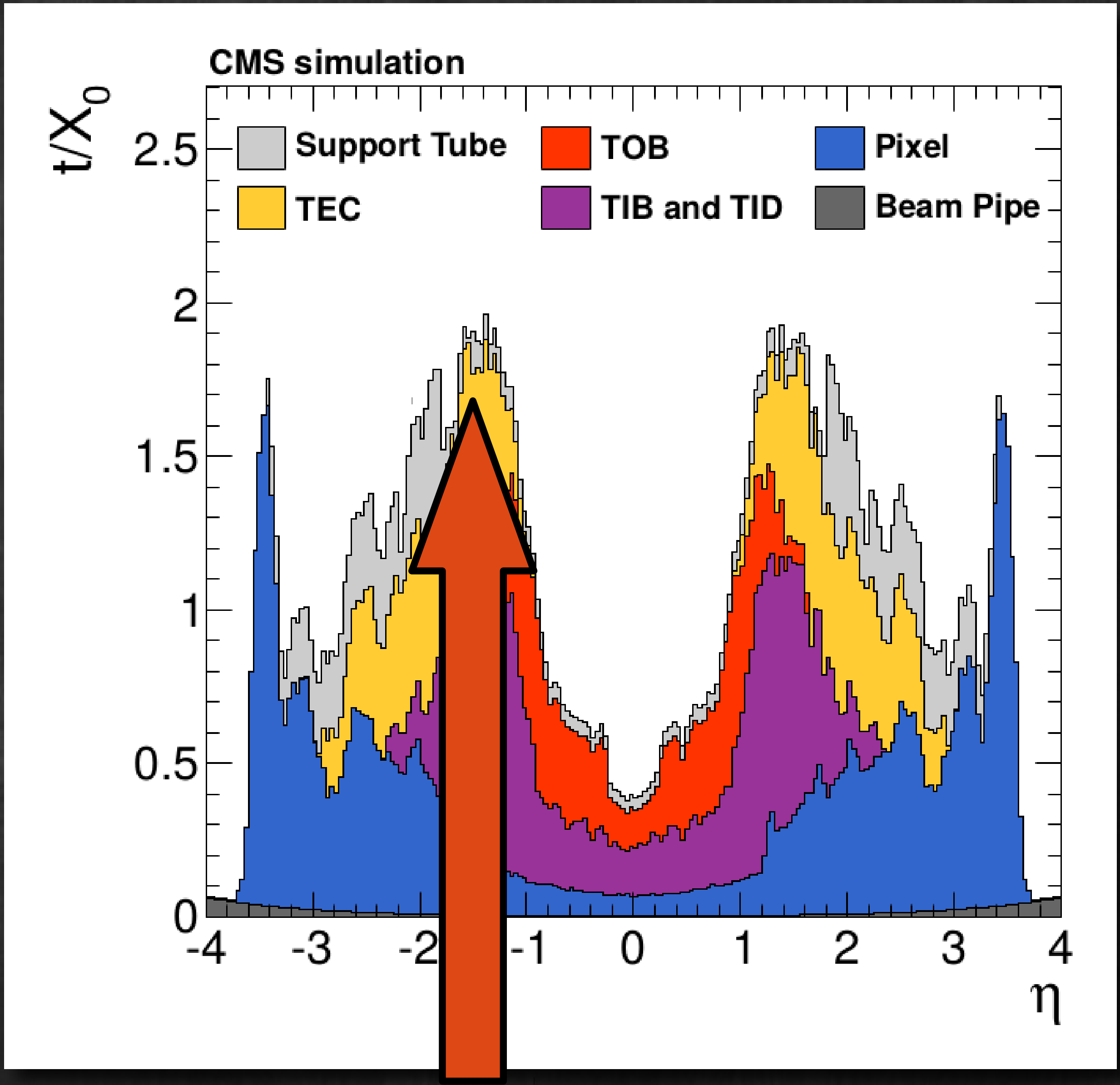
What you see (real)



Material matters...



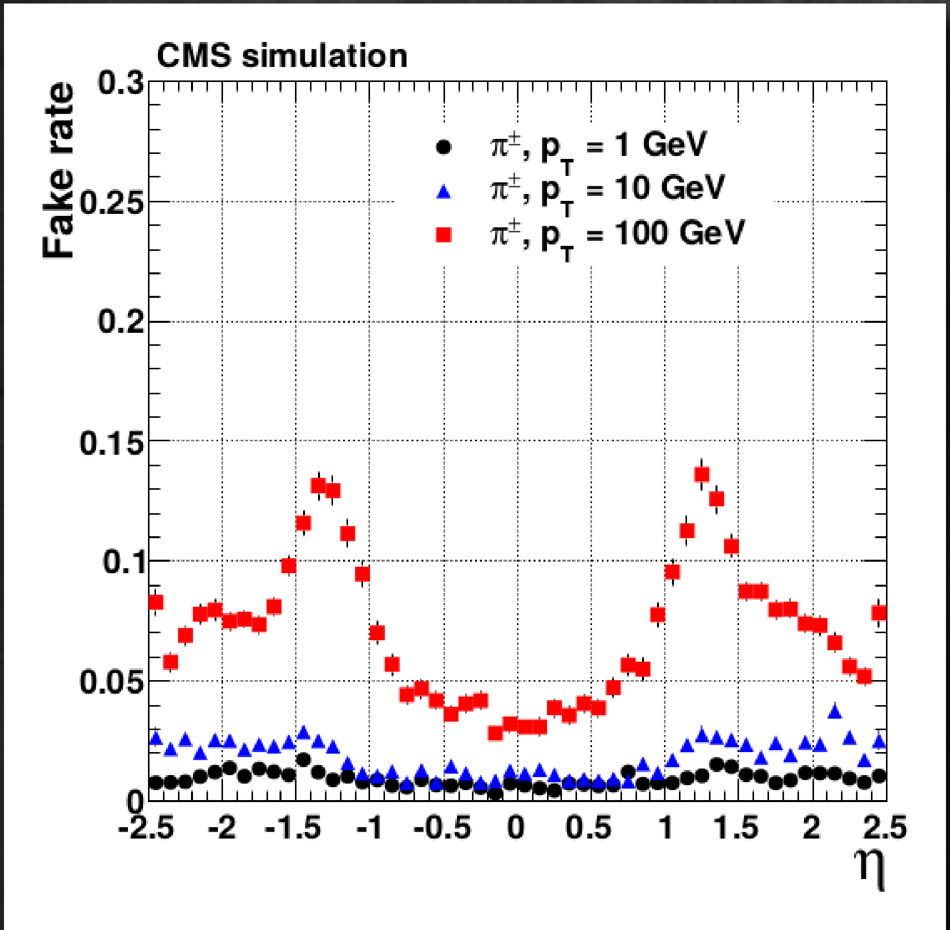
Material matters...

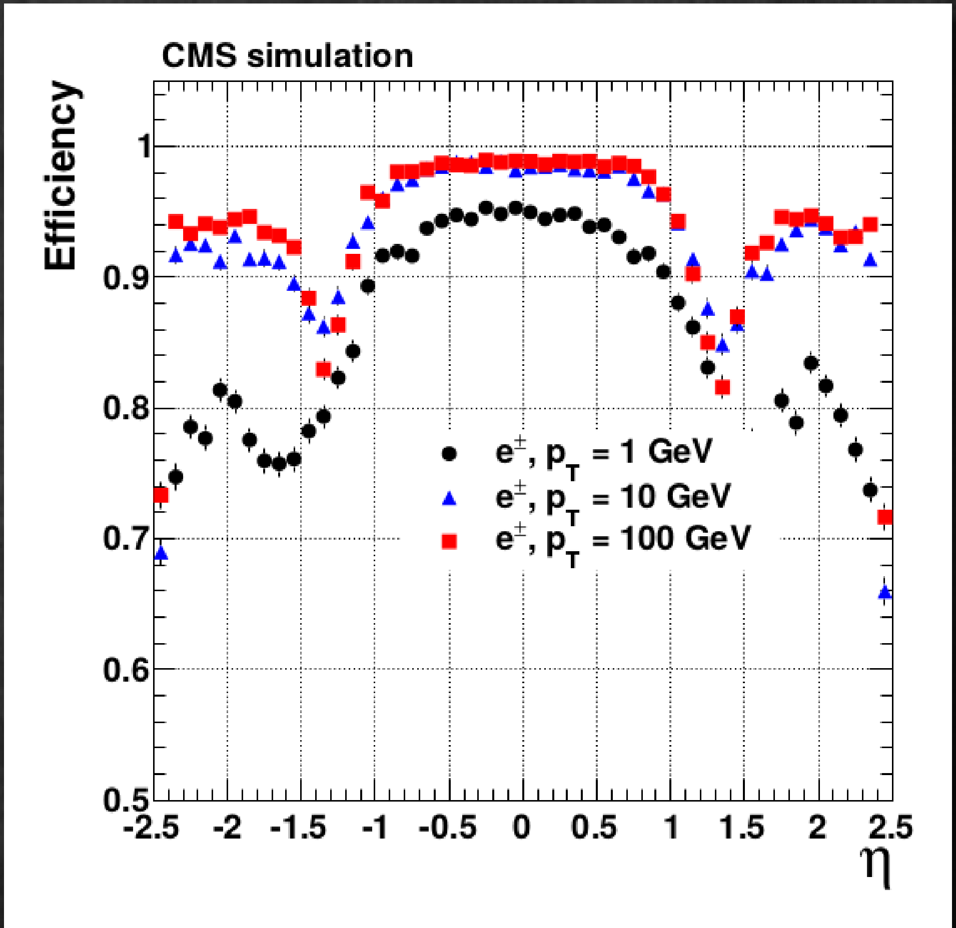


Sizeable material amount in region $1<|\eta|<2$

Material matters...

π and e tracking degraded in that region





Implications for future trackers

- (Fast signal + more FE processing) = power

  Power → cooling → material

  Power → cables → material

- Low(er) power
  - In the front-end moving from current 250 nm → 65 nm for ex.
- Novel cooling techniques: bi-phase CO_2 cooling
- Novel distribution schemes
  - DC/DC
  - Serial powering

End of intermezzo on material budget

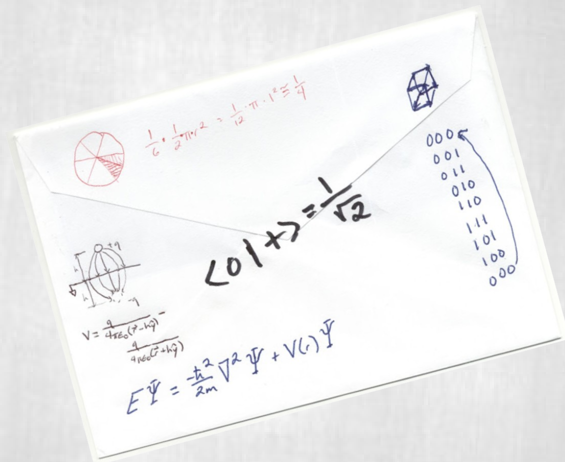
Luminosity in LHC

LHC nominal luminosity

$\mathcal{L} = 1 \times 10^{34}\ \mathrm{cm^{-2}\ s^{-1}}$

BX rate = 40 MHz

$10^{30}\ \mathrm{cm^{-2}\ s^{-1}} = 1\ \mathrm{Hz/\mu b}$
$10^{30}\ \mathrm{cm^{-2}\ s^{-1}} = 1\ \mathrm{kHz/mb}$
$10^{30}\ \mathrm{cm^{-2}\ s^{-1}} = 1\ \mathrm{MHz/b}$
$10^{33}\ \mathrm{cm^{-2}\ s^{-1}} = 1\ \mathrm{MHz/mb}$



$\mathcal{L} = 10\ \mathrm{MHz/mb}$ $\sigma_{PP} \approx 80\ \mathrm{mb}$

$$10\,\frac{MHz}{mb} \times 80\,mb \times \frac{1}{40\,MHz} = ?$$

event rate **BX rate**

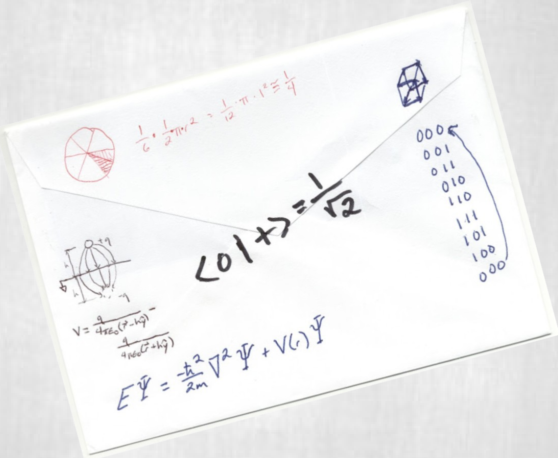
Luminosity and pile-up in LHC

LHC nominal luminosity

$\mathcal{L}=1\times10^{34}\ cm^{-2}\ s^{-1}$

BX rate = 40 MHz

$10^{30}\ cm^{-2}\ s^{-1}=1\ Hz/\mu b$
$10^{30}\ cm^{-2}\ s^{-1}=1\ kHz/mb$
$10^{30}\ cm^{-2}\ s^{-1}=1\ MHz/b$
$10^{33}\ cm^{-2}\ s^{-1}=1\ MHz/mb$

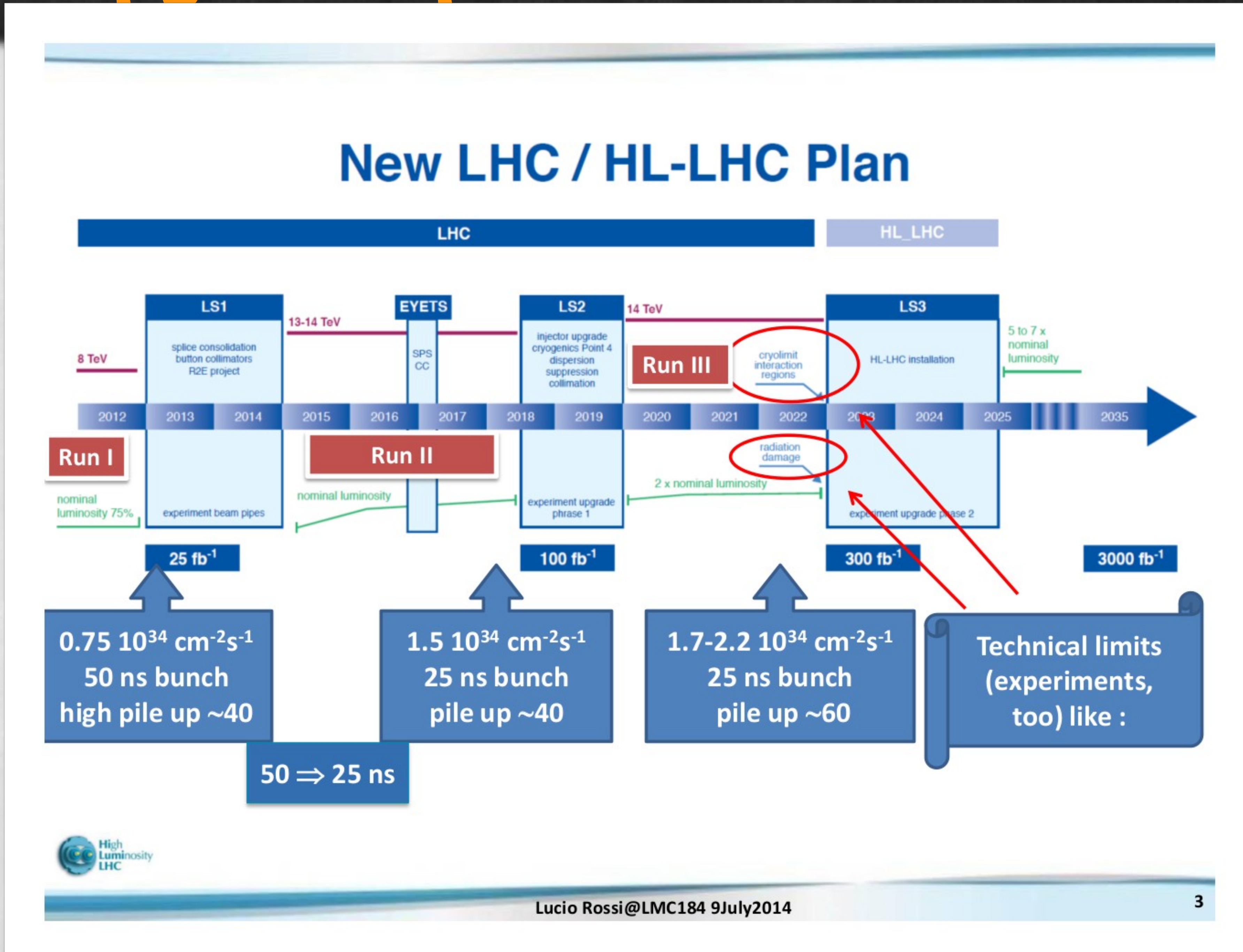


$\mathcal{L}=10\ MHz/mb$ $\sigma_{PP}\approx80\ mb$

$$10\,\frac{MHz}{mb}\times 80\,mb\times\frac{1}{40\,MHz}\simeq 20$$

Average number of pile-up events: 20

LHC Upgrades plan



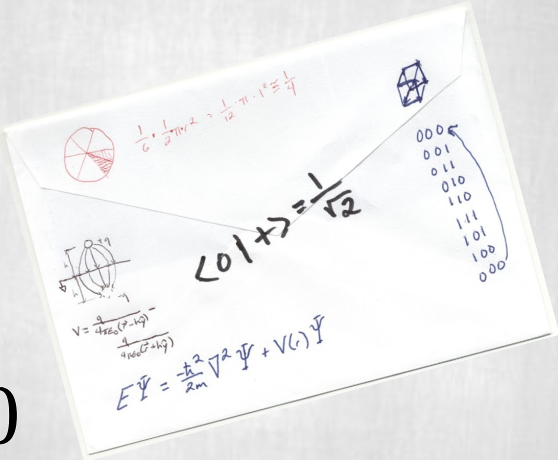
Luminosity and pile-up in HL-LHC

HL-LHC peak luminosity

$\mathcal{L}=7\times10^{34}\ \mathrm{cm}^{-2}\ \mathrm{s}^{-1}$

BX rate (eff) = 40 MHz

$10^{30}\ \mathrm{cm}^{-2}\ \mathrm{s}^{-1}=1\ \mathrm{Hz}/\mu\mathrm{b}$
$10^{30}\ \mathrm{cm}^{-2}\ \mathrm{s}^{-1}=1\ \mathrm{kHz/mb}$
$10^{30}\ \mathrm{cm}^{-2}\ \mathrm{s}^{-1}=1\ \mathrm{MHz/b}$
$10^{33}\ \mathrm{cm}^{-2}\ \mathrm{s}^{-1}=1\ \mathrm{MHz/mb}$



$\mathcal{L}=70\ \mathrm{MHz/mb}$ $\sigma_{PP}\approx 80\ \mathrm{mb}$

$$70\,\frac{MHz}{mb}\times 80\,mb\times\frac{1}{40\,MHz}\simeq 140$$

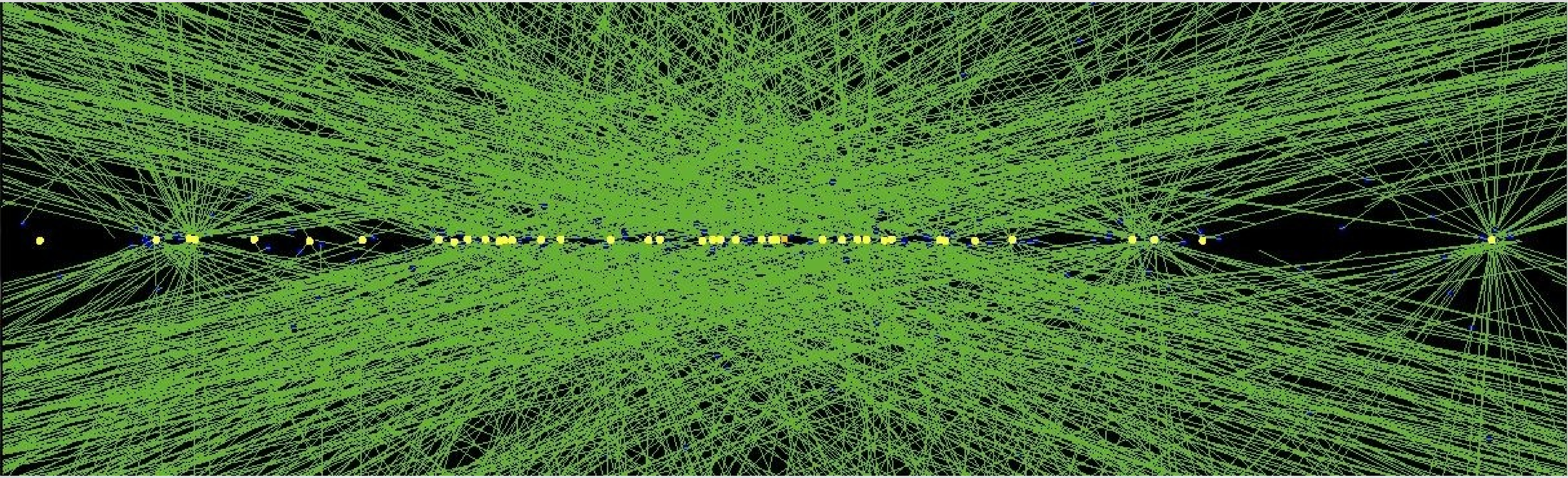
Average number of pile-up events: 140

Latest projections (for reference)

Lucio Rossi@LMC184 9July2014

Parameter	Nominal LHC (design report)	HL-LHC 25ns (standard)	HL-LHC 25 ns (BCMS)	HL-LHC 50ns
Beam energy in collision [TeV]	7	**7**	7	7
N_b	1.15E+11	**2.2E+11**	2.2E11	3.5E+11
n_b	2808	**2748**[1]	2604	1404
Number of collisions at IP1 and IP5	2808	**2736**	2592	1404
N_{tot}	3.2E+14	**6.0E+14**	5.7E+14	4.9E+14
beam current [A]	0.58	**1.09**	1.03	0.89
x-ing angle [μrad]	285	**590**	590	590
beam separation [σ]	9.4	**12.5**	12.5	11.4
β^{*} [m]	0.55	**0.15**	0.15	0.15
ε_{n} [μm]	3.75	**2.50**	2.50	3
ε_{L} [eVs]	2.50	**2.50**	2.50	2.50
r.m.s. energy spread	1.13E-04	**1.13E-04**	1.13E-04	1.13E-04
r.m.s. bunch length [m]	7.55E-02	**7.55E-02**	7.55E-02	7.55E-02
IBS horizontal [h]	80 -> 106	**18.5**	18.5	17.2
IBS longitudinal [h]	61 -> 60	**20.4**	20.4	16.1
Piwinski angle	0.65	**3.14**	3.14	2.87
Geometric loss factor R0 without crab-cavity	0.836	**0.305**	0.305	0.331
Geometric loss factor R1 with crab-cavity	(0.981)	**0.829**	**0.829**	**0.838**
beam-beam / IP without Crab Cavity	3.1E-03	**3.3E-03**	3.3E-03	4.7E-03
beam-beam / IP with Crab cavity	3.8E-03	**1.1E-02**	1.1E-02	1.4E-02
Peak Luminosity without crab-cavity [$cm^{-2} s^{-1}$]	1.00E+34	**7.18E+34**	6.80E+34	8.44E+34
Virtual Luminosity with crab-cavity: Lpeak*R1/R0 [$cm^{-2} s^{-1}$]	(1.18E+34)	**19.54E+34**	18.52E+34	21.38E+34
Events / crossing without levelling w/o crab-cavity	27	**198**	198	454
Levelled Luminosity [$cm^{-2} s^{-1}$]	-	**5.00E+34**	5.00E+34	2.50E+34
Events / crossing (with levelling and crab-cavities for HL-LHC)	27	**138**	146	135
Peak line density of pile up event [evt/mm] (max over stable beam)	0.21	**1.25**	1.31	1.20
Levelling time [h] (assuming no emittance growth)	-	**8.3**	7.6	18.0

140 pile-up

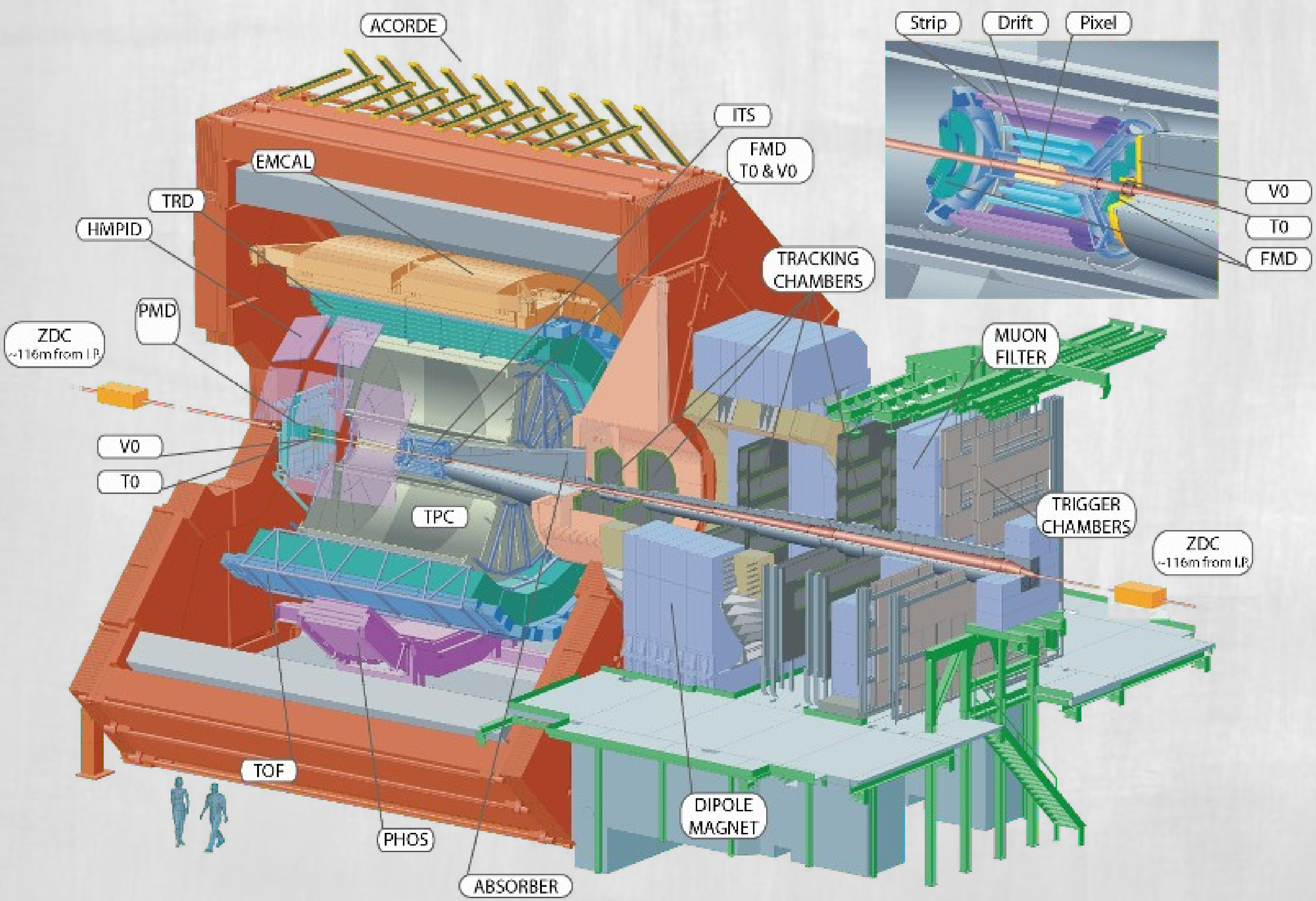


ALICE and LHCb upgrades

Since I will not talk about them, I briefly mention why:

ALICE and LHCb upgrades

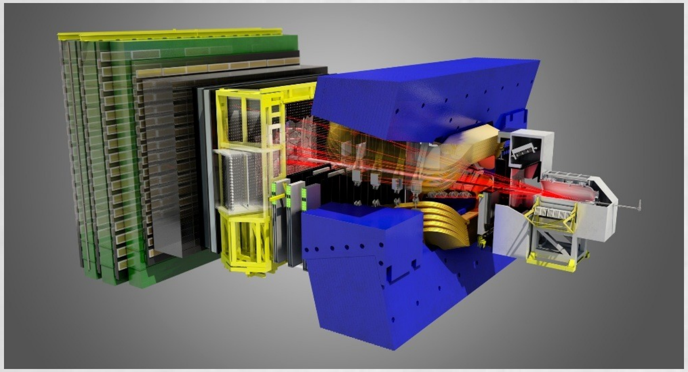
Silicon inner detector
Large TPC outside (great instrument for material budget, if rate ok!)



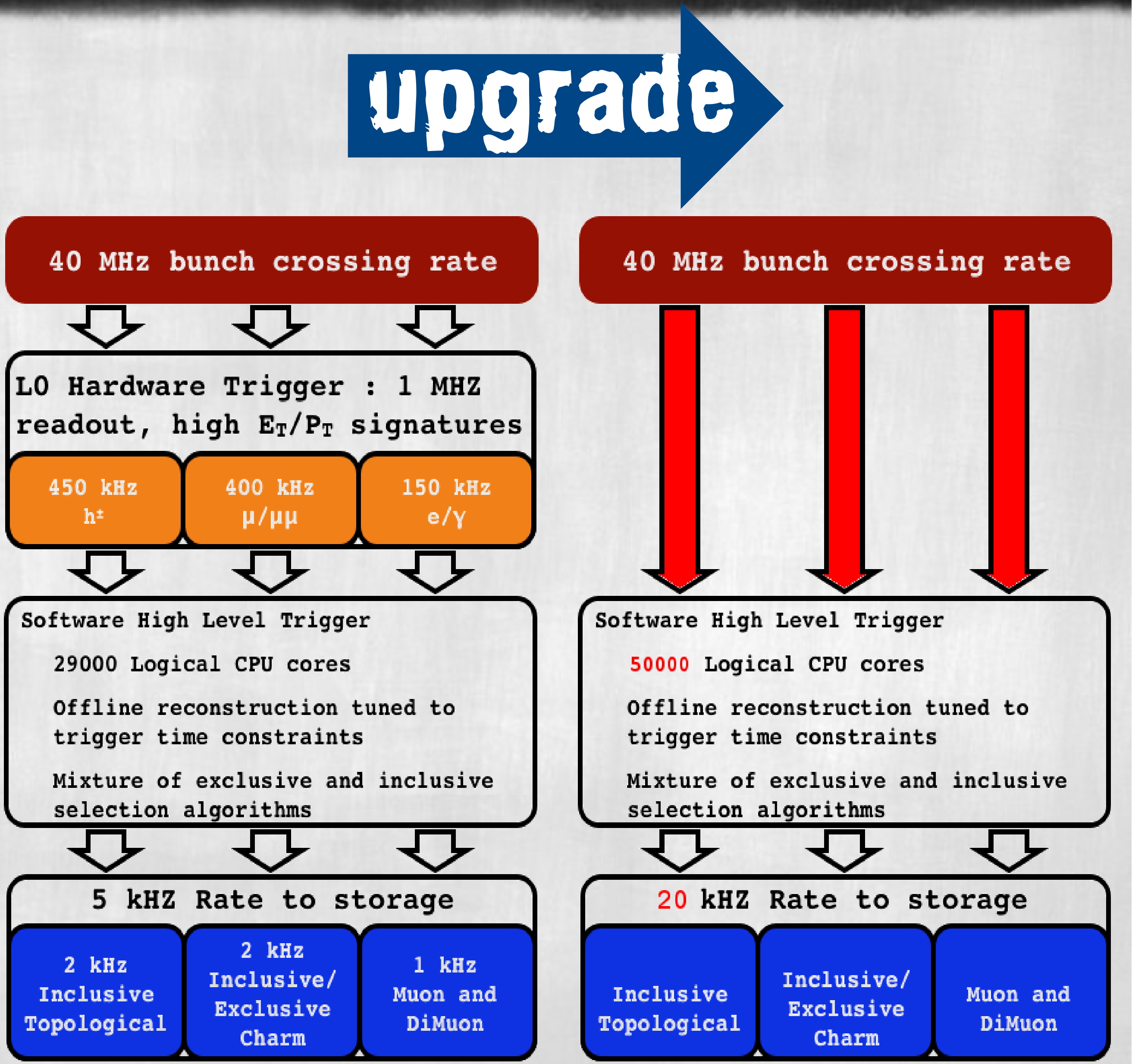
upgrade:

- Unbiased trigger (due to high background)
  - 50kHz in Pb-Pb, up to 1MHz in pp
- Less extreme environment w.r.t. ATLAS/CMS
  - Radiation level:
    - 700 kRad
    - 10^{13} 1MeV-neq cm^{-2} for the full integrated luminosity

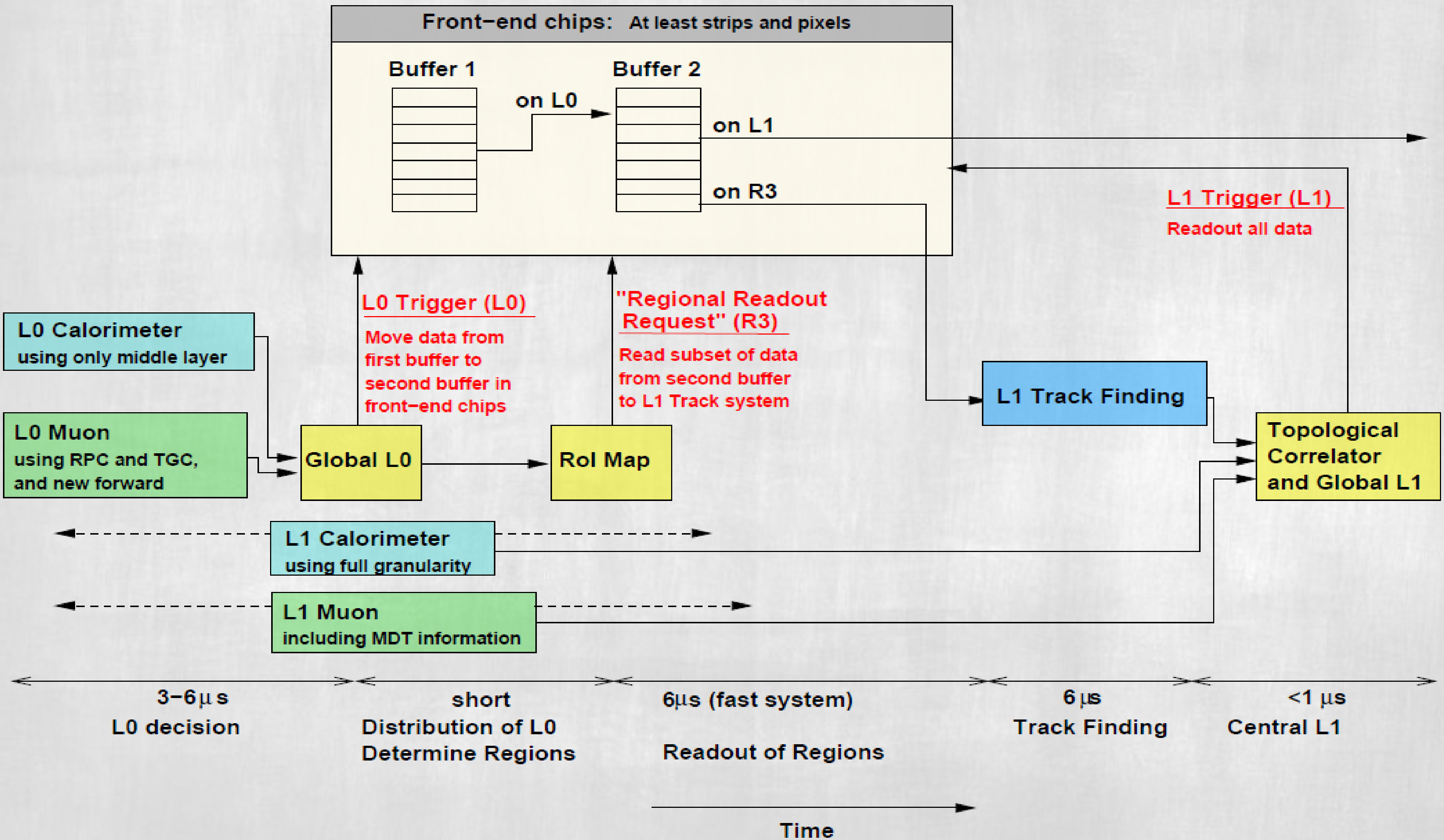
ALICE and LHCb upgrades



- Unbiased trigger
  - Great flexibility in sw-only trigger
- Large-bandwidth connectivity possible:
  - Open geometry (similar to fixed-target experiment)



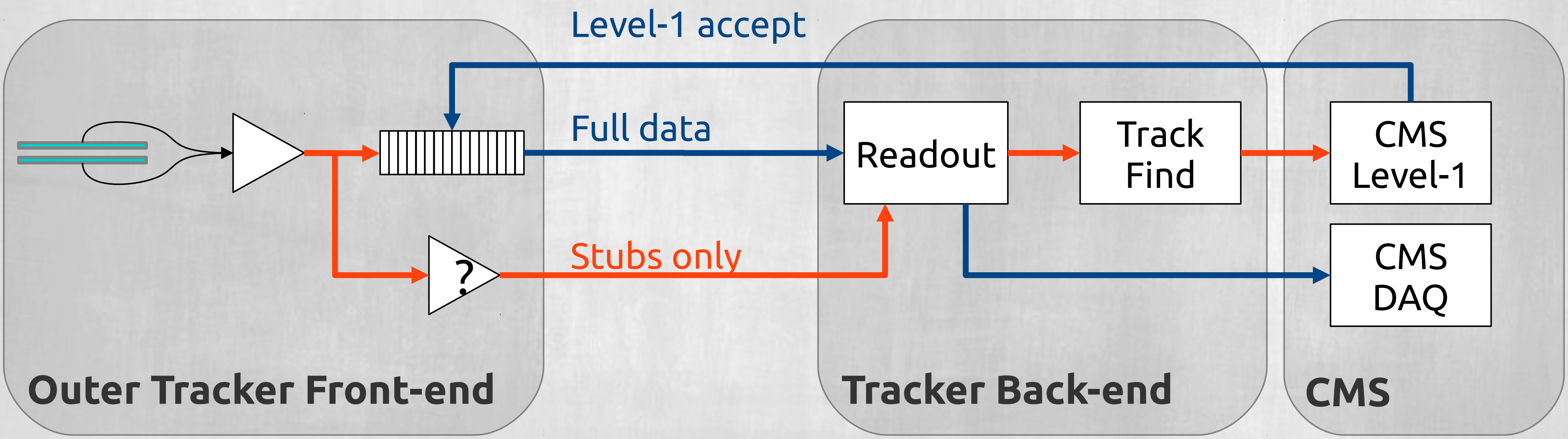
Upgrades DAQ schemes: Atlas



Upgrades DAQ schemes: CMS

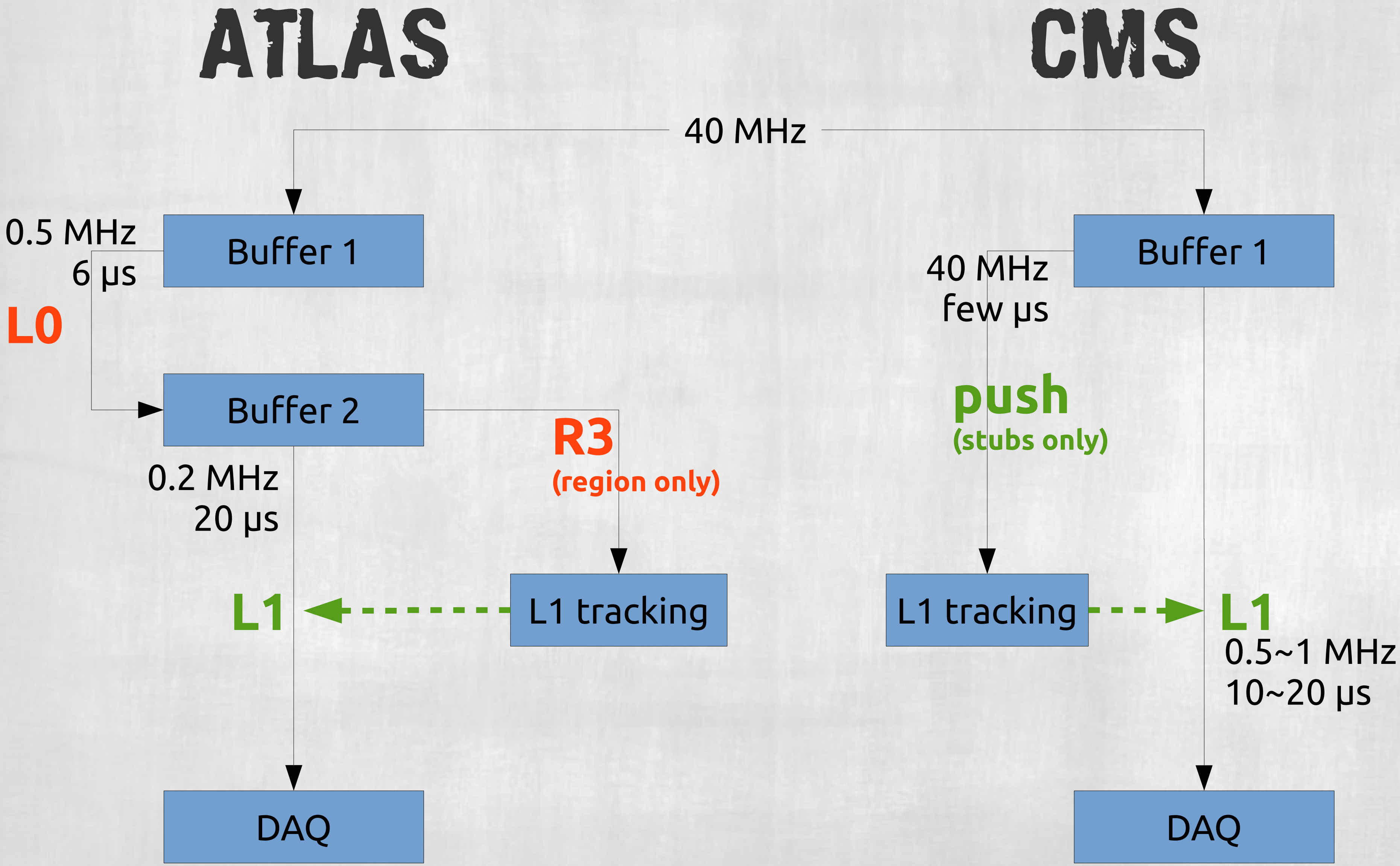
Level-1 "stubs" are processed in the back-end

Form Level-1 tracks, pT above ~ 2 GeV, contributing to CMS Level-1 trigger



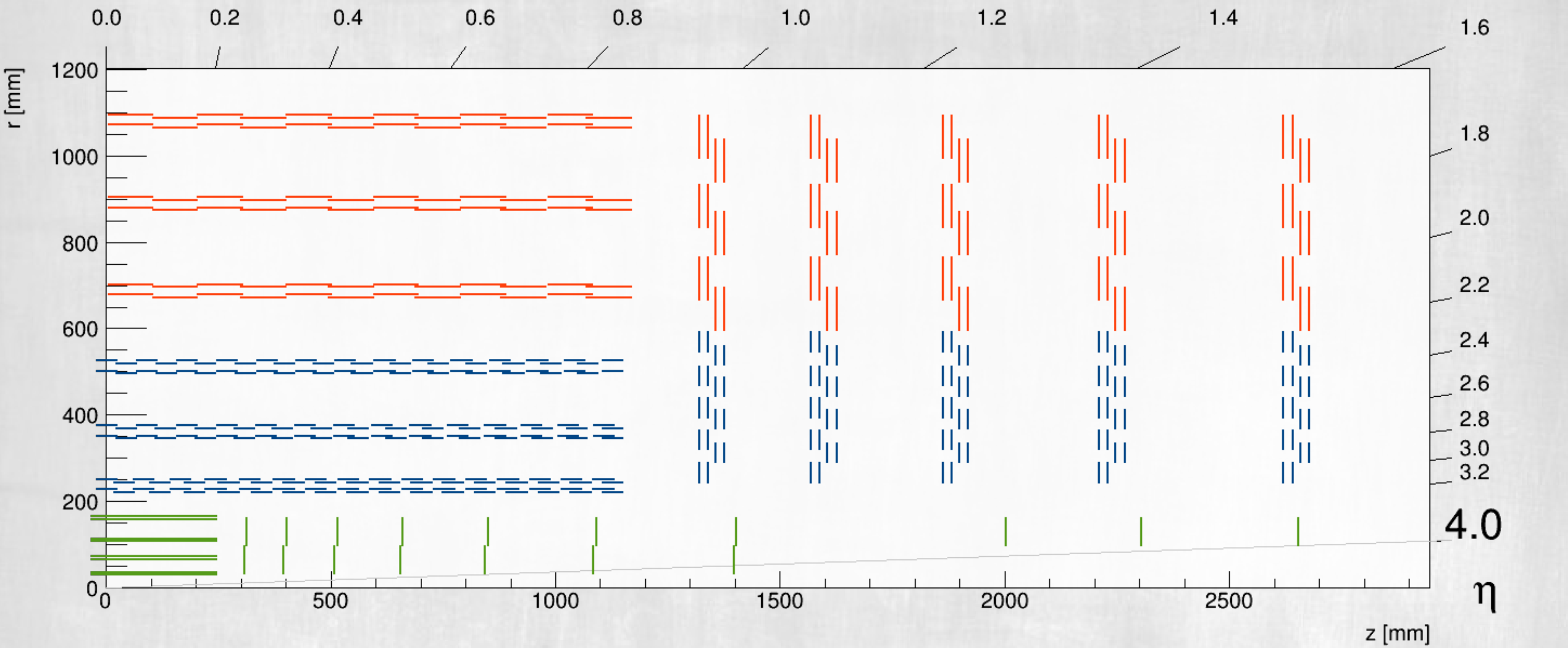
@ 40 MHz – Bunch crossing
@ 500 kHz (1 MHz) – CMS Level-1 trigger

Level-which?



ATLAS
CMS
40 MHz
Buffer 1
0.5 MHz
6 µs
L0
Buffer 2
R3
(region only)
0.2 MHz
20 µs
L1 tracking
L1
DAQ
Buffer 1
40 MHz
few µs
push
(stubs only)
L1 tracking
L1
0.5~1 MHz
10~20 µs
DAQ

Baseline CMS layout



Lower density
2S modules outside
(~8400 modules)

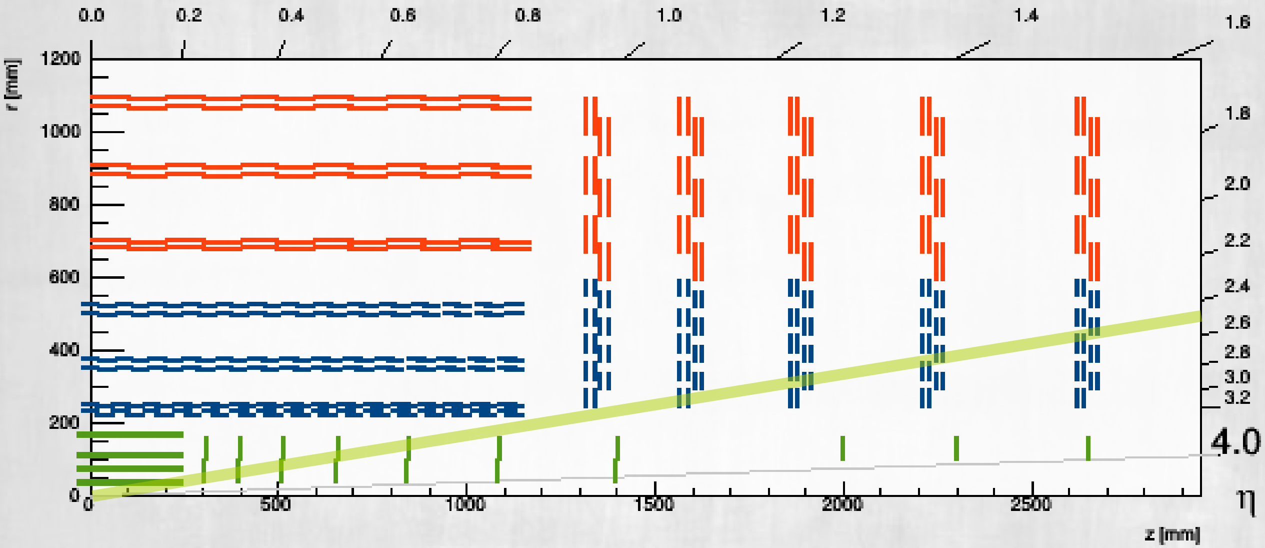
More detailed model

PS modules middle
z info in trigger
θ info in trigger
(~7100 modules)

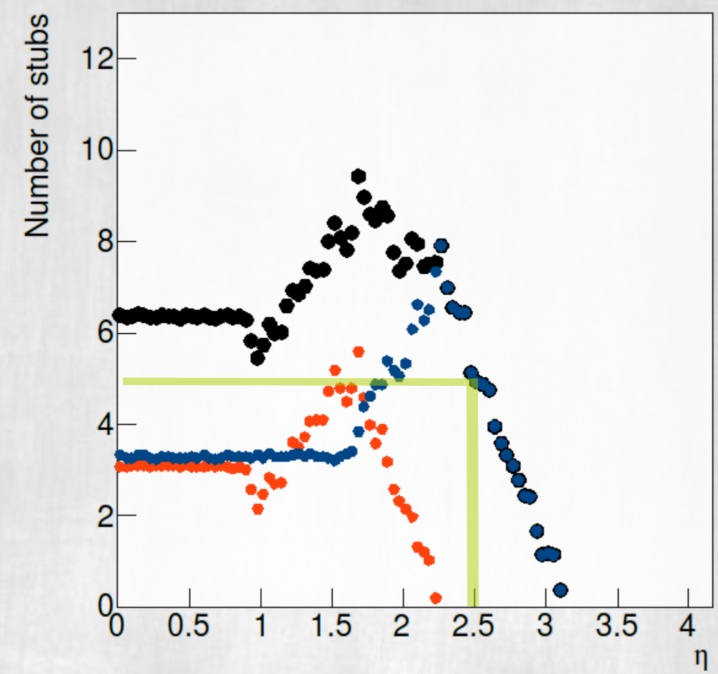
Pixel modules inside
accurate impact parameter resolution & forward coverage

No detailed model

Baseline CMS layout

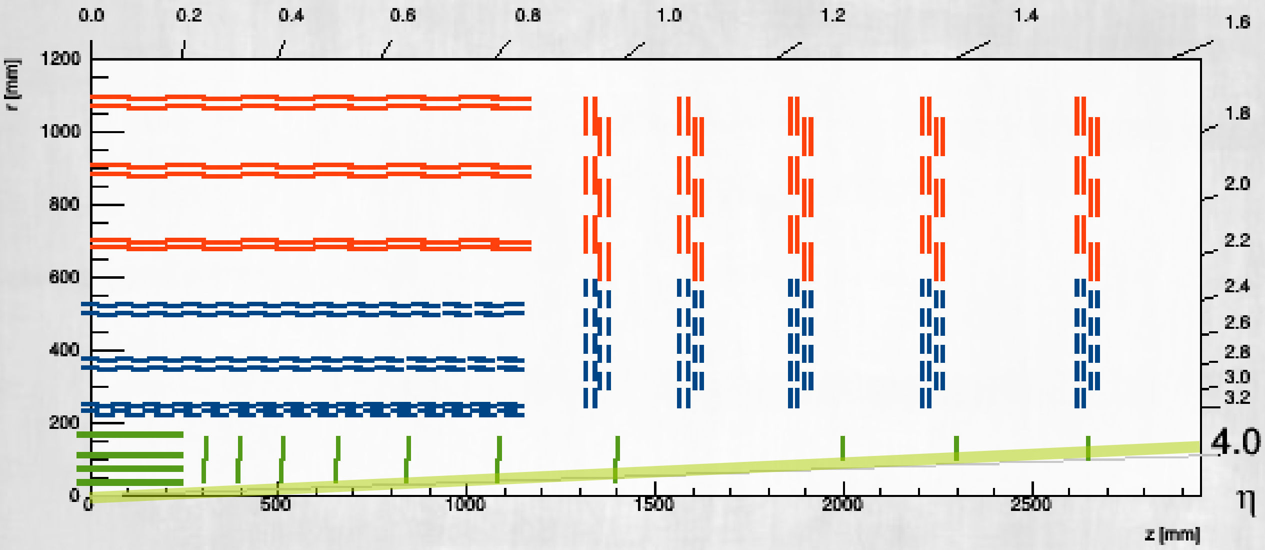


5 trigger stubs
(10 points) → η=2.5

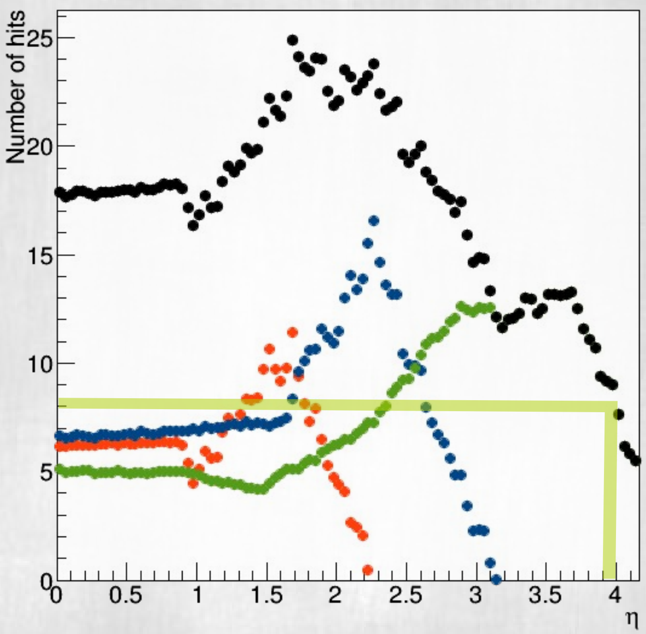


- **×4 granularity** in all strips
- +3 layers of **MacroPixel sensors**
  - Unambiguous **3D coordinates** helps track finding in high pile-up
- Up to **10 points** available for track-trigger up to η=2.5
  - Comparable to current tracker's coverage, **but at L1**

Baseline CMS layout

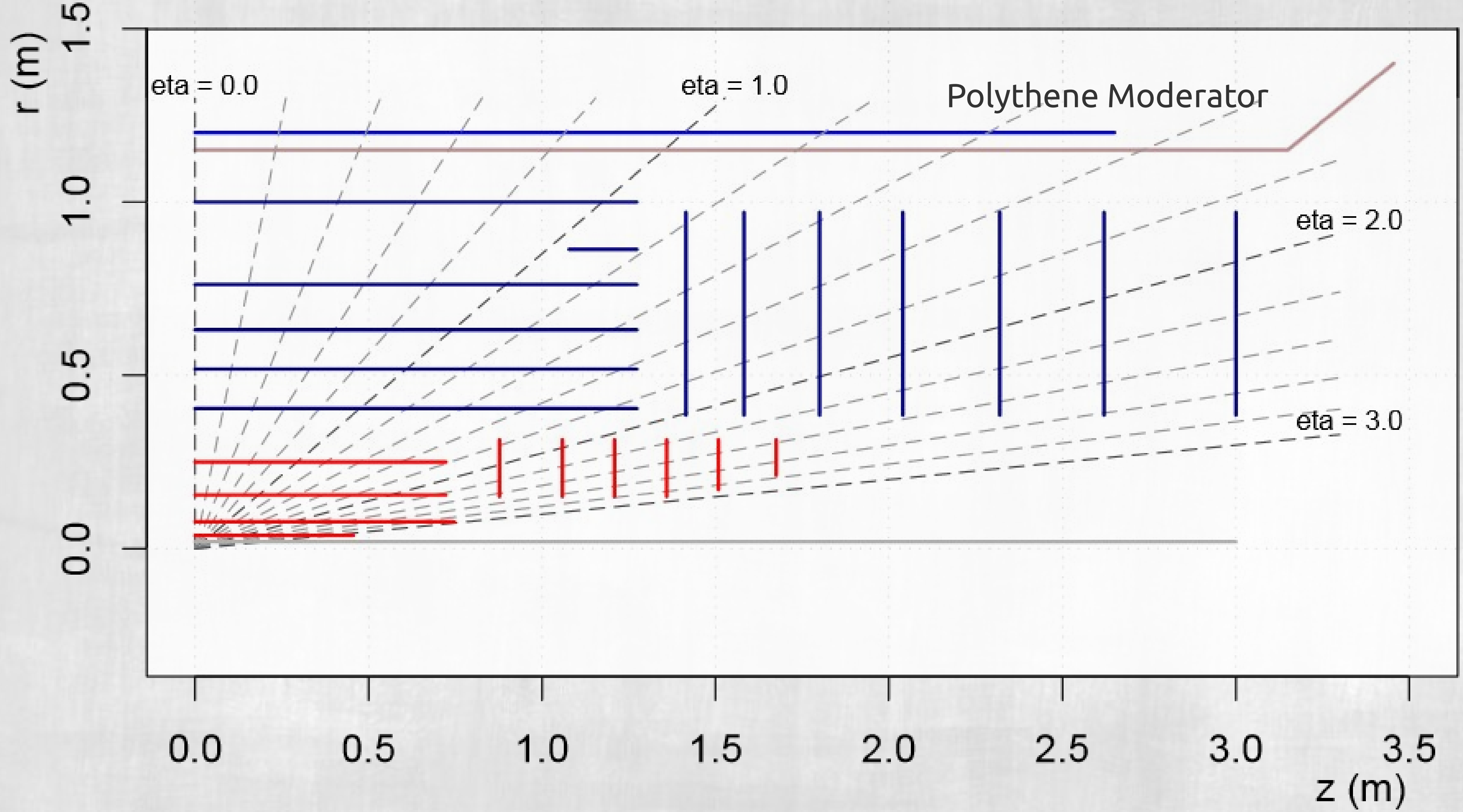


Hit coverage → η≈4



- **×4 granularity** in all strips
- +3 layers of **MacroPixel sensors**
  - Unambiguous **3D coordinates** helps track finding in high pile-up
- Up to **10 points** available for track-trigger up to η=2.5
  - Comparable to current tracker's coverage, **but at L1**
- Hit coverage up to **η≈4** in full readout (after L1 Accept)

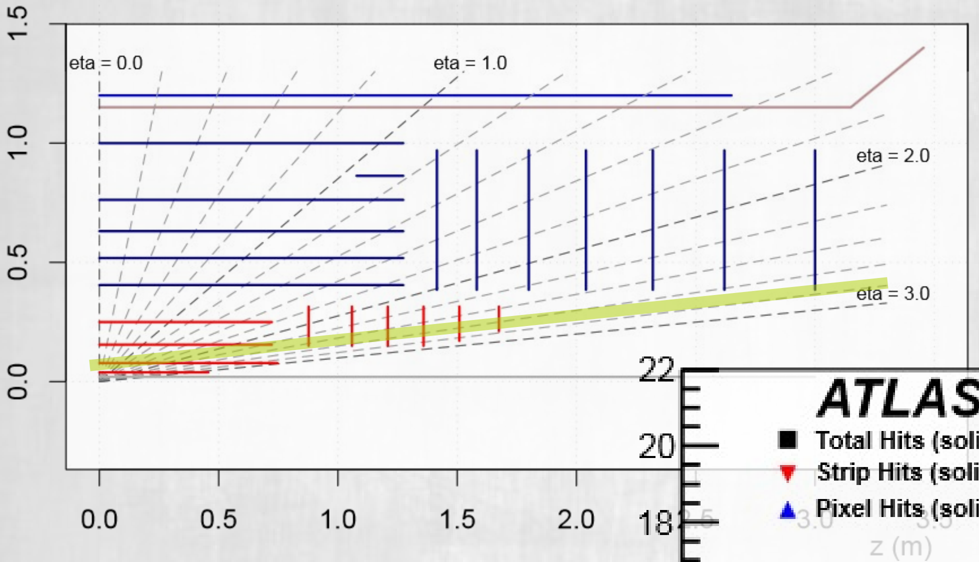
Baseline ATLAS layout



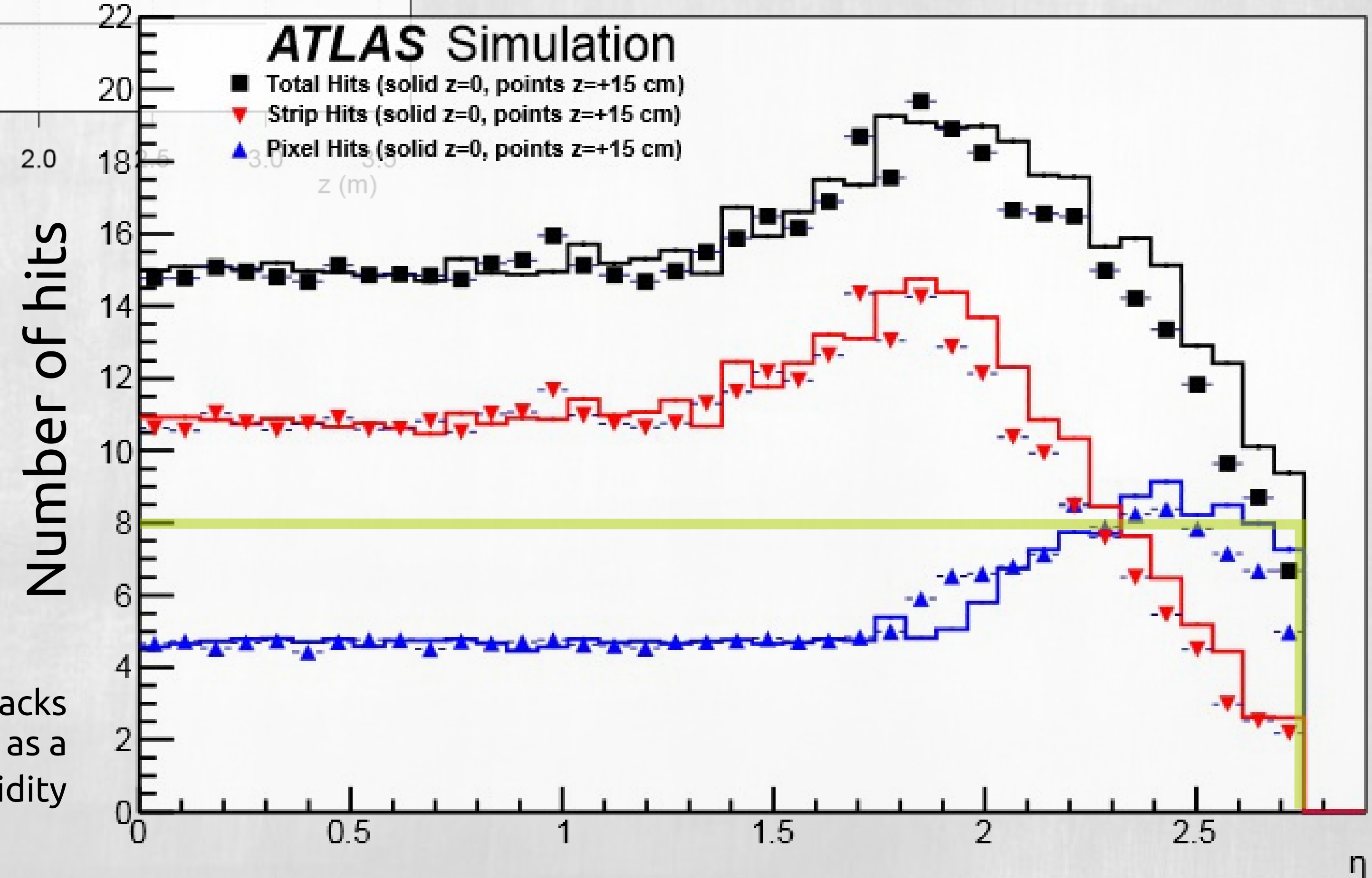
- 5 barrel + 7 end-cap 3 layers of **strip sensors**
  - All with stereo 3D coordinates
- 4 barrel + 6 end-cap layers of **pixels sensors**

See: letter of intent
http://cds.cern.ch/record/1502664?ln=en

Baseline ATLAS layout

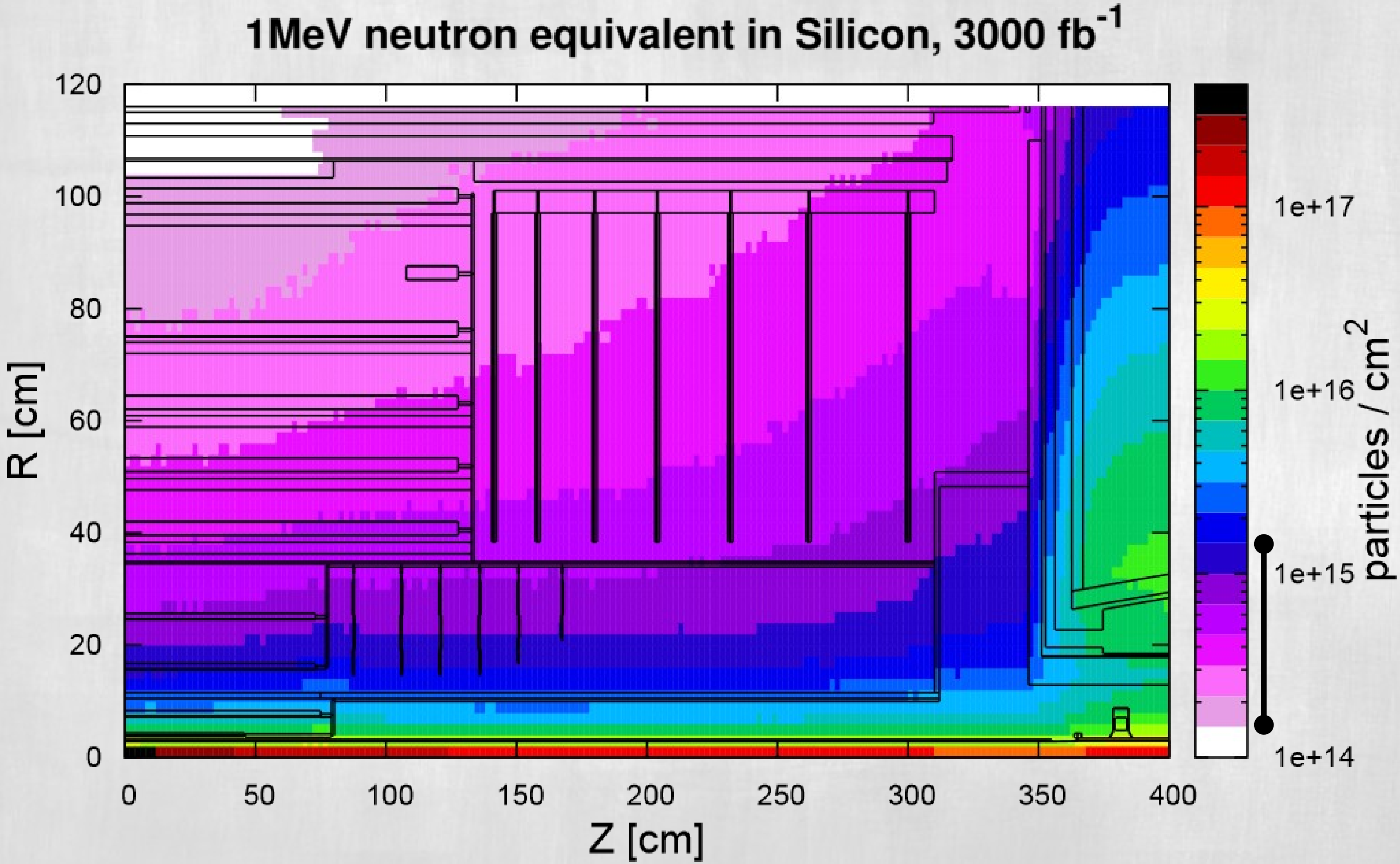


Coverage in η → 2.8 in regional readout L1 tracking **and** L2 full readout



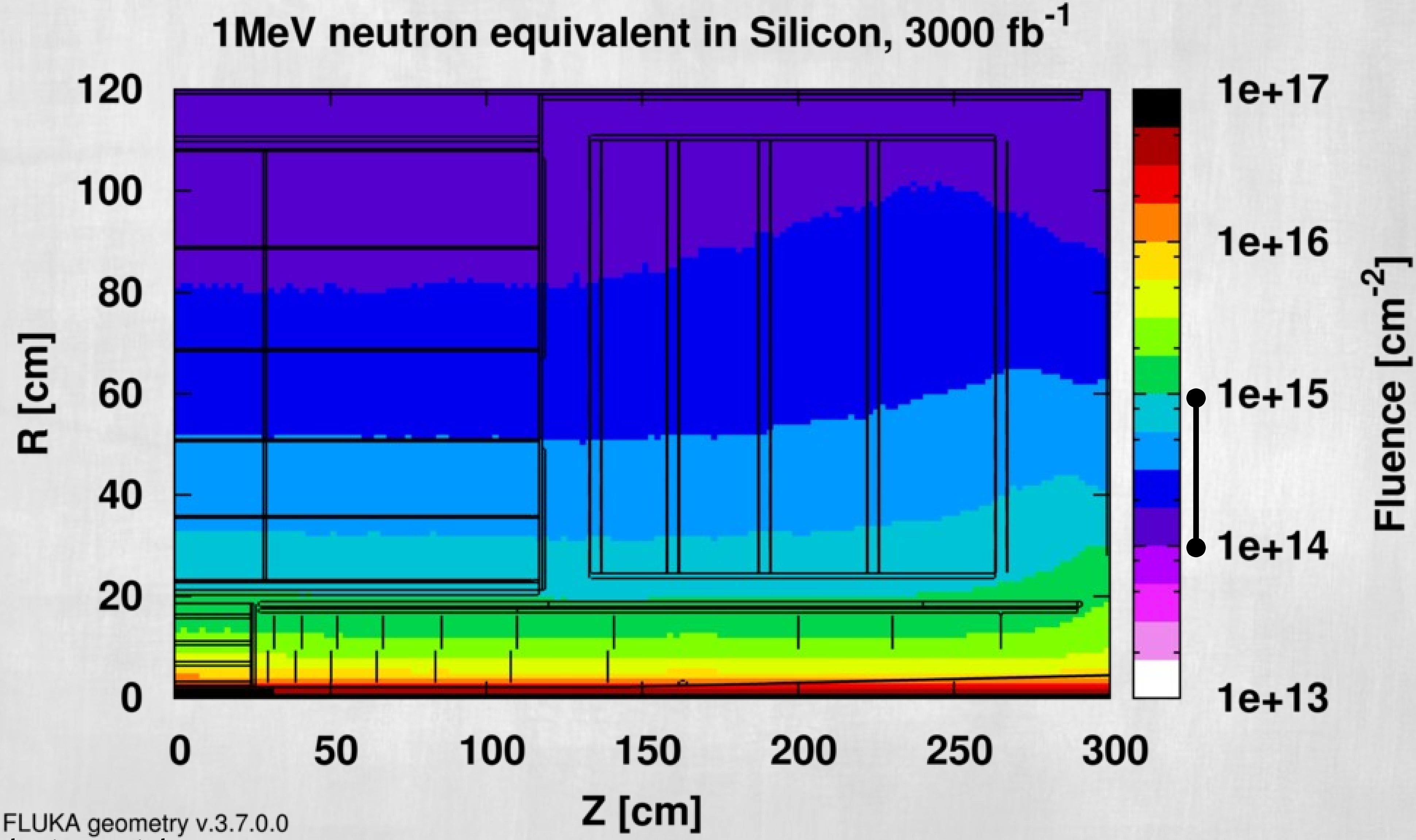
Number of hits on μ tracks with p_T > 5 GeV/c as a function of pseudo-rapidity

ATLAS integrated dose



Simulation with FLUKA

CMS integrated dose



Simulation with FLUKA

SiStrip upgrades overview

	Current		Upgrade	
CMS	206 m^2	Silicon	216 m^2	Silicon
	9.3 M	Strips	47.8 M	Strips
	0	MacroPixels	217 M	MacroPixels
	~ 100 kHz	readout rate	40 MHz	L1 readout rate*
			0.5→1 MHz	readout rate

	Current		Upgrade	
Atlas	61 m^2	Silicon	193 m^2	Silicon
	6.3 M	Strips	74 M	Strips
	0	MacroPixels	0	MacroPixels
	~ 100 kHz	readout rate	0.5 MHz	L1 readout rate**
			0.2 MHz	readout rate

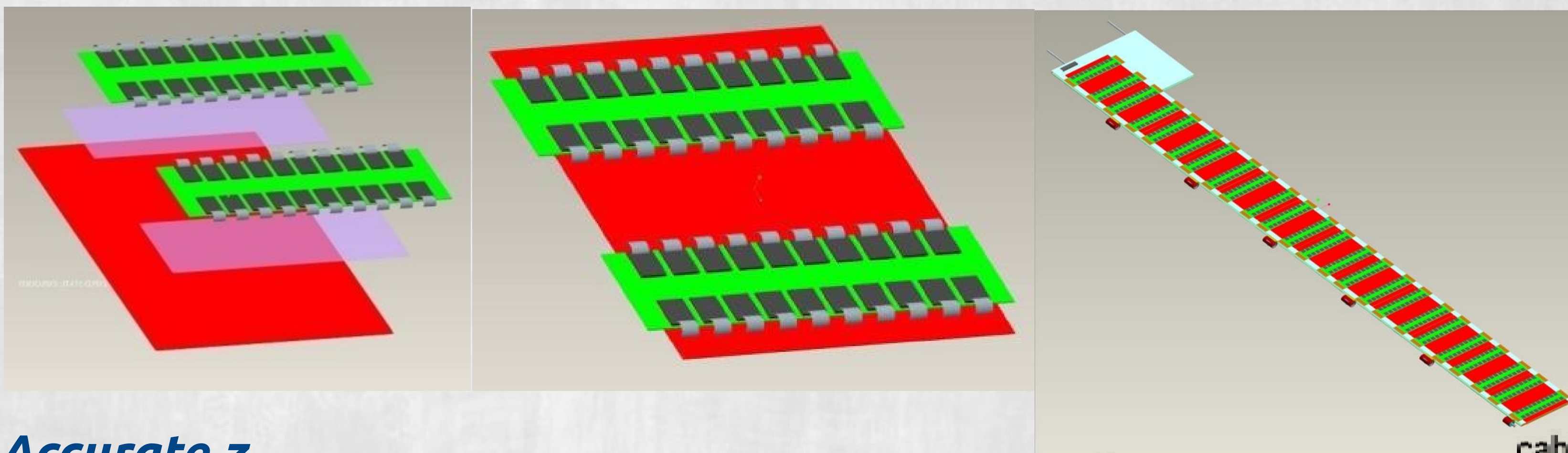
* only high-pt hits read-out
** L0 pre-fetch

Strips Front-end ATLAS & CMS

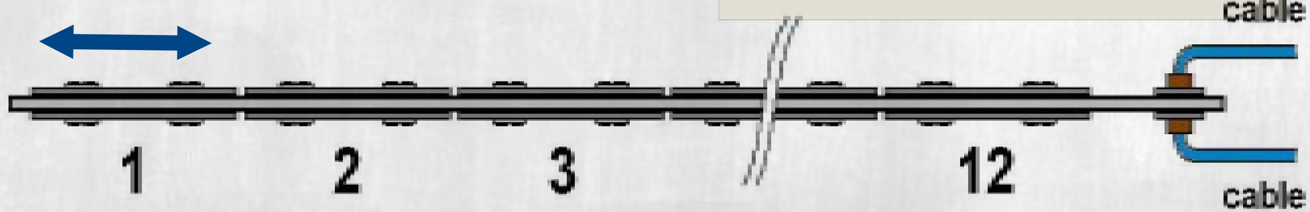
Parameter	ATLAS (ABC130)	CMS (CBC)
NIEL assumed [1MeV-neq cm^{-2}]	2×10^{15}	1.5×10^{15}
# Strips (rφ)	1280	1016
Signal coupling	AC	AC
Strip pitch [μm]	74.5	90
Stereo angle	Yes	No
Strip length [mm]	23.88, 47.75	23.13, 50.25
Signal connection	Wire bond	Wire bond + C4 bunp bond
Chip feature size [nm]	130	130
ADC resolution	1 bit	1 bit
Zero suppression for L1 data	Yes	No (outsourced)

Apparently very similar, but...

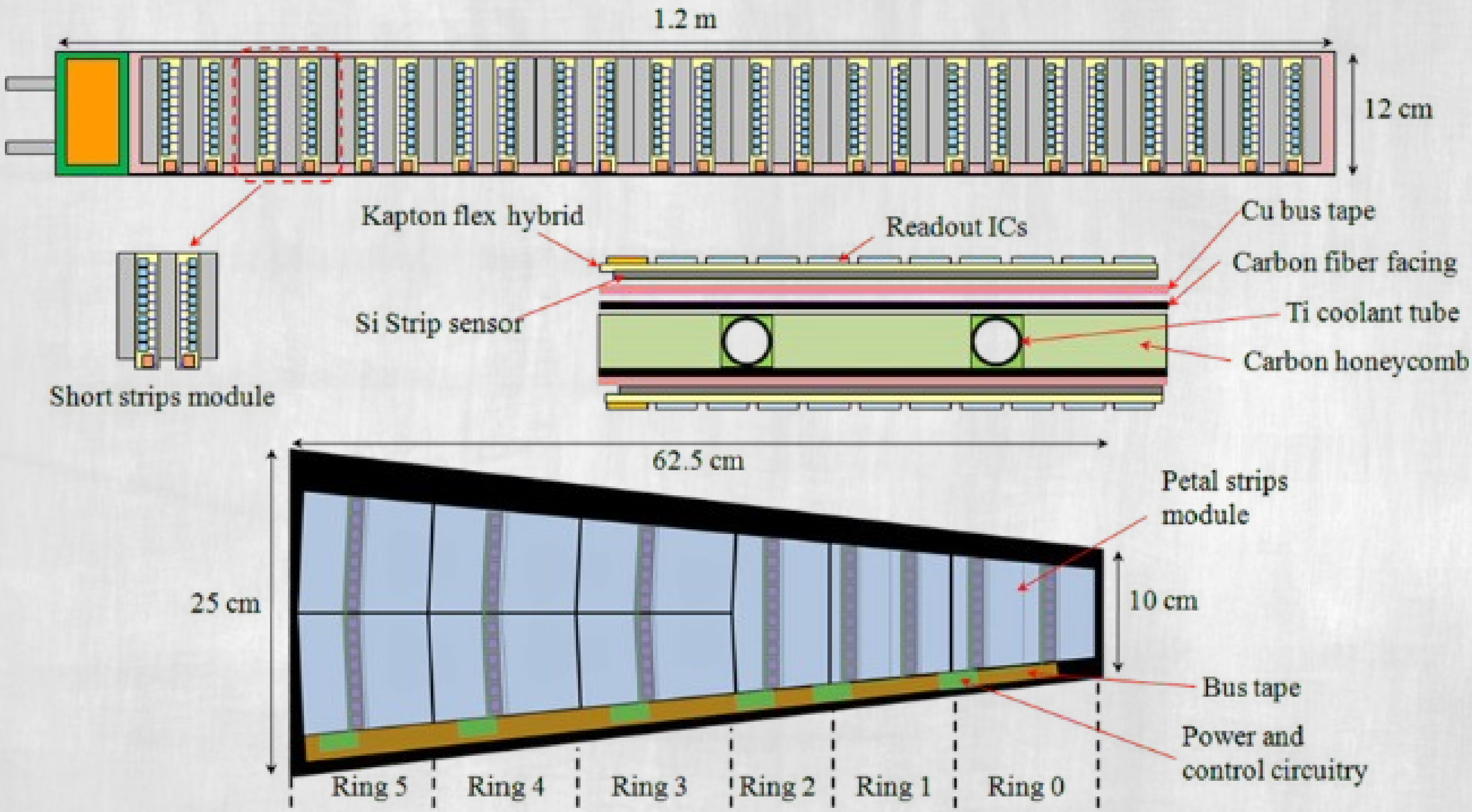
Strips Front-end ATLAS & CMS



Accurate z information through stereo angle



Strips Front-end ATLAS & CMS



Strips Front-end ATLAS & CMS

2 Strip sensors

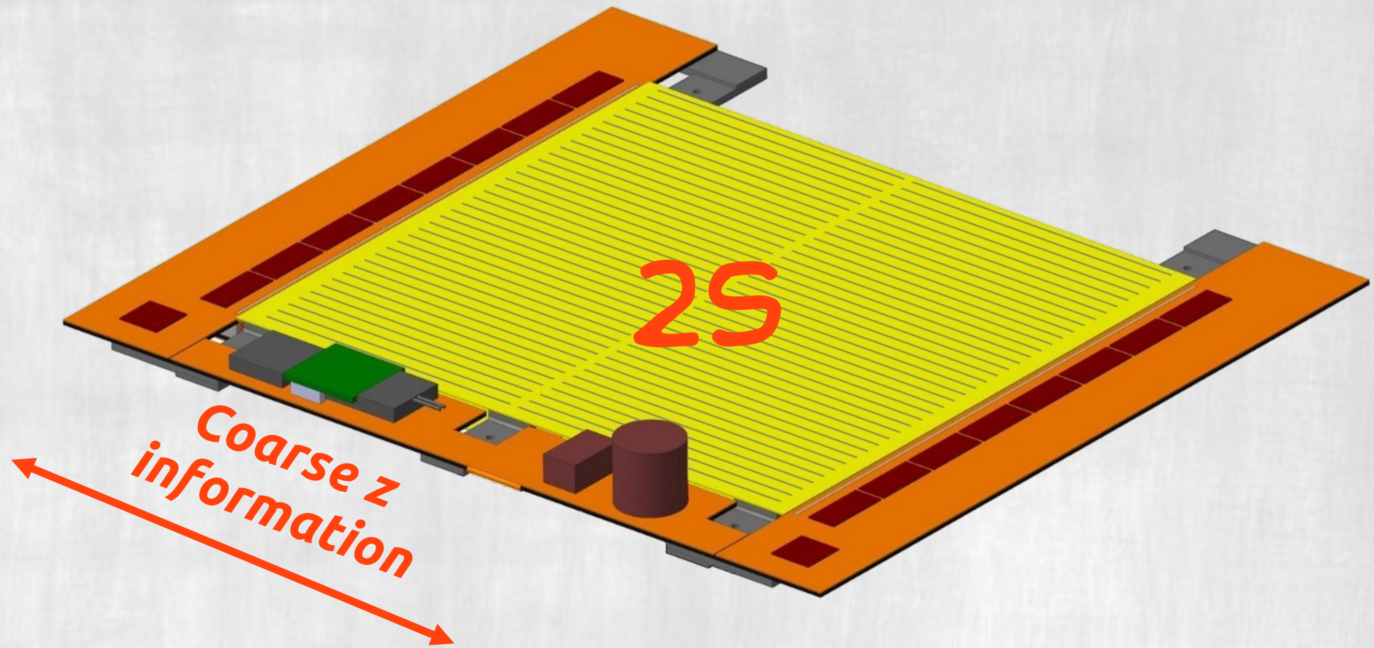
Strips: 5 cm × 90 µm

Strips: 5 cm × 90 µm

P = 2.7 W

~ 92 cm^2 active area

For r > 40 cm



Pixel + **S**trip sensors

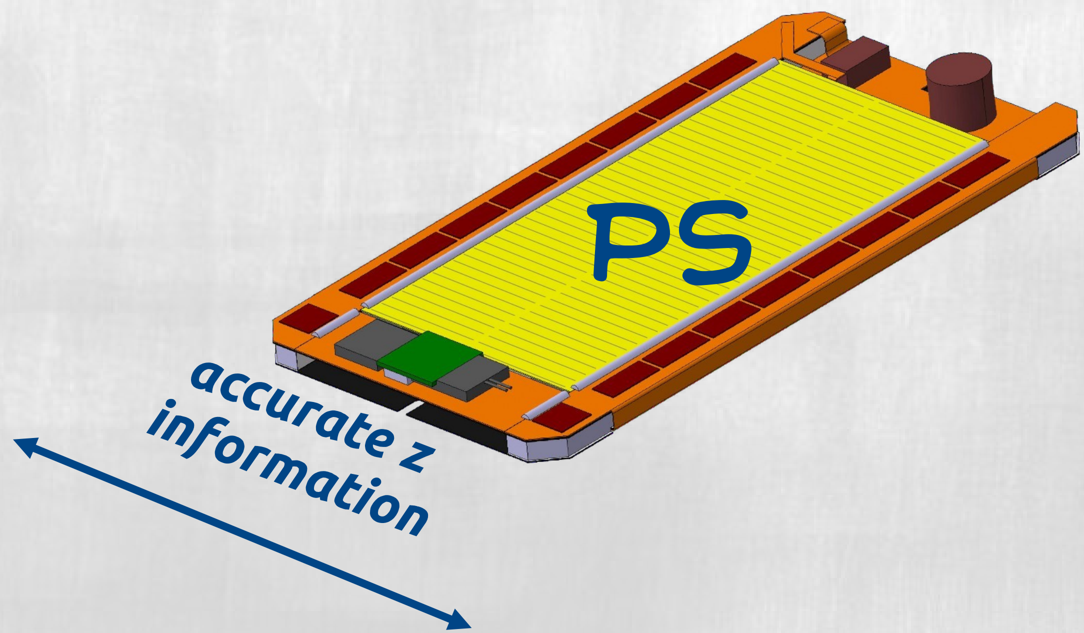
Strips: 2.5 cm × 100 µm

MacroPixels: 1.5 mm × 100 µm

P = 5.0 W

~ 44 cm^2 active area

For r > 20 cm



CMS Outer tracker front-ends

Need to ship hits off detector

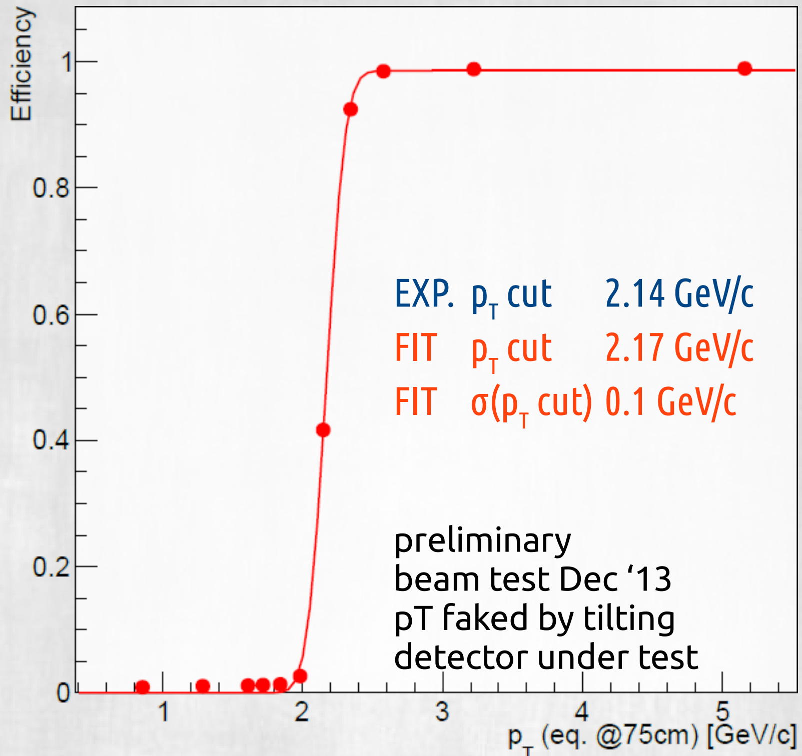
Ship all hits @ 40 MHz? No

- Bandwidth needed: off by 1 order of magnitude (order of 10 Gbps per module)
- Track reconstruction ~ impossible

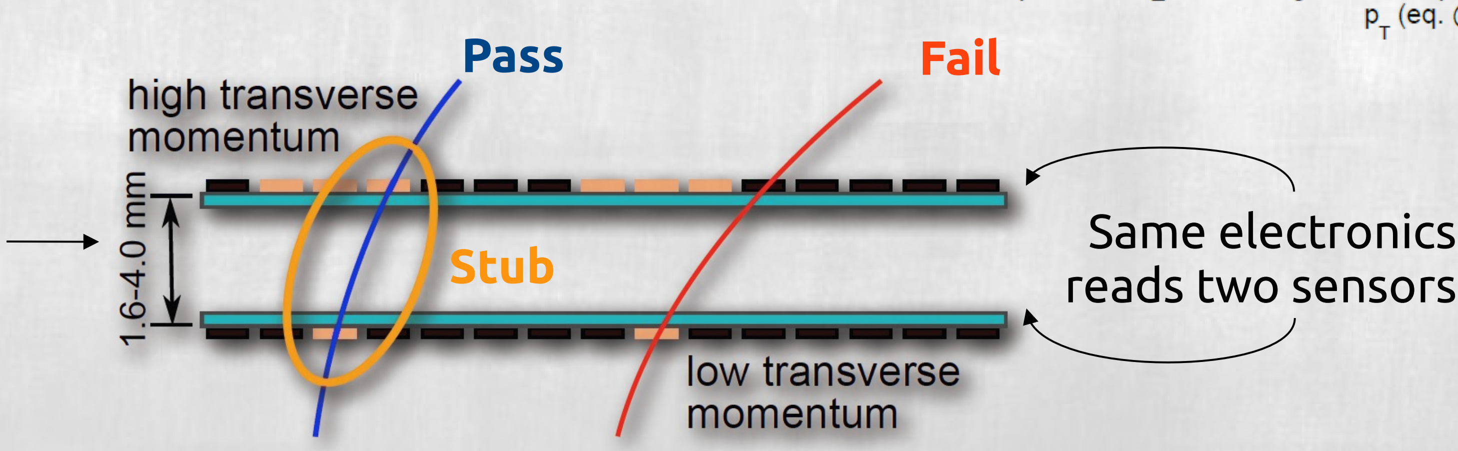
Solution: ship only high-pT hits (stubs)

- Threshold of ~ 2 GeV
- Data reduction of one order of magnitude or more

Modules with pT discrimination ("pT modules")

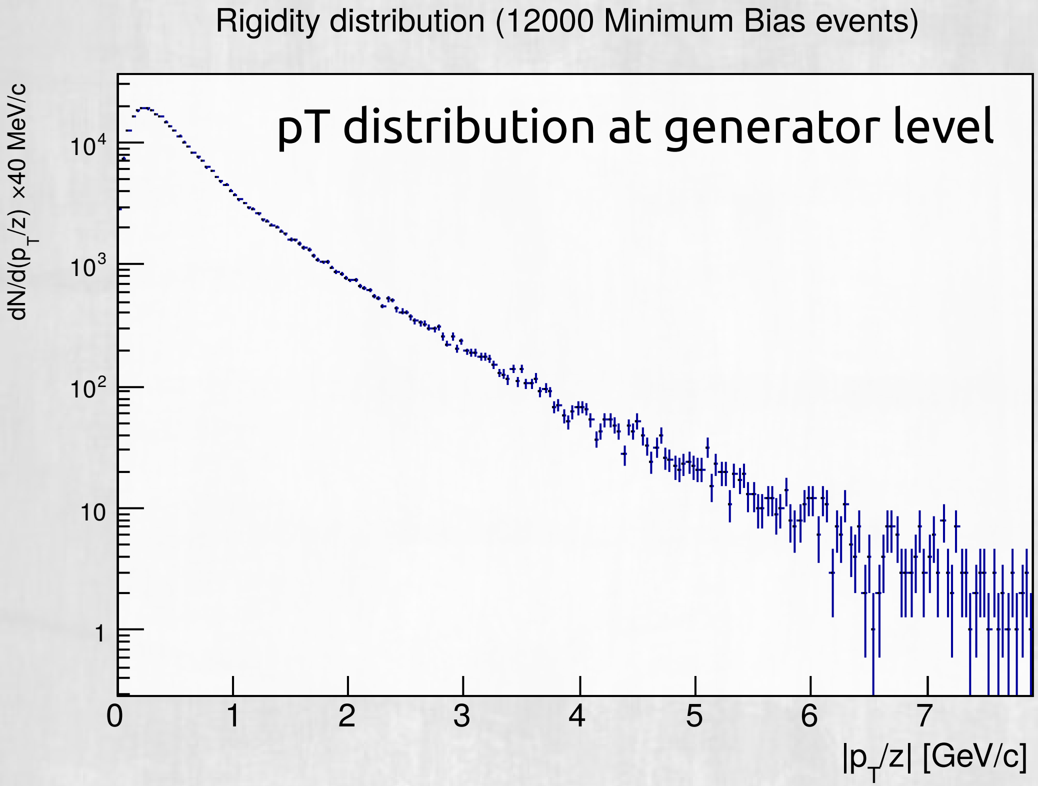


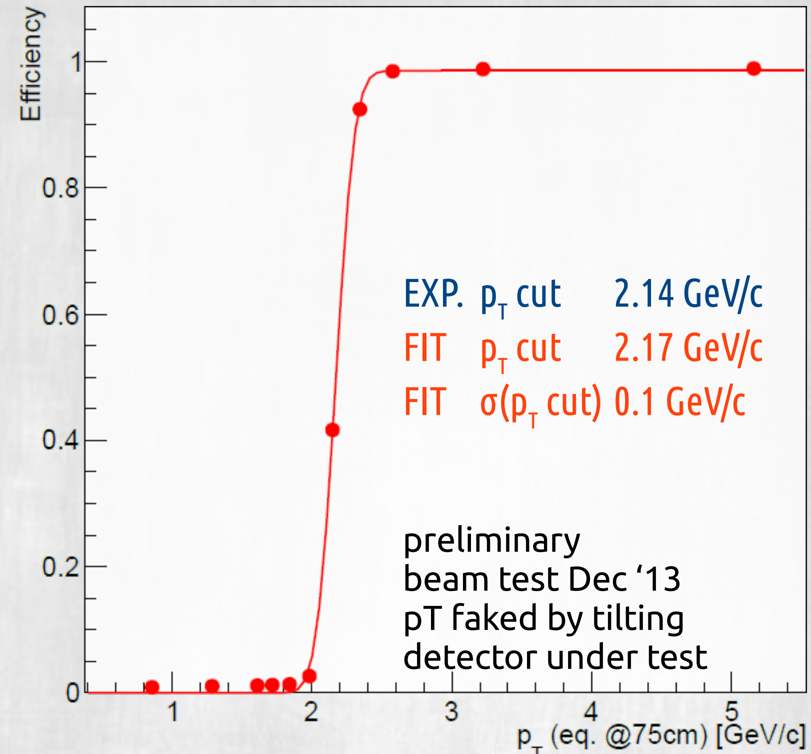
Thanks to CMS 3.8 T magnetic field!

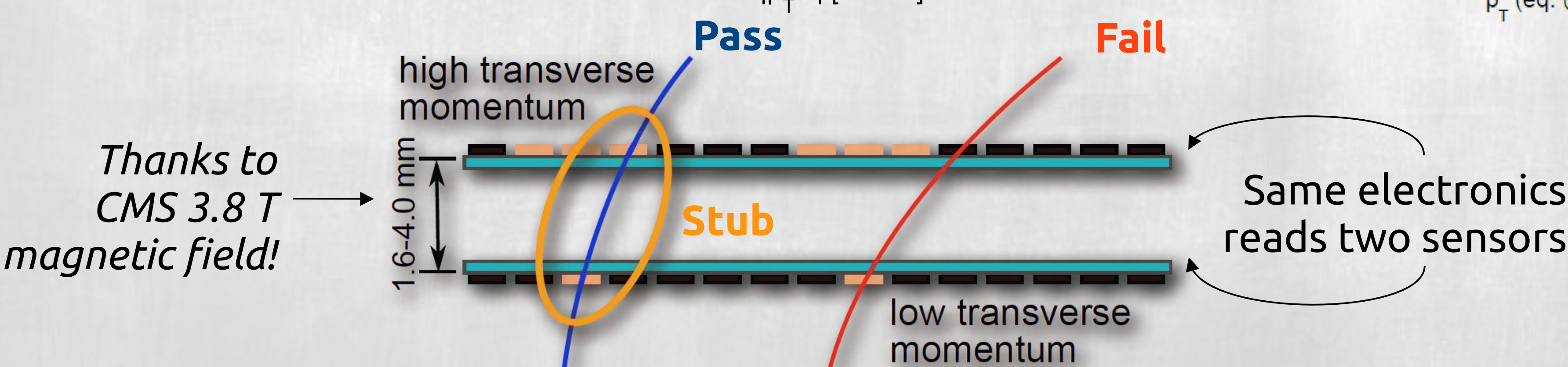


J. Jones, A. Rose, C. Foudas, G. Hall, http://arxiv.org/pdf/physics/0510228v1.pdf
F. Palla, G. Parrini, PoS VERTEX2007 (2007) 034, http://pos.sissa.it/archive/conferences/057/034/Vertex%202007_034.pdf

CMS Outer tracker front-ends

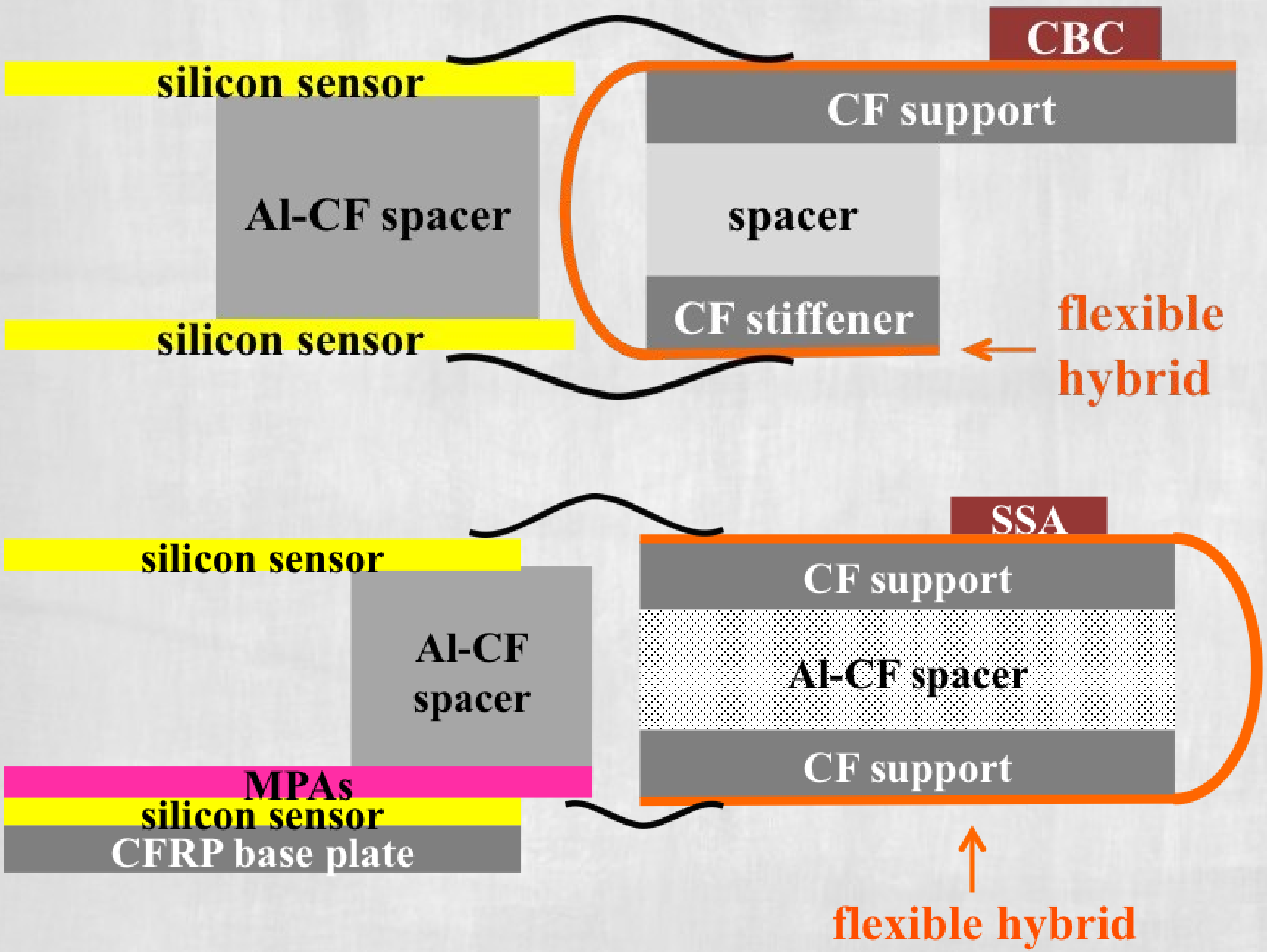


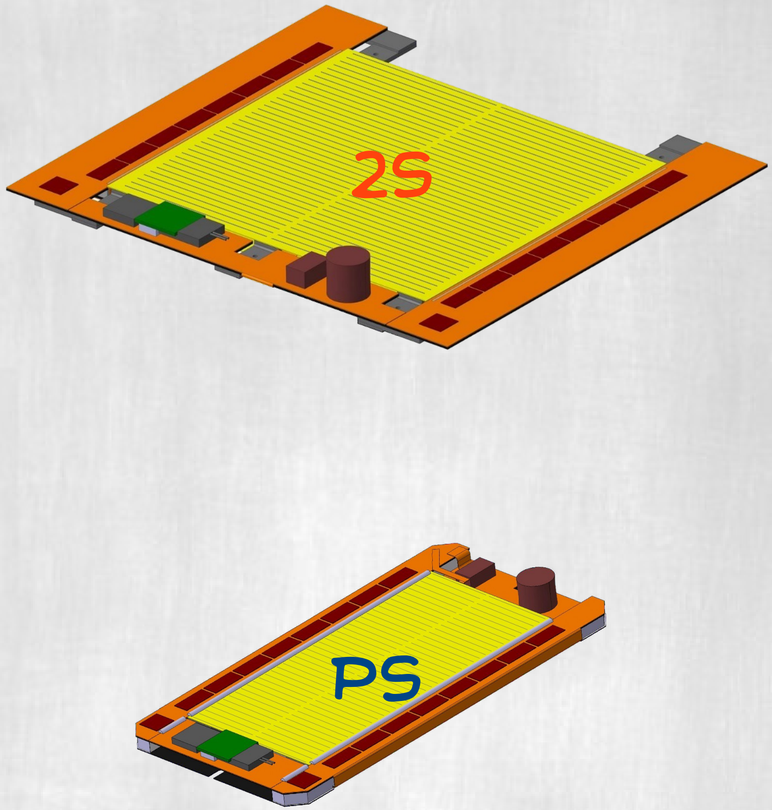




J. Jones, A. Rose, C. Foudas, G. Hall, http://arxiv.org/pdf/physics/0510228v1.pdf
F. Palla, G. Parrini, PoS VERTEX2007 (2007) 034, http://pos.sissa.it/archive/conferences/057/034/Vertex%202007_034.pdf

Front-end interconnection

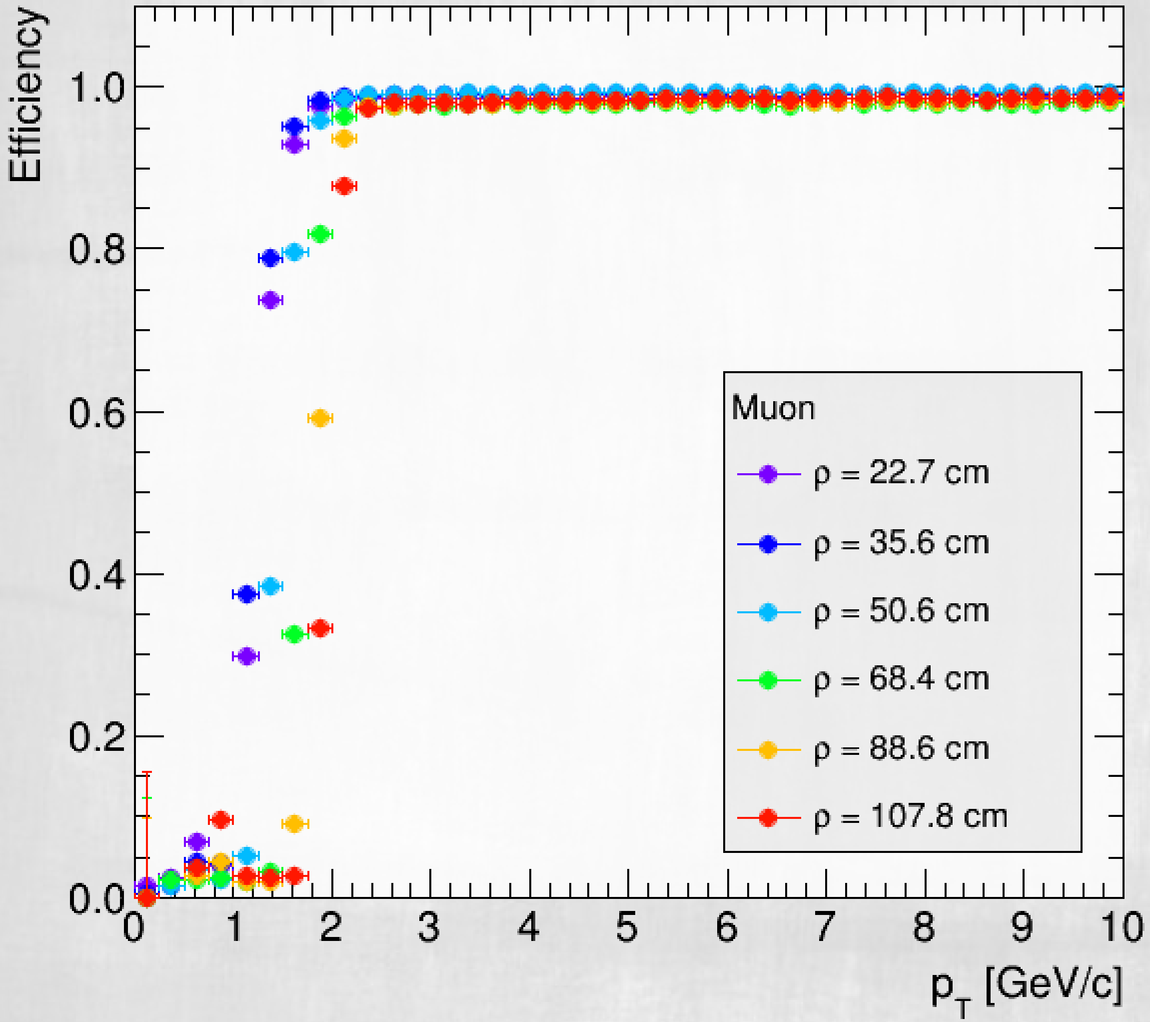


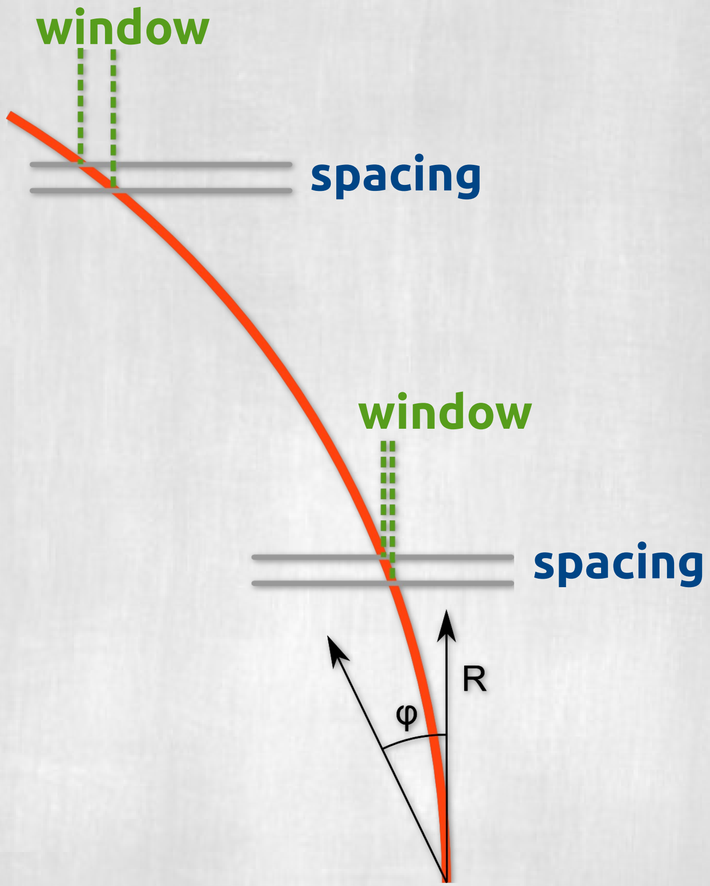


Flex hybrid:

- Technology leap
- Key element for 2-sensor design

Uniform cut



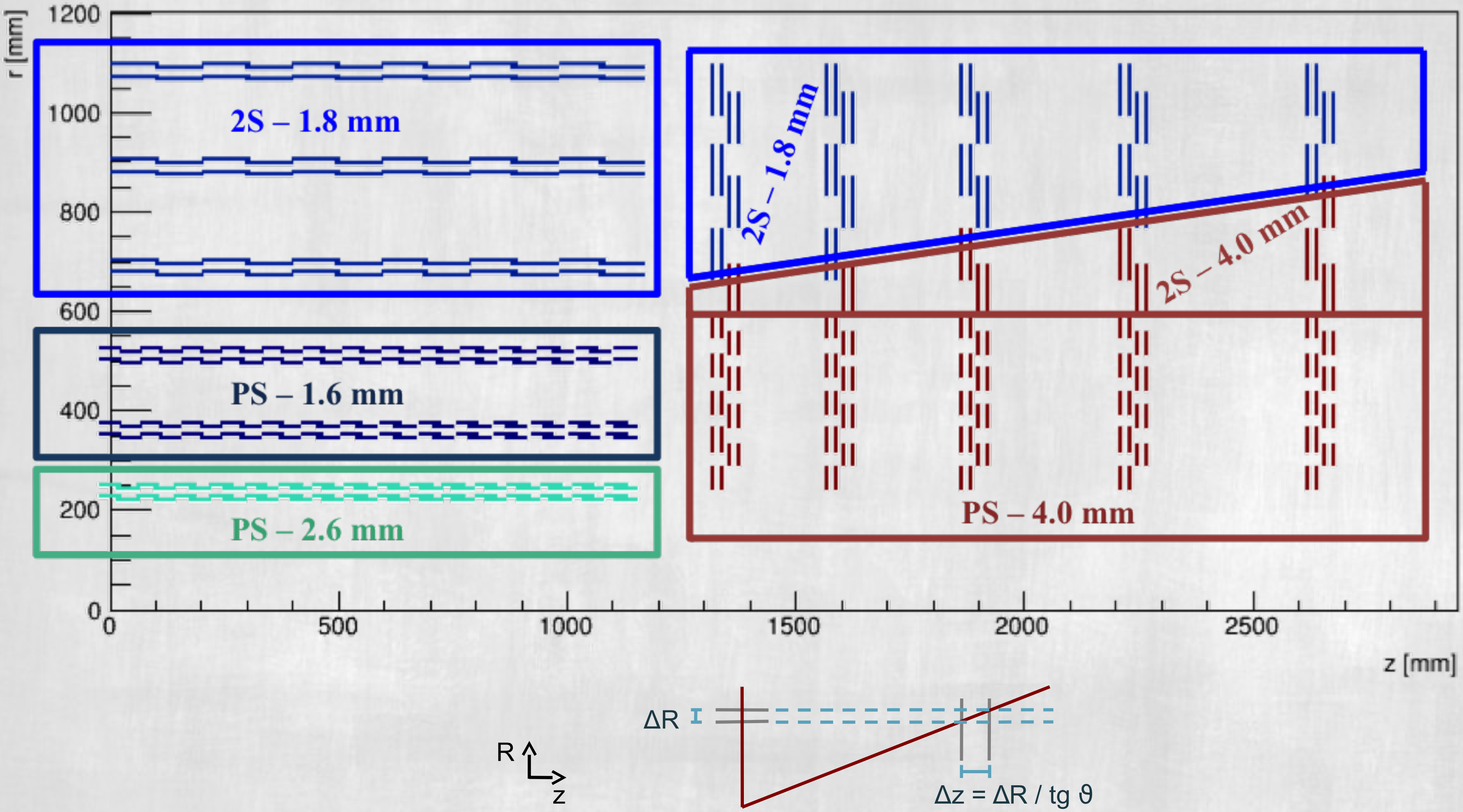


(@construction) (@front-ends)

Need to tune **sensor spacings** and **hit matching windows** are required to maintain uniform p_T cut around 2 GeV/c

Programmable windows in front-ends!

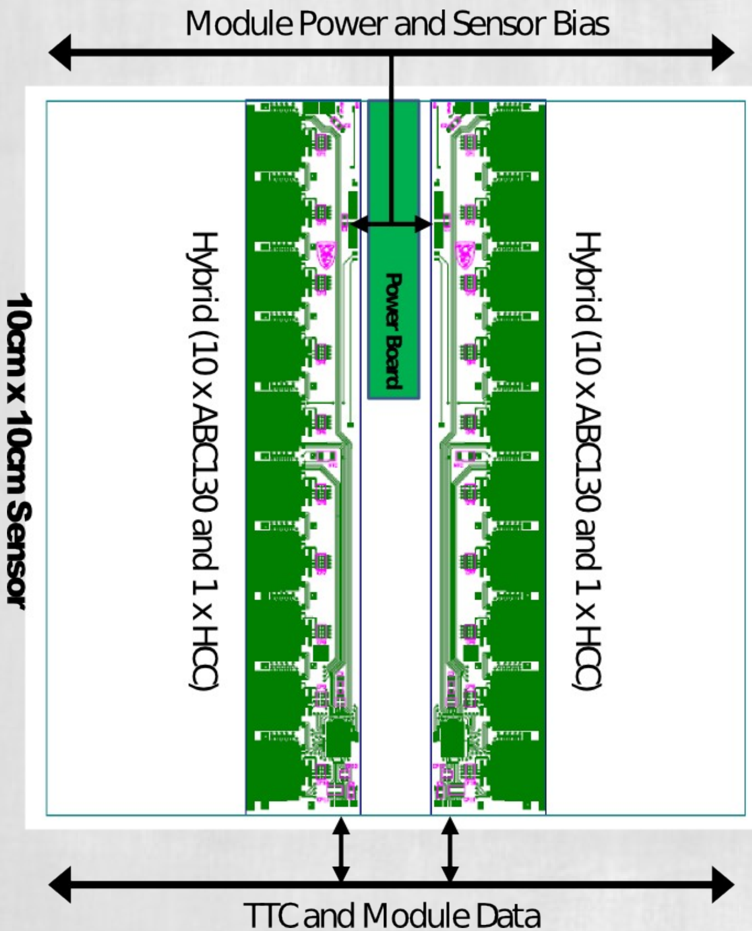
Tuning pT cuts



In the barrel, ΔR is given directly by the sensors spacing
In the end-cap, it depends on the location of the detector
End-cap configuration typically requires wider spacing (up to ~ 4 mm)

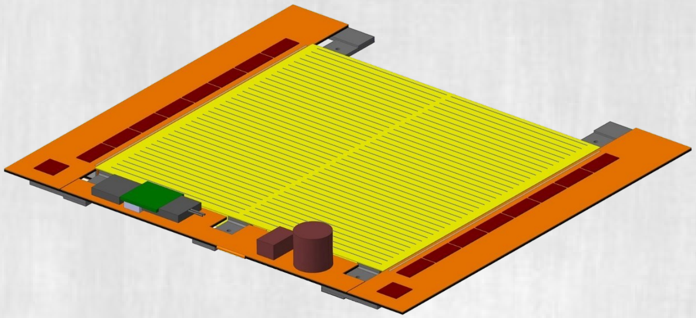
Hybrid traffic: collecting data streams

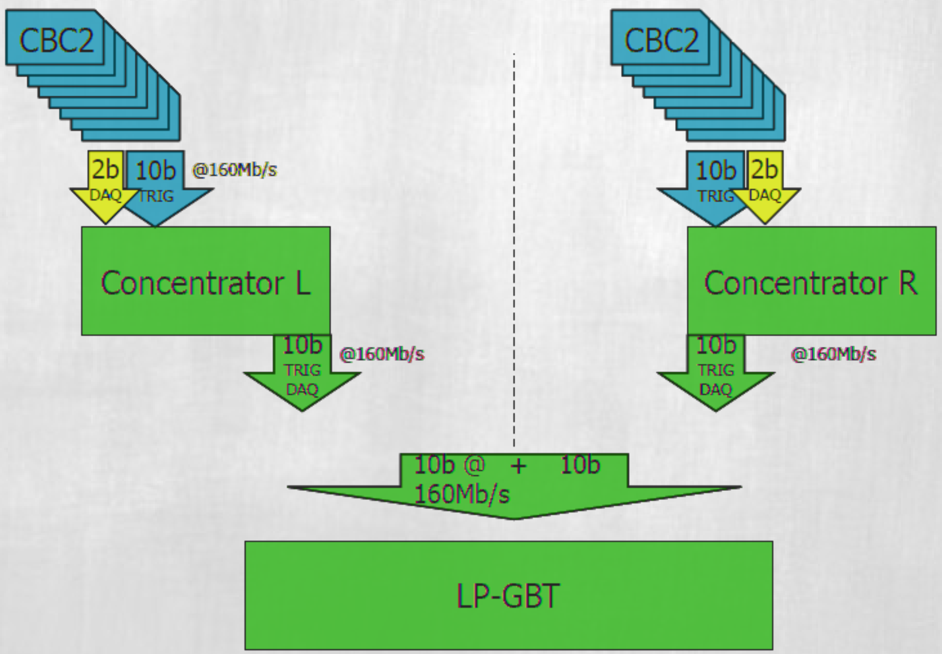
ATLAS



- ABCD130 daisy chain readout
- Data concentrator: HCC (hybrid chip controller)
- Signal arbitration

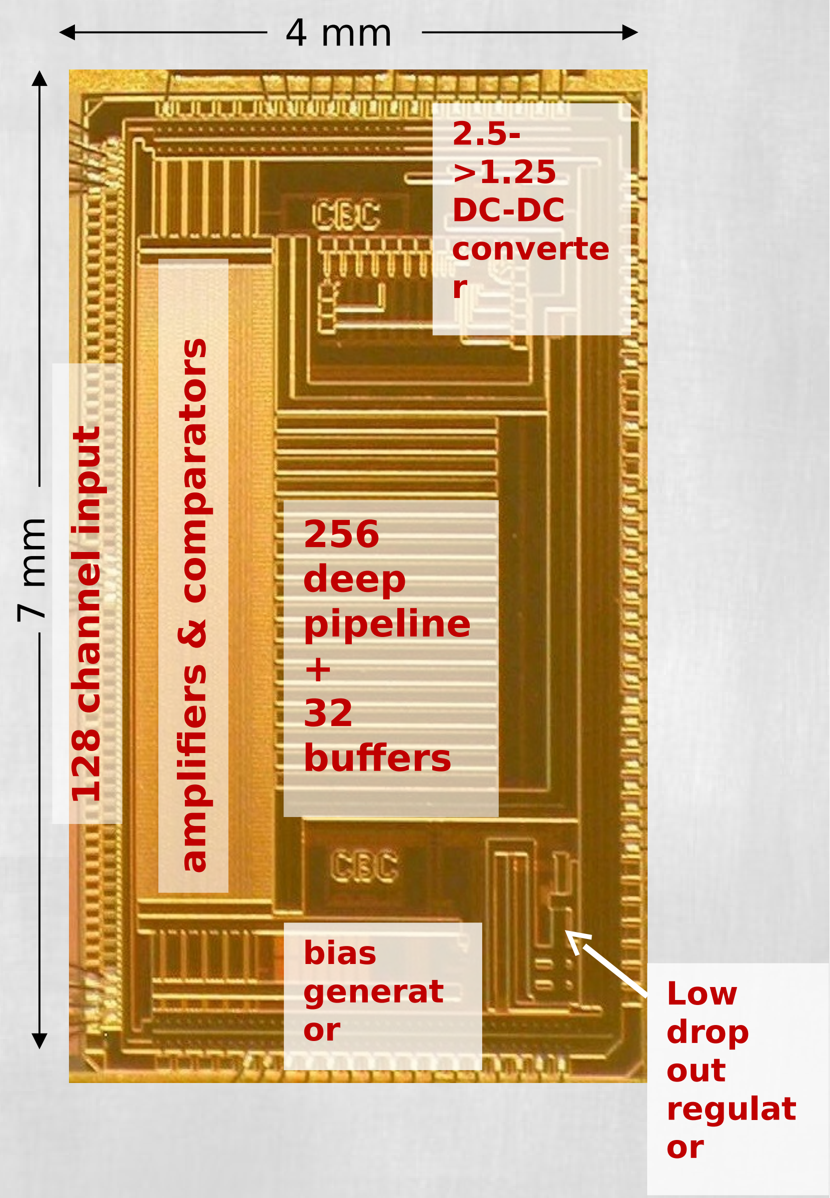
CMS





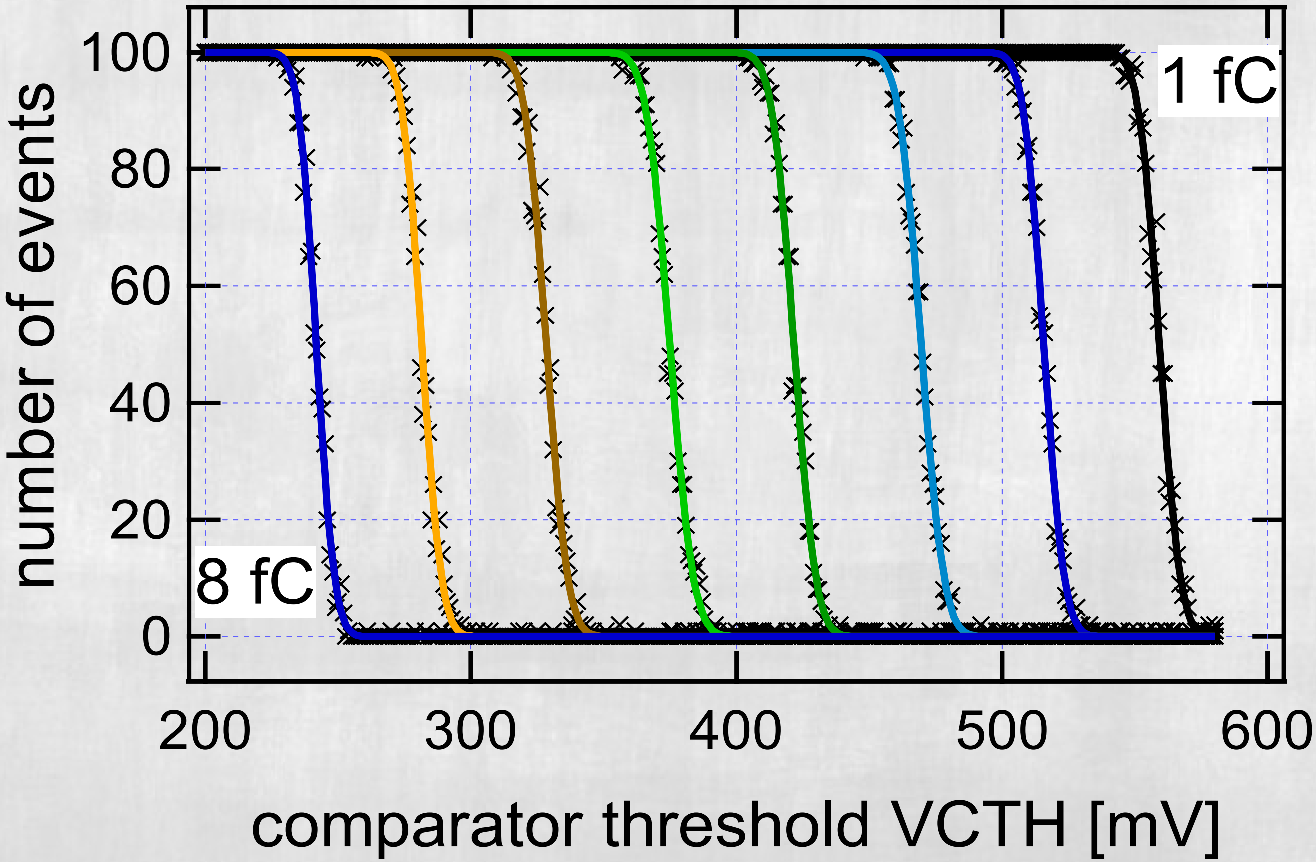
CBC v1 main features

- IBM 130nm CMOS process
- binary, un-sparsified architecture
  - retains chip and system simplicity
  - but no pulse height data
- designed for ~2.5 - 5cm µstrips < ~ 10 pF
- 128 channels, 50 mm pitch wire-bond
  - either polarity input signal
- **not contributing** to L1 trigger
- powering test features:
  - 2.5 -> 1.2 DC-DC converter
  - LDO regulator (1.2 -> 1.1) feeds analogue FE
- fast (SLVS) and slow (I2C) control interfaces



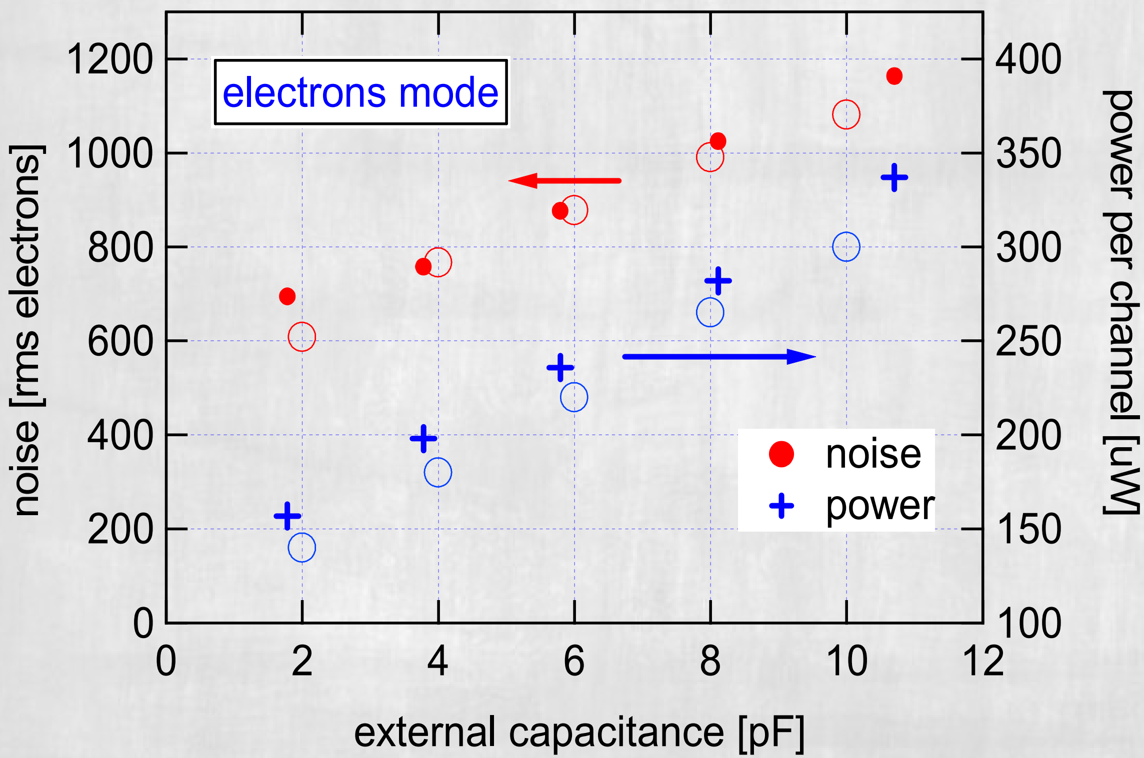
Binary chip qualification

S-curves: scans of threshold with a fixed test pulse
Then: vary test pulse
Can measure: pedestal, noise, gain

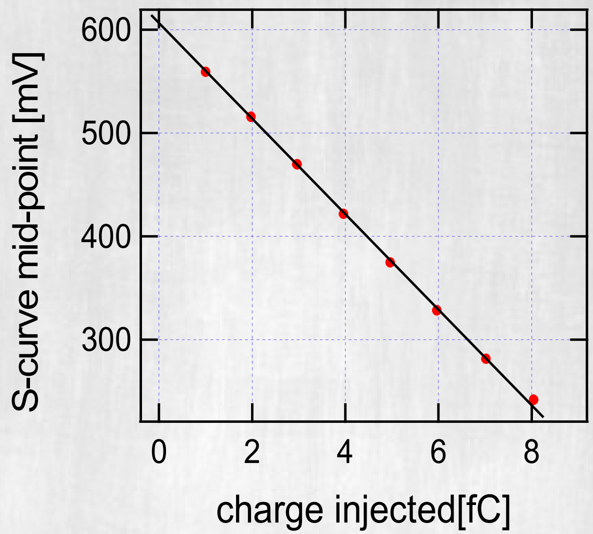


CBC v1 Prototype testing

e.g. for 5pF input capacitance:
noise: ~ 800 e_{RMS}
total power: < 300 μW/channel

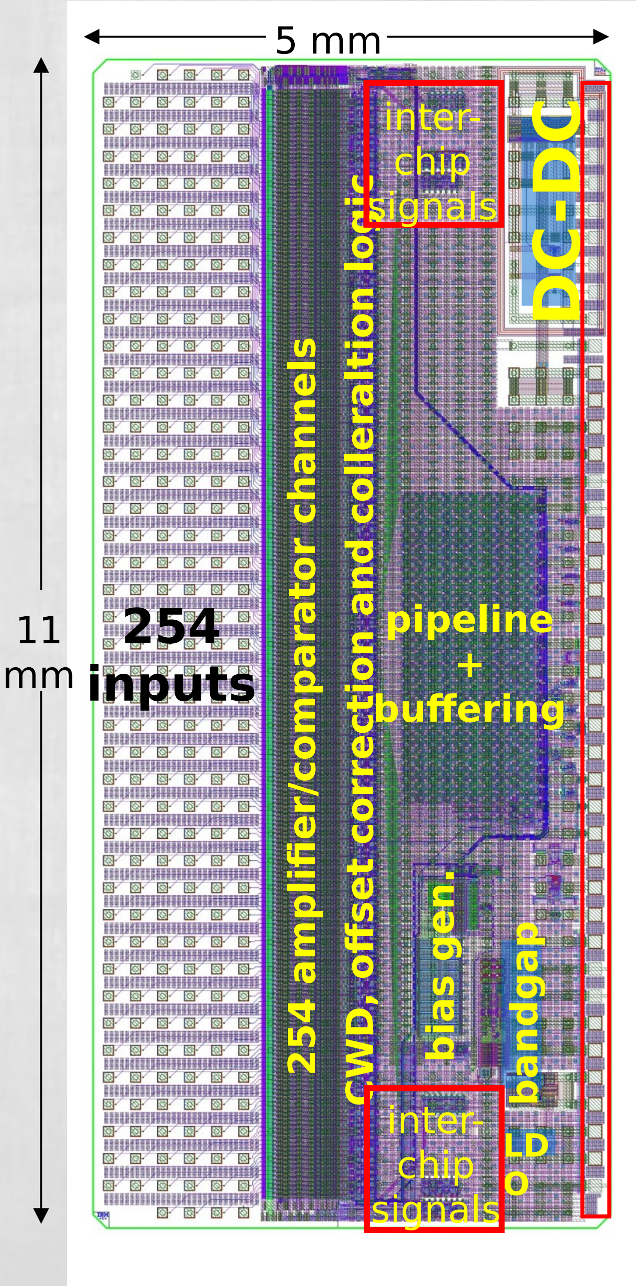


gain



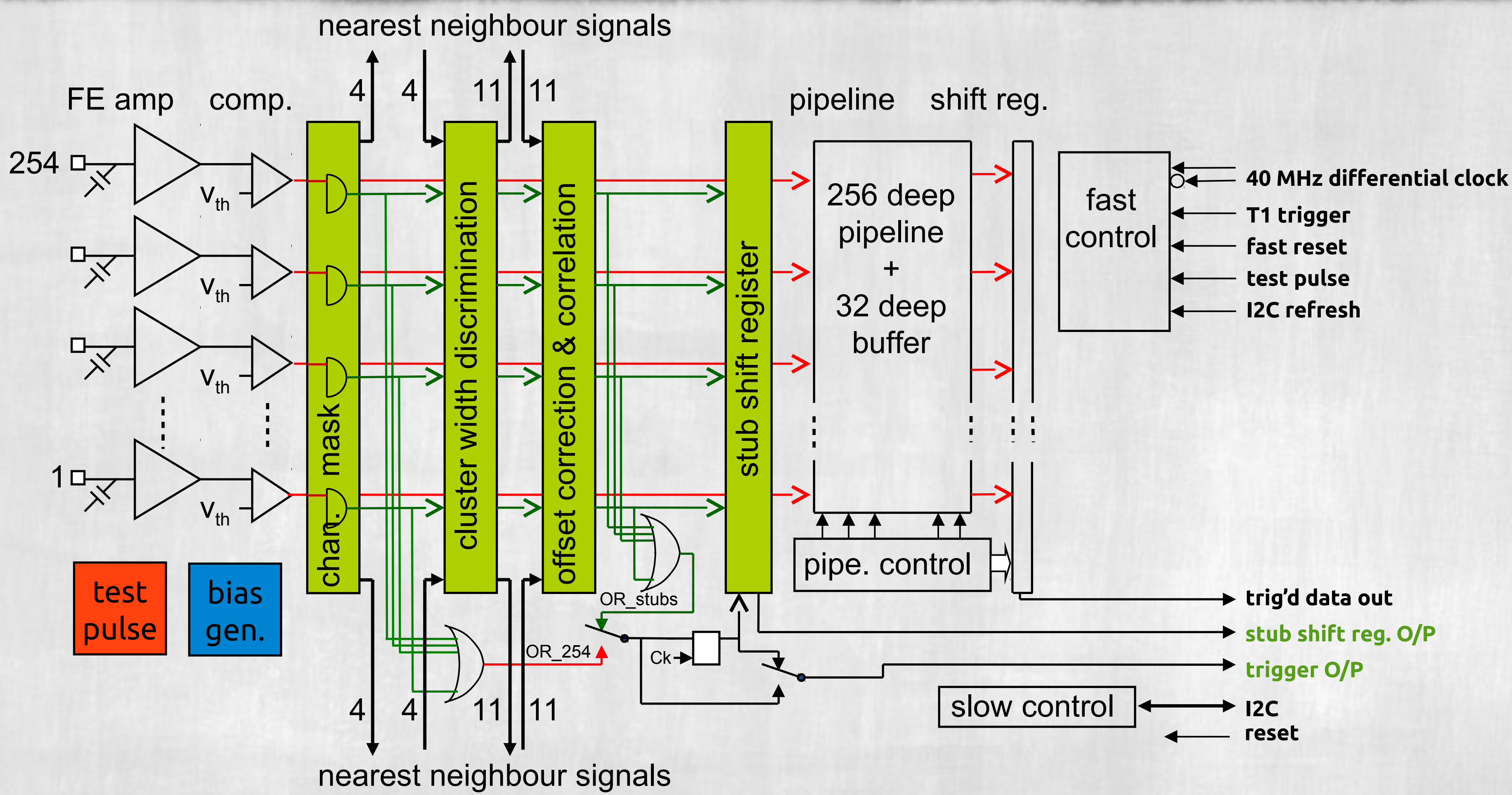
see: "M.Raymond et al 2012 JINST 7 C01033"
"W.Ferguson et al 2012 JINST 7 C08006"

CBC v2 new features



- 250μm pitch C4 layout: commercial standard
- 254 channels for 2 sensors (127 + 127 strips)
- Correlation (stub) logic
- Veto on wide clusters
- Improved DC/DC (CERN)
- Received Jan 2013 – fully functional

CBC v2 architecture



Front end, pipeline, L1 triggered readout, biasing from v1

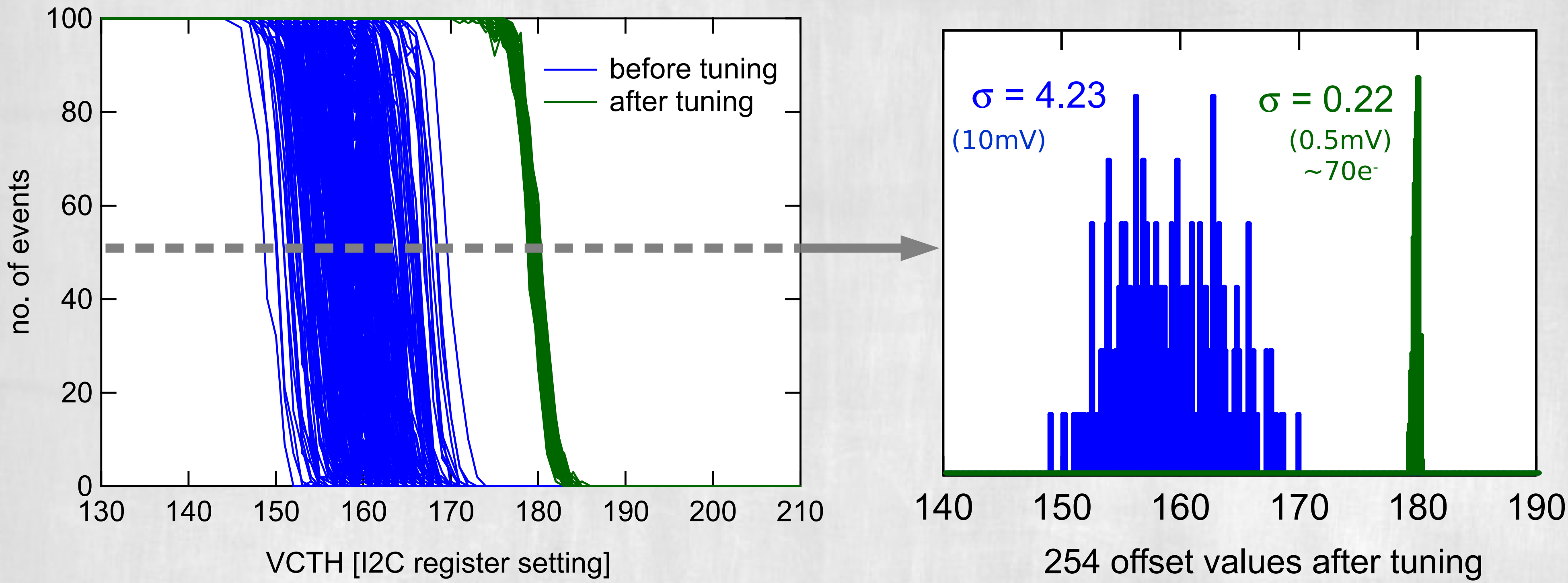
New blocks associated with Pt stub generation

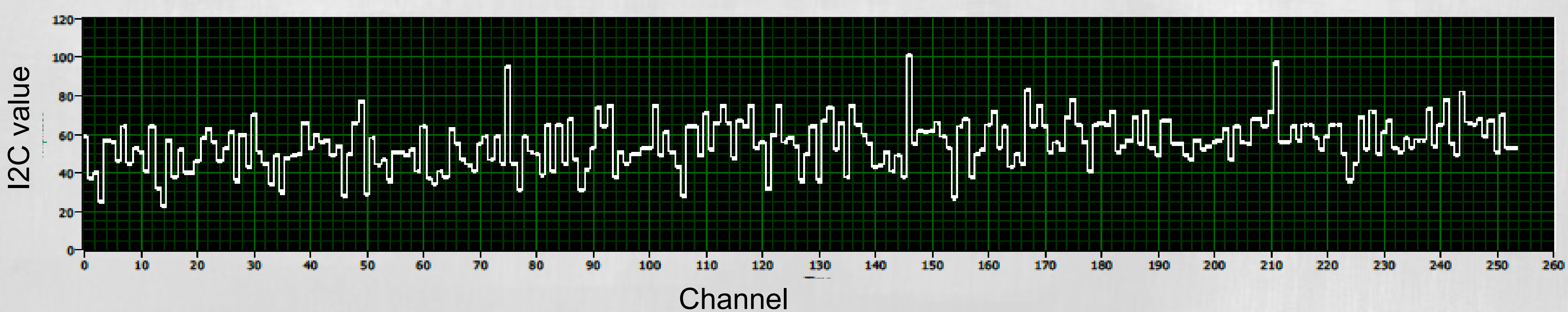
- **Channel mask**: block problem channels (not from L1 pipeline)
- **Cluster width discrimination**: exclude wide clusters > 3
- **Offset correction and correlation**: correct for phi offset across module and correlate between layers
- **Stub shift register**: test feature - shift out result of correlation operation at 40 MHz
- **Trigger O/P**: in normal operation 1 bit per BX indicates presence of high Pt stub

test pulse: charge injection to all channels (8 groups of ~32), programmable timing and amplitude

S-curves and tuning

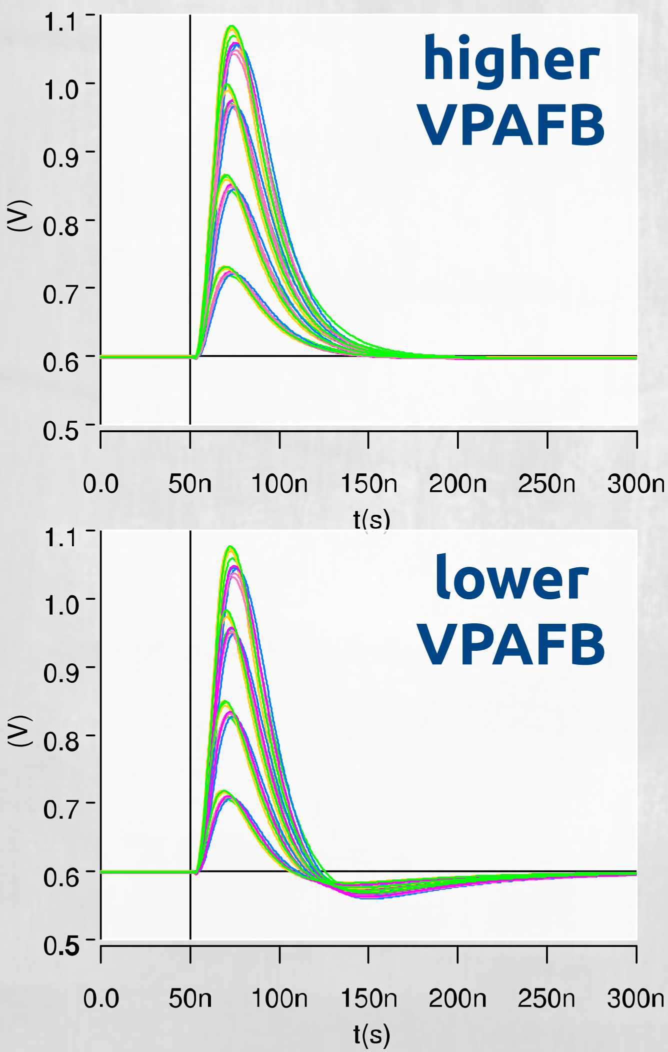
S-curve: measurement of noise and pedestal with on-chip test pulse

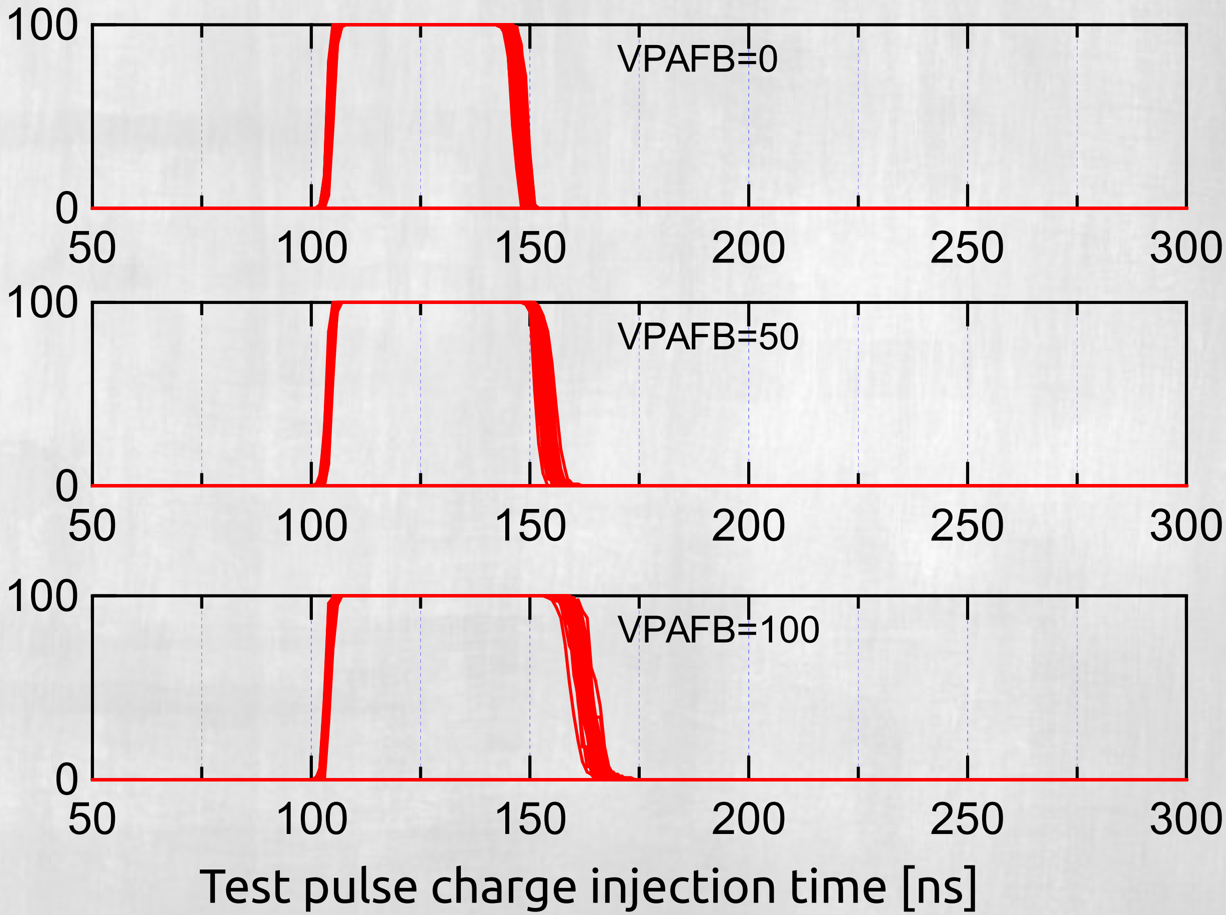




Taming large signals: post-amp

Post-amplifier reduces pulse duration dependence to signal amplitude. Can be tuned (VPAFB). Price to pay?

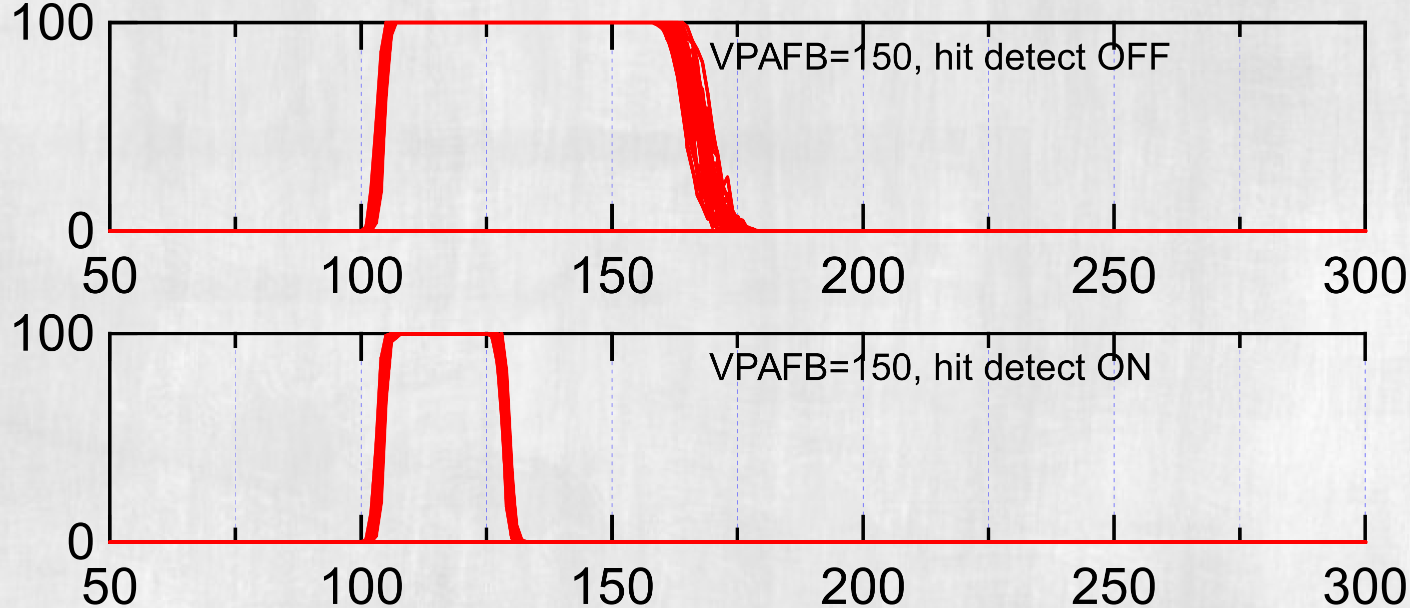




Charge injected ~ 2 fC – Threshold ~ 1 fC

Taming large signals: hit detect

Hit detect circuit: only single hit in pipeline irrespective of how long comparator output stays high



Test pulse charge injection time [ns]

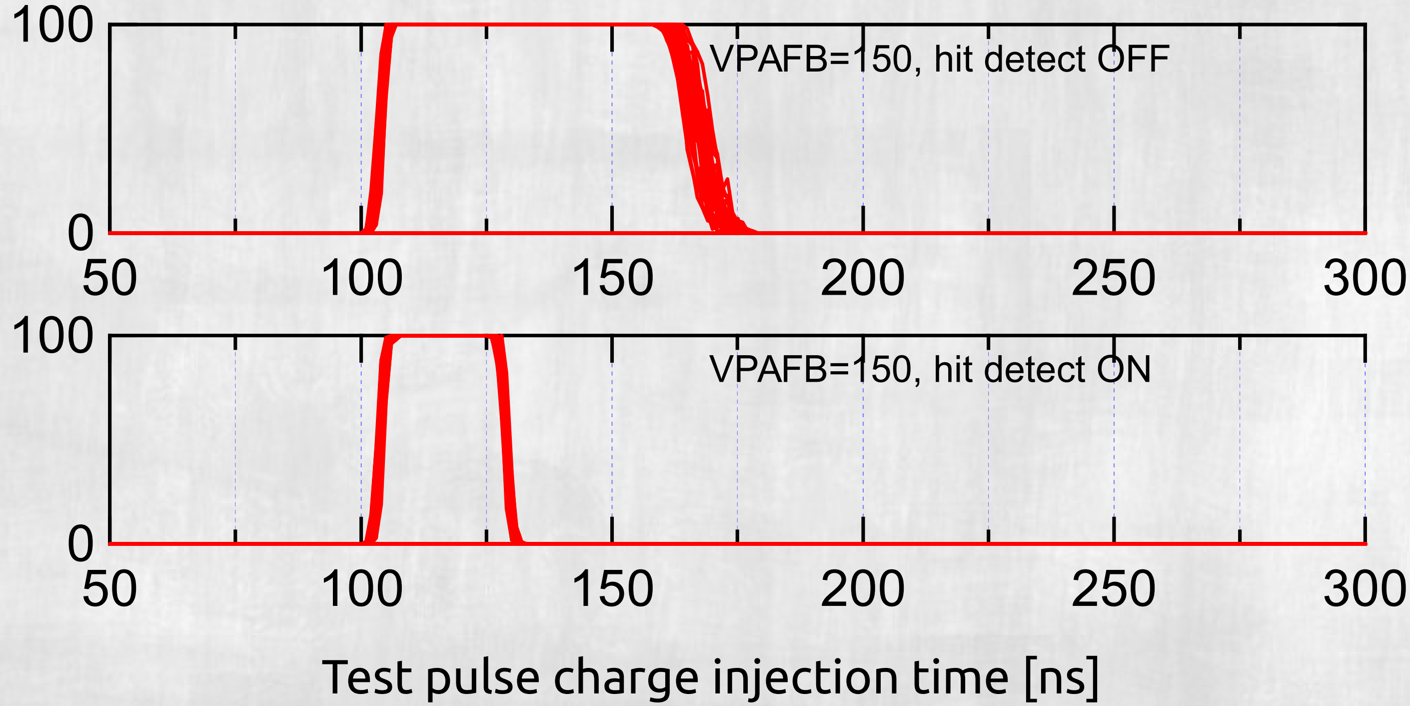
Charge injected ~ 2 fC – Threshold ~ 1 fC

Price to pay: inefficiency

How much?

Taming large signals: hit detect

Hit detect circuit: only single hit in pipeline irrespective of how long comparator output stays high



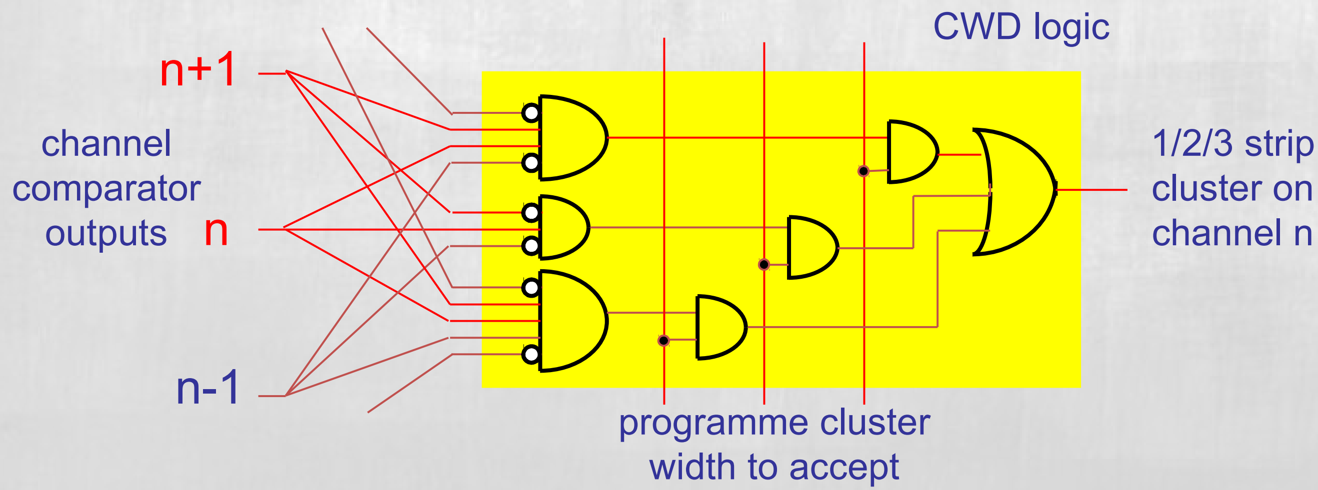
Charge injected ~ 2 fC – Threshold ~ 1 fC

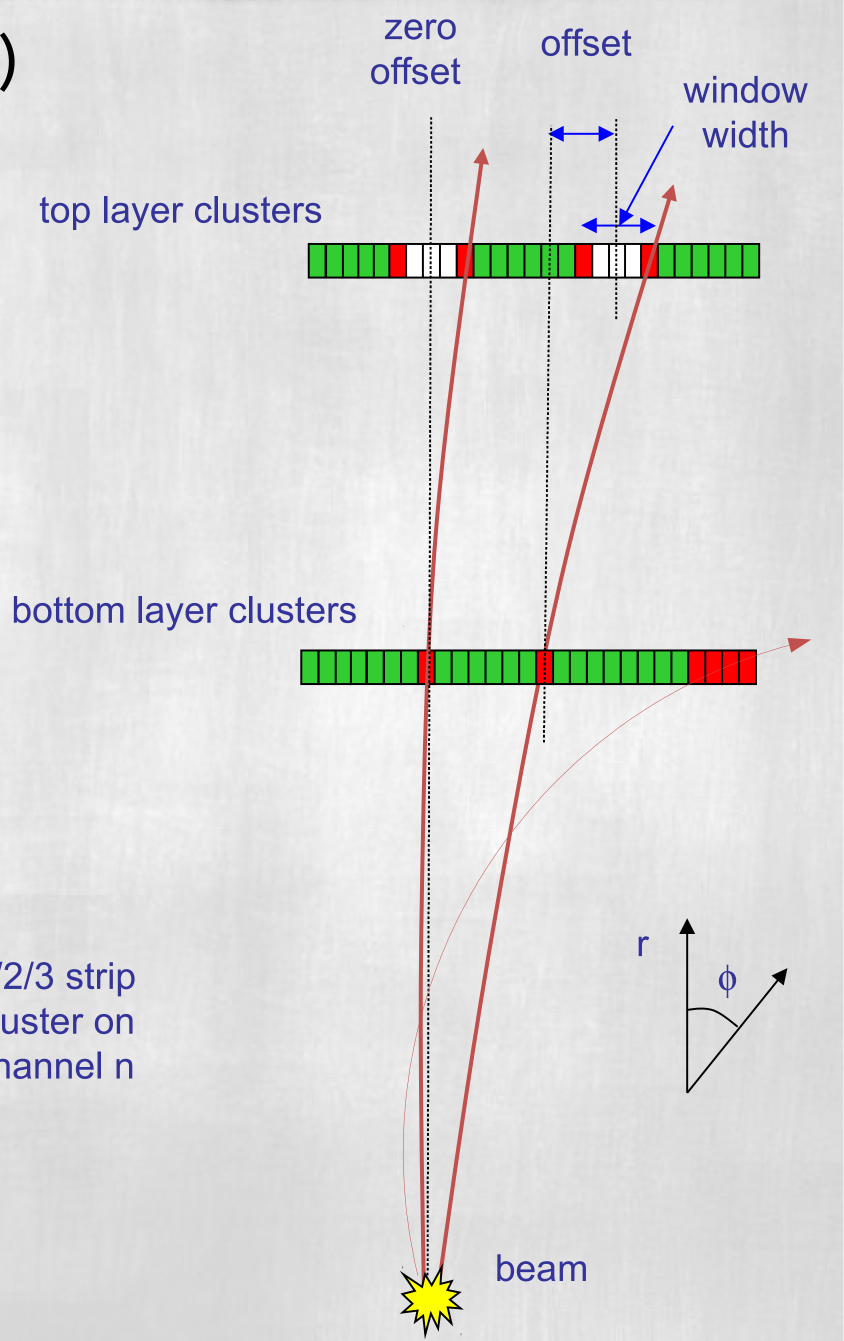
Price to pay: inefficiency

Small: inefficiency = occupancy^2

CBC v2 stub finding logic

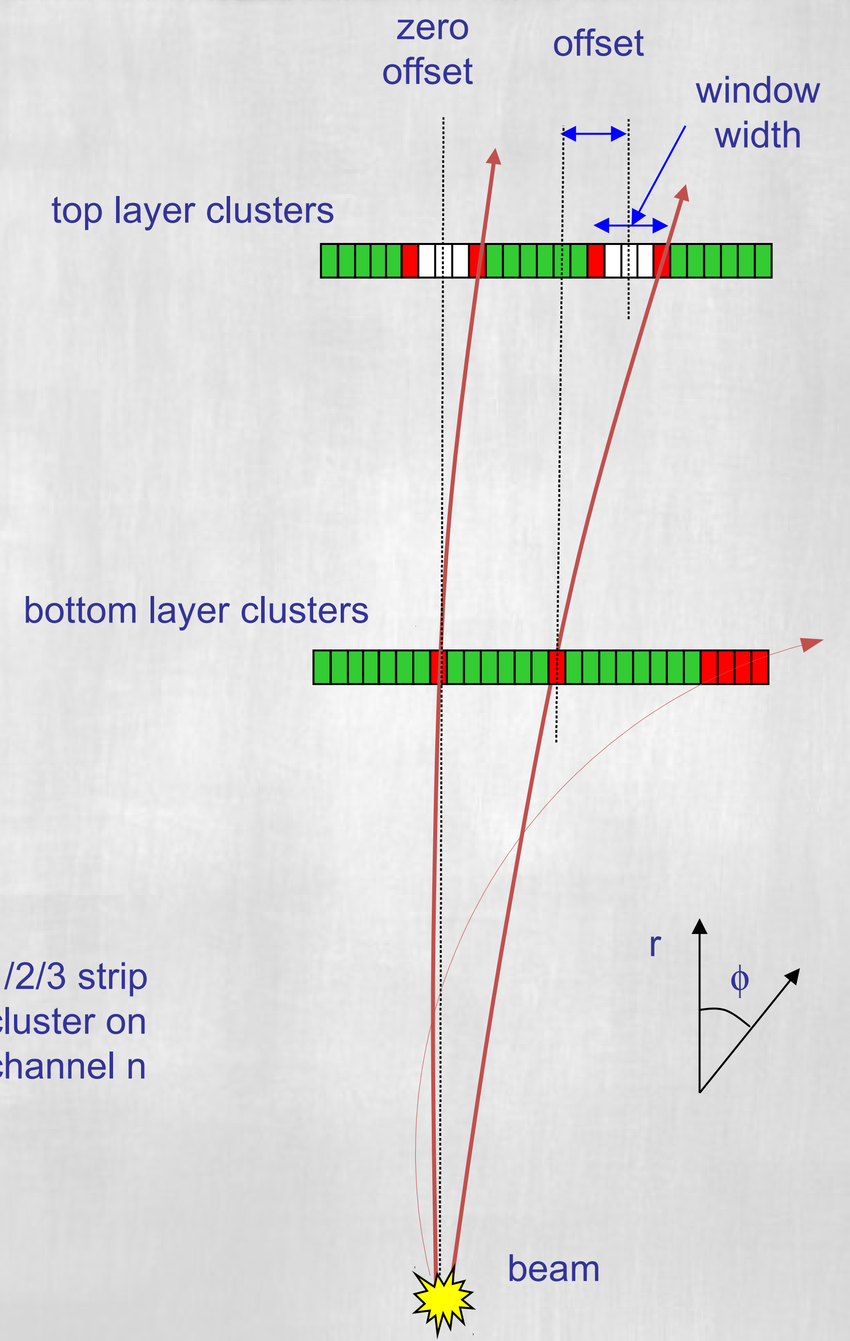
- **Cluster Width Discrimination** logic (CWD)
  - ...
  - ...
- **Offset correction**
  - ...
  - ...
- **Cluster matching**
  - ...
  - ...

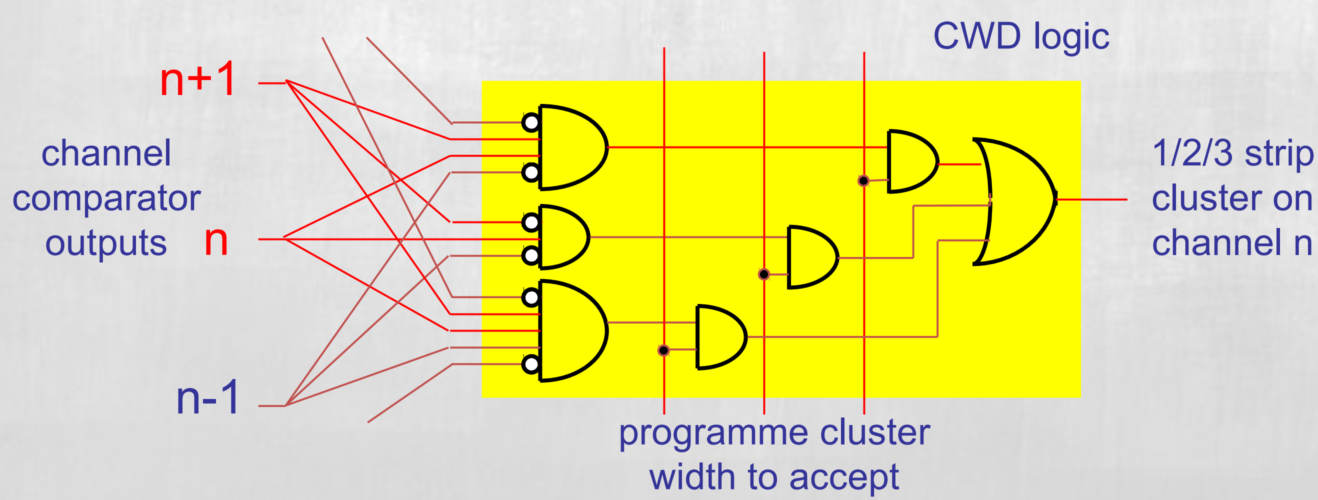




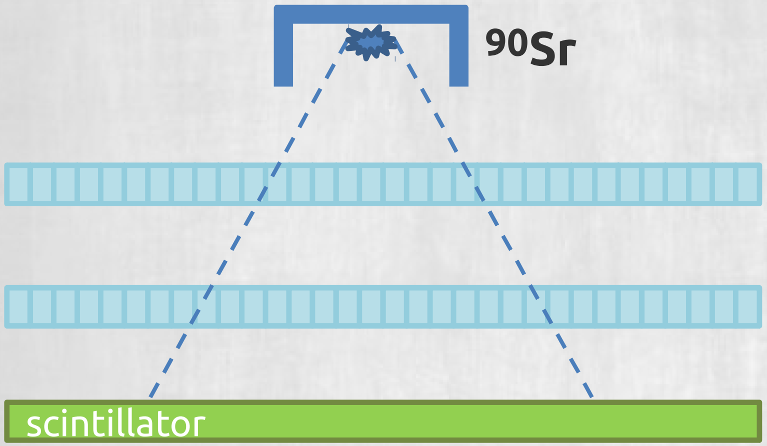
CBC v2 stub finding logic

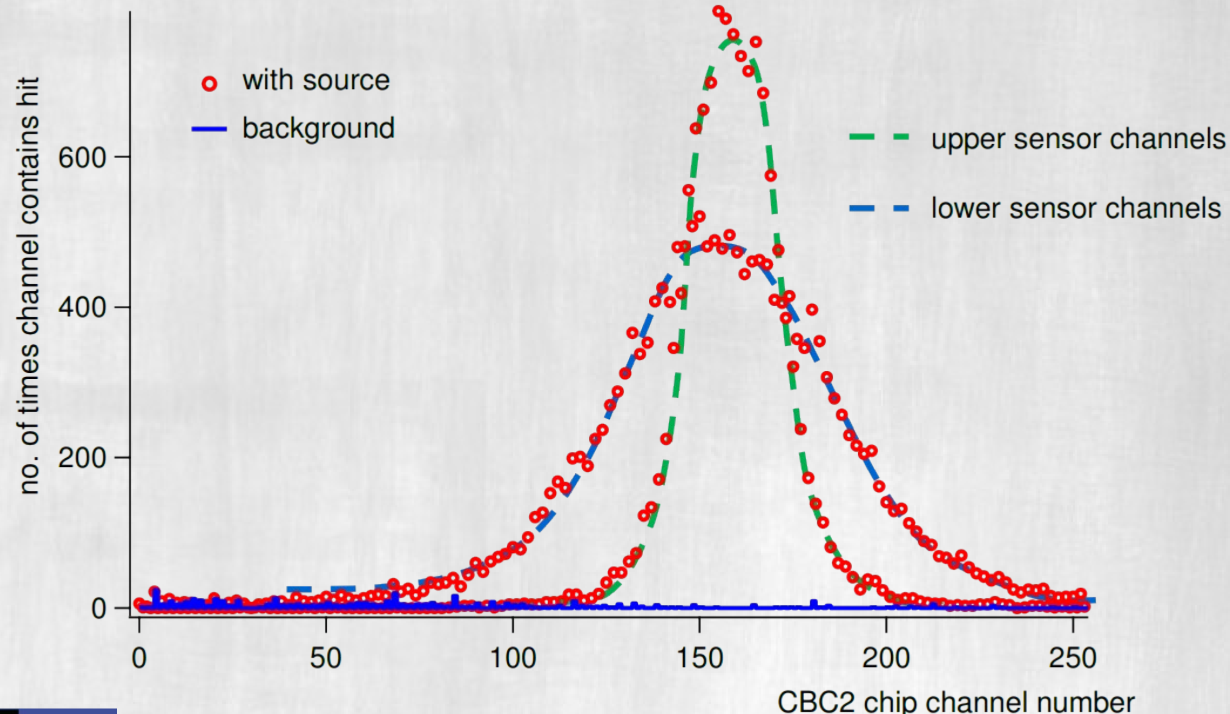
- **Cluster Width Discrimination** logic (CWD)
  - wide clusters not consistent with high p_T track
  - exclude clusters width > **3 channels**
- **Offset correction**
  - lateral displacement of window across chip
  - programmable up to **± 3 channels**
- **Cluster matching**
  - Window width controls pT cut
  - programmable up to **± 8 channels**

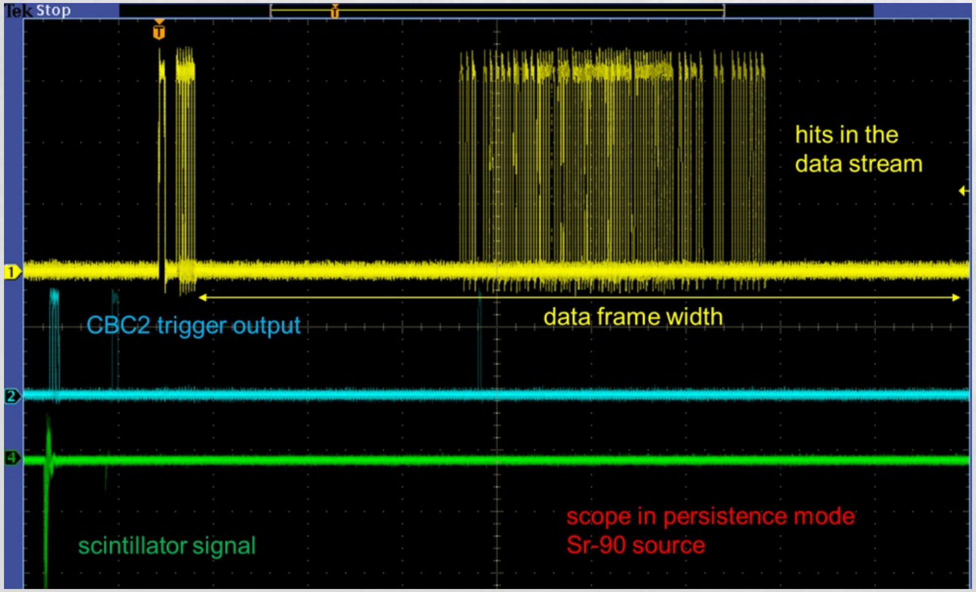


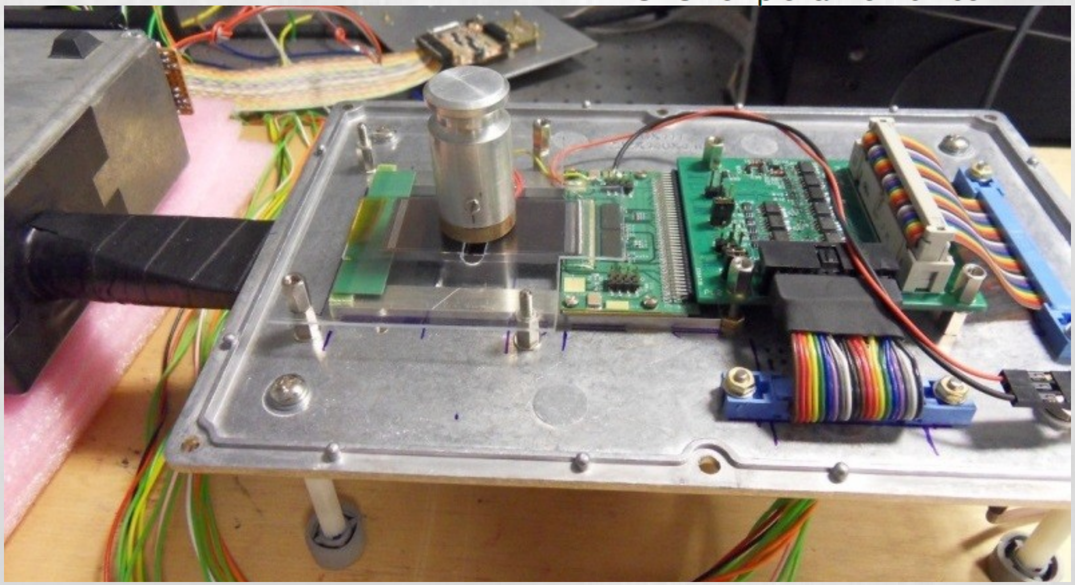


CBC v2 test with source



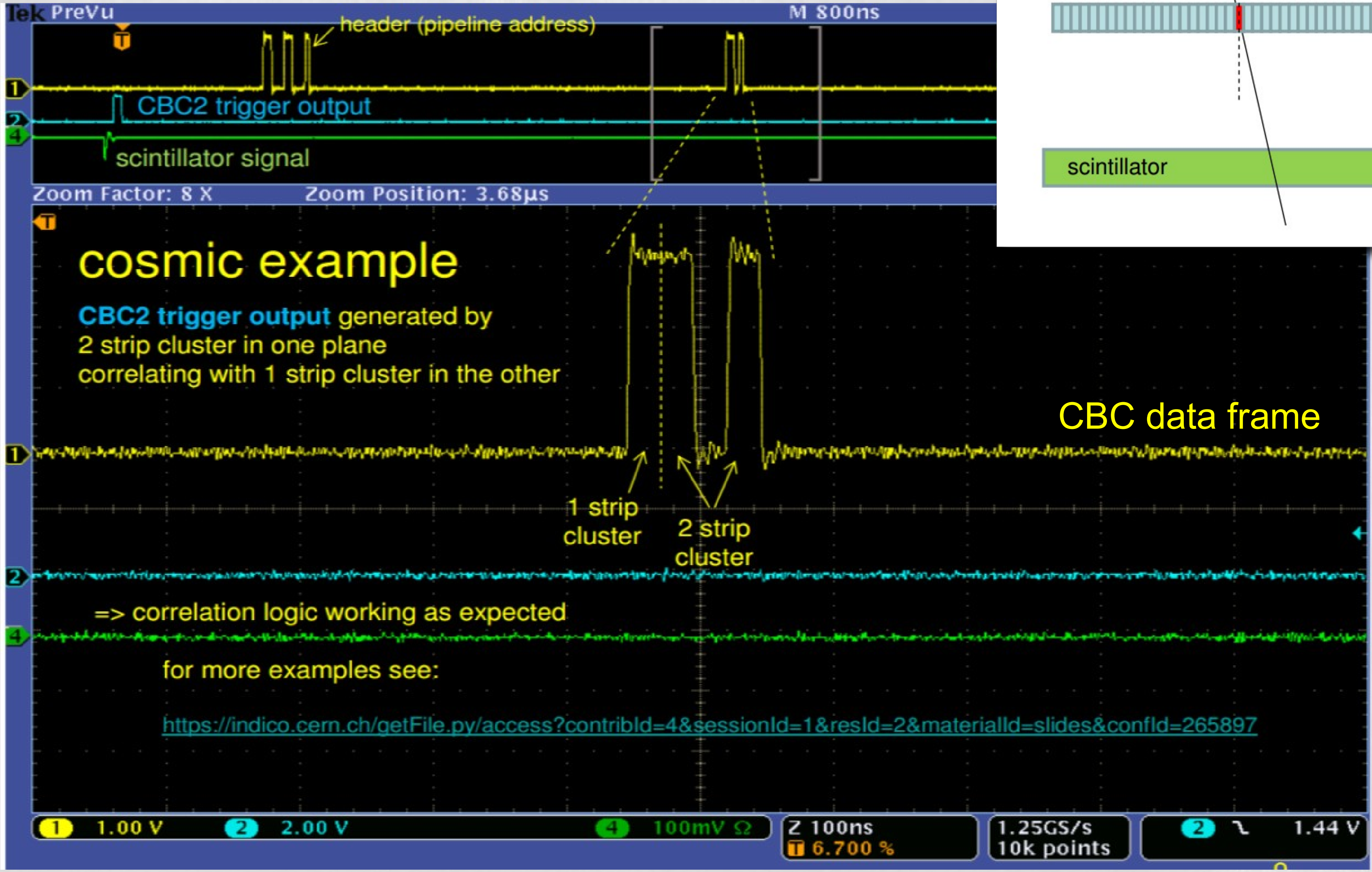


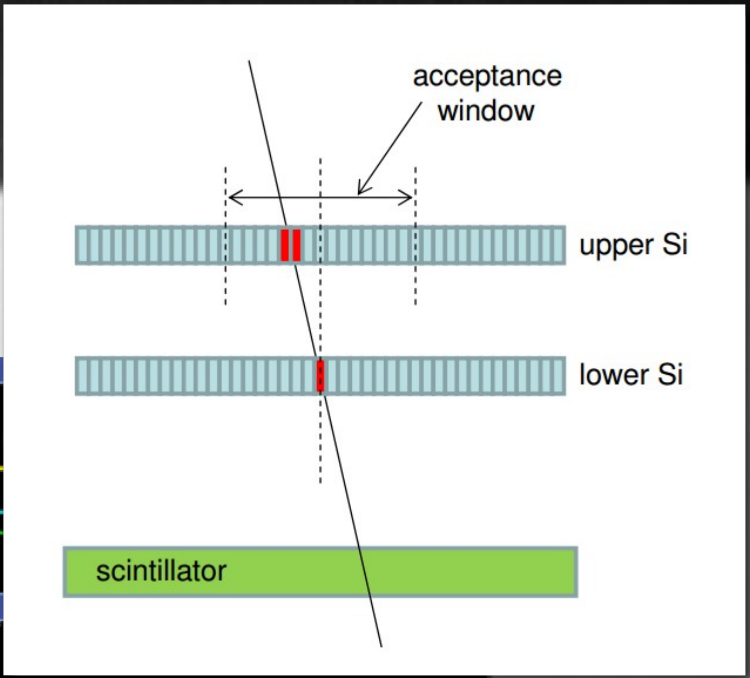




CBC v2 test with cosmics

...and patience! Rate << 1 Hz even with large hit matching windows



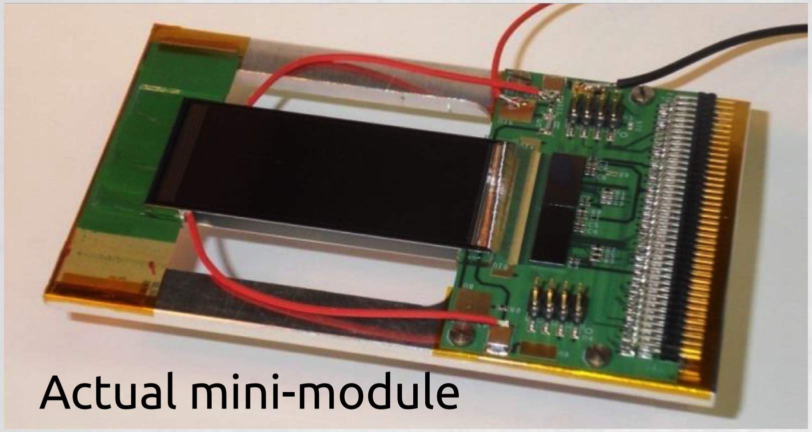


CBC v3 waiting

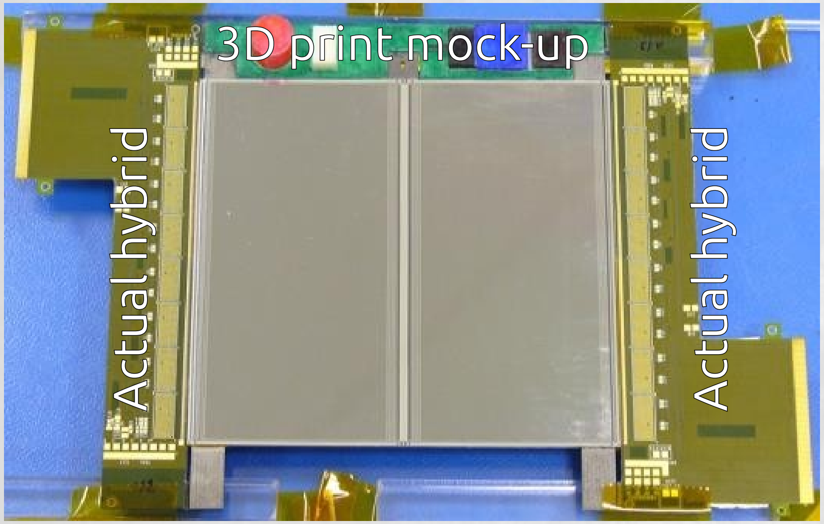
Some of the specifications are **fixed**, some are **possibly still open**:

- Optimized for **5 cm strips** (possibly longer), **AC coupled**, **n-on-p**
- Stub data definition
  - **½ strip cluster resolution**
  - **Cluster size cut 3 → 4**
  - **8b address (for ½ strip resolution) of cluster in bottom layer**
  - **5b for stub bend information (rough p_T)**
- Stub data formatting & transmission
  - **13b/stub, up to 3 stubs/BX ⇒ 39 bits**
  - **+1 bit un-sparsified L1 triggered readout data**
- **Designed for final trigger rate & latency**
- Other useful features
  - **Priority encoding of Pt stubs (if desired)**
  - **e.g. slow ADC to monitor bias levels**
  - **...**

CMS module prototypes



2xCBC functional module:
- 2 chips (instead of 8)
- Electrical readout (instead of optical)
- No data concentration
- Rigid hybrid
+ Stub-finding logic
+ Nominal noise and thresholds

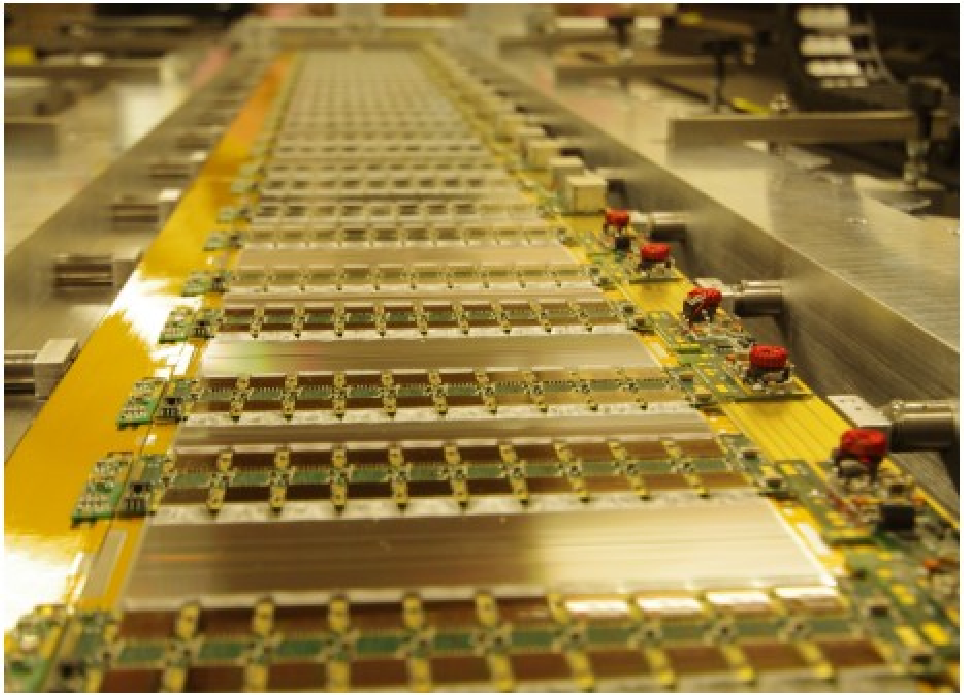


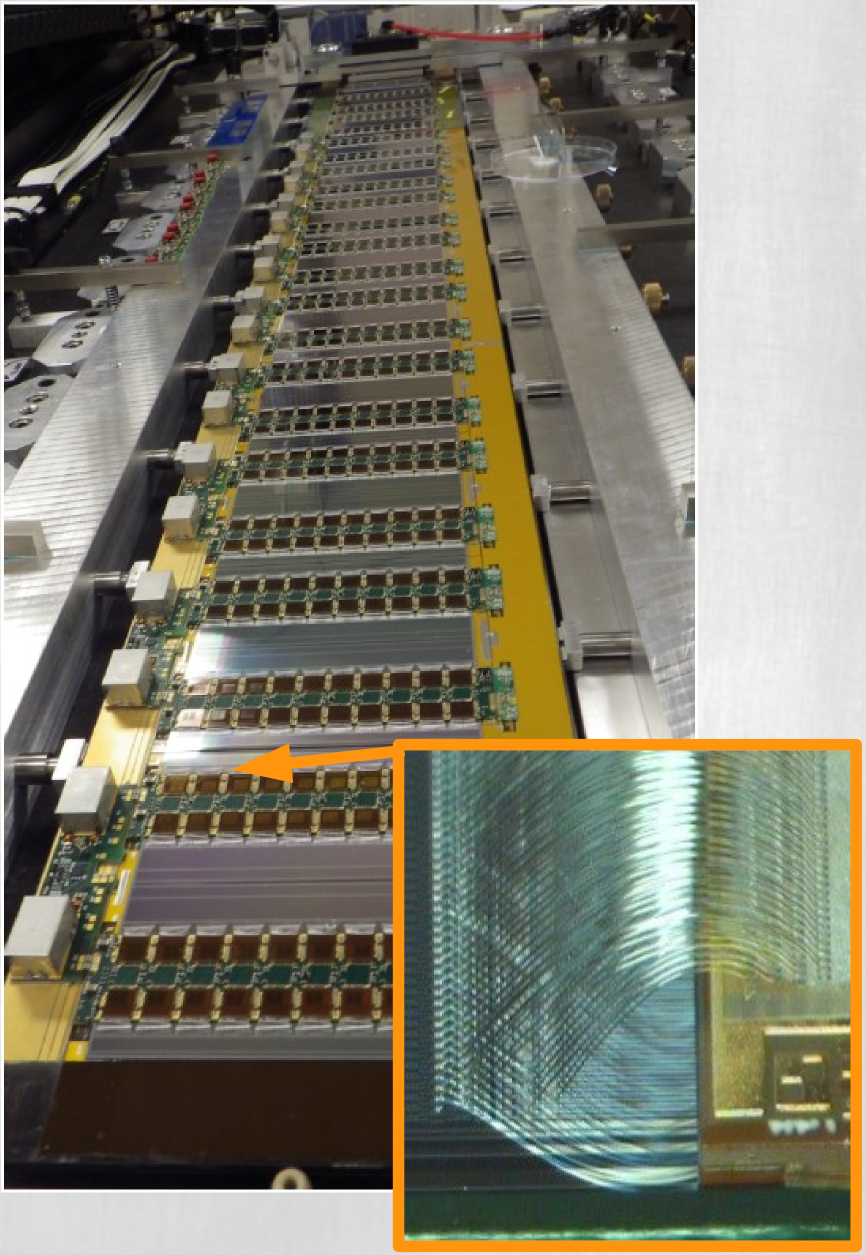
8xCBC prototype:
+ 2x8 chips
- Electrical readout (instead of optical)
- No data concentration
+ Flex-hybrid
+ Stub-finding logic
Just produced

Prototype readout format **defined**

Data concentrator will be produced later fitting both PS and 2S modules

ATLAS module prototypes

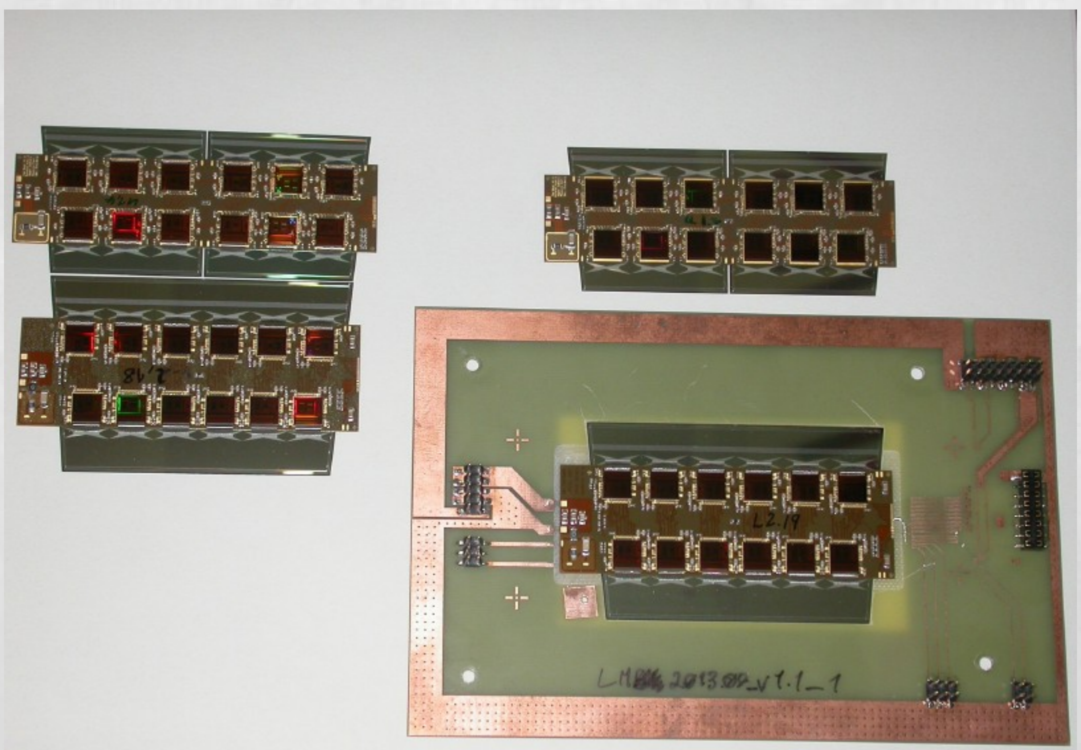


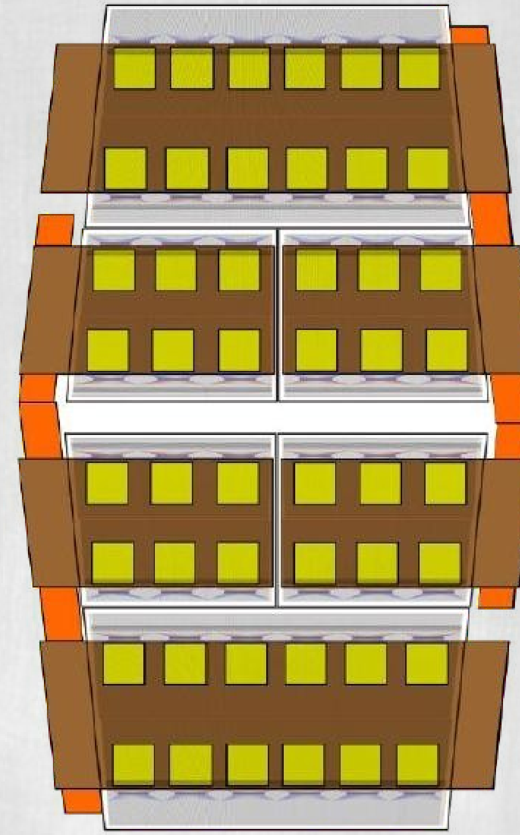


Fully populated
DC-DC powered ABC(250nm) stave
in December 2013
New 130nm currently under
evaluation

ATLAS petalet hybrids

- 1 lower and 2 upper hybrids designed and produced
  - Population with passive components
  - ASIC assembly with flip-chip bonder
- Noise:
  - Upper and lower hybrids have noise of ~380 ENC
  - Lower modules have noise of ~660 ENC





Outline of the lesson

~~Silicon strip tracking detectors~~

~~Front-end signal processing~~

~~Examples of detector design~~

➡ Real-time tracking

Outline of the lesson

~~Silicon strip tracking detectors~~

~~Front-end signal processing~~

~~Examples of detector design~~

Real-time tracking ?

Outline of the lesson

~~Silicon strip tracking detectors~~

~~Front-end signal processing~~

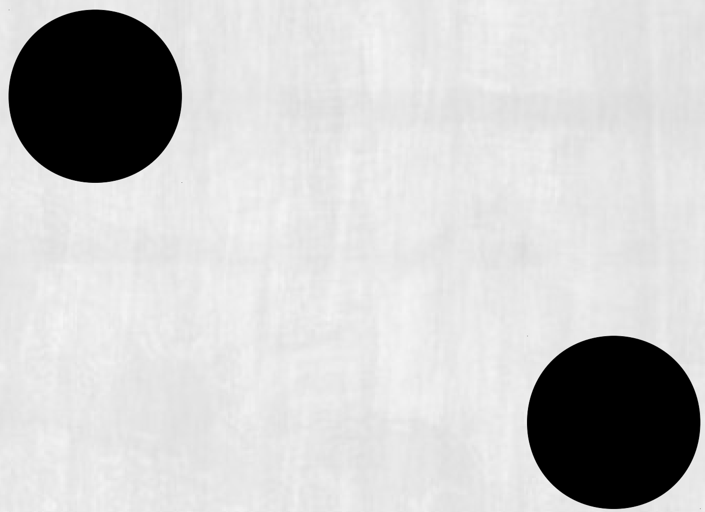
~~Examples of detector design~~

→ Real-time tracking

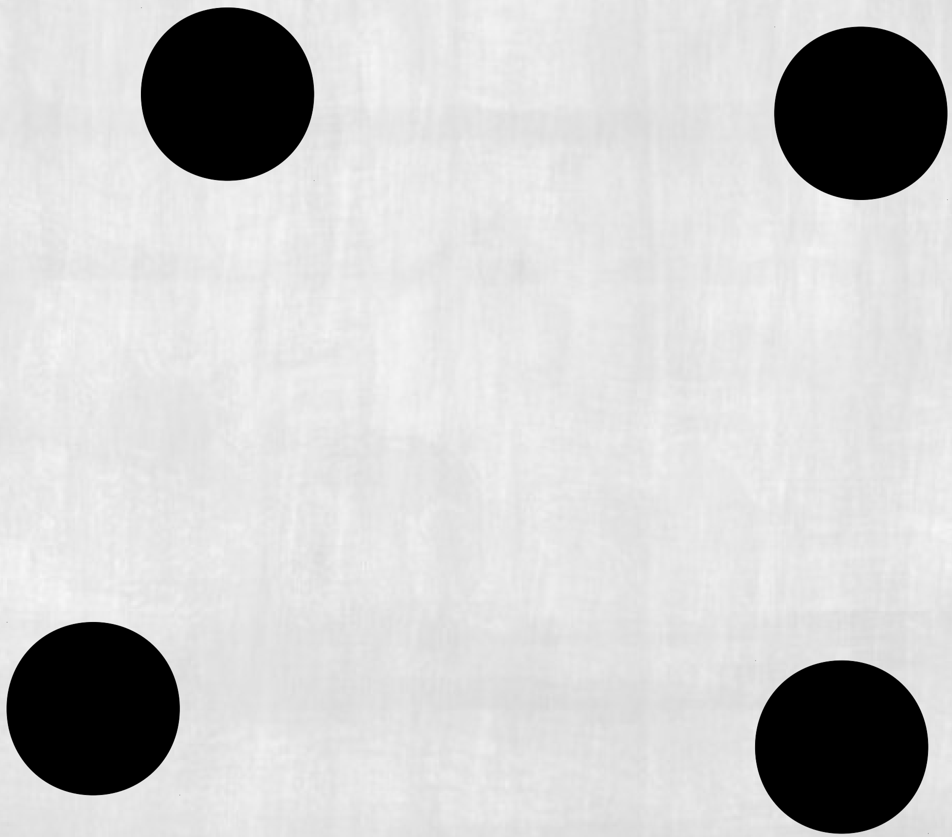
? ?

Please count the dots

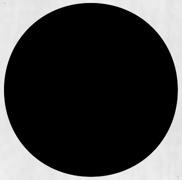
As fast as you can…



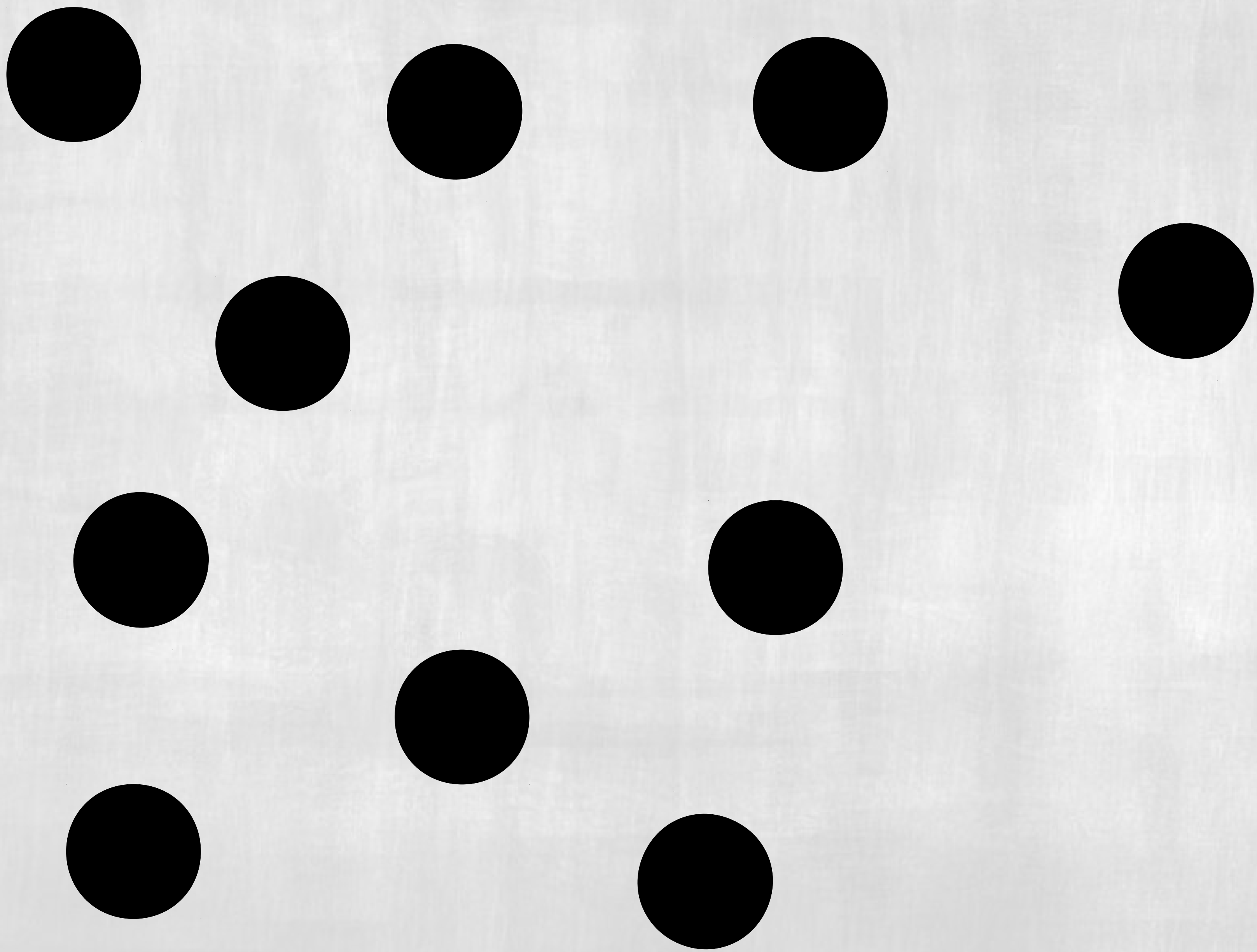
Please count the dots



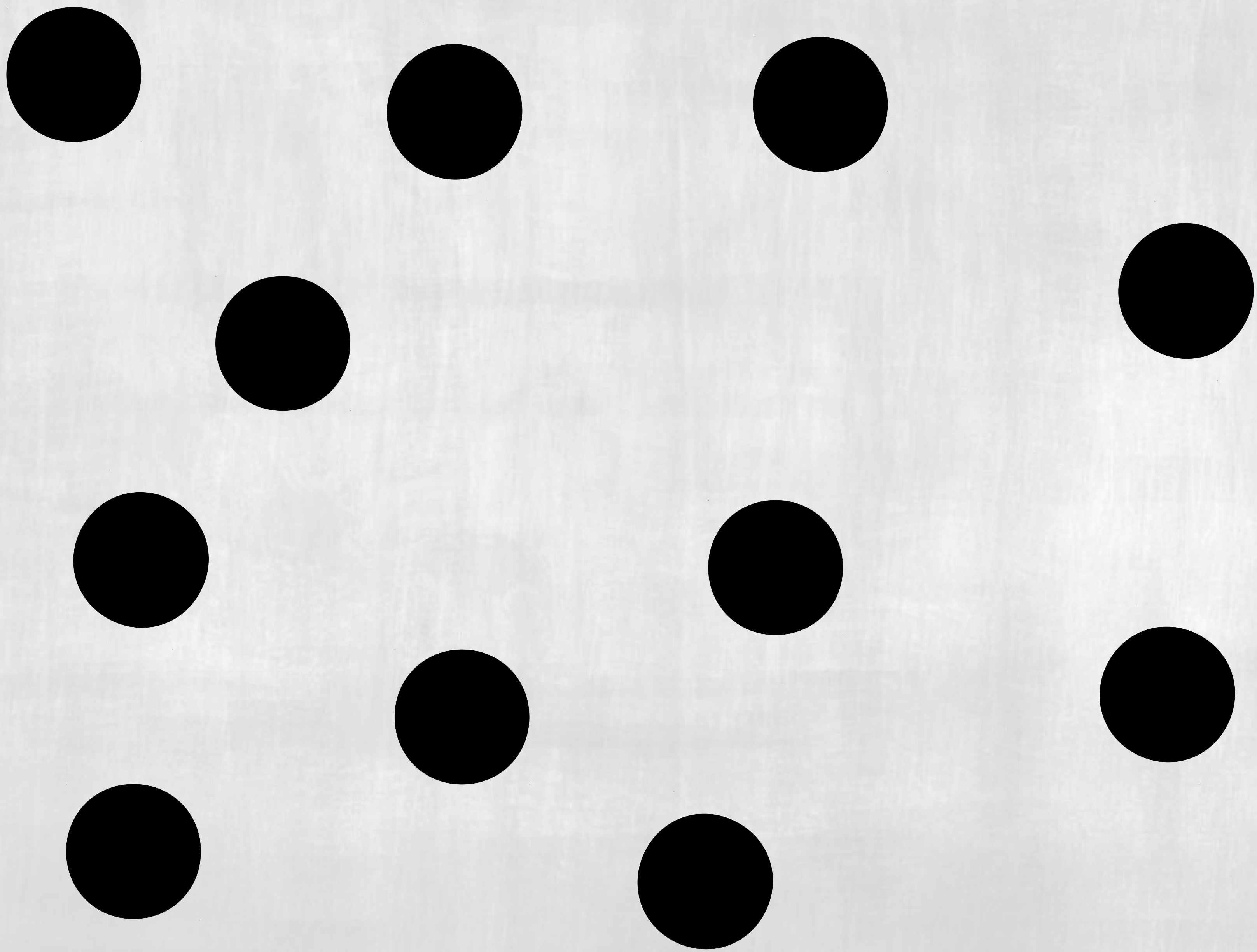
Please count the dots



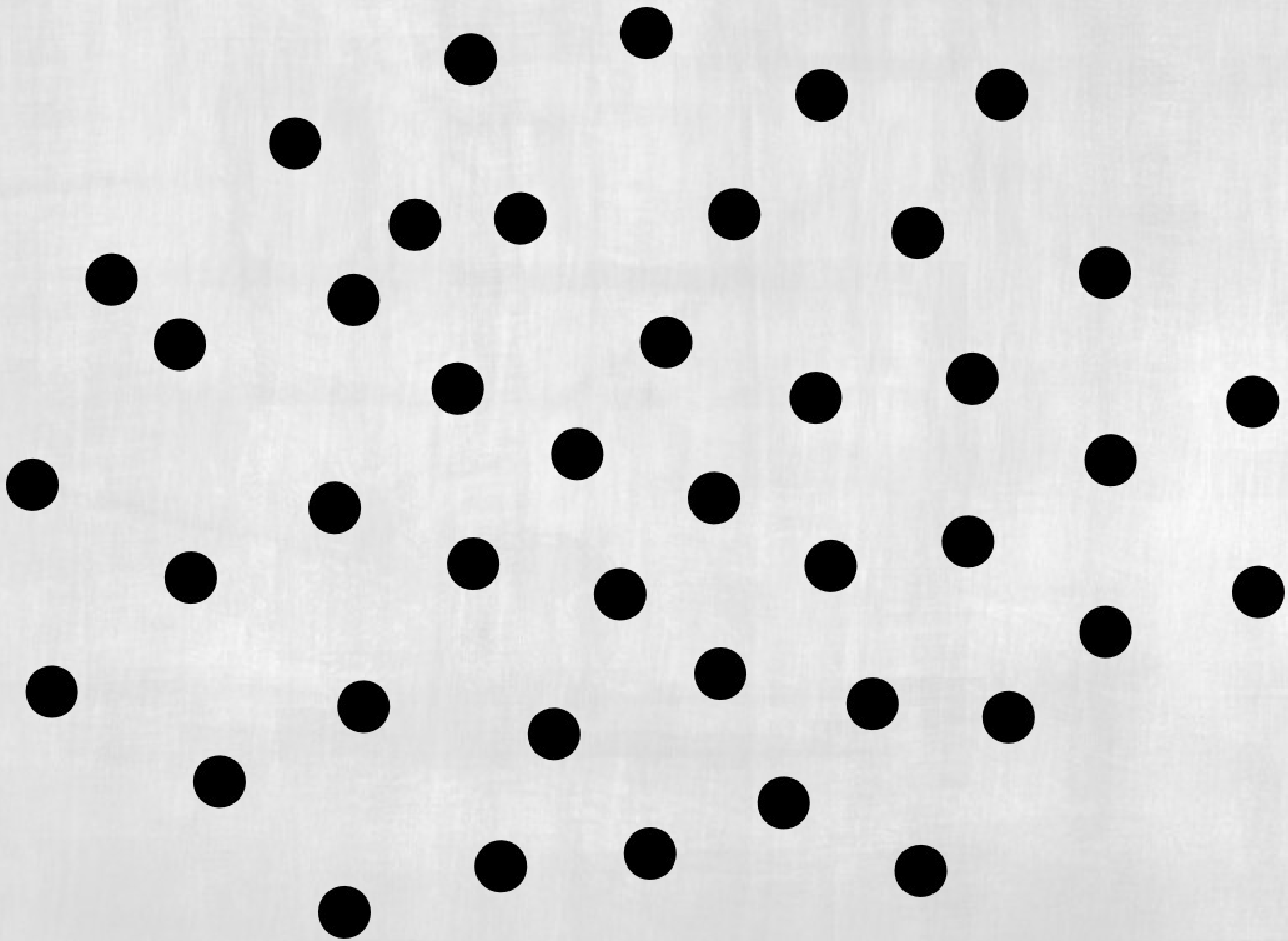
Please count the dots



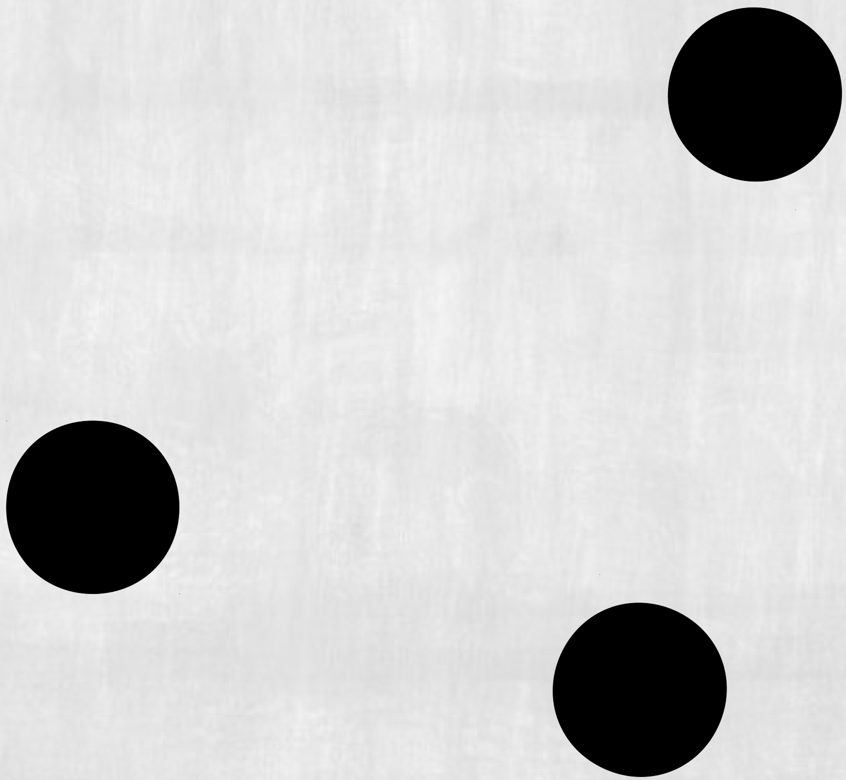
Please count the dots



Please count the dots



Please count the dots



Please count the dots

Bravo!

Please count the dots

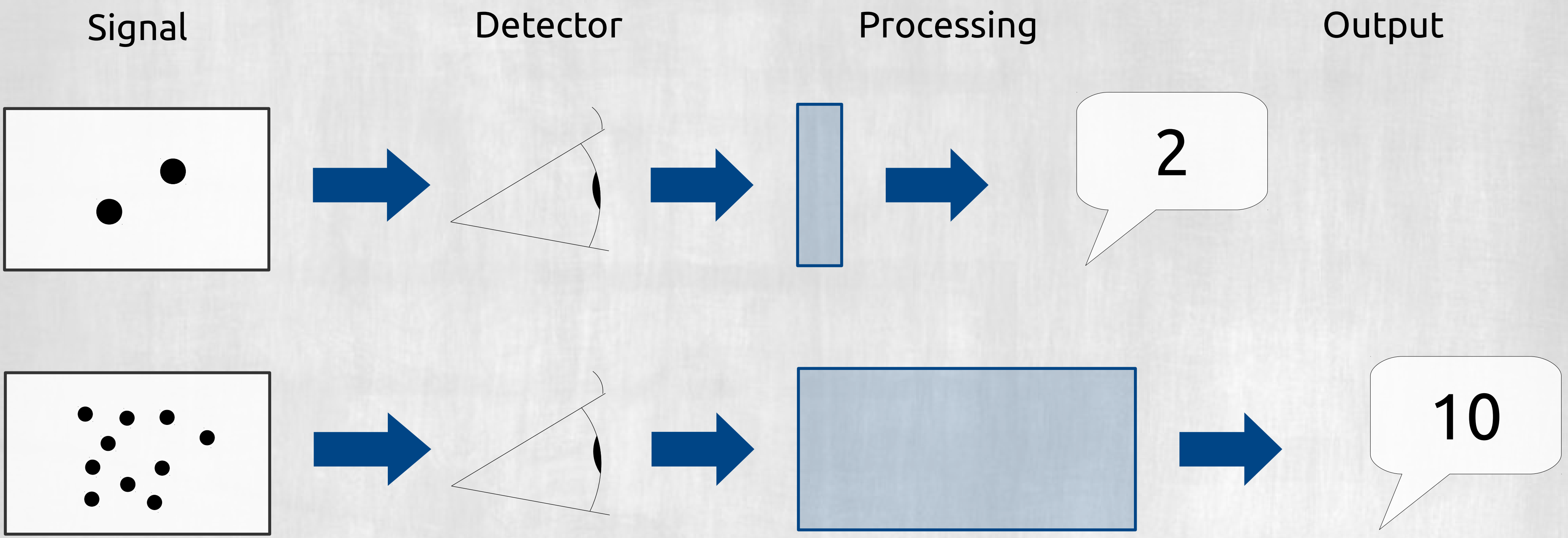
Bravo!

1 dot

Experimental findings

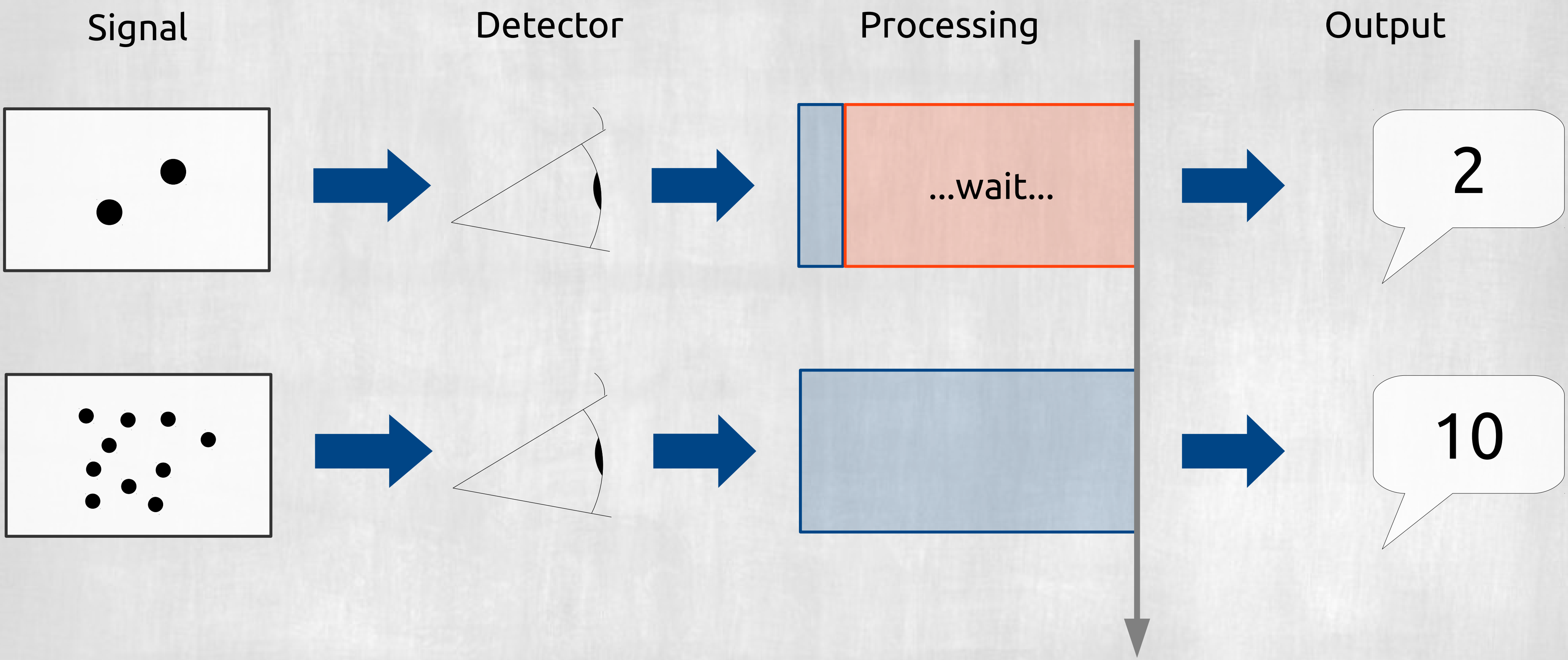
- What did you notice?
- What do you think is the meaning of “real time”?

Variable latency

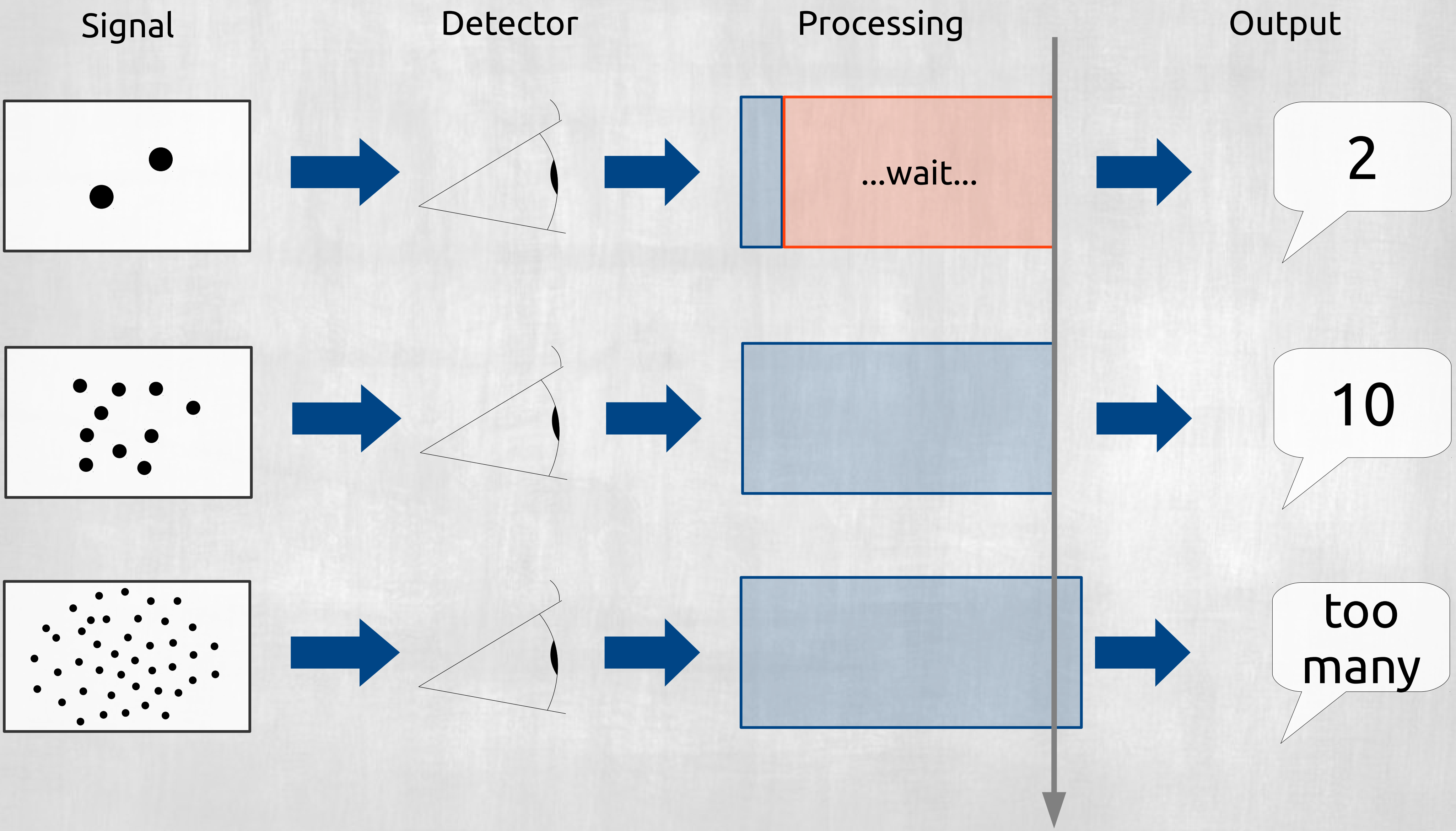


How to fix this?

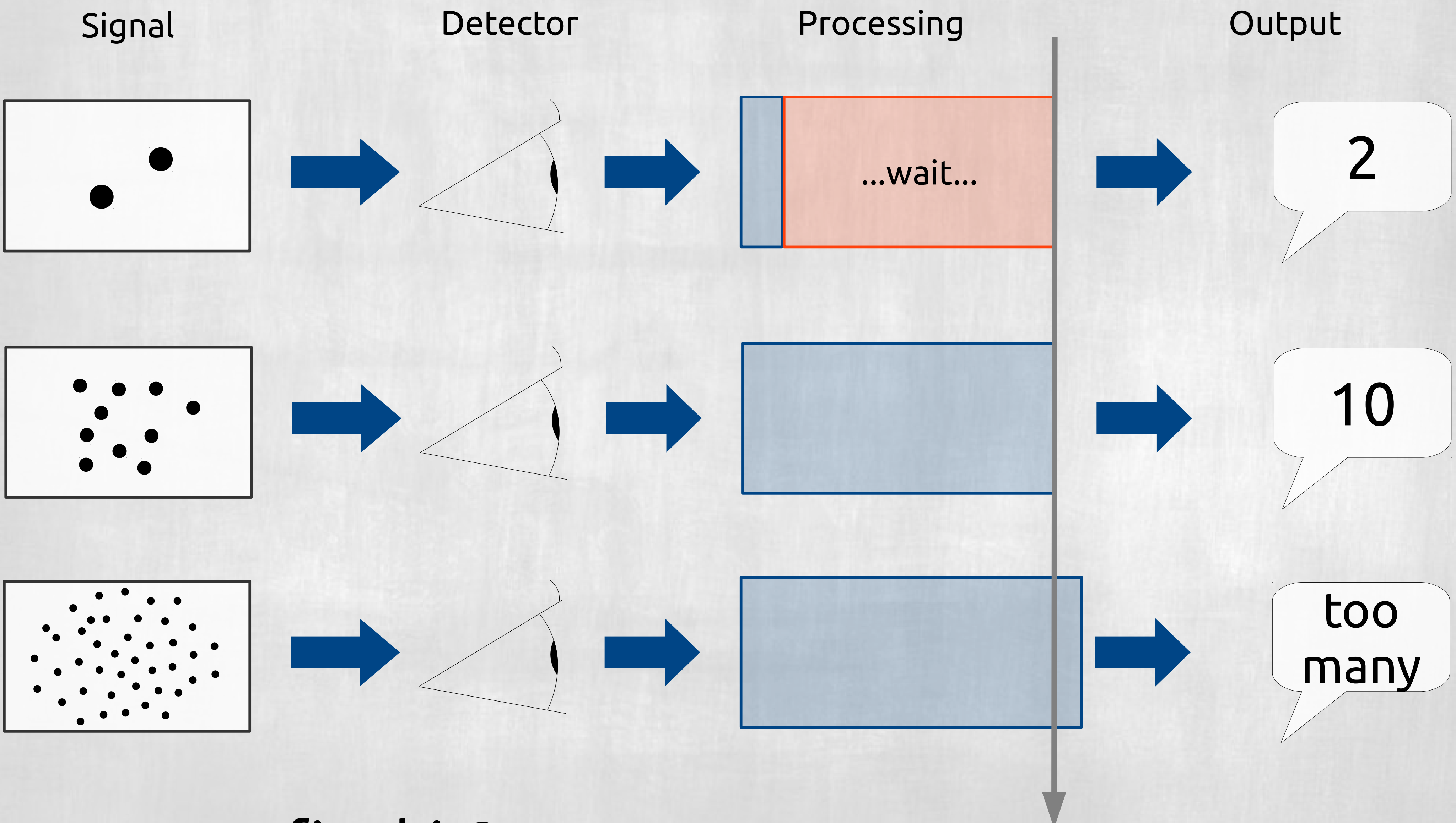
Variable latency



Variable latency

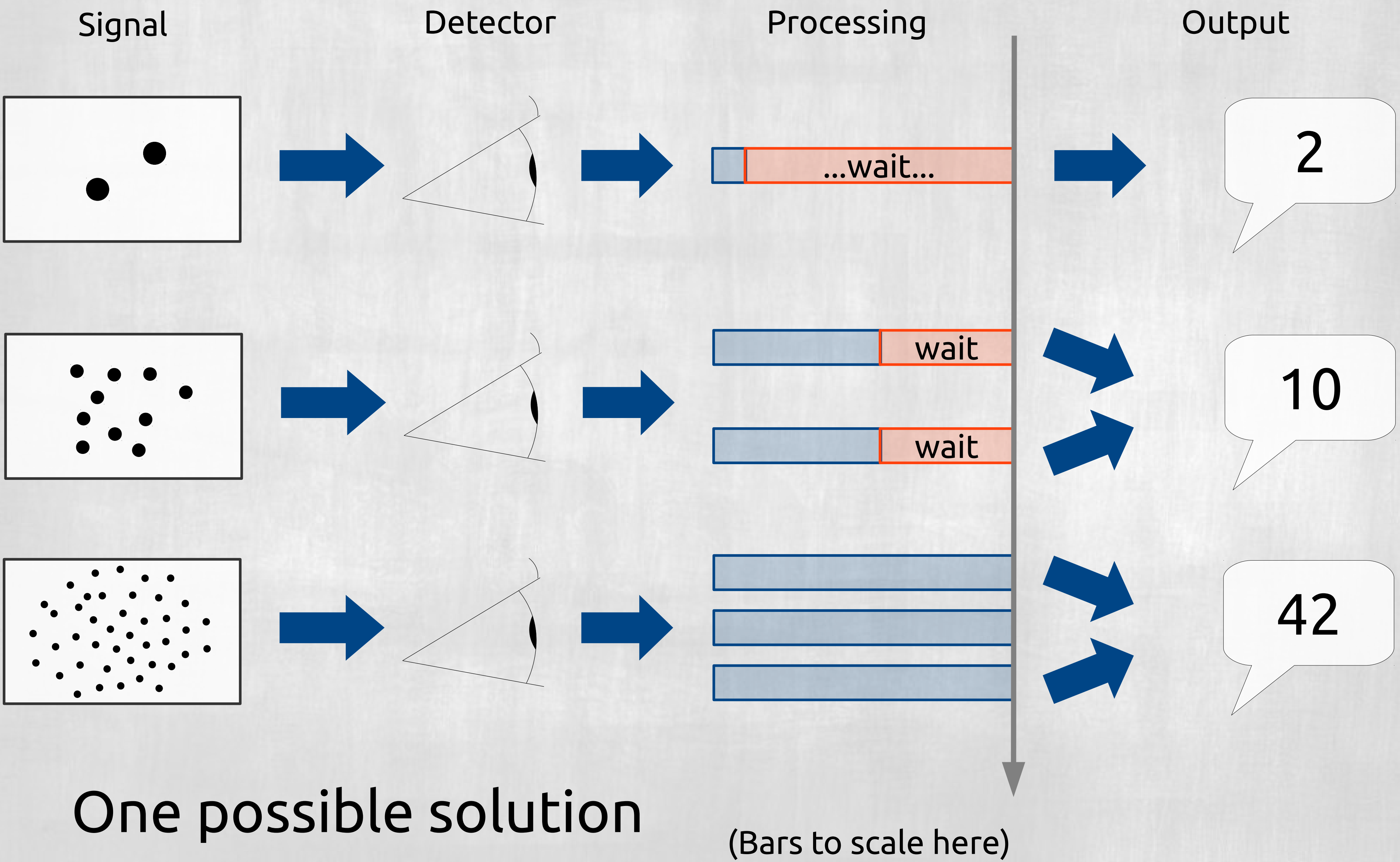


Variable latency



How to fix this?

Variable latency: load balancing



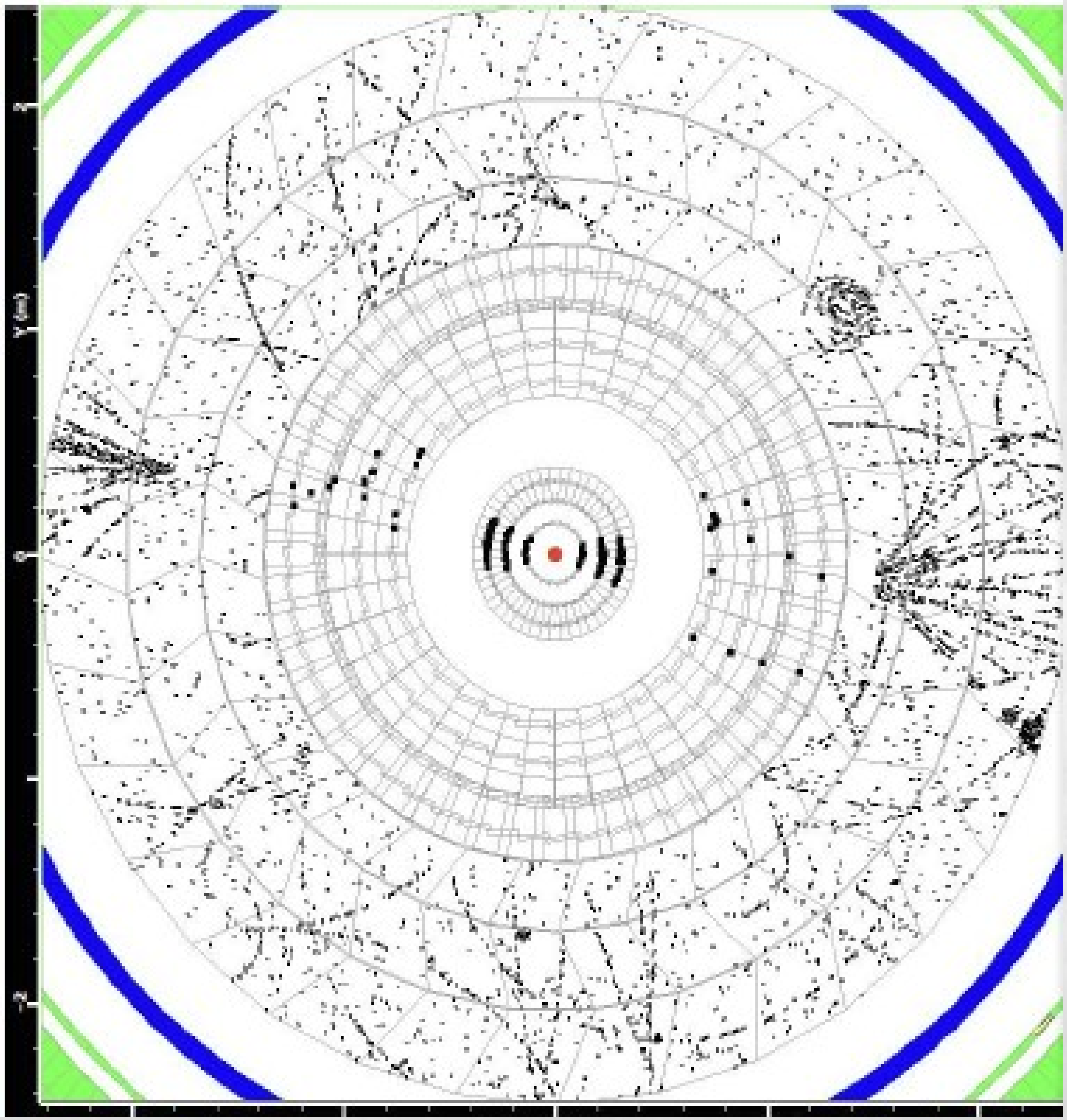
One possible solution

My personal conclusions

Real time is

- Fast enough for your application
- At a predictable latency (better if fixed)
- ...

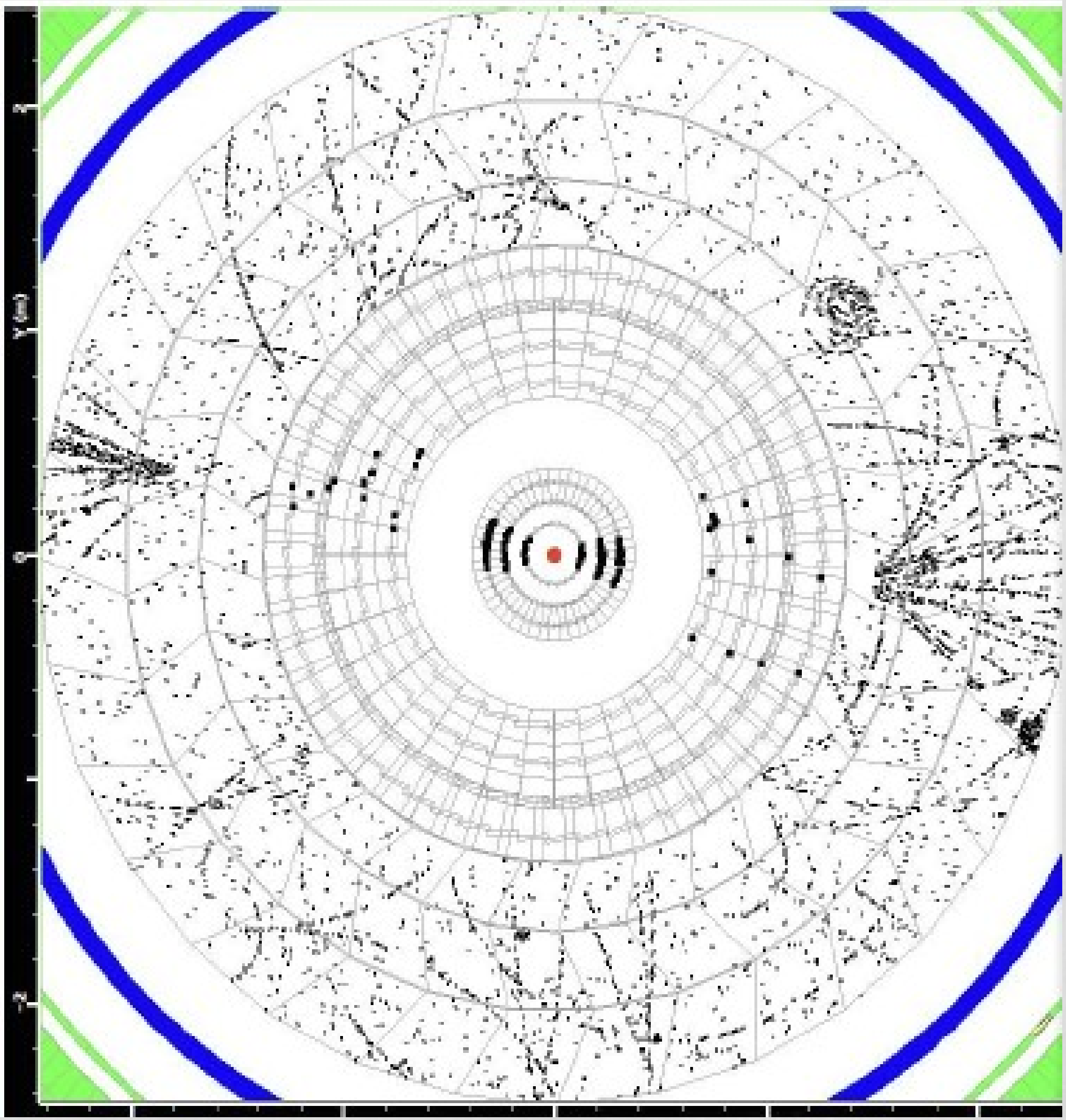
What is tracking?



What is tracking?

Identify all (charged) particles?

Perfect measurement of parameters?



What is tracking?

Track finding:

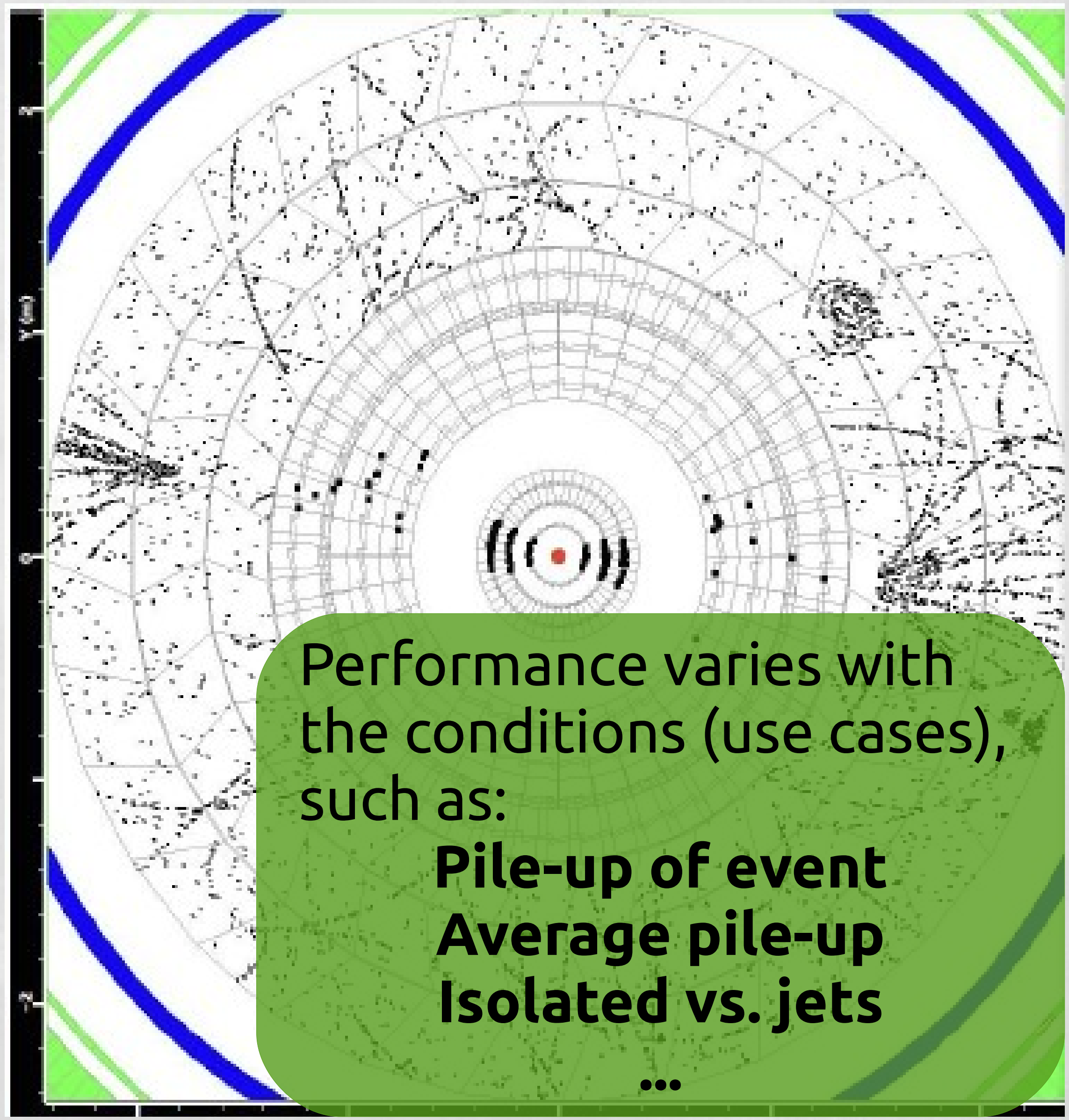
Inefficiency

Fakes (Duplicates)

Efficiency

Resolution **needed** on parameters:

- **p_T, φ, d_0**
- **η, z_0**



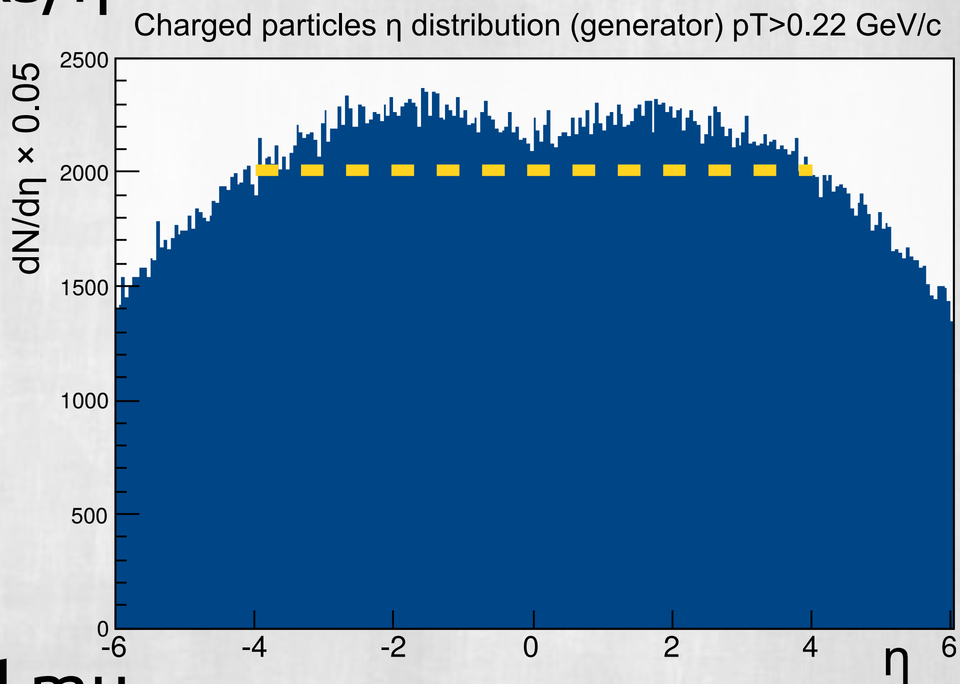
Performance varies with the conditions (use cases), such as:

- **Pile-up of event**
- **Average pile-up**
- **Isolated vs. jets**
- **…**

HL-LHC tracker in trigger

Conditions:

- Radiation equivalento to 3000 fb-1 (10× LHC)
- PU = 140 (200) => 1000 tracks/η (~ uniform in η for |η|<4)

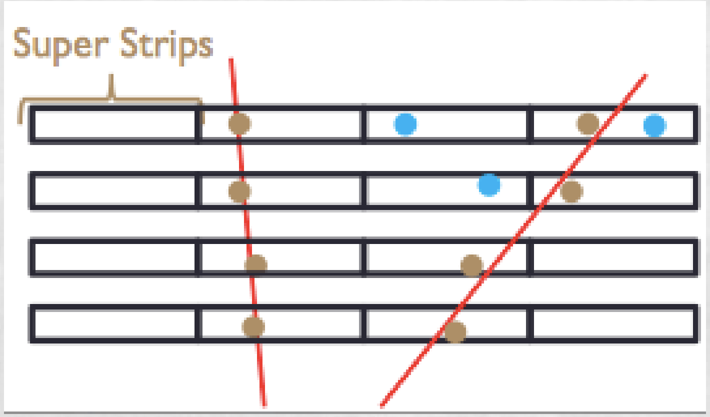


Requirements (minimal?):

- Measure p_T of isolated e and mu
- Identify vertices of PU events
- ID vertex of hard scatter

ATLAS FTK for Run 2

- Hardware-based tracking is (almost) already a reality at LHC
- Fast TracKer (FTK) : Level-1.5 hardware processor for full silicon tracking at L1 output rate (100 kHz)
  - reduce timing required for software tracking
  - selection more closely matched to offline
  - provides primary vertex position and multiplicity

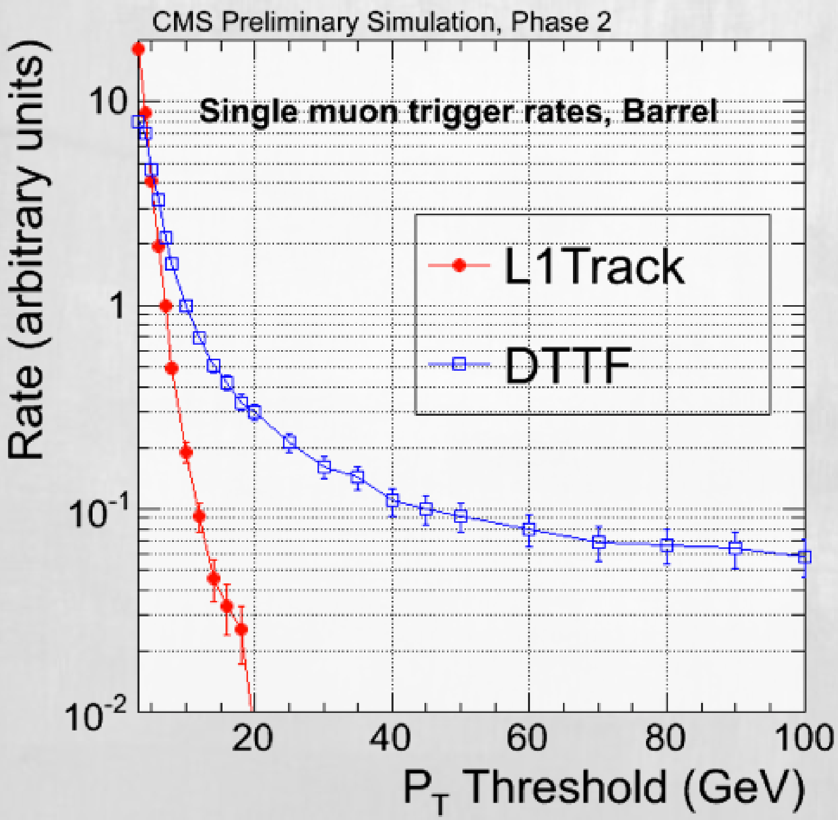


Associative Memory technology:
- massively parallel
- latency < 100 μs
- processing rate <100 kHz
- pile-up < 70

Why a Track Trigger at L1

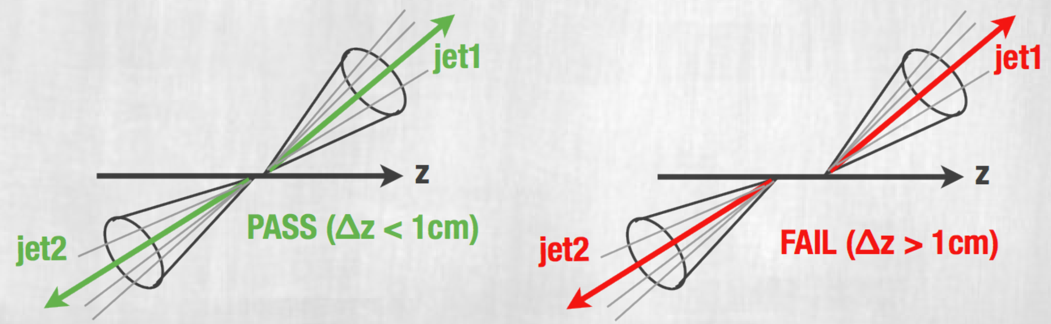
(Not detailed: see lecture by O. Buchmueller this afternoon)
Rates grow with luminosity + trigger degradation from pile-up

Huge rate of μ from heavy flavours	⇒	use better p_T resolution from tracker
Prompt electrons at L1 need to be separated from huge γ	⇒	tracker tracks
High ET jets from (many) different primary vertices	⇒	jet-vertex association
Photon isolation in Calorimeters compromised by large pileup	⇒	use tracks

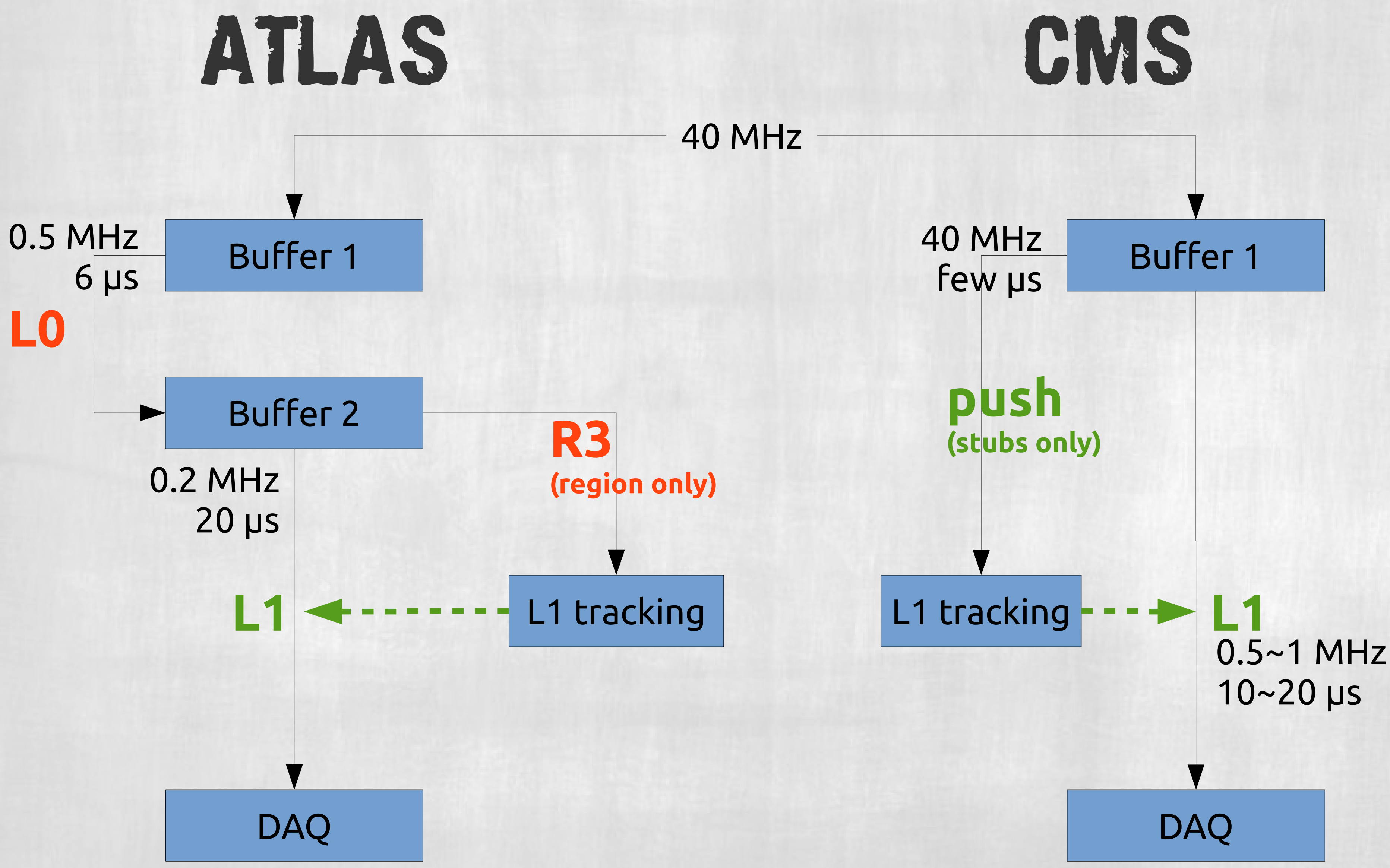


Trigger rates tamed at reasonable thresholds

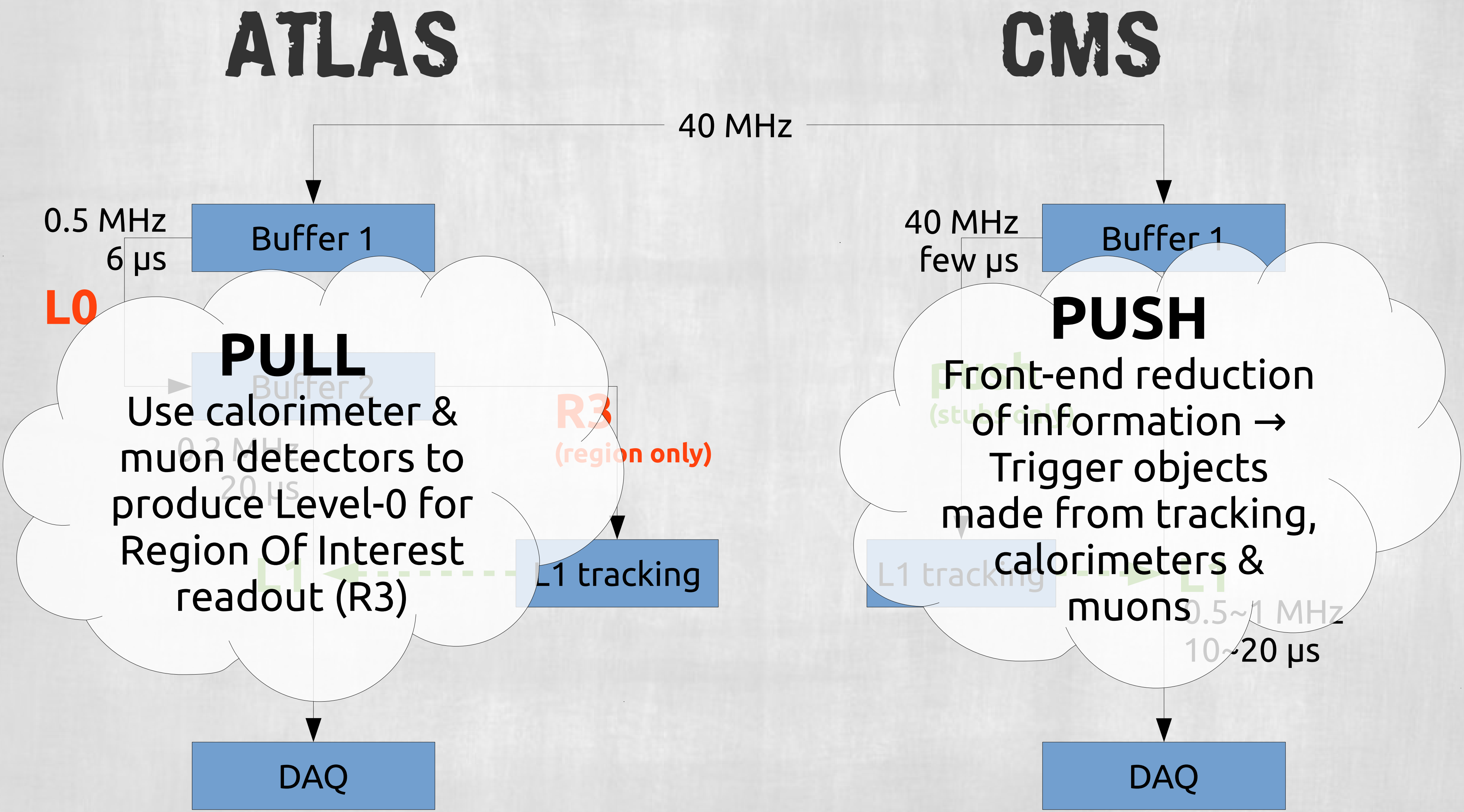
Jet vertex association needs tracking



Level-which?


ATLAS
CMS
40 MHz
0.5 MHz
6 μs
Buffer 1
L0
Buffer 2
0.2 MHz
20 μs
R3
(region only)
L1
L1 tracking
DAQ
40 MHz
few μs
Buffer 1
push
(stubs only)
L1 tracking
L1
0.5~1 MHz
10~20 μs
DAQ

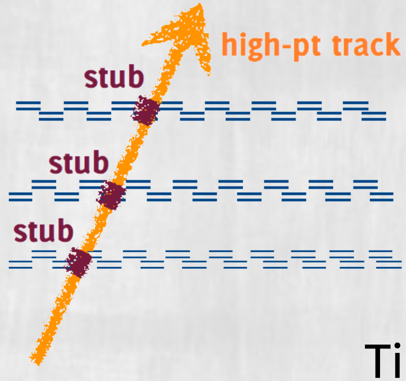
Level-which?

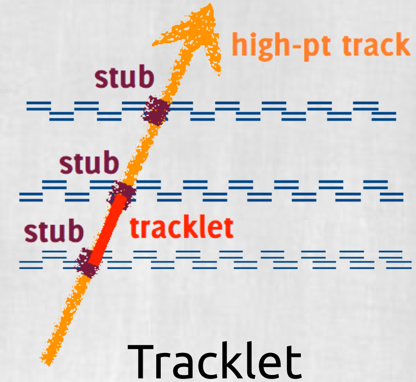

ATLAS
CMS
40 MHz
0.5 MHz
6 μs
L0
Buffer 1
PULL
Use calorimeter & muon detectors to produce Level-0 for Region Of Interest readout (R3)
R3
(region only)
L1 tracking
DAQ
40 MHz
few μs
Buffer 1
PUSH
Front-end reduction of information → Trigger objects made from tracking, calorimeters & muons
0.5~1 MHz
10~20 μs
DAQ

CMS L1-tracking 3 strands of R&D

Extreme challenge: reconstruct **O(100)** tracks from **~15000 stubs** at **40 MHz**

Track finding step is performed here (main step)



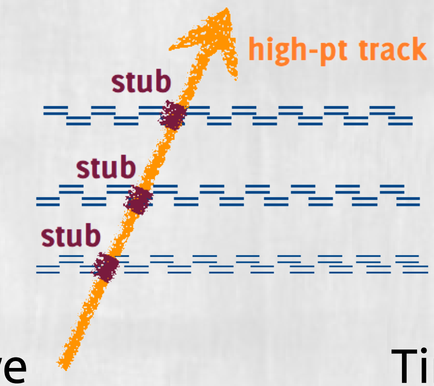


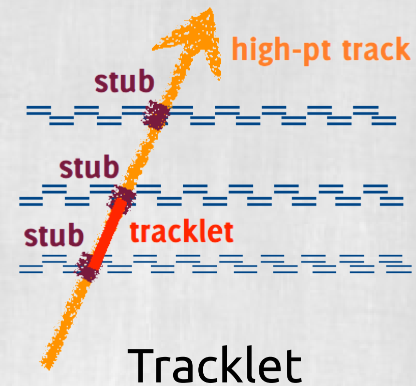
		Associative Memories	Time Multiplexed Trigger	Tracklet algorithm
1st pass	Hardware	Dedicated	FPGA	FPGA
	Primitives	**Stubs**	**Stubs**	**Stubs**
	Method	Pattern match (10^8)	Projective binning	Tracklet find
	Generates	**Patterns**	**Track candidates**	**Tracklets**
2nd pass	Hardware	FPGA	FPGA	FPGA
	Primitives	**Patterns** + **stubs**	**Track candidates** + **stubs**	**Tracklets** + **stubs**
	Method(s)	PCA or Hough transform or Retina	Under study	X^2 fit
	Generates	L1-Tracks	L1-Tracks	L1-Tracks
slices	Sectors	48 = **8×6** ($\varphi \times \eta$)	5 = **5×1** ($\varphi \times \eta$)	28 = **28×1** ($\varphi \times \eta$)
	Time MUX	(Load balancing)	**24×** (BX)	**4×** (BX)

CMS L1-tracking 3 strands of R&D

Extreme challenge: reconstruct **O(100)** tracks from **~15000 stubs** at **40 MHz**

Track finding step is performed here (main step)





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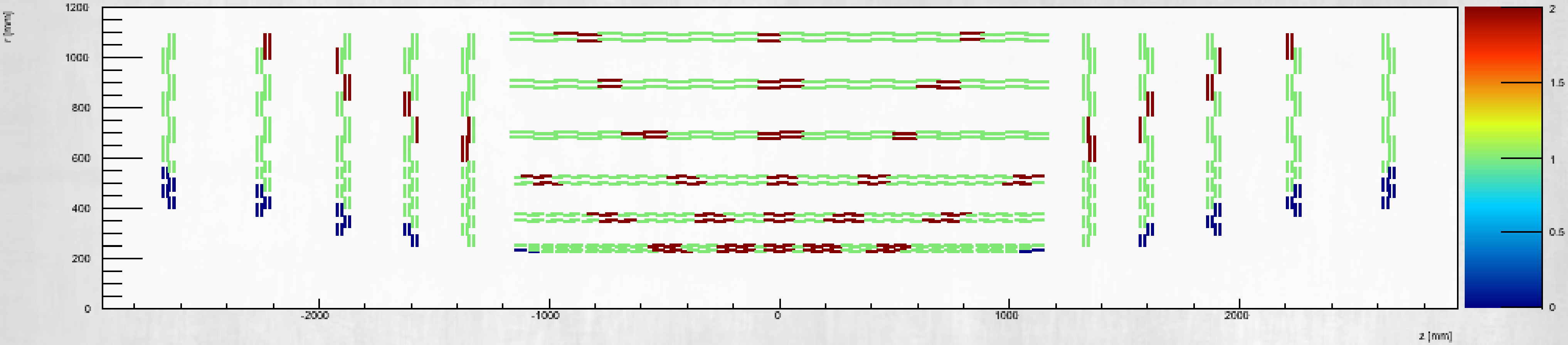
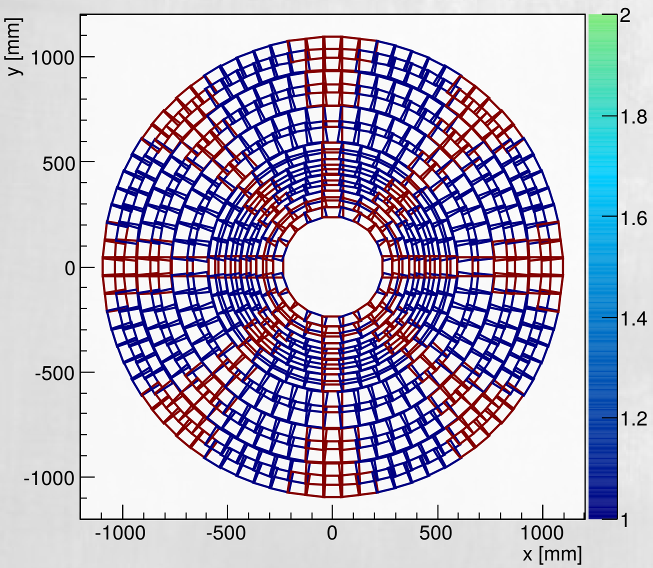
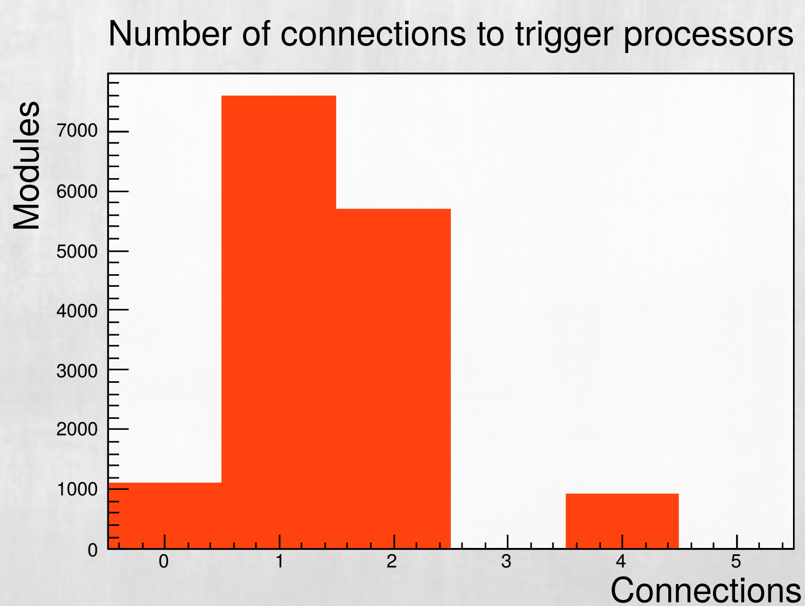
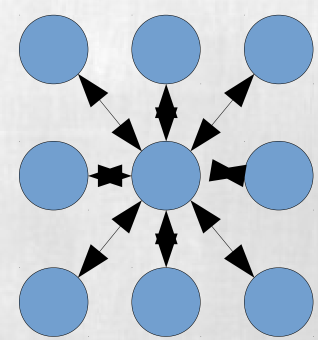
CMS possible sectors scheme





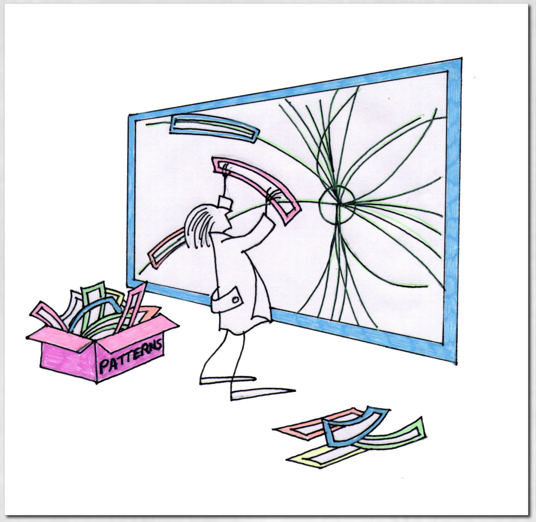


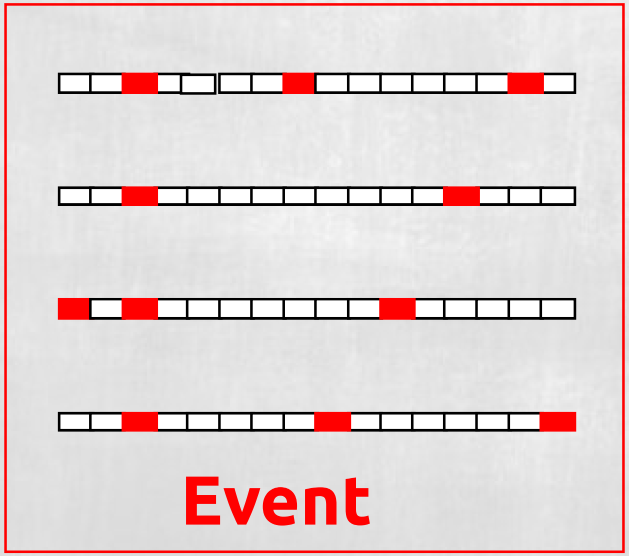
Every trigger tower only needs a fraction of data from its neighbours

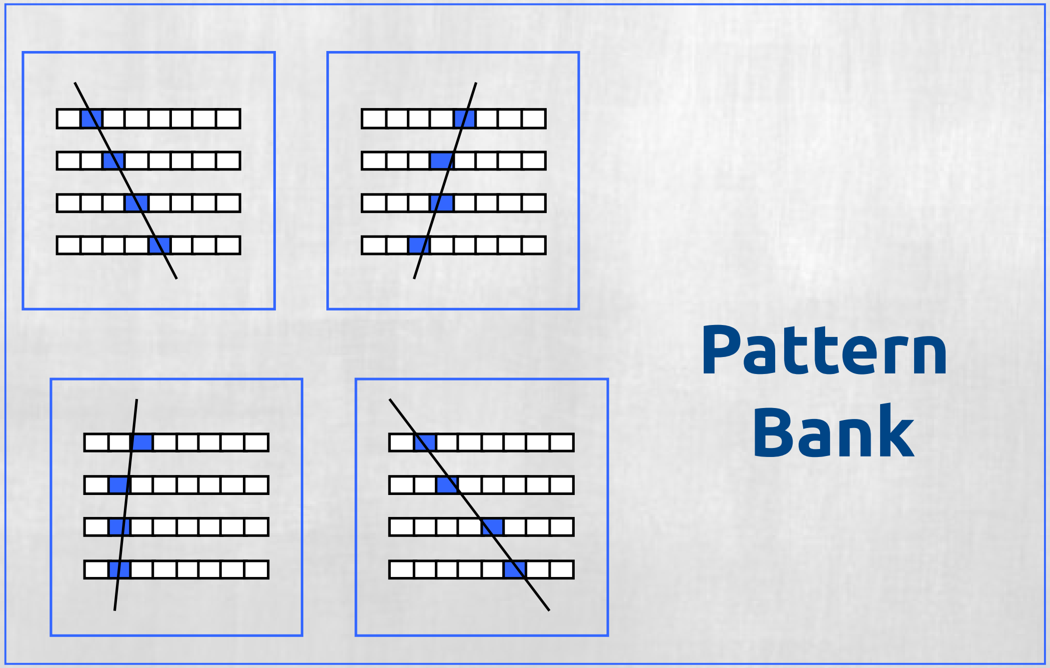


Pattern matching

- Pre-programmed patterns are flexible. Can be tuned on real data and can account for:
  - can account for misalignment
  - changing detector conditions
  - beam movement
  - …

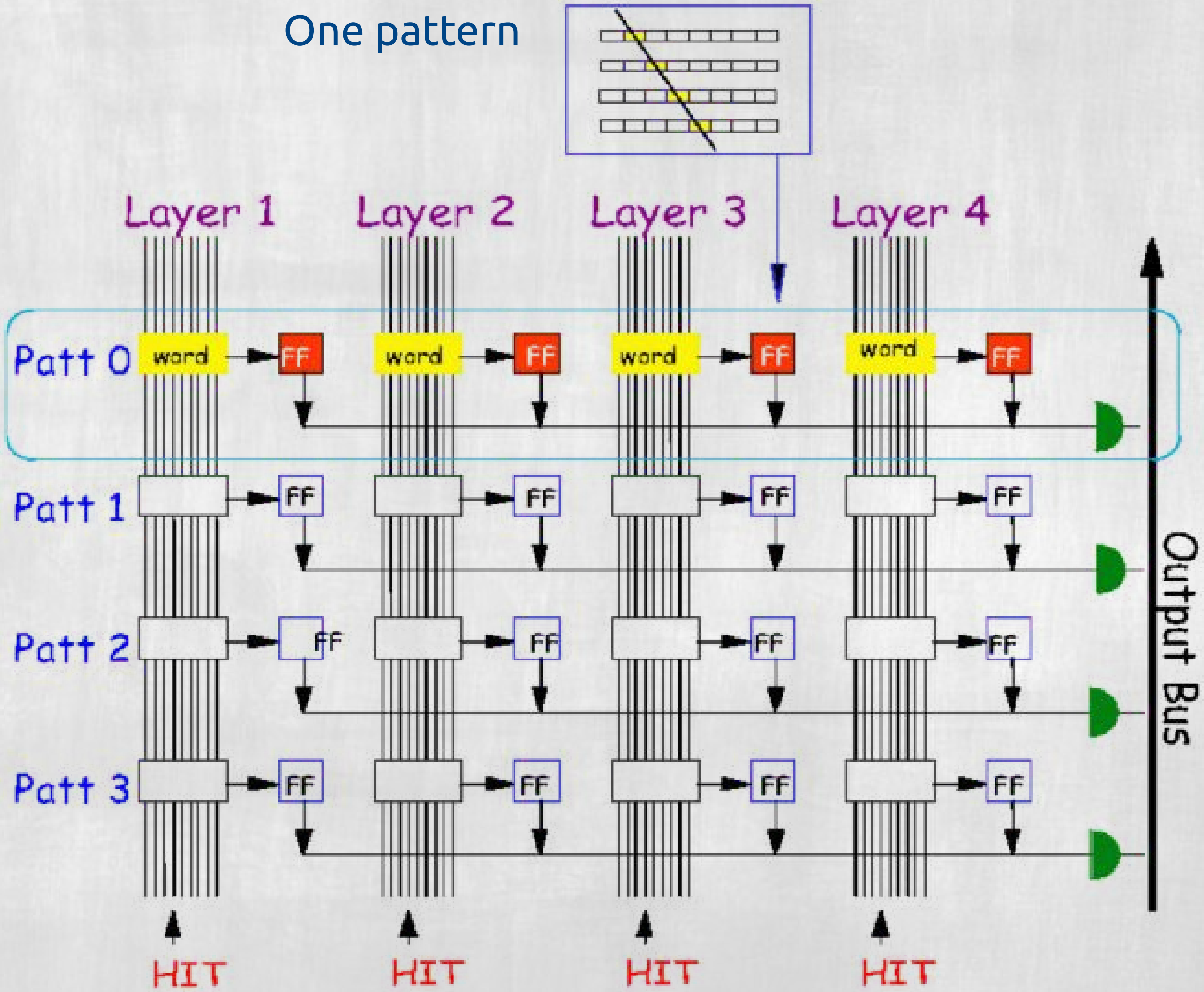






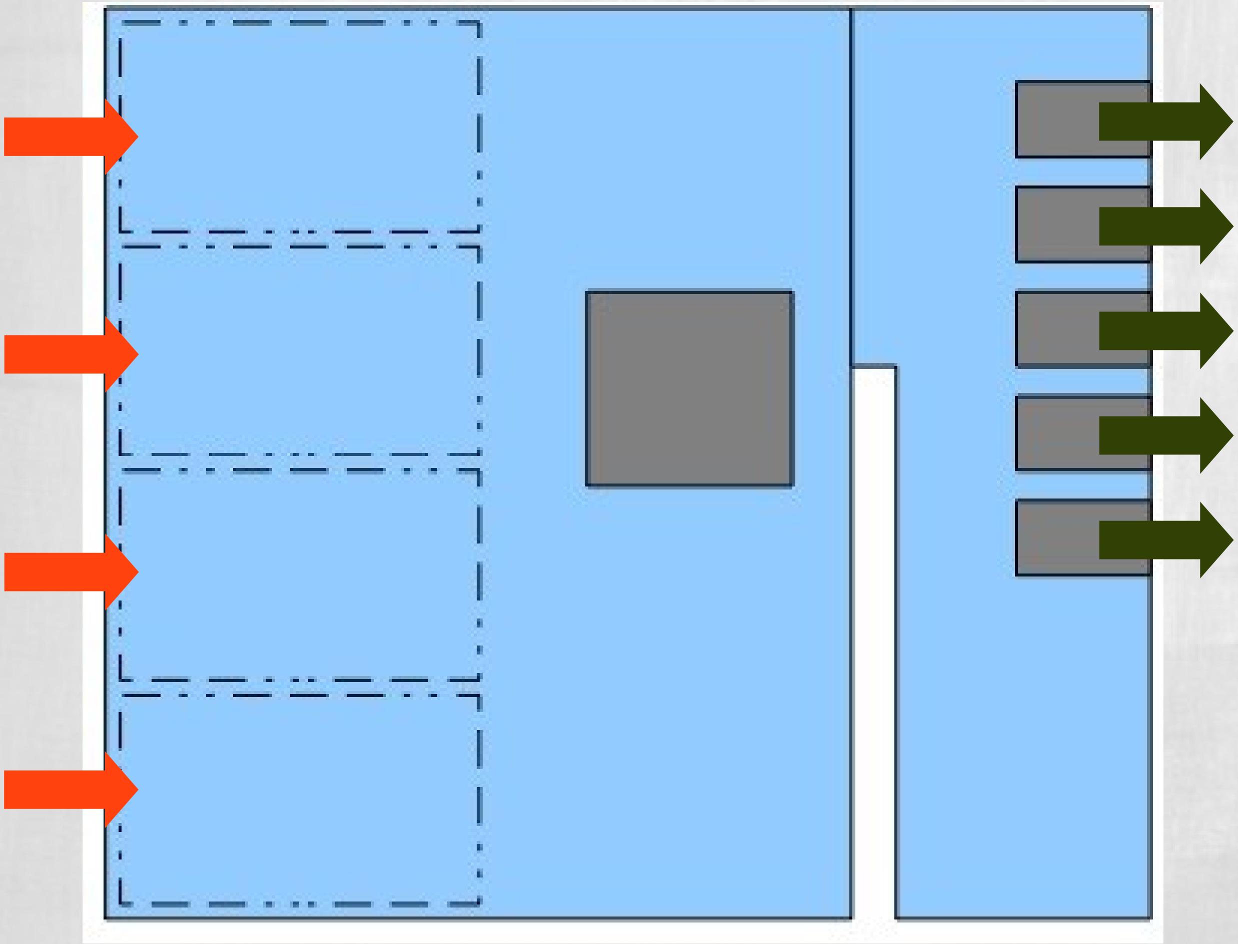
Pattern matching: associative memory

1 register
1 comparator
1 match
/ layer / patt



CMS: toward a demonstrator (ATCA)

Input Data Board



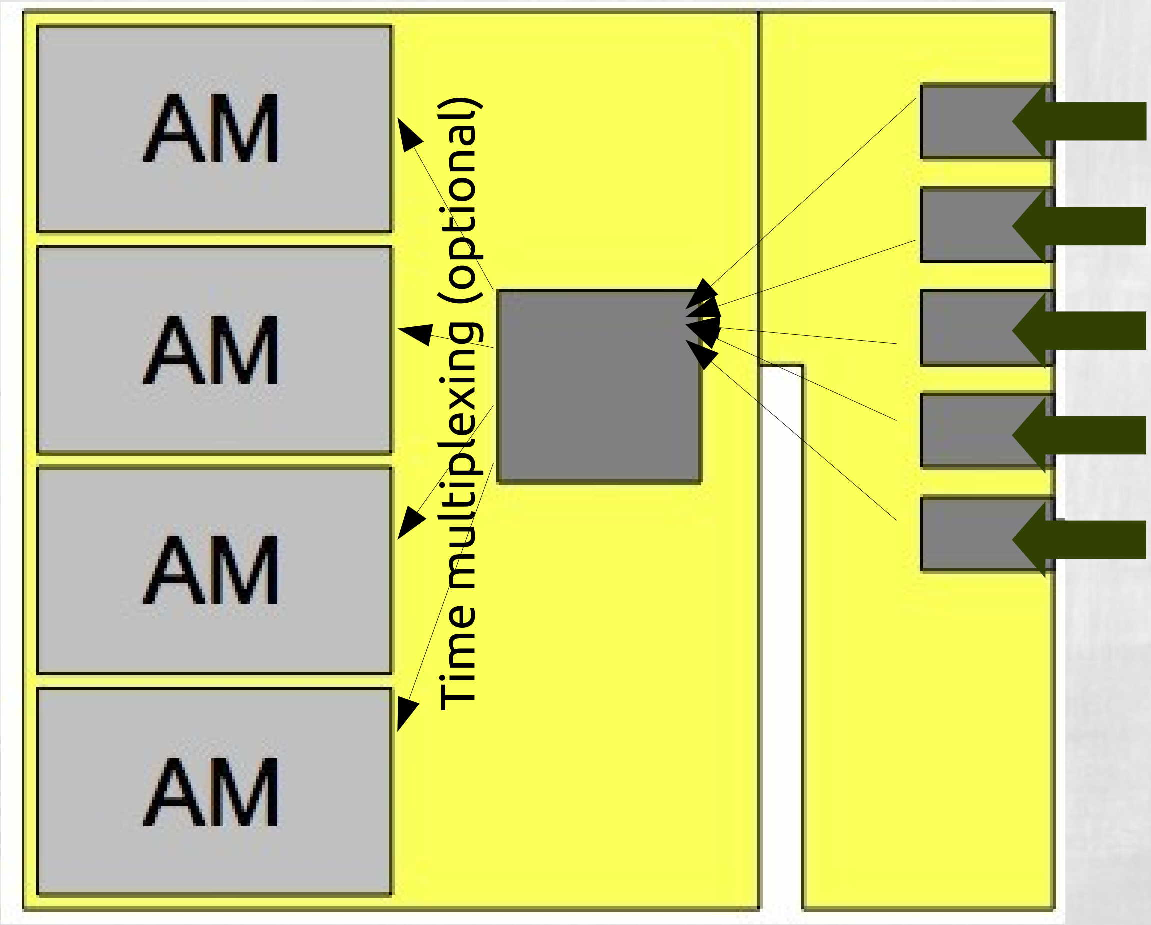
Up to 48 pairs of connection, Bidirectional

Up to 48 **inputs** with 3.25 Gbps each

With 40G full-mesh **backplane**

CMS: toward a demonstrator (ATCA)

Pattern Recognition Board



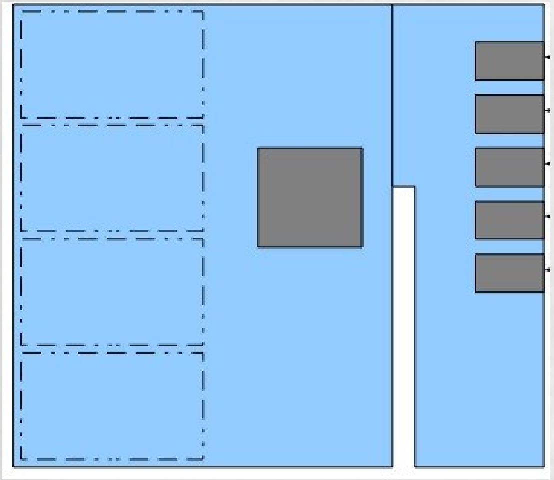
Up to 8×40 Gbps = 320 Gbps

Can be time multiplexed on the mezzanines

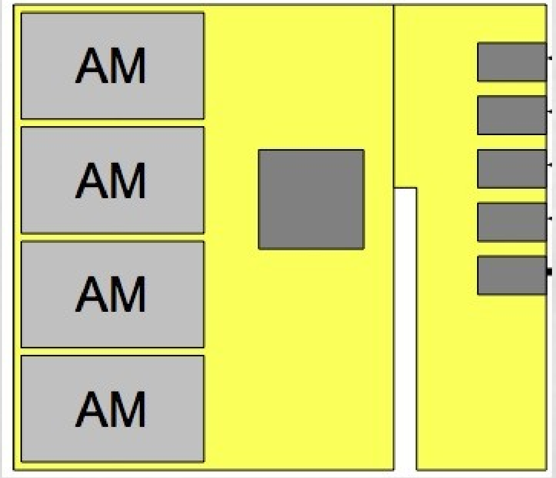
AM could be replaced by FPGA doing the same job

CMS: toward a demonstrator (ATCA)

Input Data Board x 8



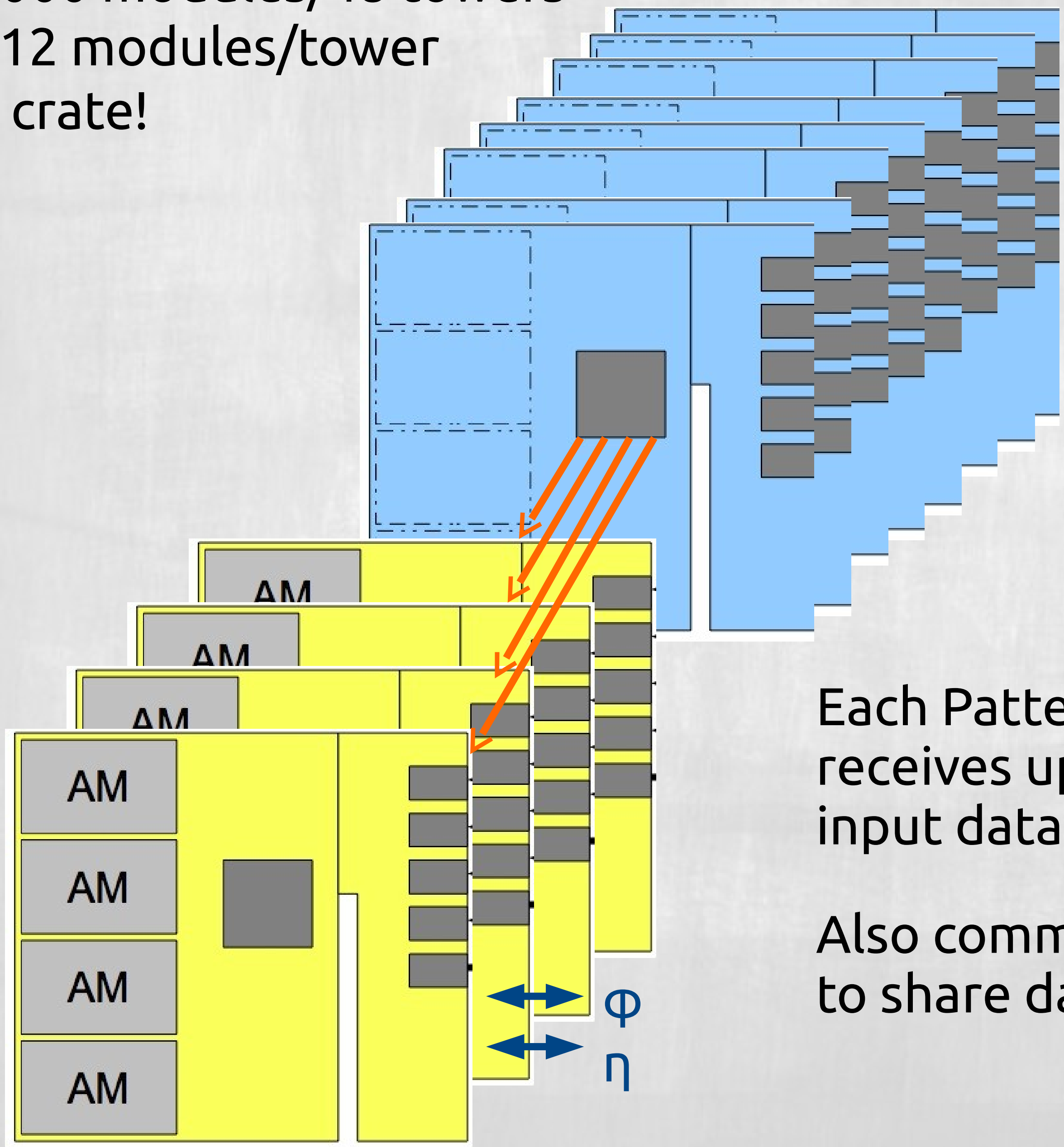
Pattern Recognition Board x 4



One Trigger Tower = 1 crate

Trigger towers

15,000 modules/48 towers
≈ 312 modules/tower
≈ 1 crate!



Each board up to 48 modules @ 3.25Gbps
8 boards up to 384 modules
(one trigger tower worth)

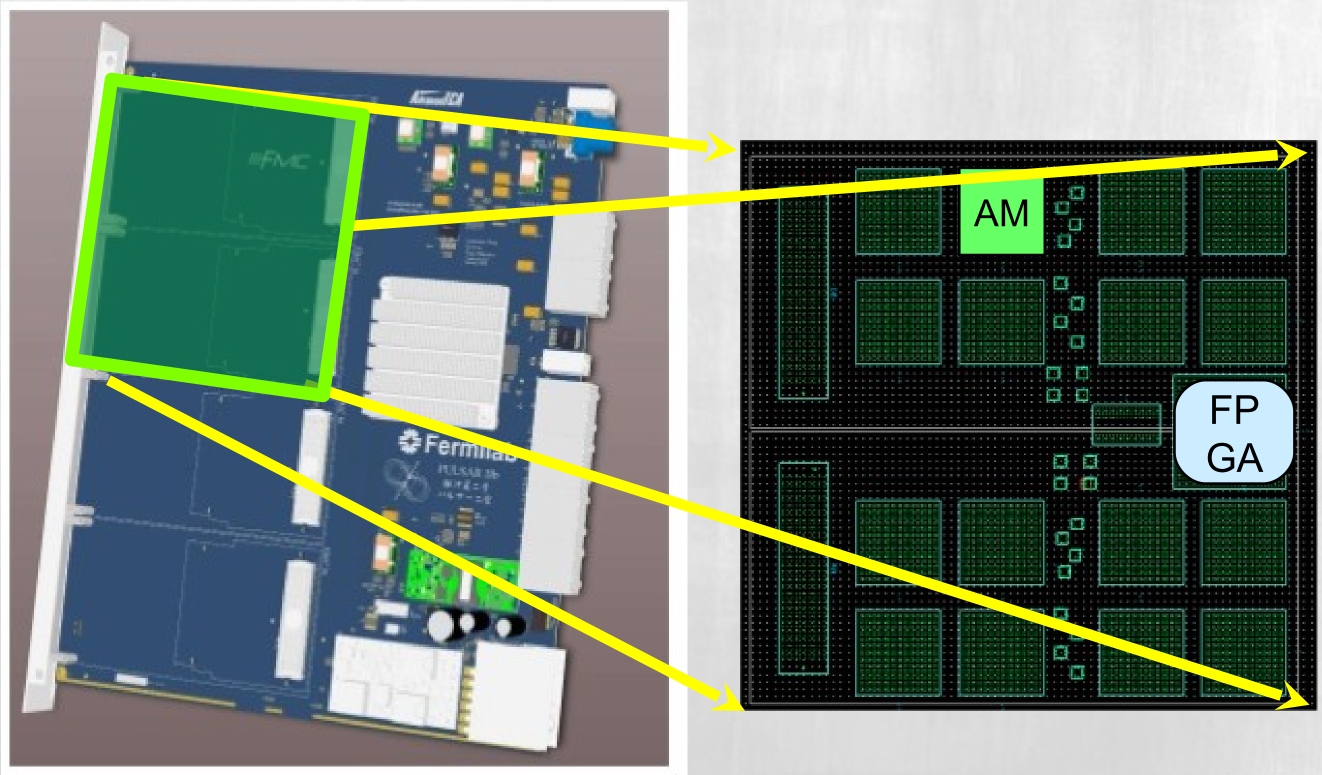
Each Pattern Recognition board receives up to 8×40 Gbps = 320 Gbps input data over full Mesh backplane.

Also communicate with other crates to share data in φ,η for each time slice

Pattern recognition & track fit

Associative Memories (pattern recognition) + FPGA (track fit)

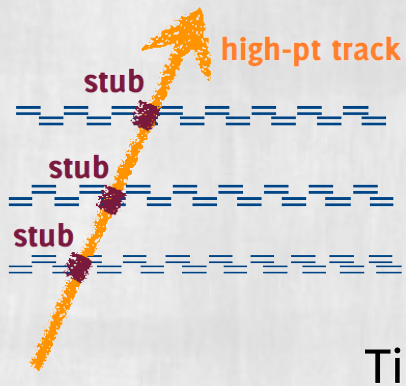
- CMS trigger sectors need ~1M patterns: only 8 state-of-the-art AM06-chip (but higher I/O speed (currently 2Gb/s/layer) to reduce time multiplexing)
- ~3000 Track fitting engines using Principal Component Analysis Alternative methods under study (Hough Transform, Retina)

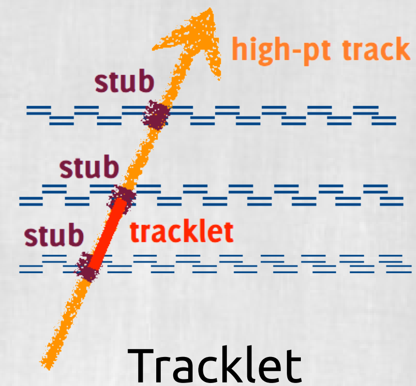


L1-tracking 3 strands of R&D

Extreme challenge: reconstruct **O(100)** tracks from **~15000 stubs** at **40 MHz**

Track finding step is performed here (main step)





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	Primitives	**Stubs**	**Stubs**	**Stubs**
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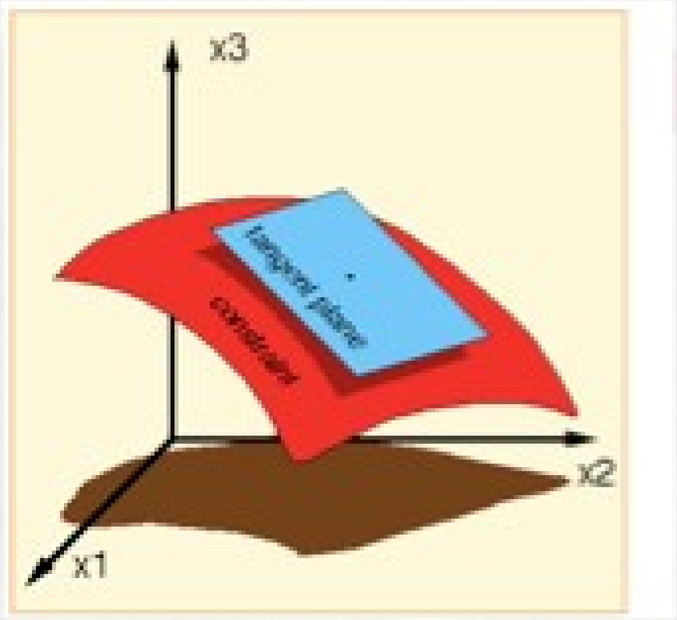
	Time MUX	(Load balancing)	**24×** (BX)	**4×** (BX)

Principal Component Analysis

Over a narrow region in the detector, equations linear in the local silicon hit coordinates give resolution nearly as good as a time-consuming helical fit.

Uses **pre-computed** parameters (LUT)

$$p_i = \sum_{j=1}^{14} a_{ij} x_j + b_i$$

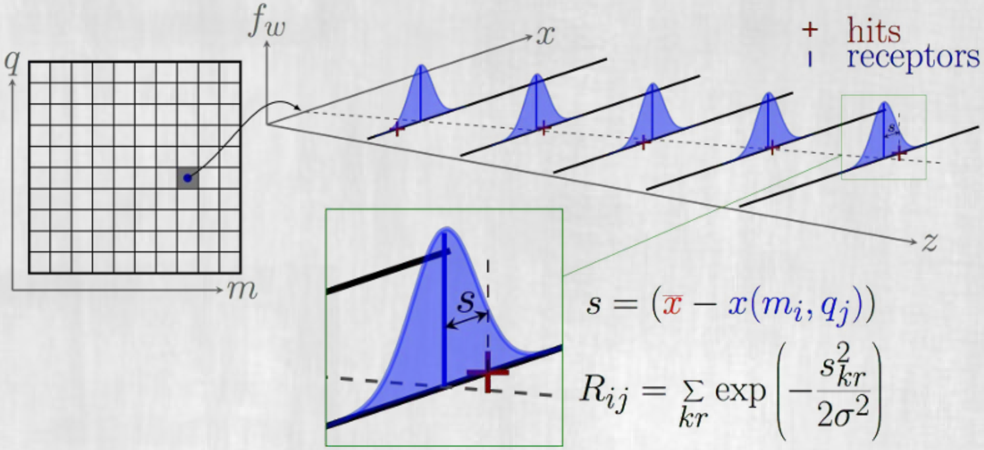


- pi's are the helix parameters and 2 components.
- x_j's are the hit coordinates in the silicon layers.
- a_{ij} & b_i are pre-stored constants determined from full simulation or real data tracks.
- The range of the linear fit is a "sector" which consists of a single silicon module in each detector layer.
- This is VERY fast in FPGA DSPs.

NIM A623:540-542,2010 doi:10.1016/j.nima.2010.03.063

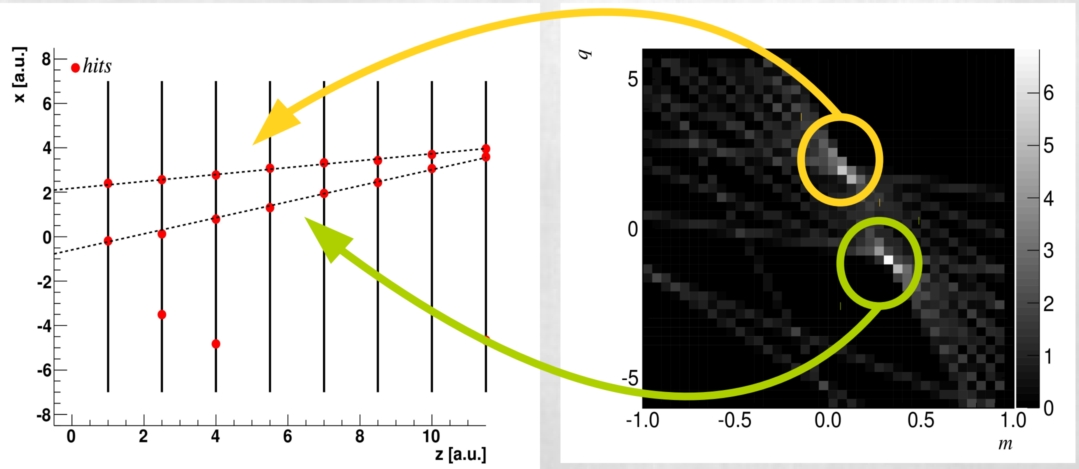
Retina algorithm

- Tracks project to a virtual "retina"
- Retina's cell activate proportionally to the distance from the signal
- A simple 2D example to visualize how the retina algorithm works:
  - n parallel single-coordinate layers,
  - no magnetic field, straight line tracks identified by two parameters (m,q).
  - Tracks are peaking structures (over-a-threshold)
- For 5-parameter tracking: 5-dimensional grid



$$s = (\overline{x} - x(m_i, q_j))$$

$$R_{ij} = \sum_{kr} \exp\left(-\frac{s_{kr}^2}{2\sigma^2}\right)$$



L1-tracking 3 strands of R&D

Extreme challenge: reconstruct **O(100)** tracks from **~15000 stubs** at **40 MHz**

Track finding
step is performed here
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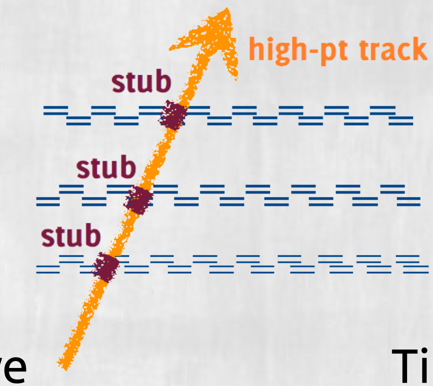

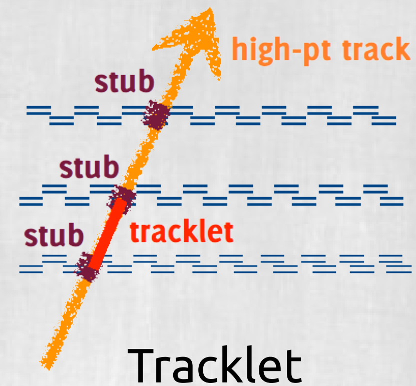

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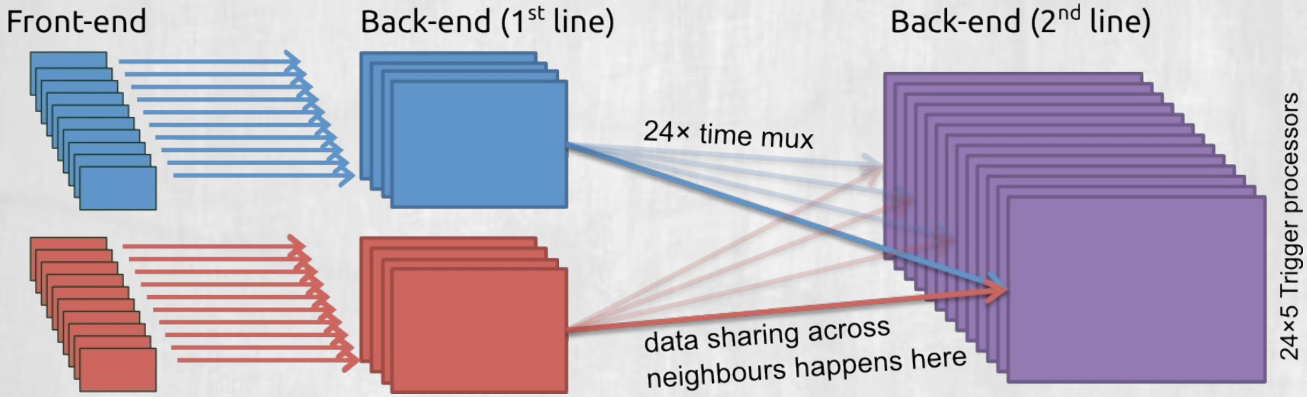
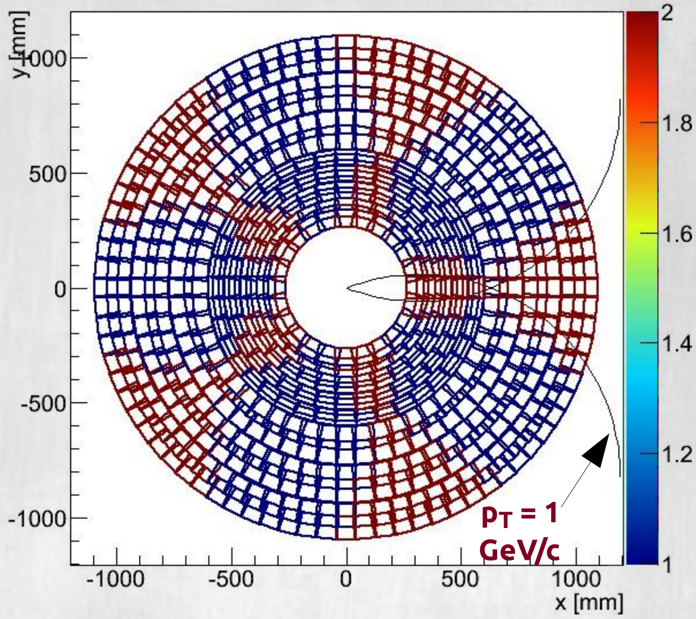
Time-multiplexed trigger

- Geometric sectioning kept to minimum, with constraints:
  - 1 module cannot be shared more than 2 regions
  - boundary for regions at pT=1 GeV/c

slices	Sectors	5 = **5×1** (φ×η)
	Time MUX	**24×** (BX)





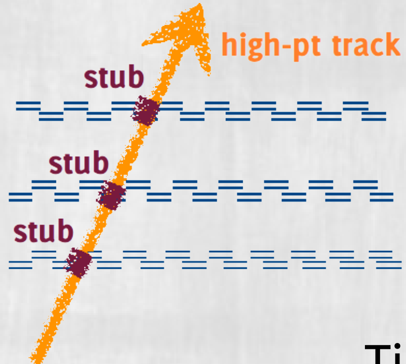
Benefits:

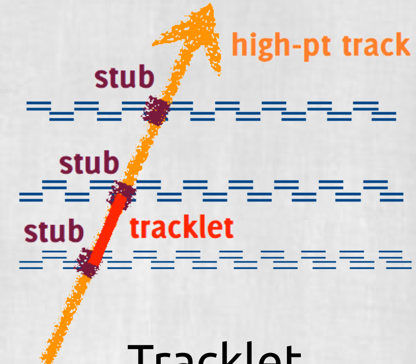
- No boundary sharing is required after duplication/ no removal of duplicates necessary
- Builds on experience from μTCA-based L1 trigger upgrade (hardware is available)
- Can be implemented in FPGA
- Only a fraction of the system is needed to fully demonstrate it

L1-tracking 3 strands of R&D

Extreme challenge: reconstruct **O(100)** tracks from **~15000 stubs** at **40 MHz**

Track finding step is performed here (main step)





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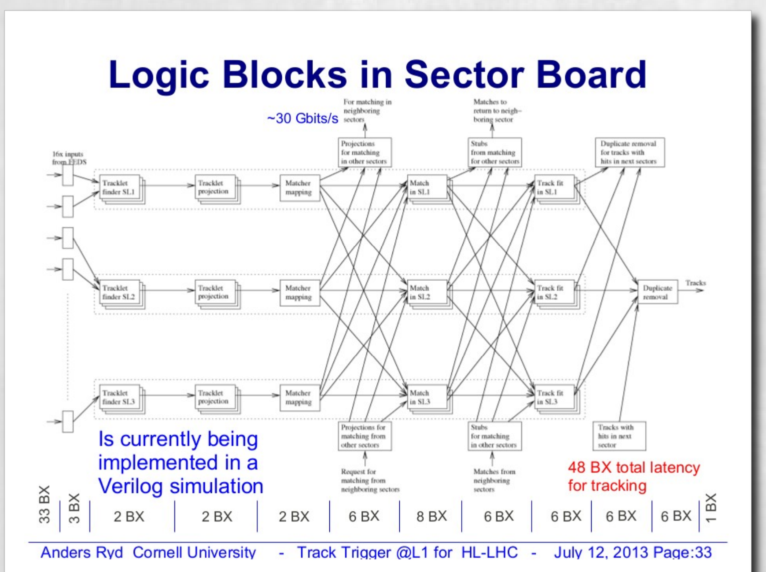
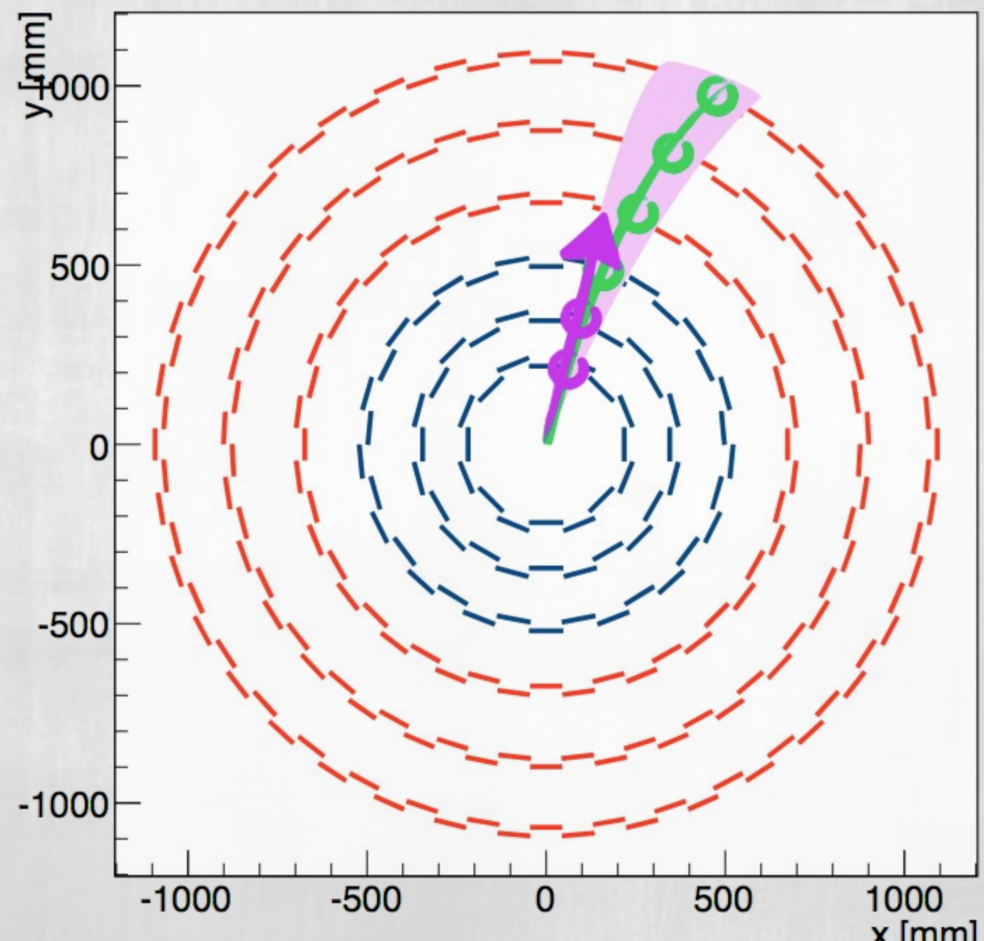
Tracklet algorithm

- Find track seeds by correlating stubs in subsequent layers
- “Kalman Filter”-like approach: propagate stubs from one layer to another and concatenate stubs within matching windows
- Linearised Track Fitter
- Ghost removal
- Verilog simulation is under study:

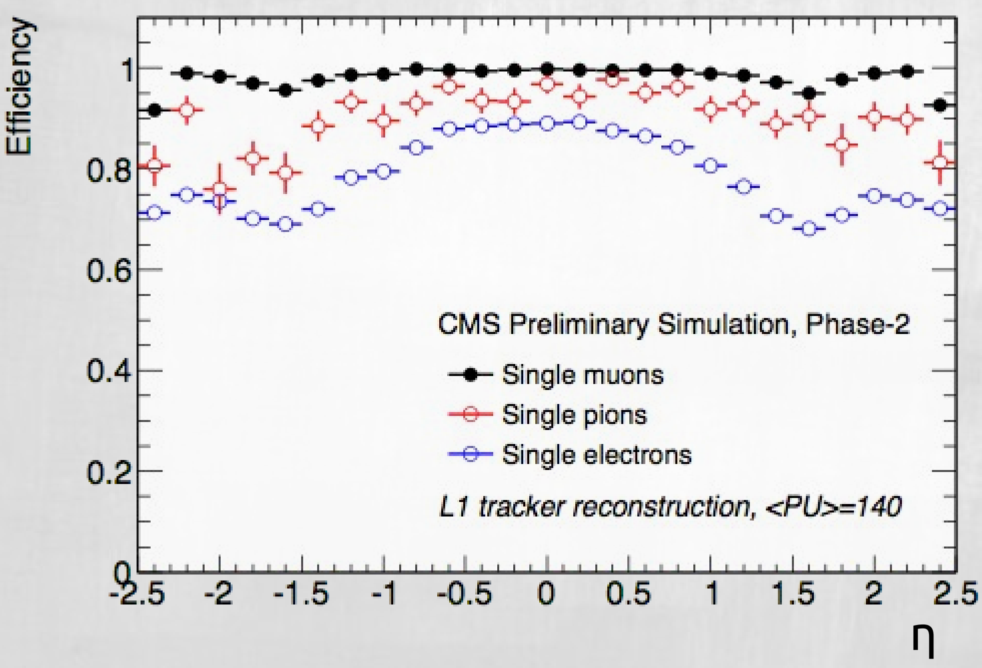


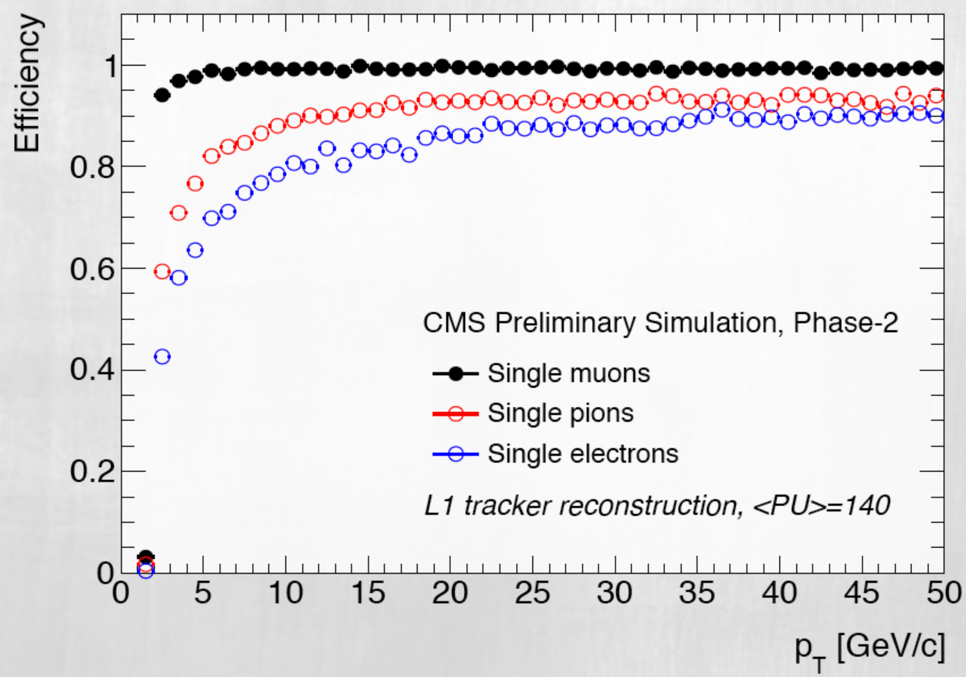


Performance (tracklet algorithm)

L1 tracking efficiency for single μ, π, e with <PU>=140

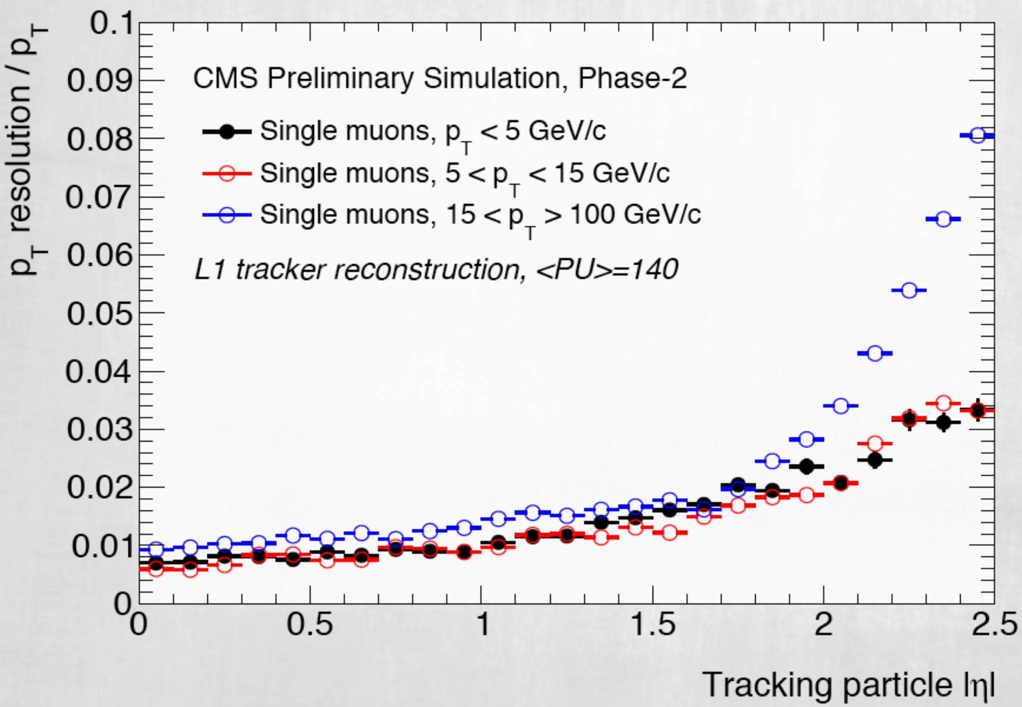
- **Muons**: sharp turn-on @ 2 GeV/c and high efficiency across η
- **Pions**: somewhat lower efficiency due to higher interaction rate
- **Electrons**: slower turn-on curve, efficiency reduced from Bremssrahlung

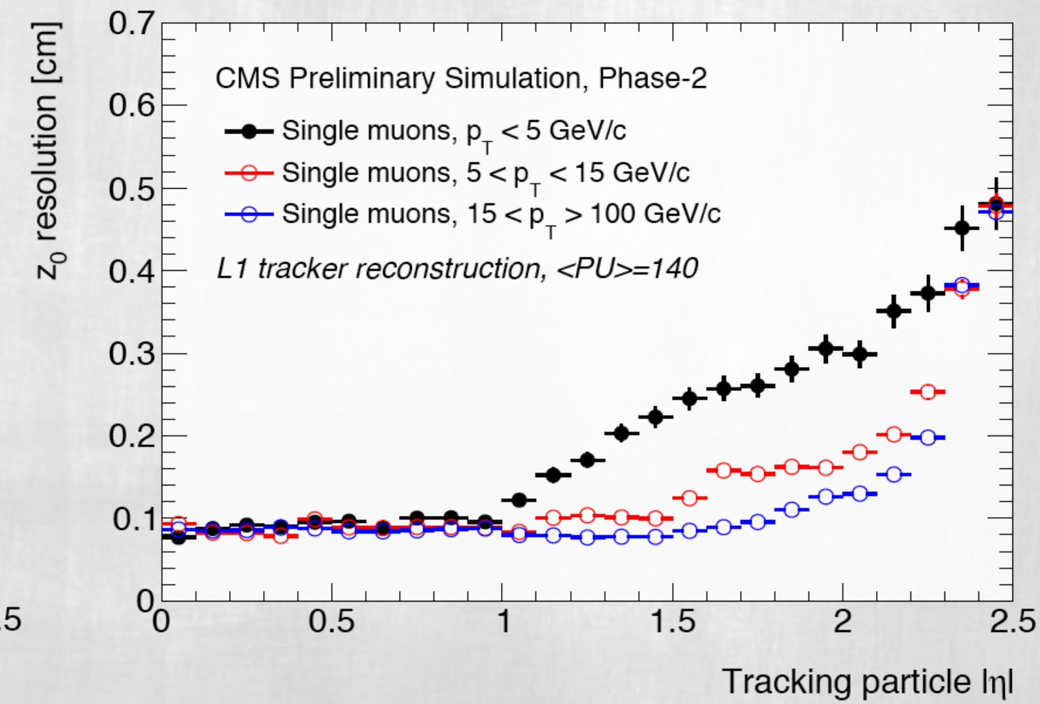




Performance (tracklet algorithm)

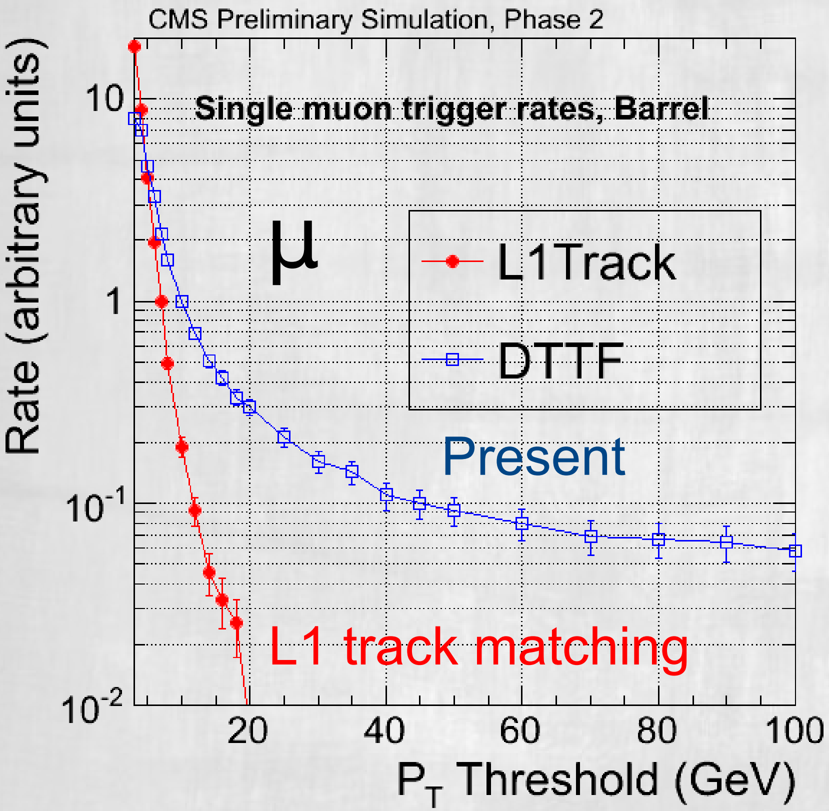
- Track finding performance taken from “tracklet” method
  - Estimates with AM track finding qualitatively similar
- N.B. Track finding not (yet) demonstrated in hardware: indication of the performance that could be achievable



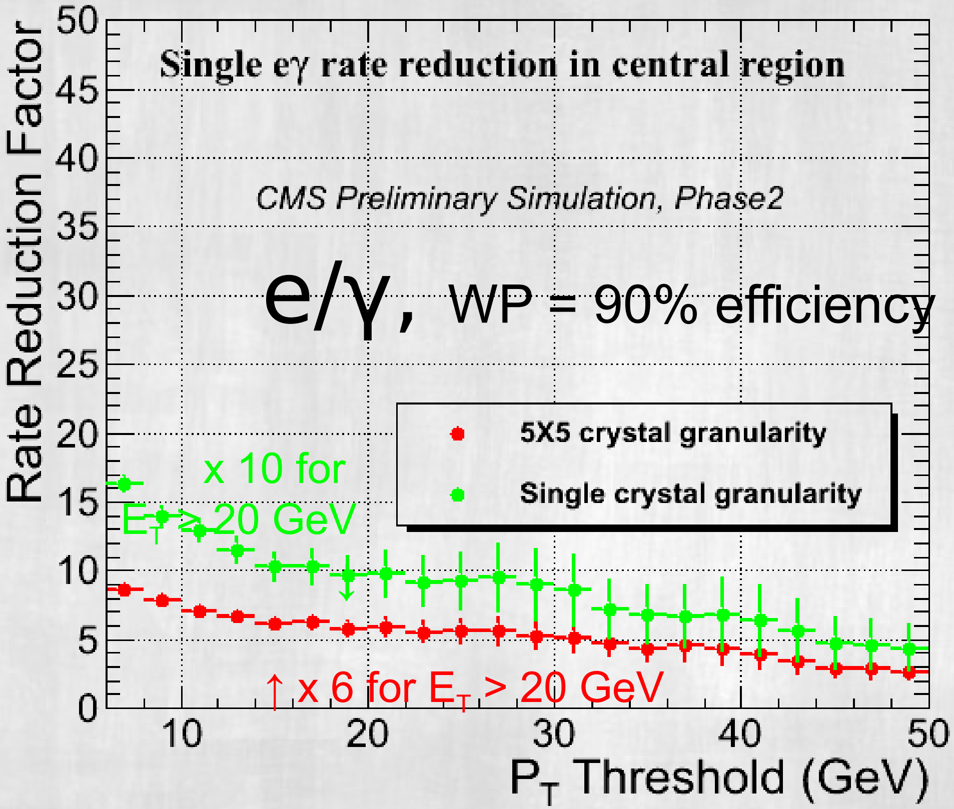


Use of L1-tracks

Just a taste of the advantages:



Matching Drift Tube trigger primitives with L1Tracks: large rate reduction: > 10 at threshold > ~ 14 GeV Normalized to present trigger at 10 GeV. Removes flattening at high Pt



Rate reduction by matching L1 e/γ to L1Track stubs for | η | < 1
Red: with current (5x5 xtal) L1Cal granularity.
Green : using single crystal-level position resolution improves matching

That's all, folks!