



Introduction to analog integrated circuit design: from schematic to layout

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Introduction

 **Level 0: IC chip (die)**

 **Level 1: Packaged chip**

 **Level 2: Printed circuit board**

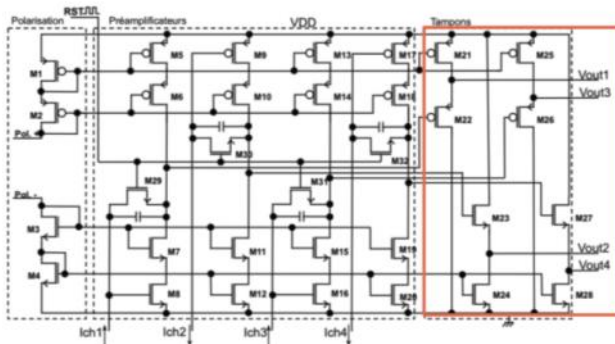
 **Level 3: Card-on-board
(backplane)**

Level 4: Cabinet 

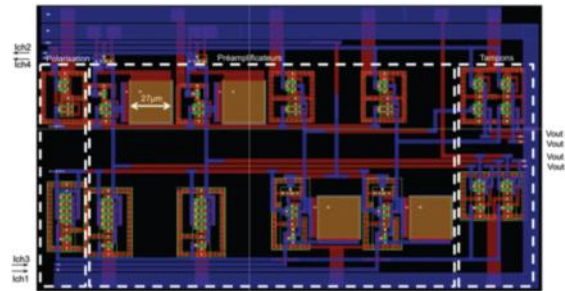
Level 4: System 

Introduction

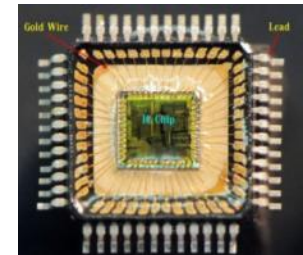
This lab is focused on the methodology and design flow for the design of CMOS analog integrated circuits (Full custom design).



Schematic



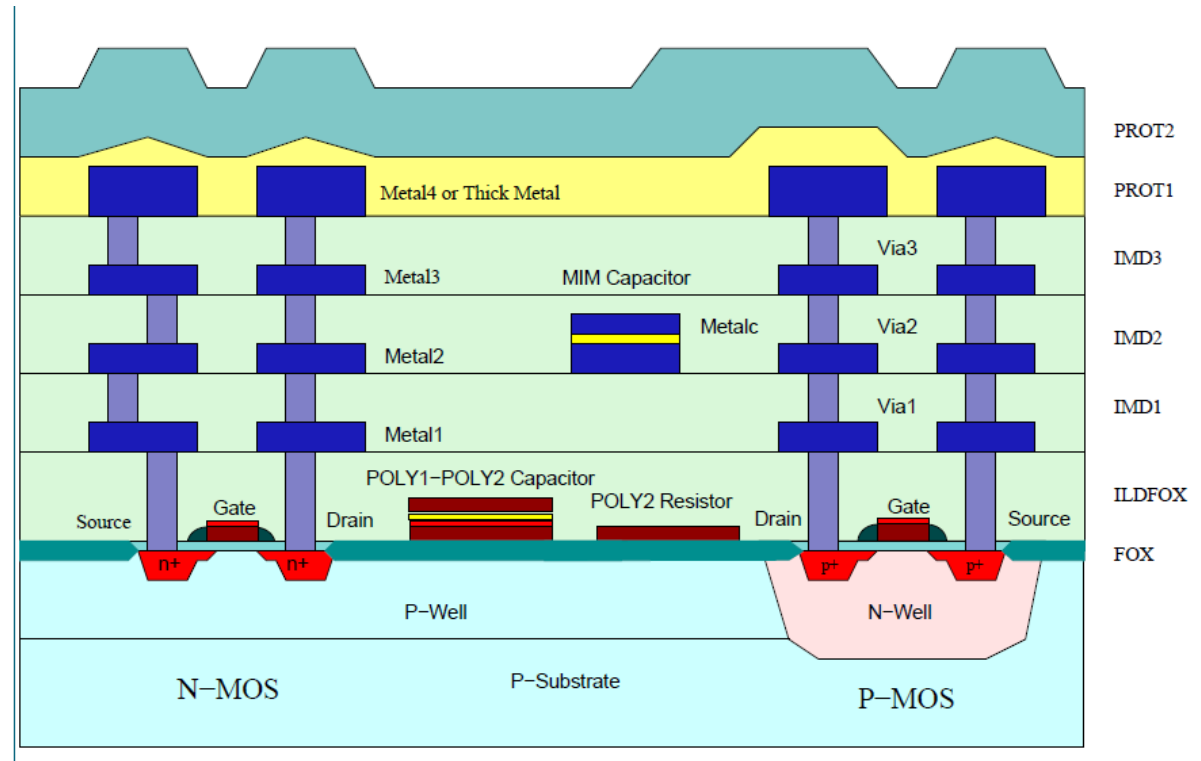
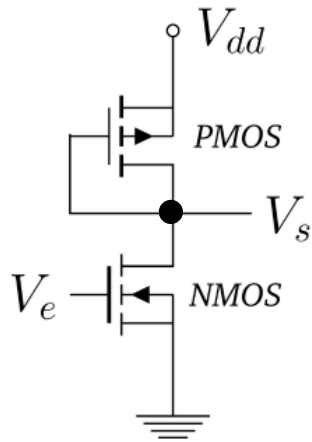
Layout



Packaged IC

This class implements Cadence CAD-Tools.

Analog cell and CMOS technology

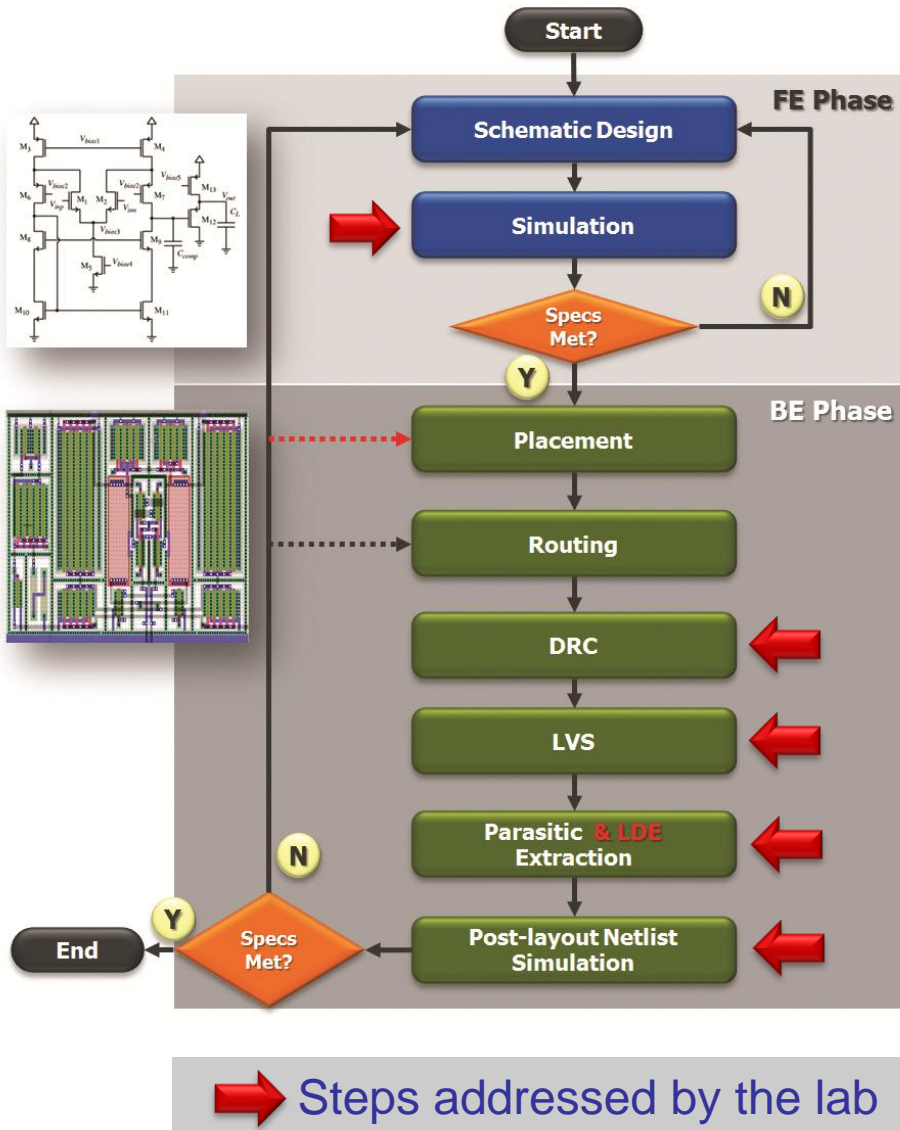


Analog cell
(inverter)

Austriamicrosystems (AMS) 0.35 μm CMOS

(http://cmp.imag.fr/aboutus/slides/slides2007/03_KT_AMS.pdf)

IC design flows



Schematic:

- Basics design computations
- Parametric study based on static, transient, small signal simulations and noise analysis

Layout:

- Design Rule check
- Layout versus Schematic verification
- Parasitic components extraction
- Post-layout simulation

Design calculations

Design calculations.xlsx - Microsoft Excel

Mise en page Formules Données Révision Affichage Compléments

Calibri 11 A A

Revenir à la ligne automatiquement Standard

G I S Police

Fusionner et centrer

Alignement

Nombre

Mise en forme conditionnelle

fx

A B C D E F G H

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14 **In the saturation region ($|V_{GS}| > V_T$ and $|V_{DS}| > |V_{DS,sat}|$):**

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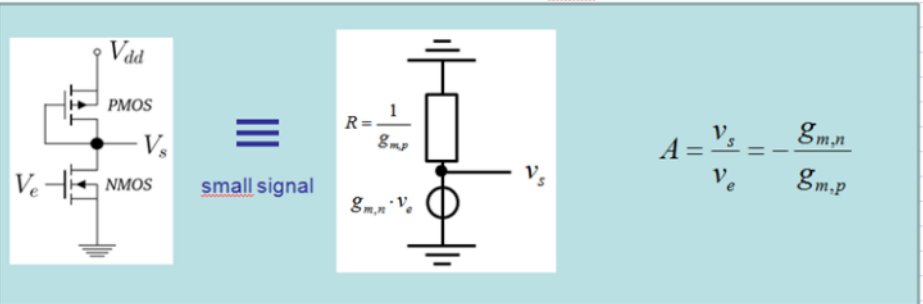
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small signal

$$R = \frac{1}{g_{m,p}}$$

$$A = \frac{v_s}{v_e} = -\frac{g_{m,n}}{g_{m,p}}$$

$$|I_{d,p}| = \frac{K_p W_p}{2 L_p} (V_{GS,p} - V_{T,p})^2$$

$$g_{m,n} = \sqrt{2 \times K_n \times \frac{W_n}{L_n} \times I_d}$$

$$|A| = \left| \frac{v_s}{v_e} \right| = \sqrt{\frac{K_n W_n L_p}{K_p W_p L_n}}$$

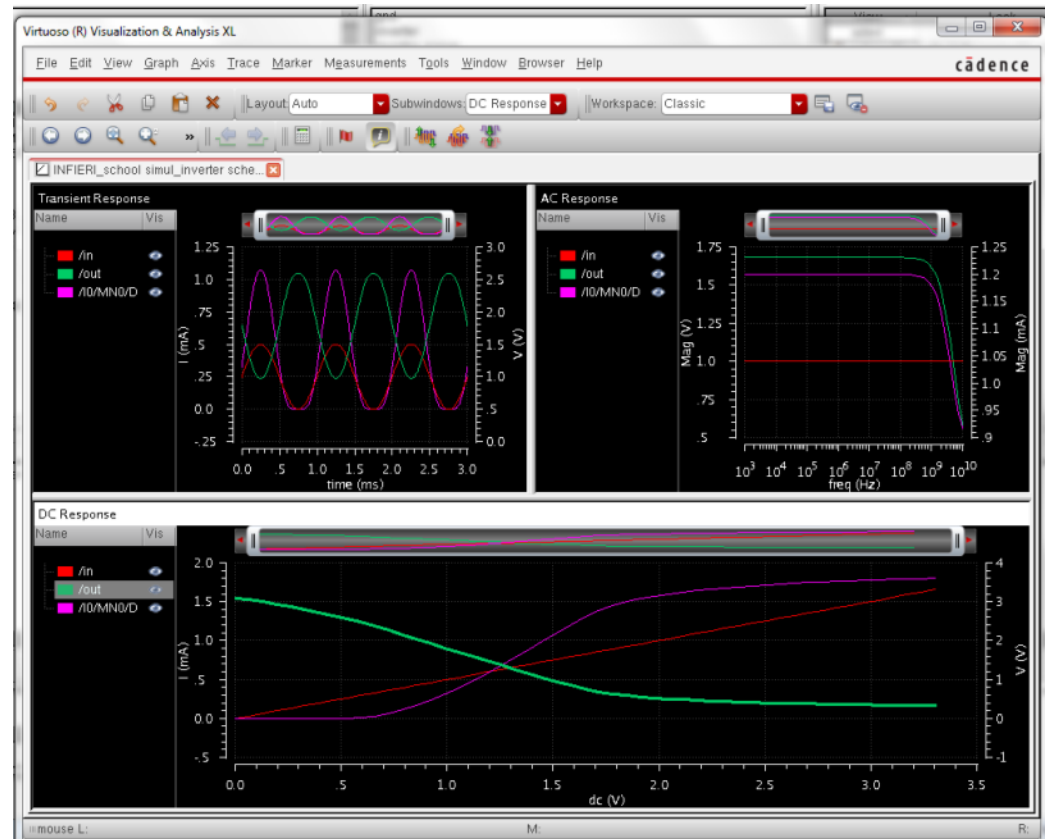
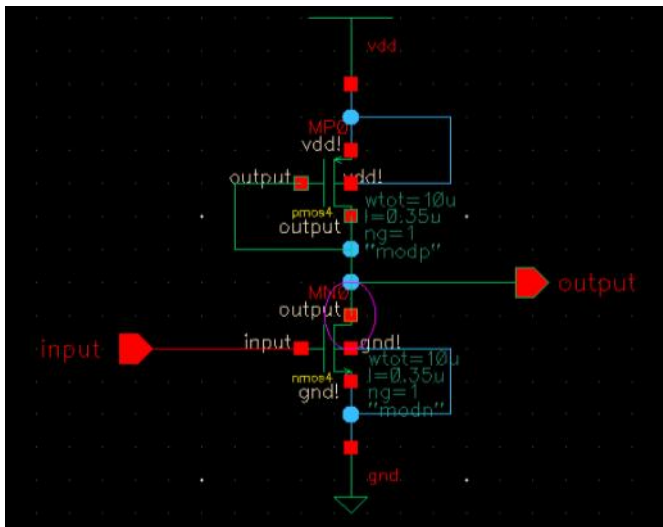
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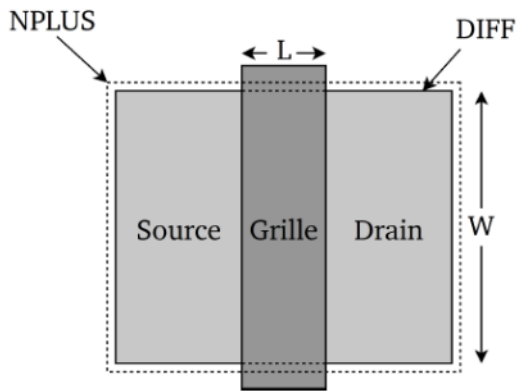
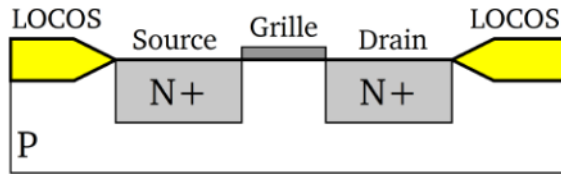
Transistor sizes are chosen for DC bias point and AC gain achievements

Typical Technological parameters @3.3V			
Vdd	3,3	Ve (V)	0,55
Kp	58	Vs (V)	2,6
Vtp	0,65	Ln (μm)	0,35
Kn (μA/V ²)	170	Wn (μm)	10
Vtn (V)	0,5	Lp (μm)	0,35
		Wp (μm)	29
		Idp (μA)	6,1
		Idn (μA)	6,1
		Gain	-1

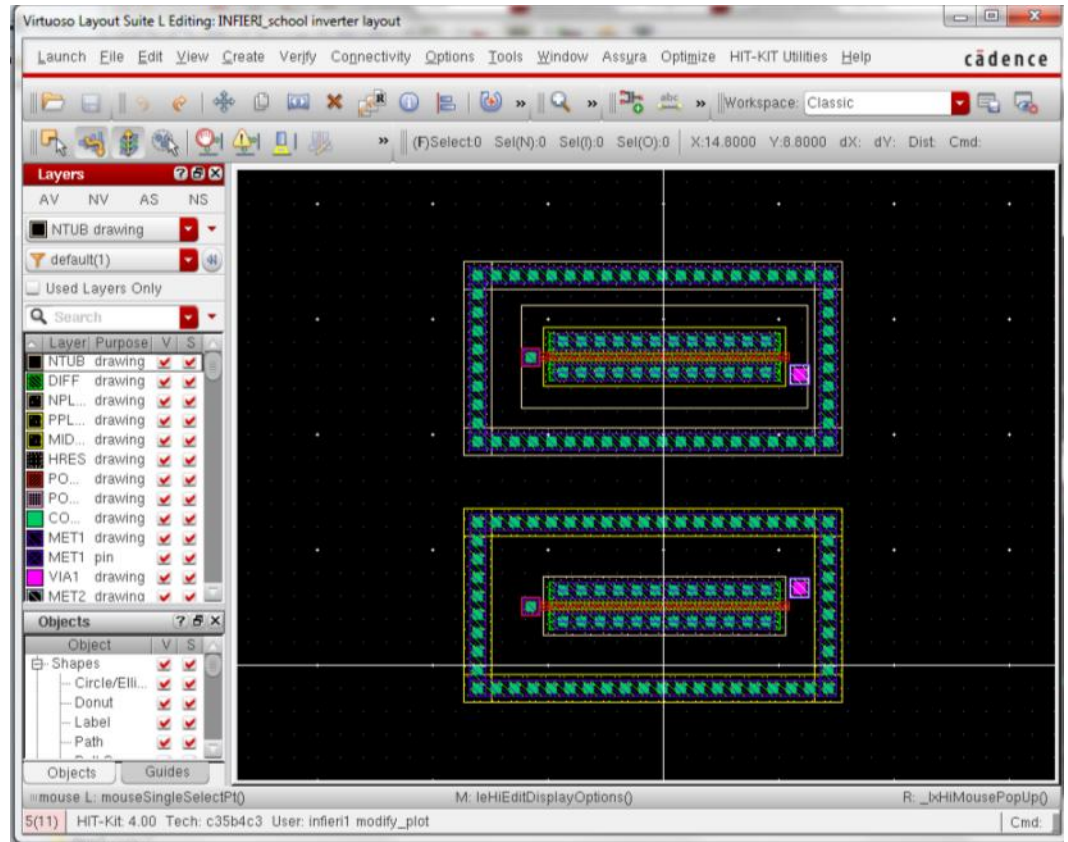
Simulations



Layout

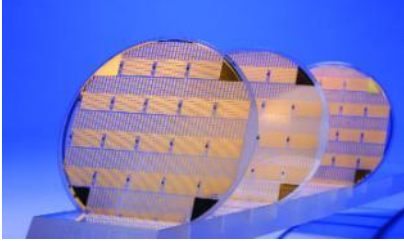


(a) Transistor NMOS

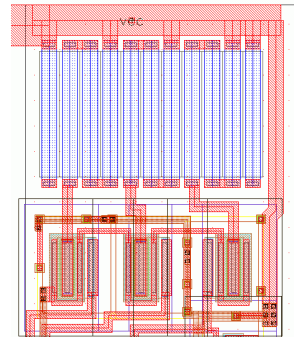


Process and Mismatch simulations

- Wafer production will always show some variation of technological parameter



- Mismatch on design parameters components



=> Monte-Carlo Process and Mismatch simulations will be run

