Introduction to analog integrated circuit design: from schematic to layout

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Introduction

Level 0: IC chip (die)

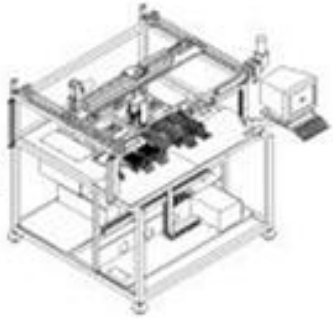
Level 1: Packaged chip

Level 2: Printed circuit board

Level 3: Card-on-board (backplane)

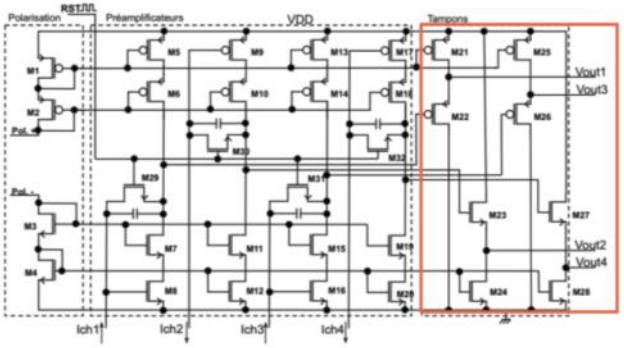
Level 4: Cabinet

Level 4: System

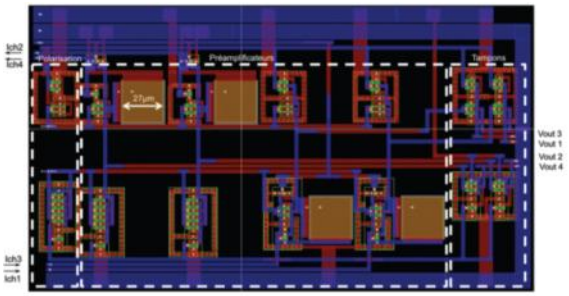


Introduction

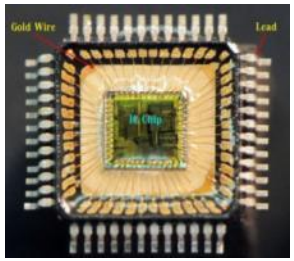
This lab is focused on the methodology and design flow for the design of CMOS analog integrated circuits (Full custom design).



Schematic



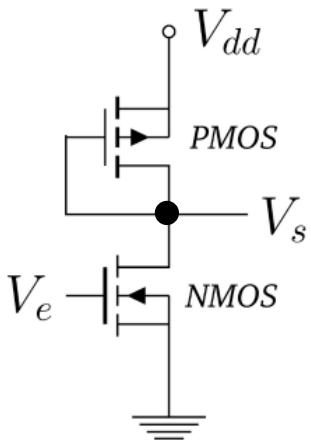
Layout



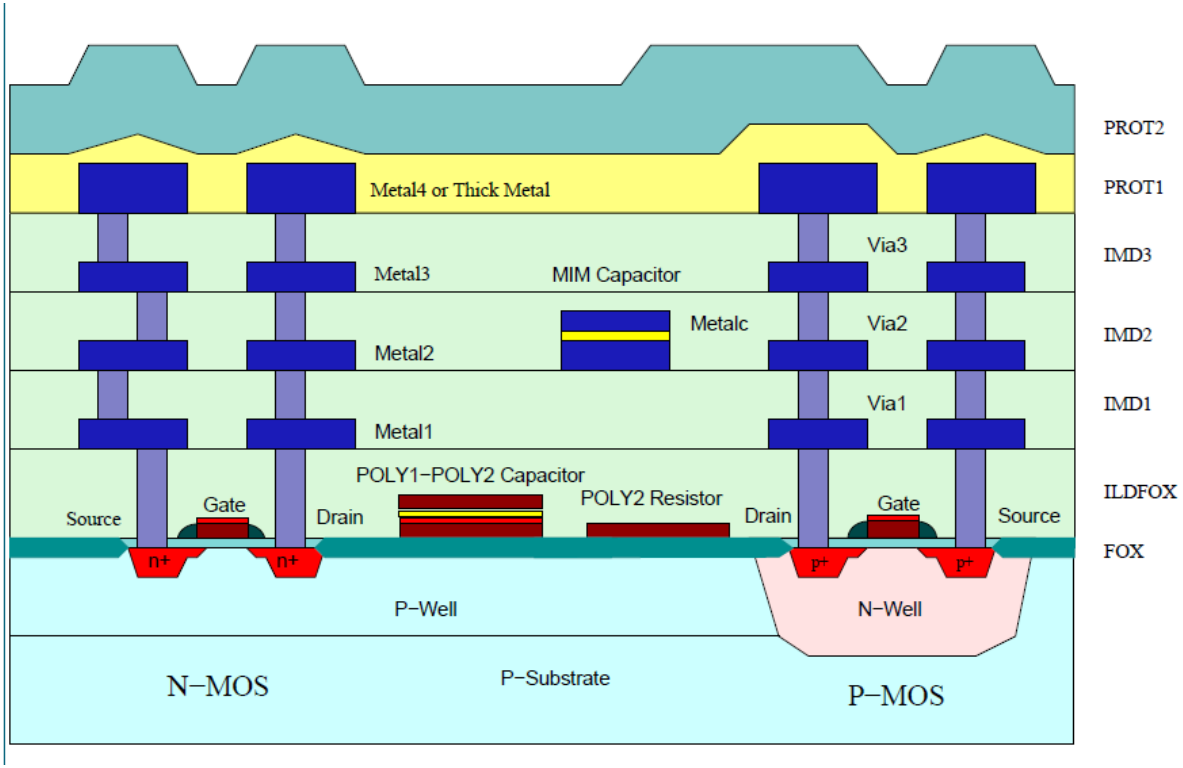
Packaged IC

This class implements Cadence CAD-Tools.

Analog cell and CMOS technology



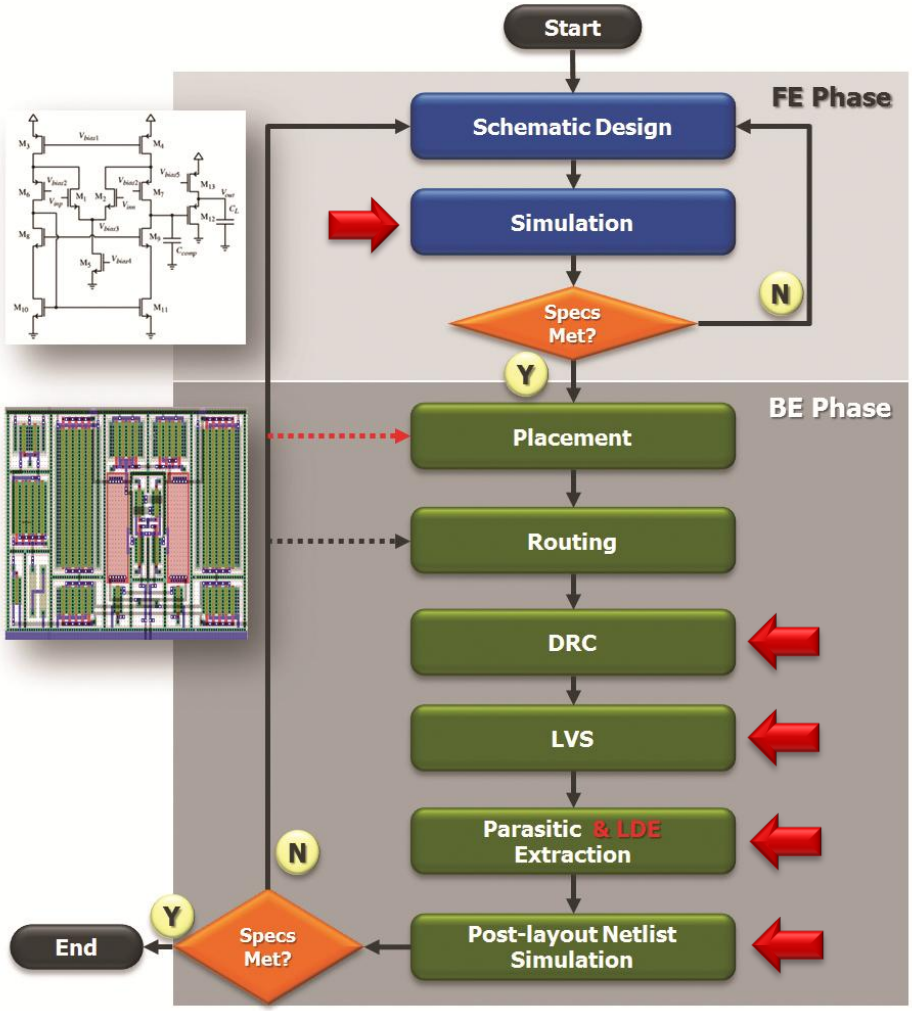
Analog cell (inverter)



Austriamicrosystems (AMS) 0.35 µm CMOS

(http://cmp.imag.fr/aboutus/slides/slides2007/03_KT_AMS.pdf)

IC design flows



Schematic:
- Basics design computations
- Parametric study based on static, transient, small signal simulations and noise analysis

Layout:
- Design Rule check
- Layout versus Schematic verification
- Parasitic components extraction
- Post-layout simulation

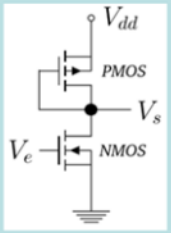
Steps addressed by the lab

Design calculations

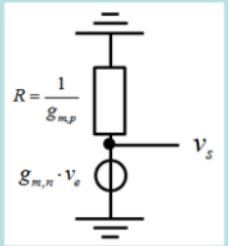
Design calculations.xlsx - Microsoft Excel

Mise en page | Formules | Données | Révision | Affichage | Compléments

In the saturation region ($|V_{GS}| > V_T$ and $|V_{DS}| > |V_{DS\,sat}|$) :



small signal



$$A = \frac{v_s}{v_e} = -\frac{g_{m,n}}{g_{m,p}}$$

$$|Id_p| = \frac{K_p}{2}\frac{W_p}{L_p}(V_{GSp} - V_{Tp})^2$$

$$Id_n = \frac{K_n}{2}\frac{W_n}{L_n}(V_{GSn} - V_{Tn})^2$$

$$g_{m,n} = \sqrt{2 \times K_n \times \frac{W_n}{L_n} \times I_d}$$

$$g_{m,p} = \sqrt{2 \times K_p \times \frac{W_p}{L_p} \times I_d}$$

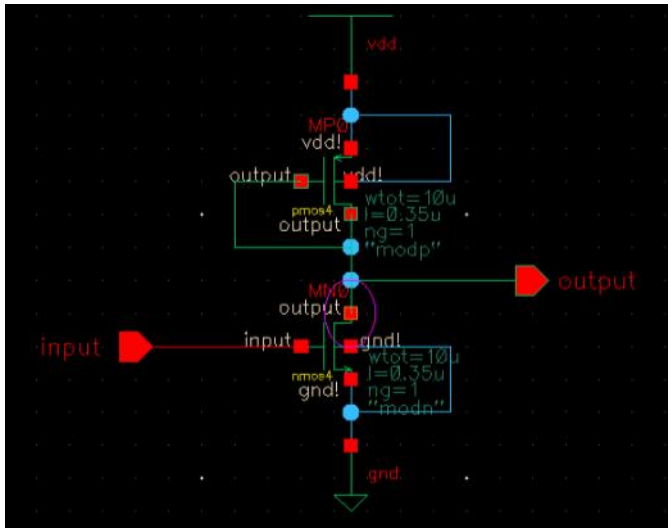
$$|A| = \left|\frac{v_s}{v_e}\right| = \sqrt{\frac{K_n W_n L_p}{K_p W_p L_n}}$$

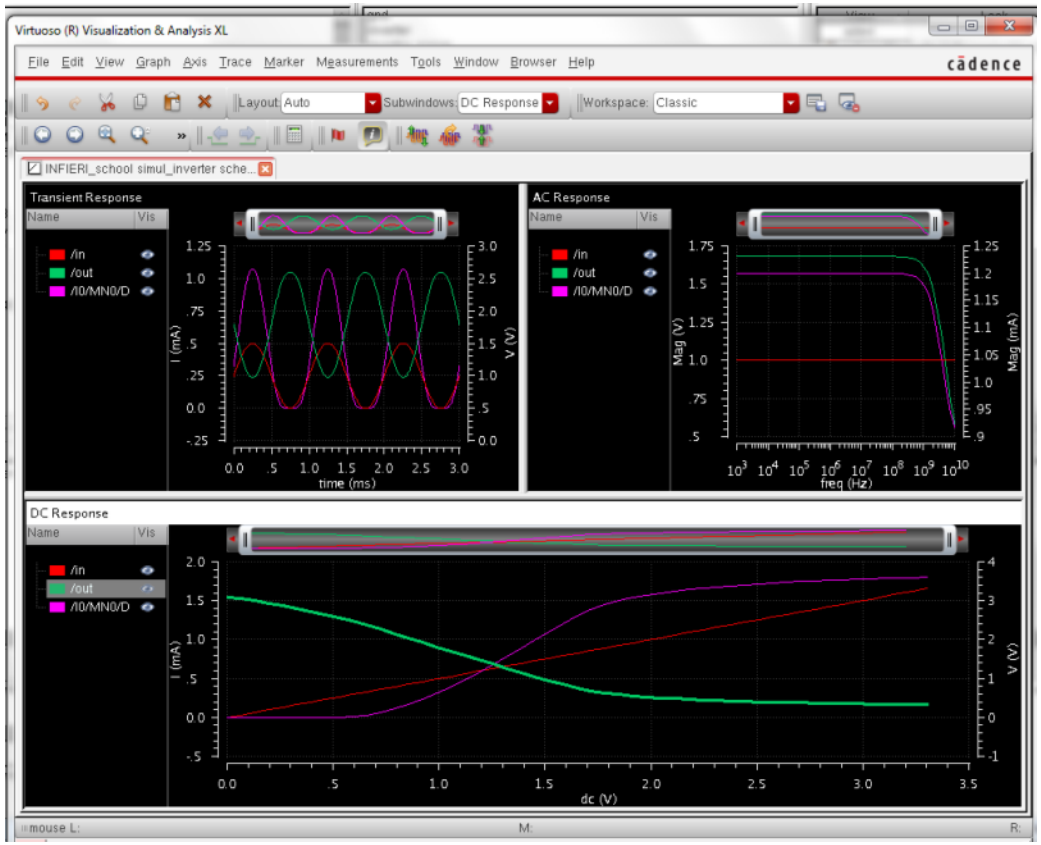
Transistor sizes are chosen for *DC* bias point and *AC* gain achievments

Typical Technological parameters @3.3V	
Vdd	3,3
|Kp|	58
|Vtp|	0,65
Kn (µA/V²)	170
Vtn (V)	0,5

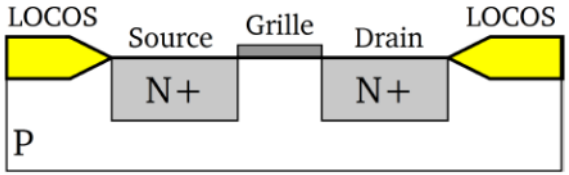
Ve (V)	0,55
Vs (V)	2,6
Ln (µm)	0,35
Wn (µm)	10
Lp (µm)	0,35
Wp (µm)	29
Idp (µA)	6,1
Idn (µA)	6,1
Gain	-1

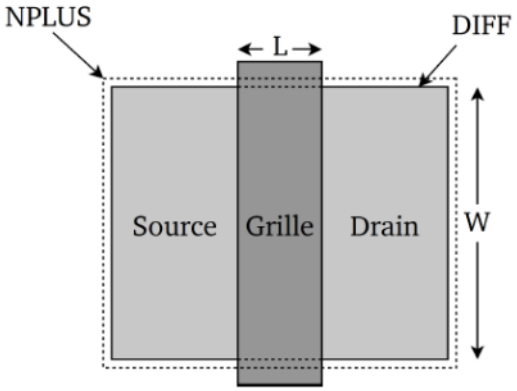
Simulations



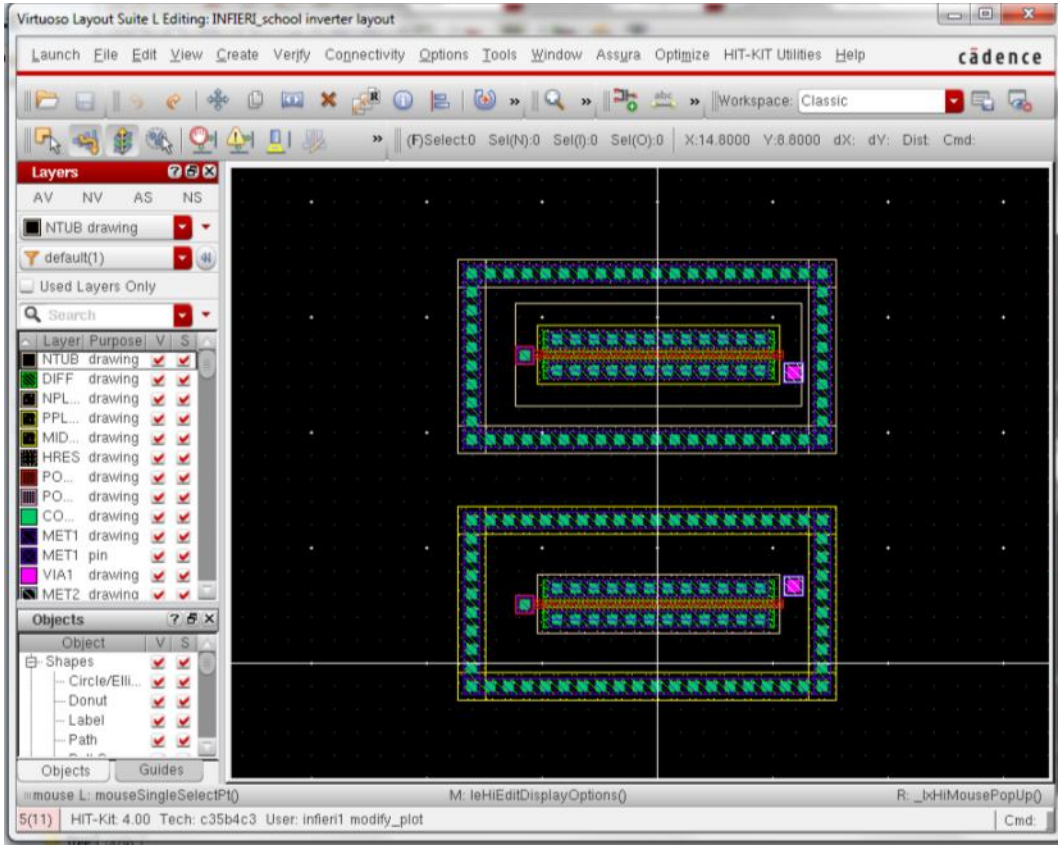


Layout



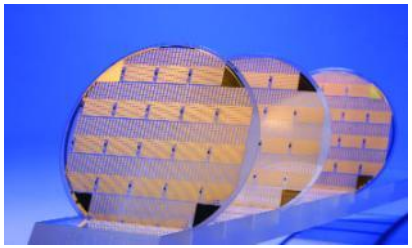


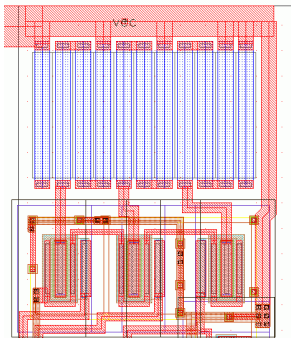
(a) Transistor NMOS



Process and Mismatch simulations

- Wafer production will always show some variation of technological parameter





- Mismatch on design parameters components

=> Monte-Carlo Process and Mismatch simulations will be run