Introduction to 2.5/3D Semiconductors

Robert Patti, CTO

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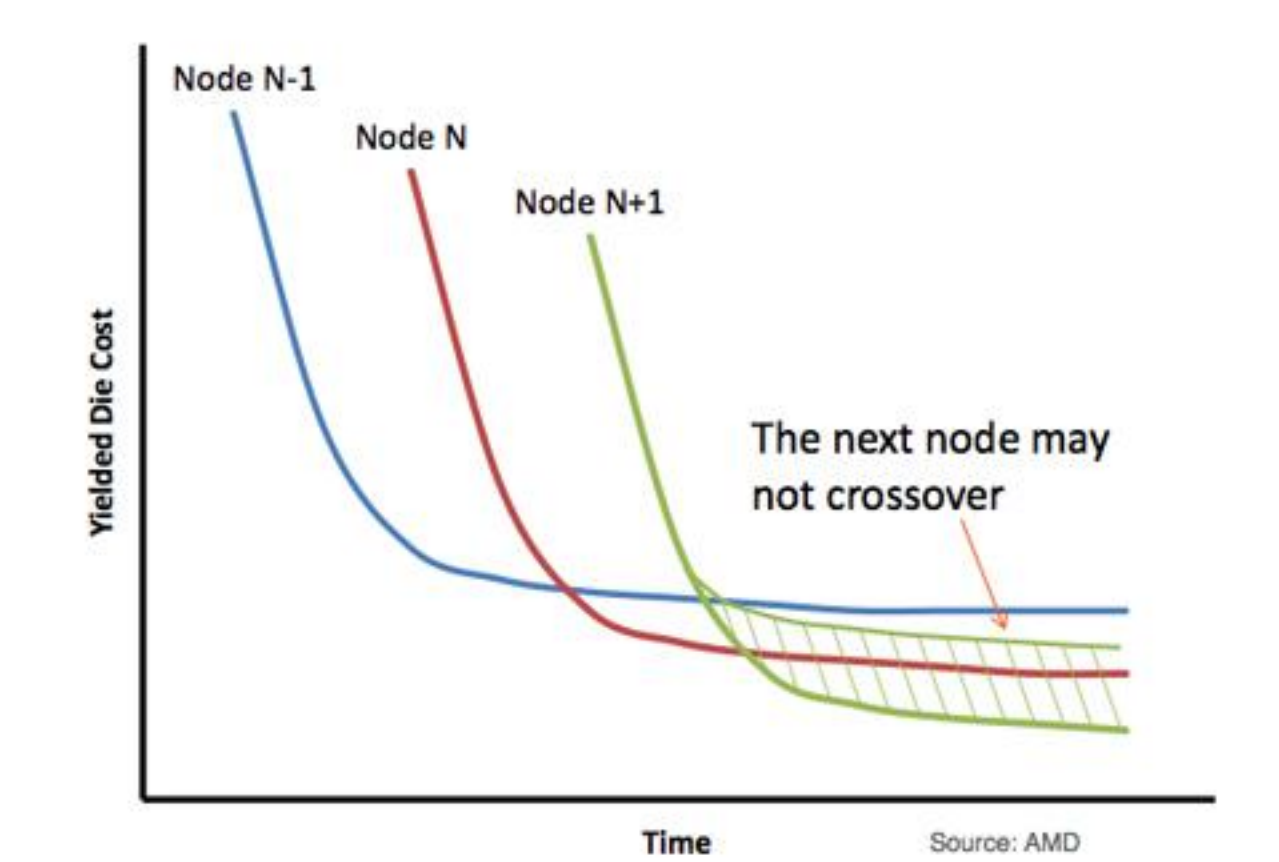
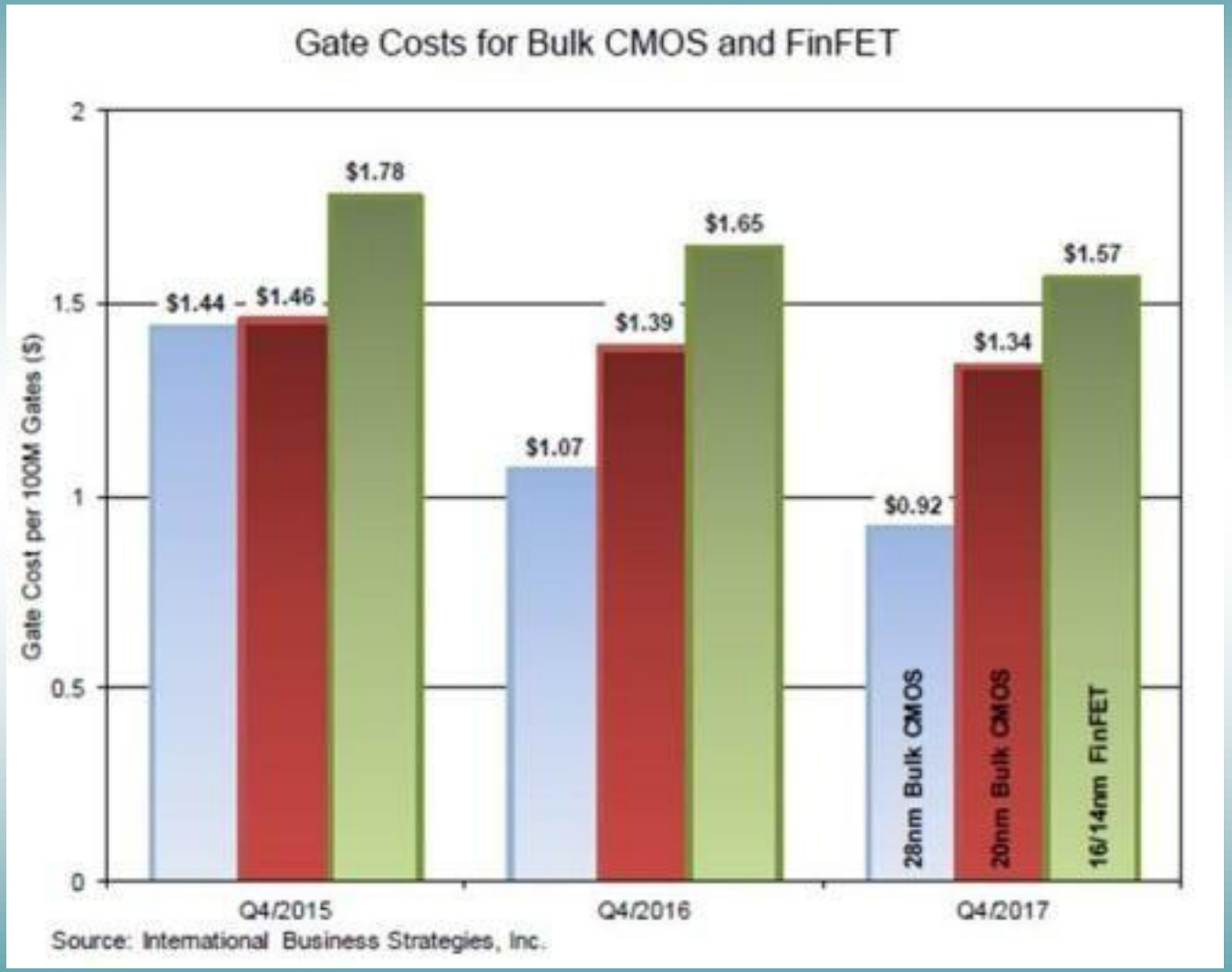
Why 3D? – Expiring Economics

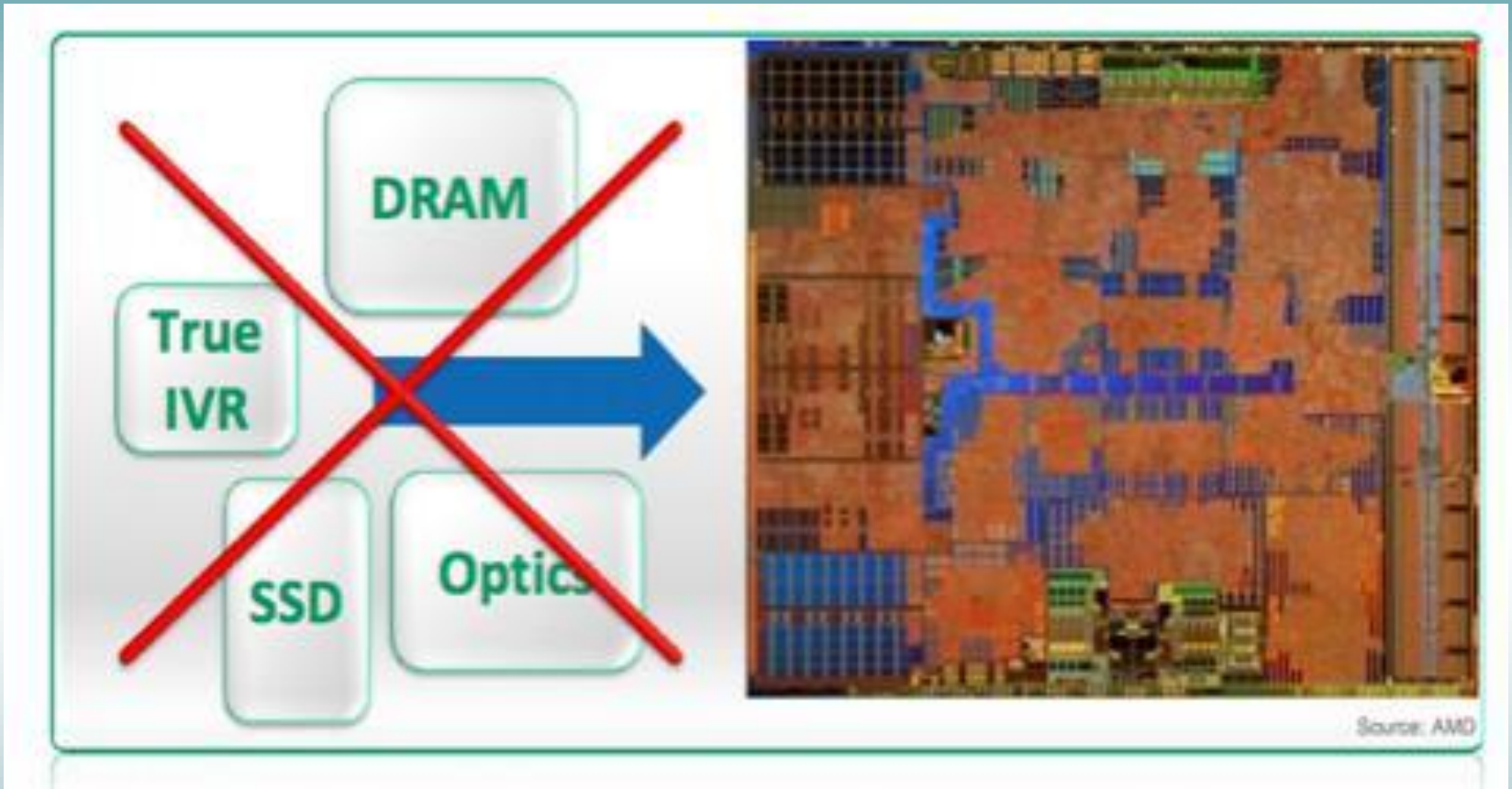


AMD 2014 3D-ASIP

Why 3D? – Expiring Economics

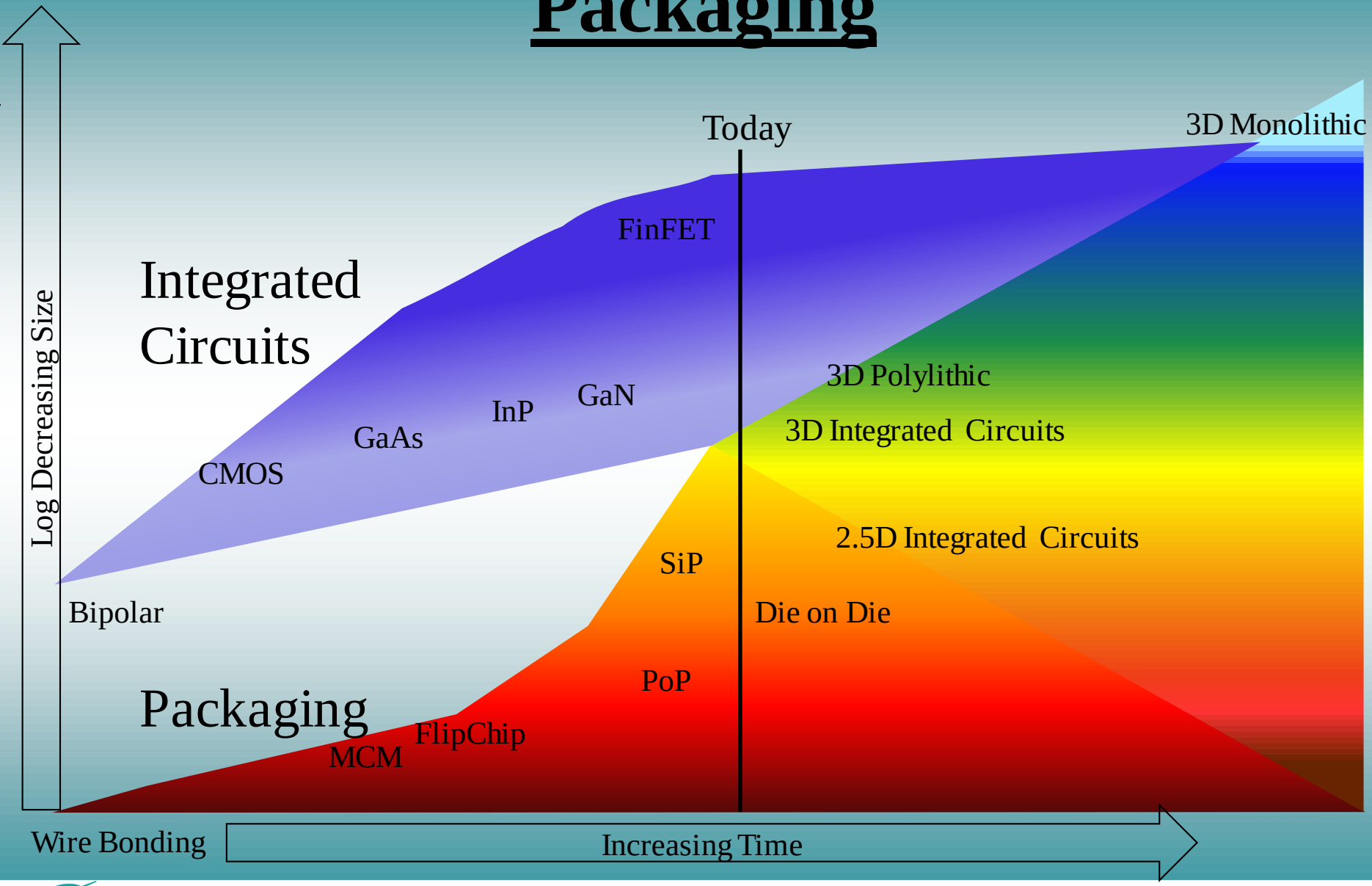


Why 3D? – Apples & Oranges

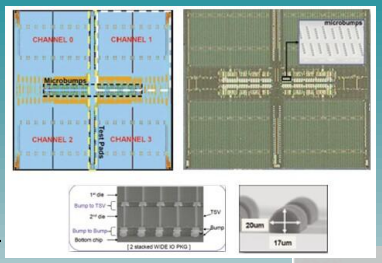


It's a car and it's a boat, that flies… And it's a ***submarine*** *… which can travel to the moon…*

Blending of Integrated Circuits and Packaging

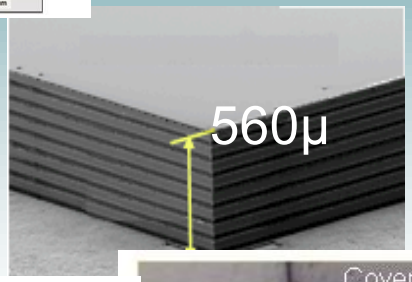


There is a lot of 3D today



Samsung

16Gb NAND flash (2Gx8 chips),
Wide Bus DRAM

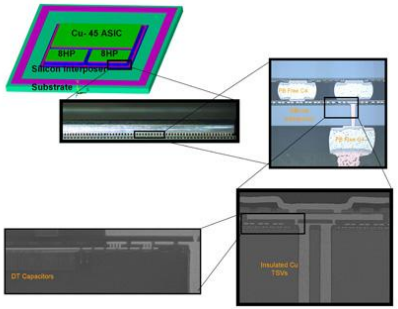


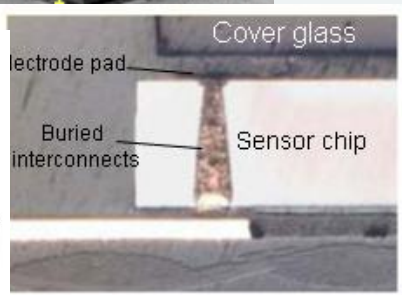
Micron

HMC DRAM

Intel

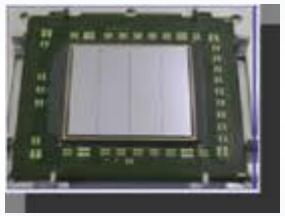
CPU + memory





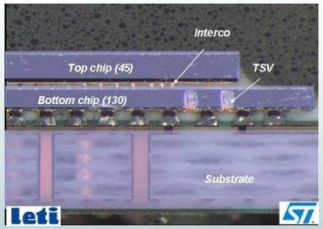
Sony

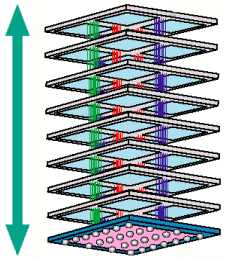
CMOS Sensor

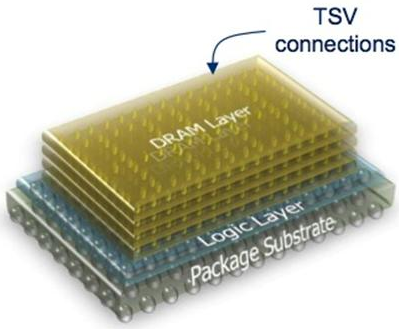


Xilinx

4 die 65nm interposer

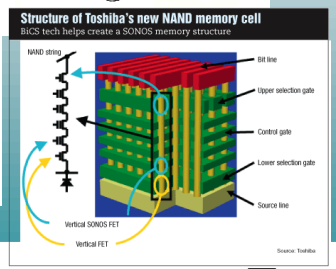


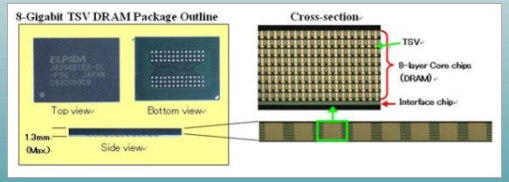




Raytheon

PIN Detector Device





IBM

RF Silicon Circuit Board / TSV
Logic & Analog

Toshiba

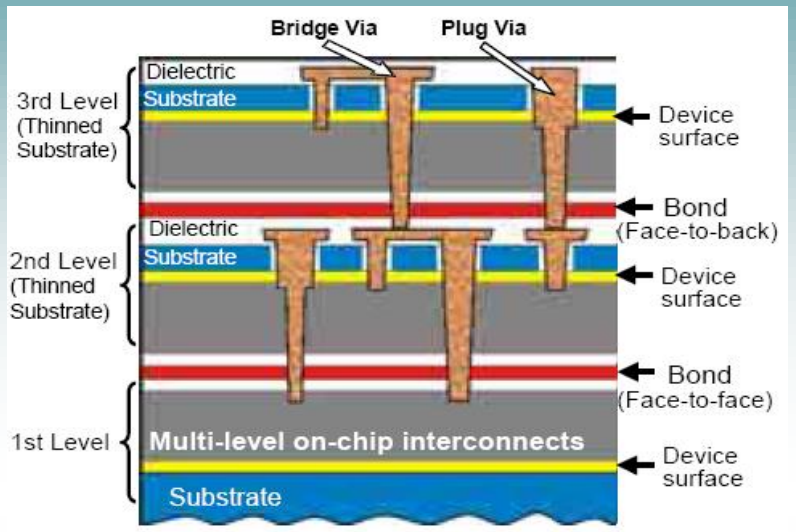
3D NAND

The Killer Apps

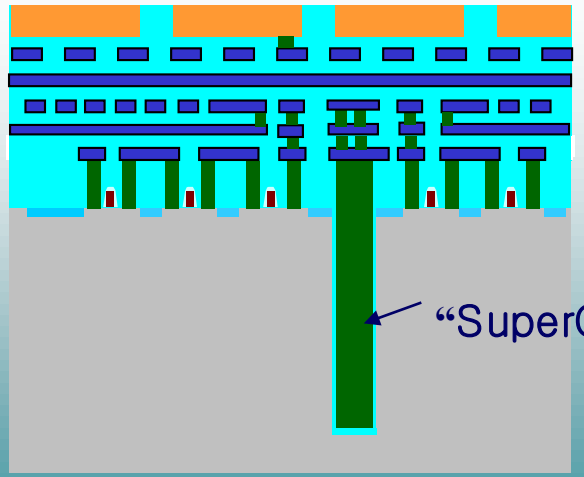
- Sensors
  - Heterogeneous materials
  - 100% array efficiency
  - Data reduction
- Computing
  - Eases power issues – a lot in some cases
  - Improves latency
  - Accelerates new technology introduction
- Mixing MEMS, RF, Mixed Signal, Processing
  - Johnson Figure of Merit
- Photonics

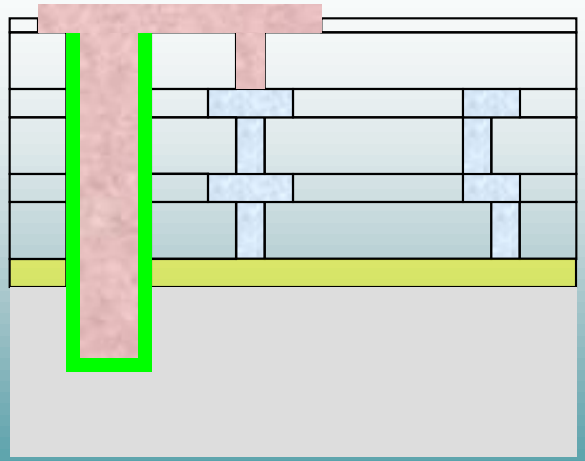
Through-Silicon Via (TSV)

- Via First
- Via Last
- Via at Front end (FEOL)
- Via at Mid line (MEOL)
- Via at Back end (BEOL)



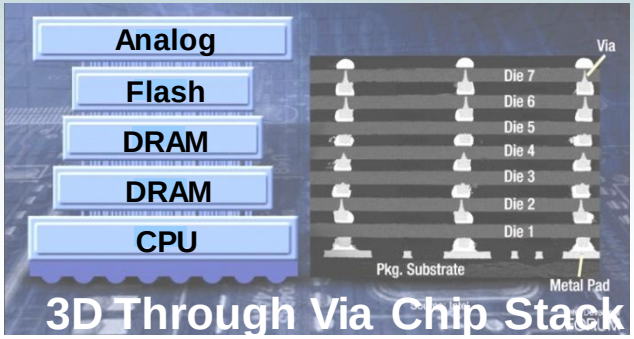
Dr. J.Q. Lu
RPI





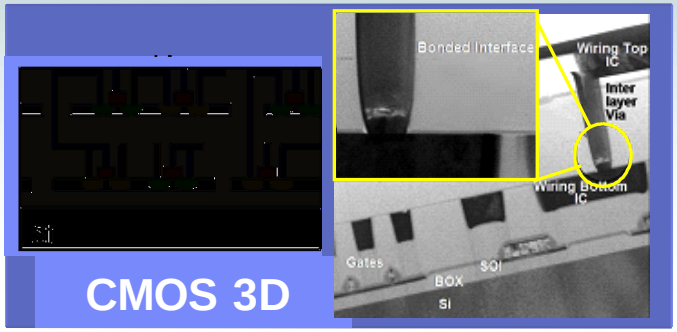
Span of 3D Integration

Packaging



IBM/Samsung

Wafer Fab



IBM

3D-ICs

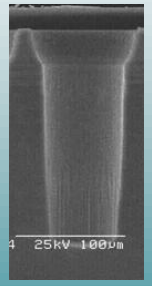
100-1,000,000/sqmm

1000-10M Interconnects/device

1s/sqmm

Peripheral I/O

- Flash, DRAM
- CMOS Sensors



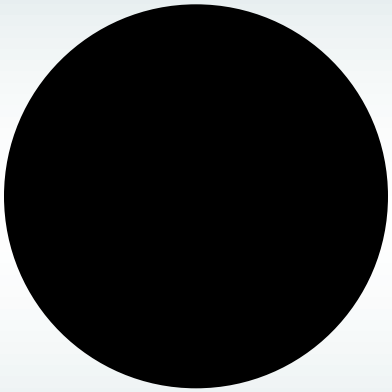
100,000,000s/sqmm

Transistor to Transistor

- Ultimate goal

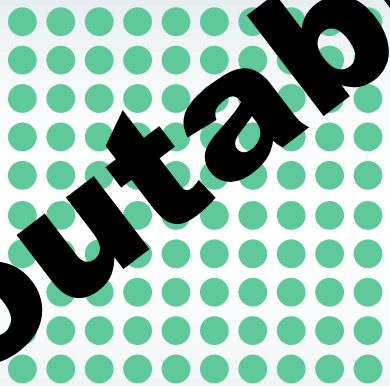
Smaller is Better!

One



10µ Diameter
Copper TSV

100



Routable

1µ Diameter
Tungsten SuperContact

3D Interconnect Characteristics

	SuperContact™ I 200mm Via First, FEOL	SuperContact™ IV 200mm Via First, FEOL	SuperContact™ V 300mm Via F/L, FEOL	SuperContact™ VI 300mm Via F/L, FEOL	Interposer TSV	Bond Points	Die to Wafer
Size L X W X D Material	1.2 µ X 1.2 µ X 6.0µ W in Bulk	0.6 µ X 0.6 µ X 2µ W in SOI	1.2 µ X 1.2 µ X 6µ W in Bulk	0.8 µ X 0.8 µ X 6µ W in Bulk	10 µ X 10 µ X 100 µ Cu	1.2 µ X 1.2 µ Cu	2.5 µ X 2.5 µ Cu
Minimum Pitch	<2.5 µ	1.2 µ	2.4 µ	1.6 µ	30 µ	2.4 µ	5 µ
Feedthrough Capacitance	2fF	0.2fF	1.5fF	1.2fF	150fF	<<	<25fF
Series Resistance	<1.5 Ω	<1.75 Ω	<2.0 Ω	<3.0 Ω	<0.5 Ω	<	<

Small fine grain TSVs are fundamental to 3D enablement

3D Approaches

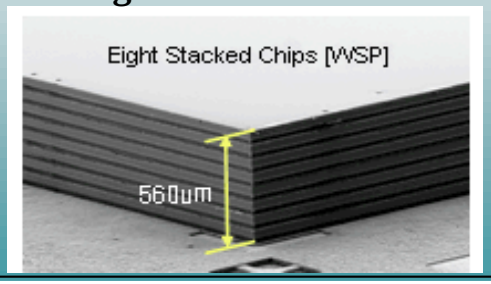
Chip Level

- TSMC
- Tezzaron
- Xilinx
- Intel
- Micron
- Samsung
- Hynix

Amkor : 4S CSP (MCP)

Irvine Sensors : Stacked Flash

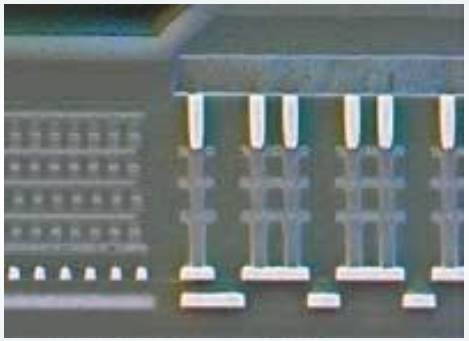
Samsung : Stacked Flash

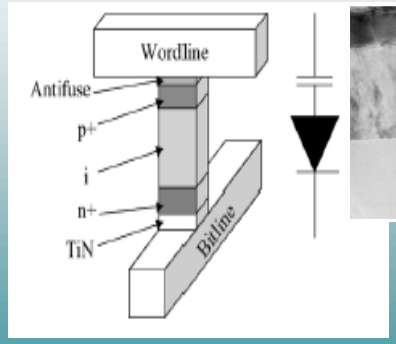


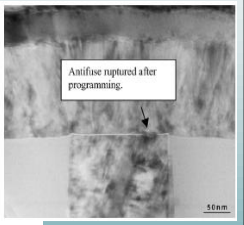
Device Level

- Stanford
- Besang
- LETI
- Sandisk

Matrix: Vertical TFT



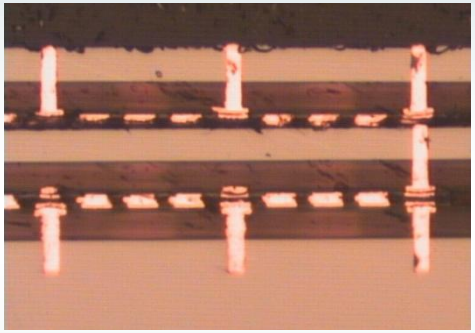


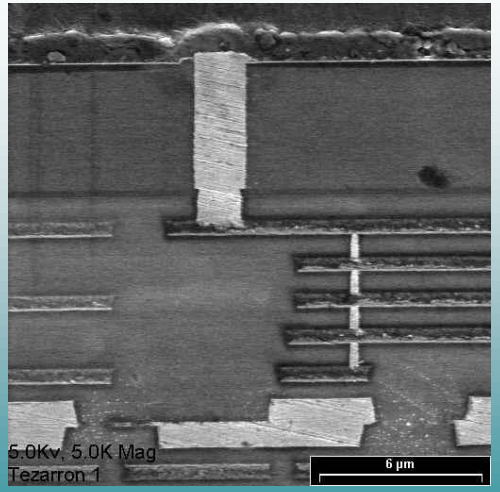


Wafer Level

- Tezzaron
- RPI
- IMEC
- LETI

Tezzaron

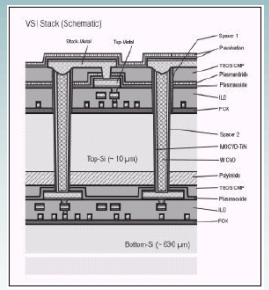


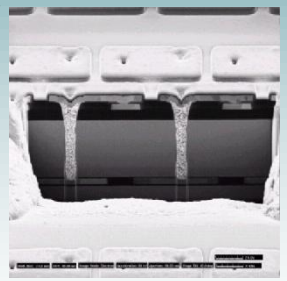


3D Assembly Techniques

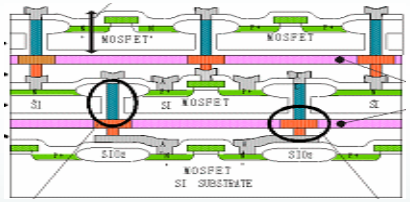
"Glue"

Infineon : W deep via



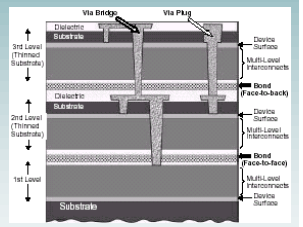


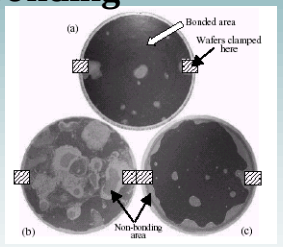
ZyCube : Injection glue bonding



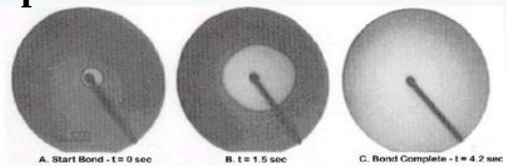
Oxide

RPI : Dielectric bonding

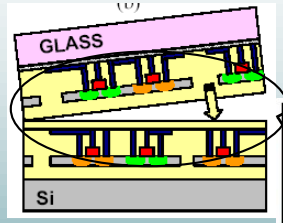


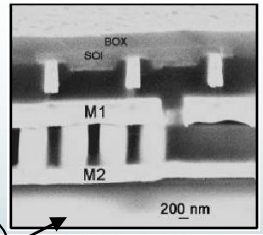


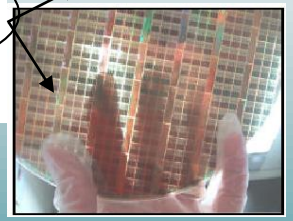
Ziptronix : Covalent bond



IBM : SOI wafer thinning

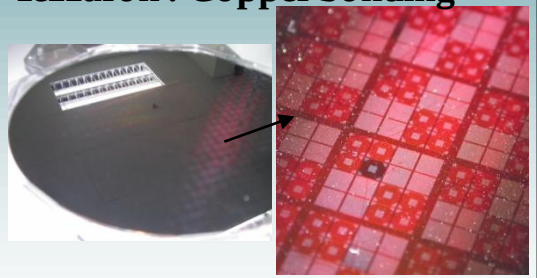




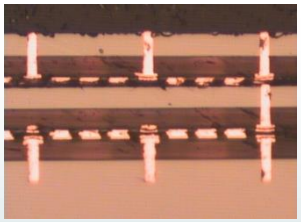


Copper

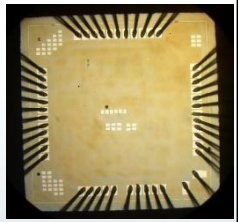
Tezzaron : Copper bonding



Backside of the stacked wafer



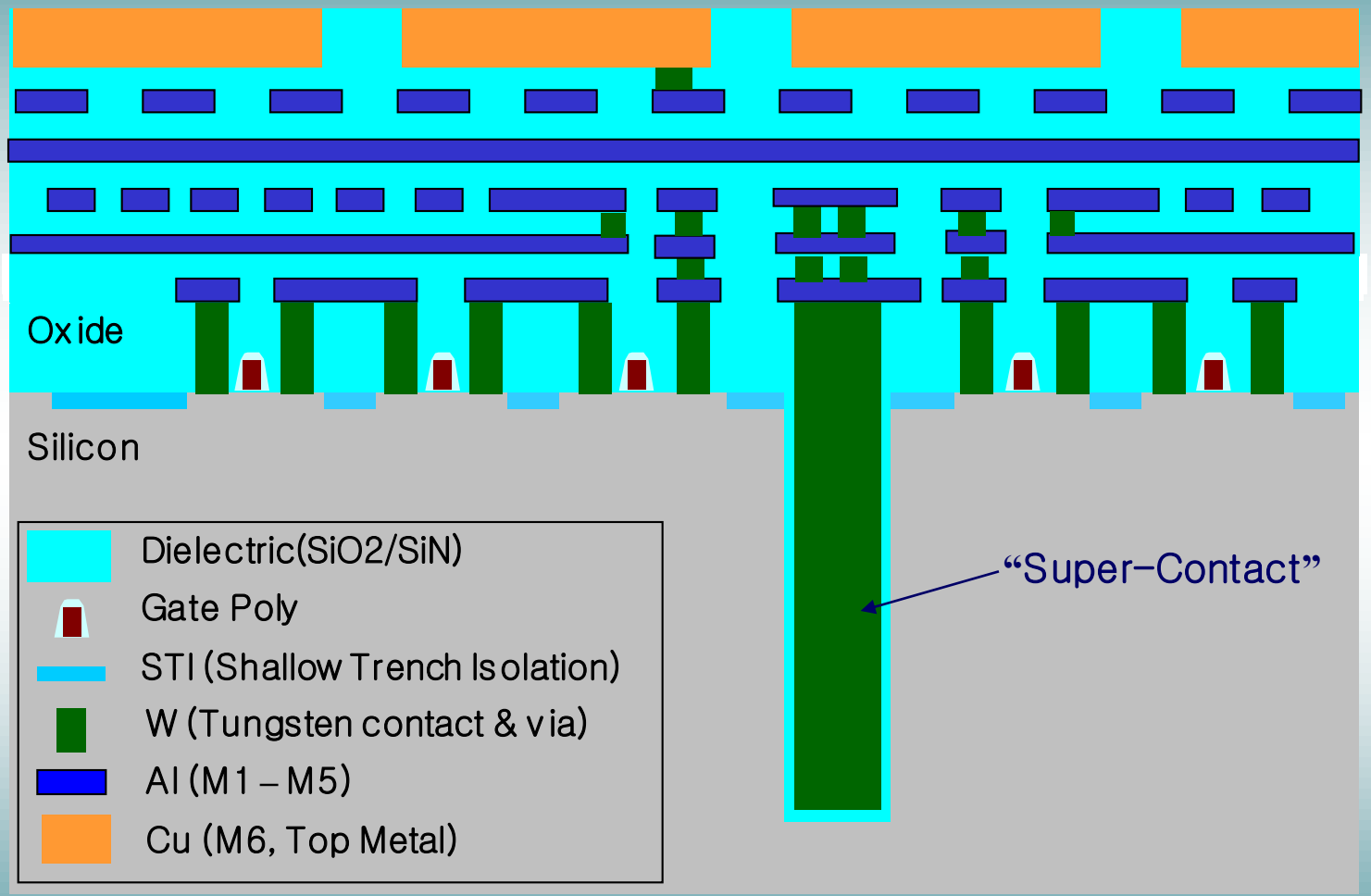
3 wafer stack



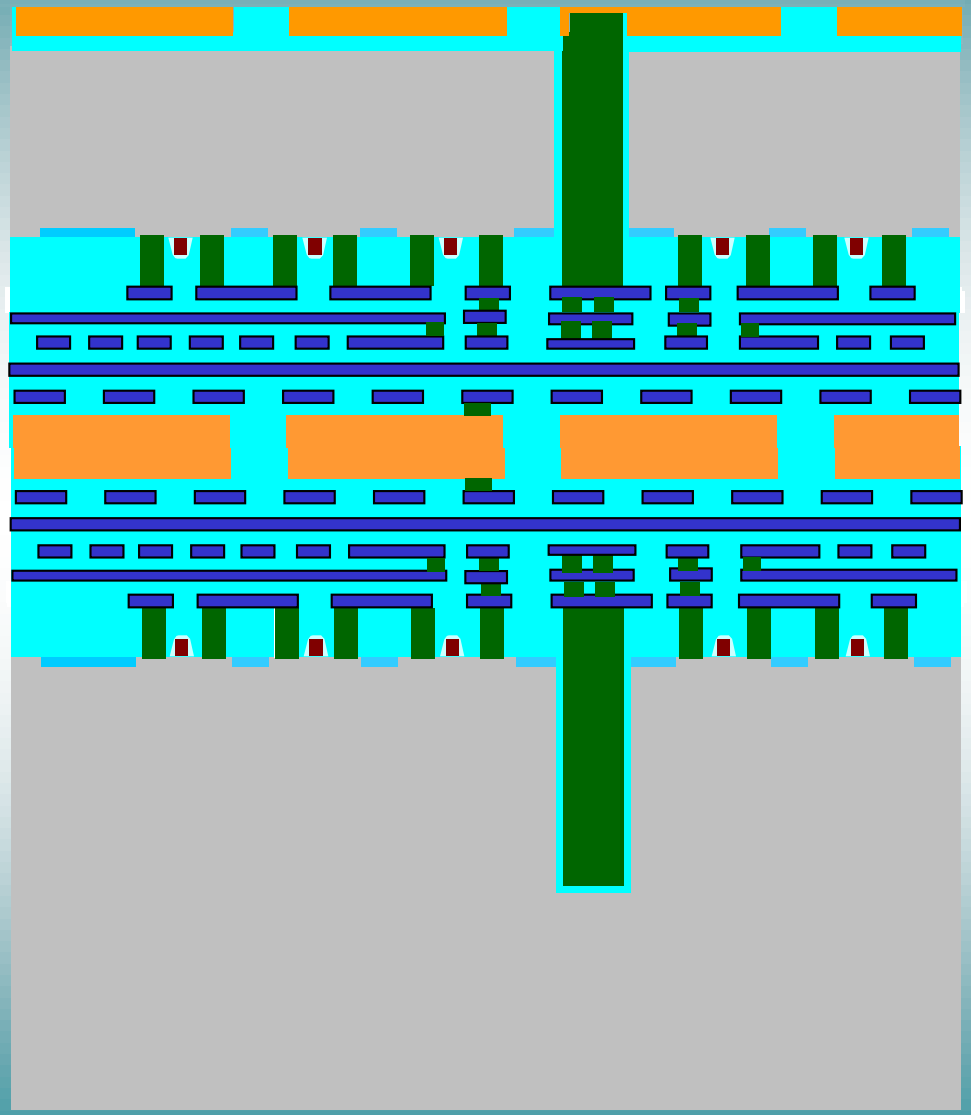
3D Sensor

Hybrid Bonding

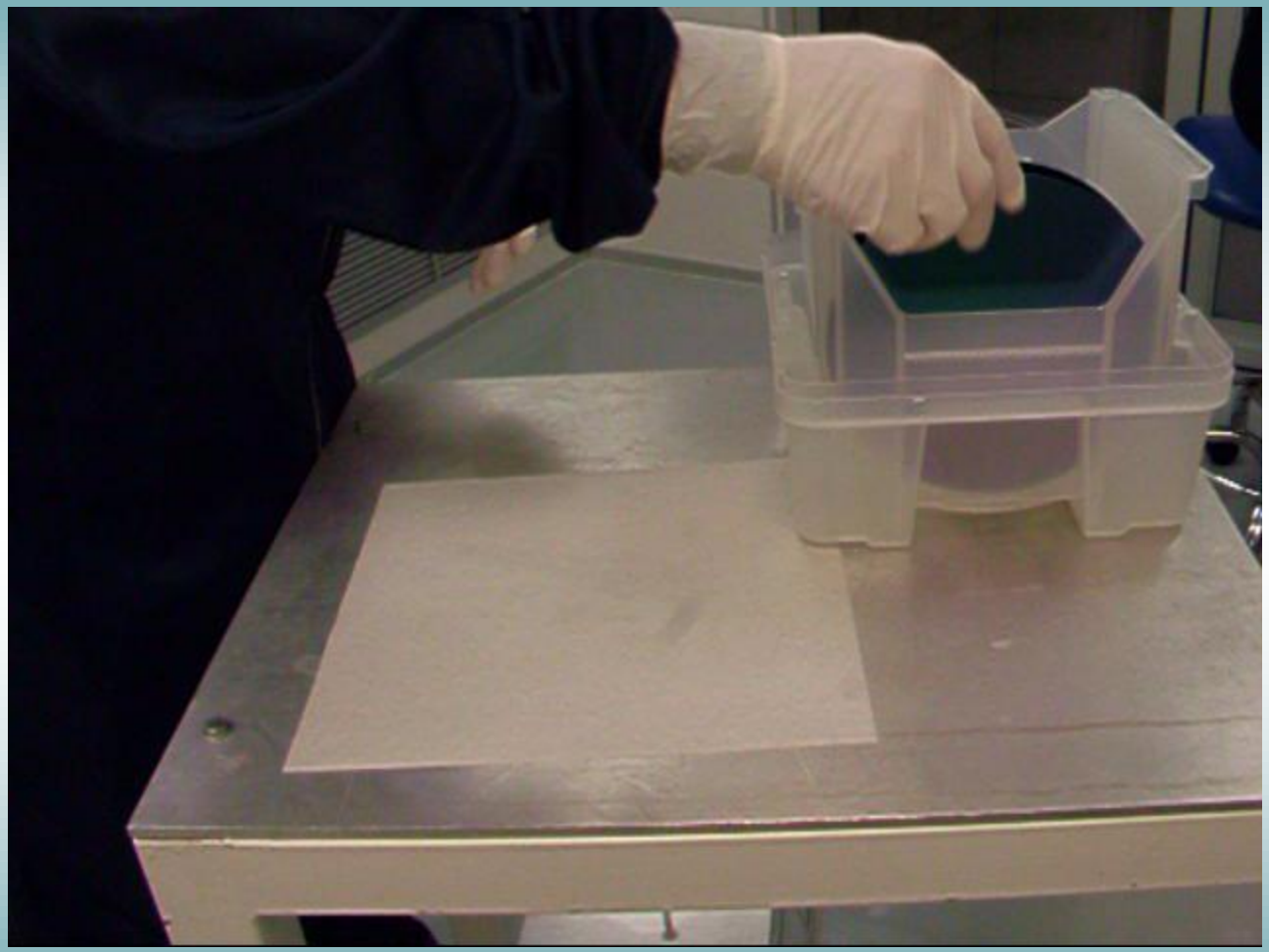
A Closer Look at Wafer-Level Stacking



Next, Stack a Second Wafer & Thin:



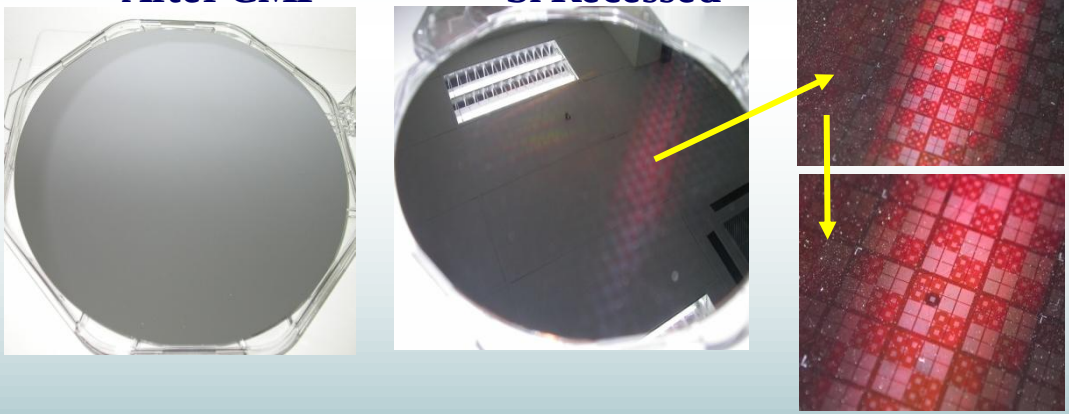
Covalent Oxide Wafer Bonding



Stacking Process Sequential Picture

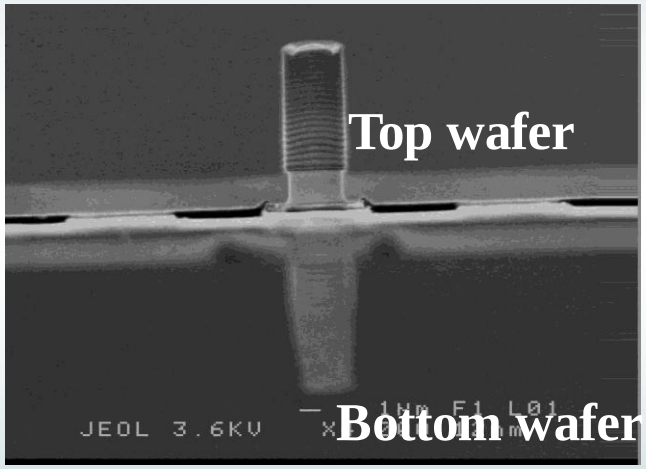
Two wafer Align & Bond → Course Grinded → Fine Grinded

→ After CMP → Si Recessed

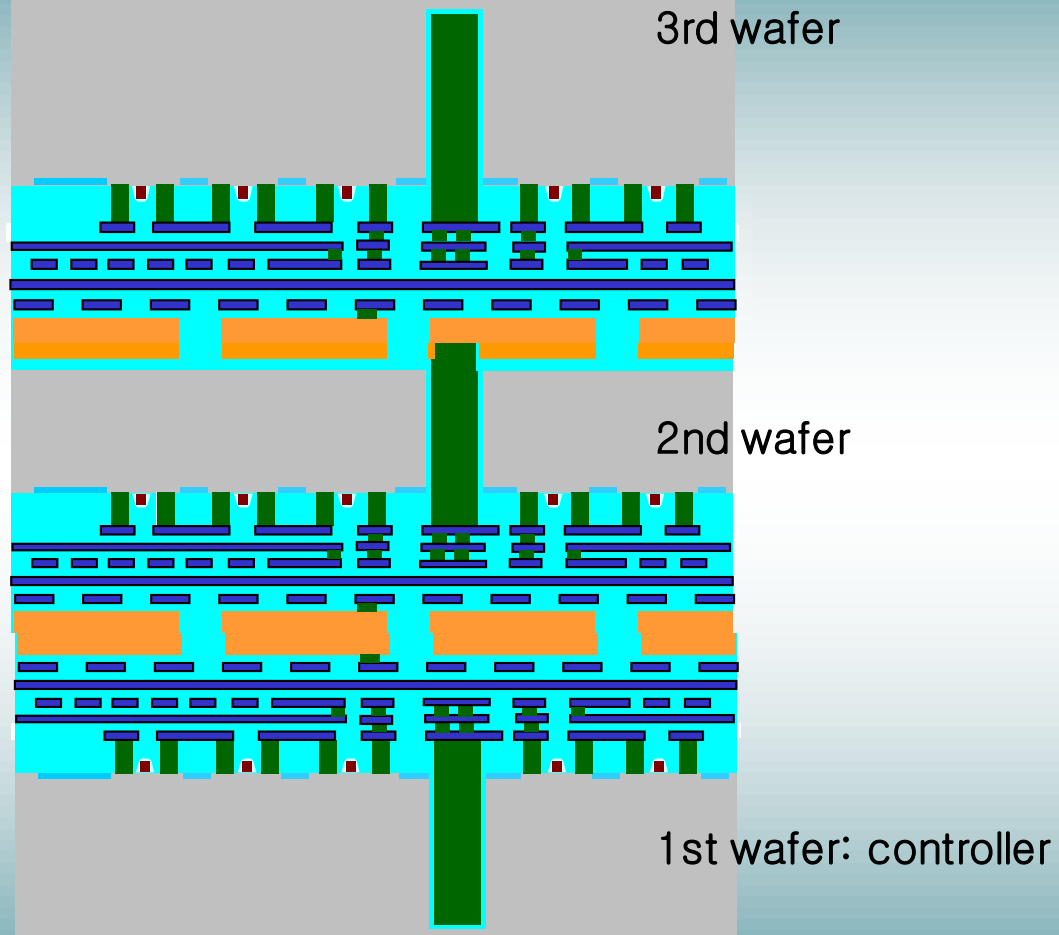


High Precision Alignment

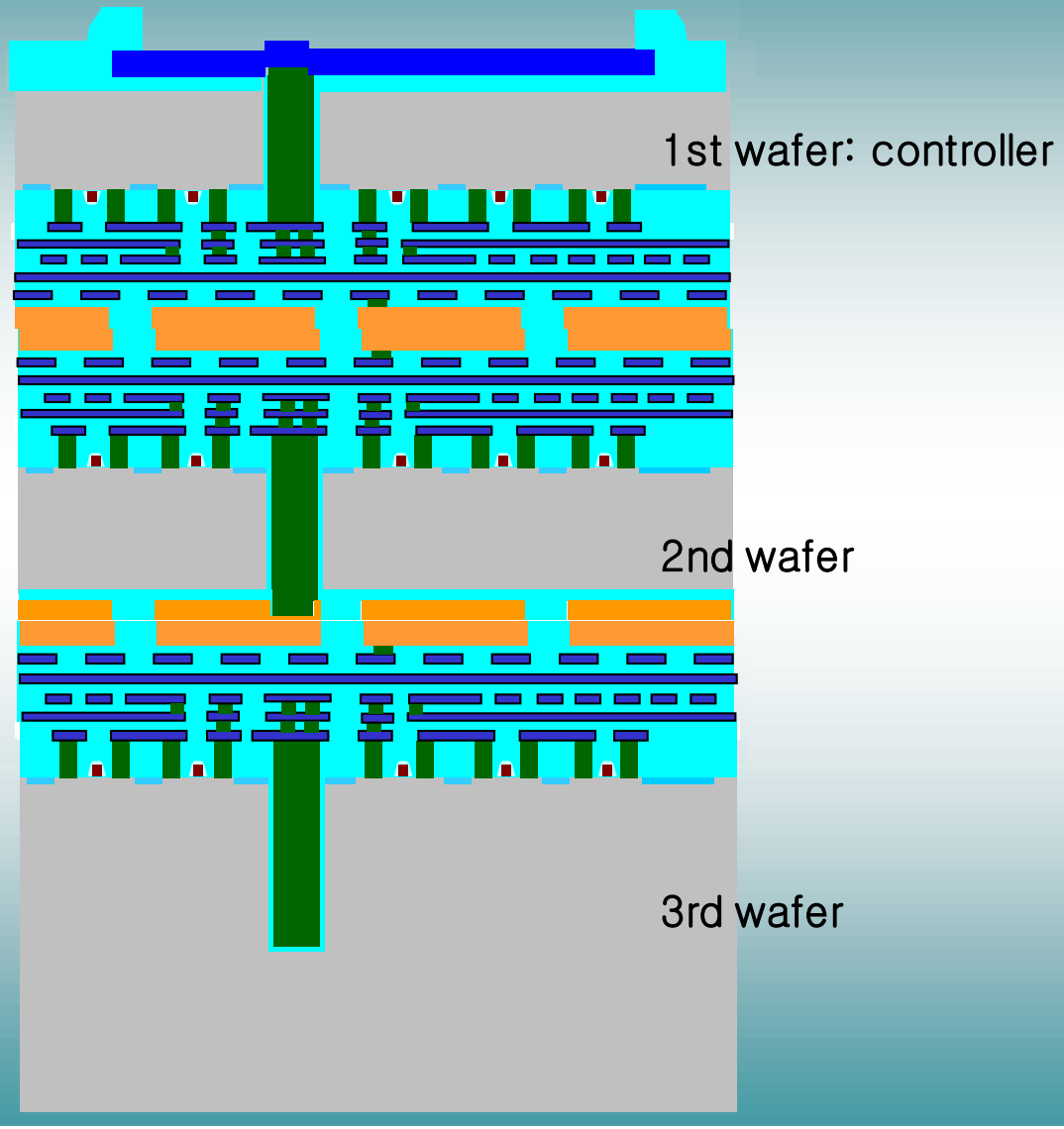
Misalign=0.3um



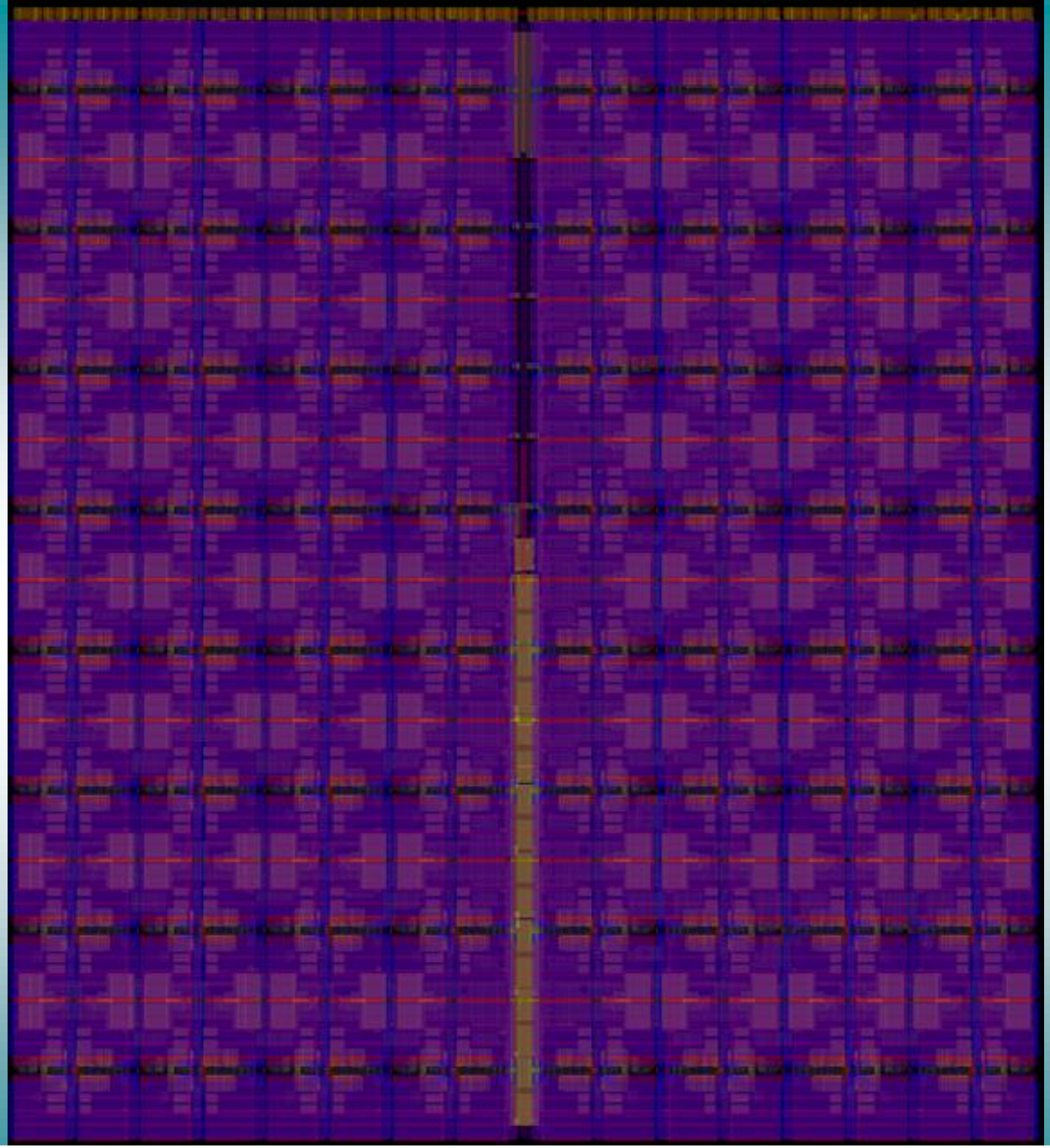
Then, Stack a Third Wafer:

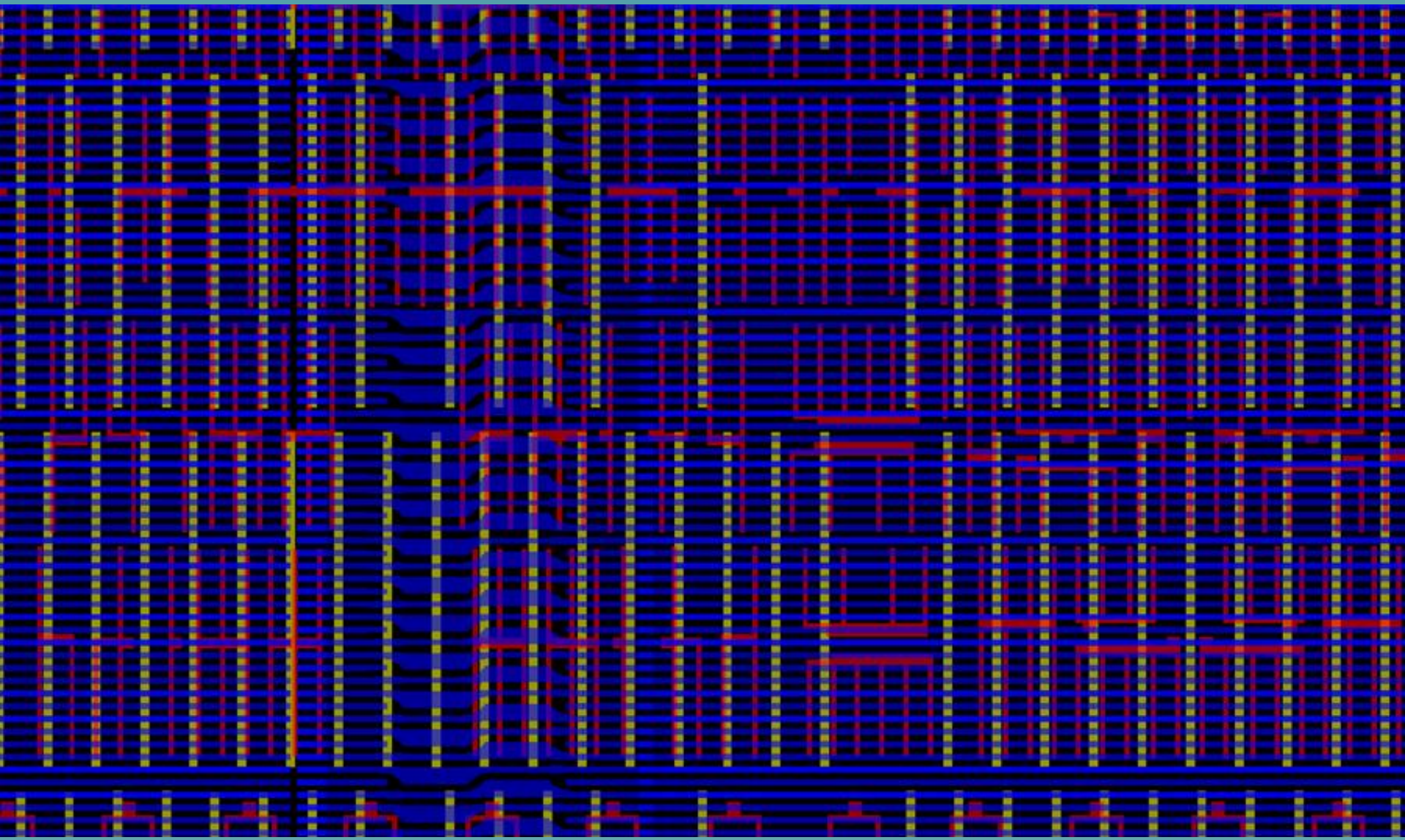


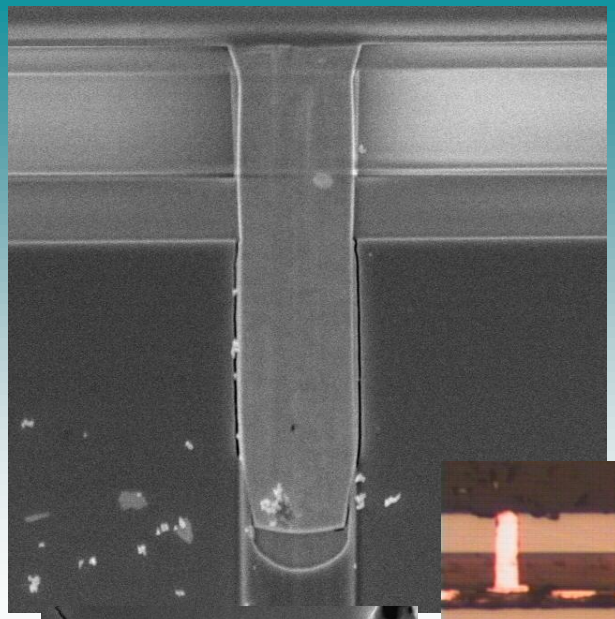
Finally, Flip, Thin & Pad Out:

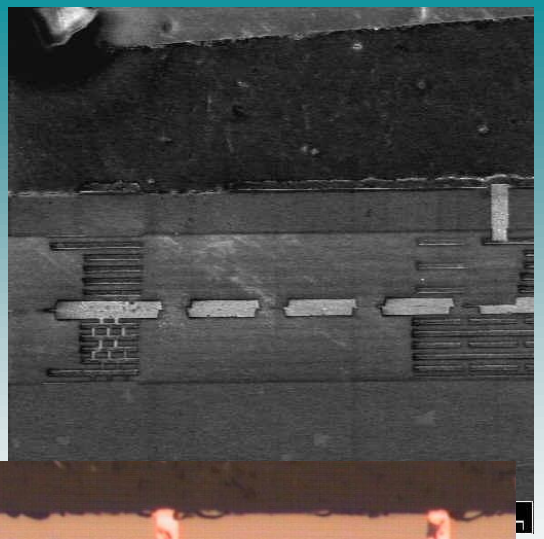


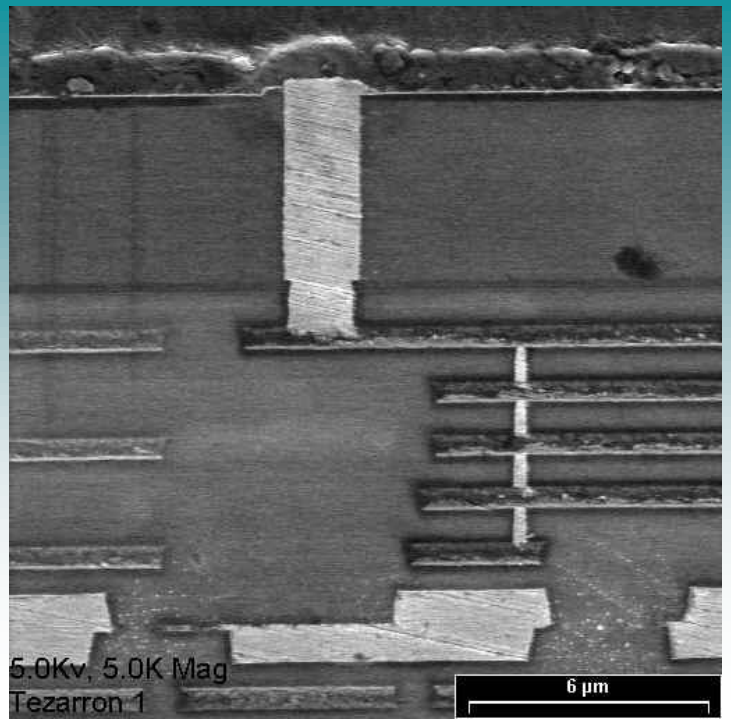
This is the completed stack!

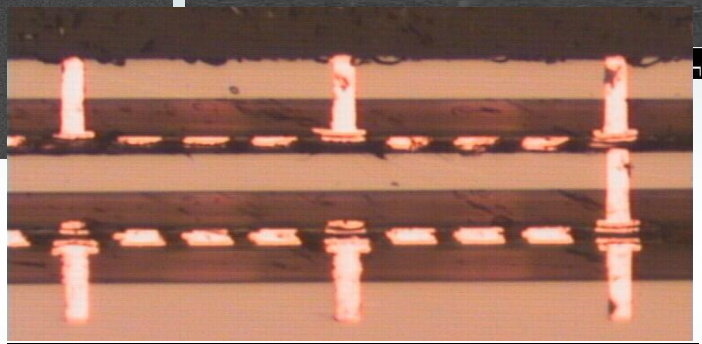


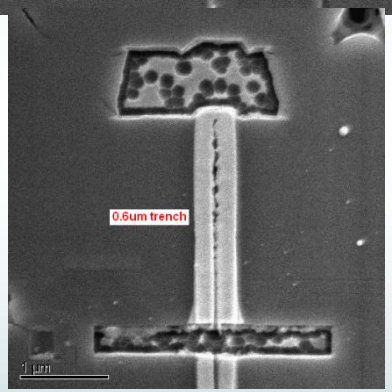


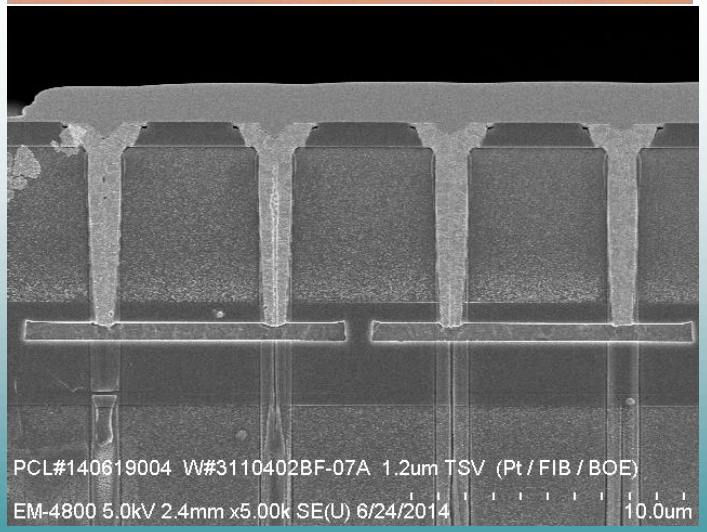


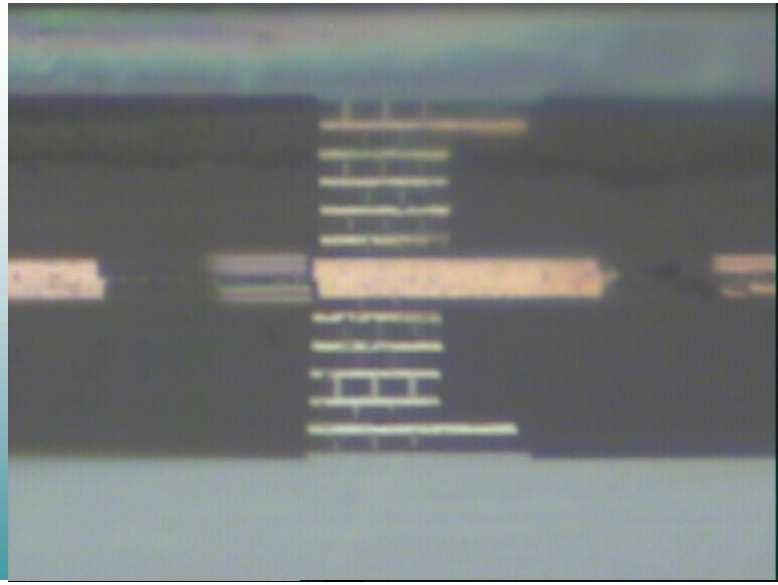



5.0Kv, 5.0K Mag
Tezarron 1
6 µm

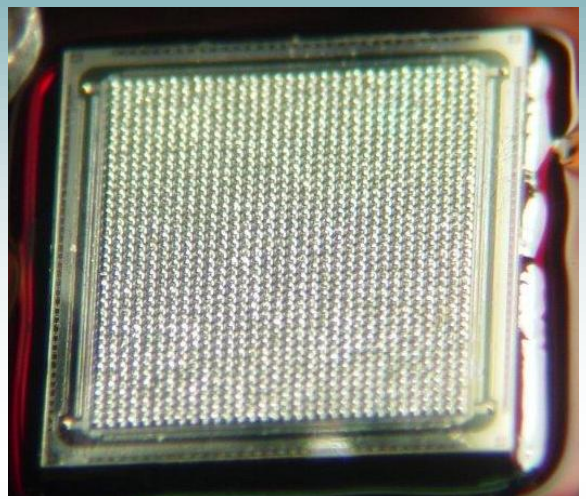


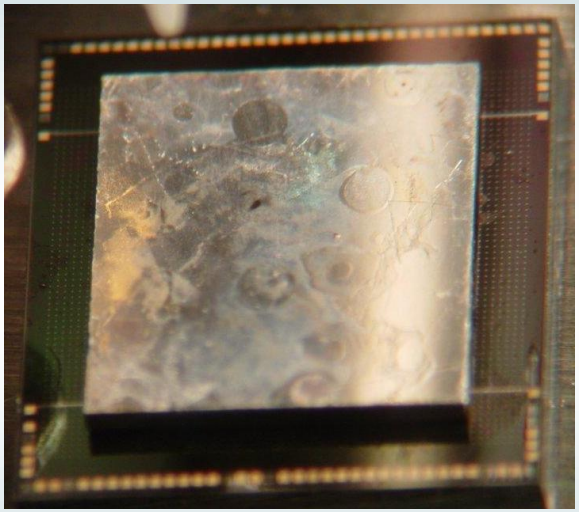

0.6um trench
1 µm

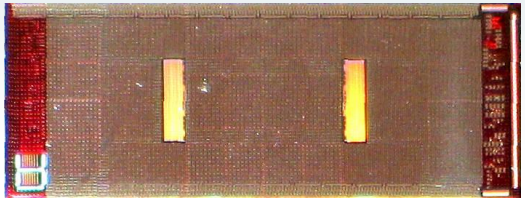

PCL#140619004 W#3110402BF-07A 1.2um TSV (Pt / FIB / BOE)
EM-4800 5.0kV 2.4mm x5.00k SE(U) 6/24/2014
10.0um

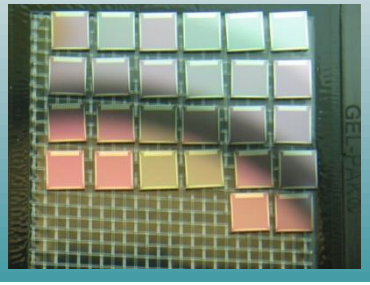


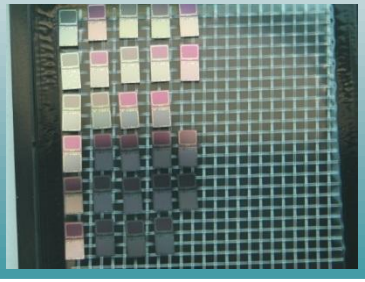
3D Devices

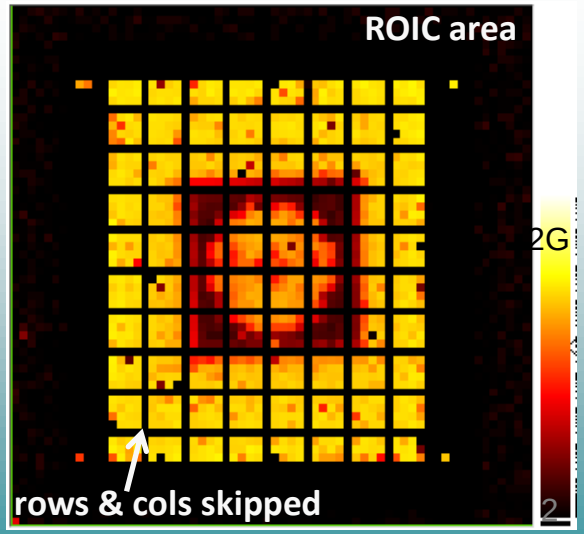




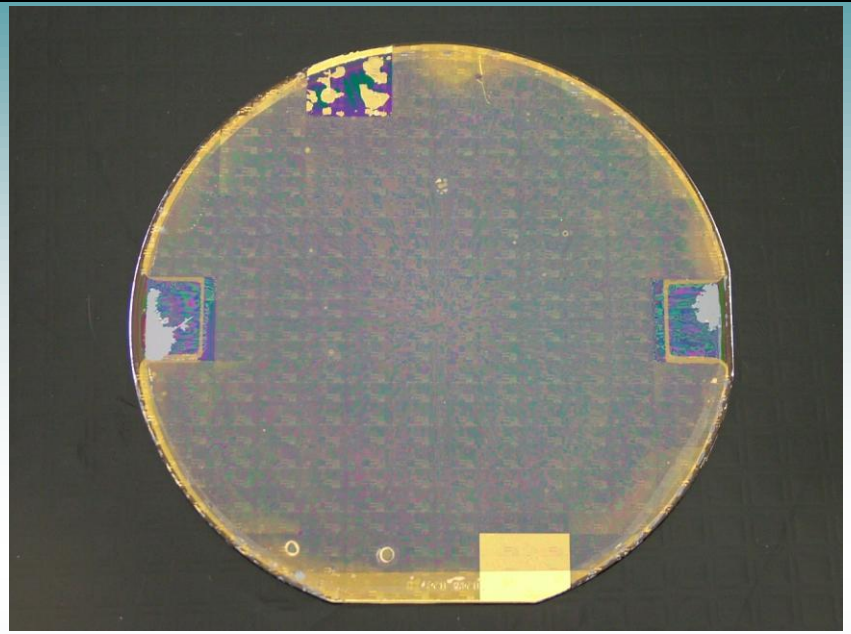








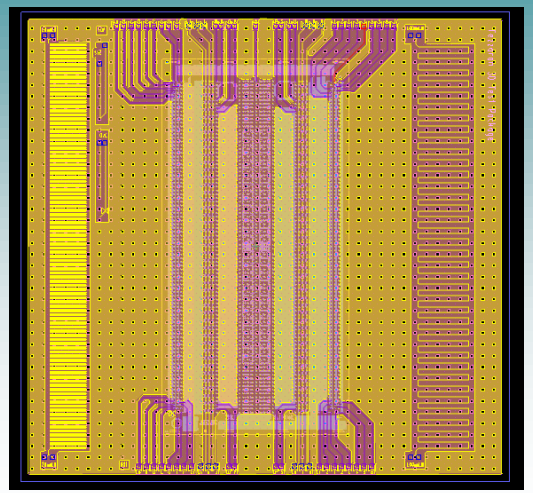
Mixed CMOS-3/5 100mm InP/CMOS

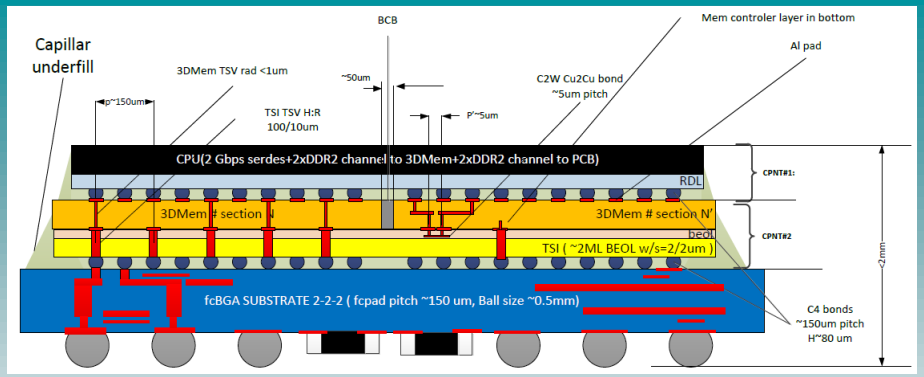


- GaN
- 3D CMOS/InP/GaN
- Graphene

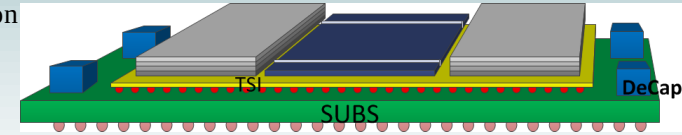
2.5/3D Circuits

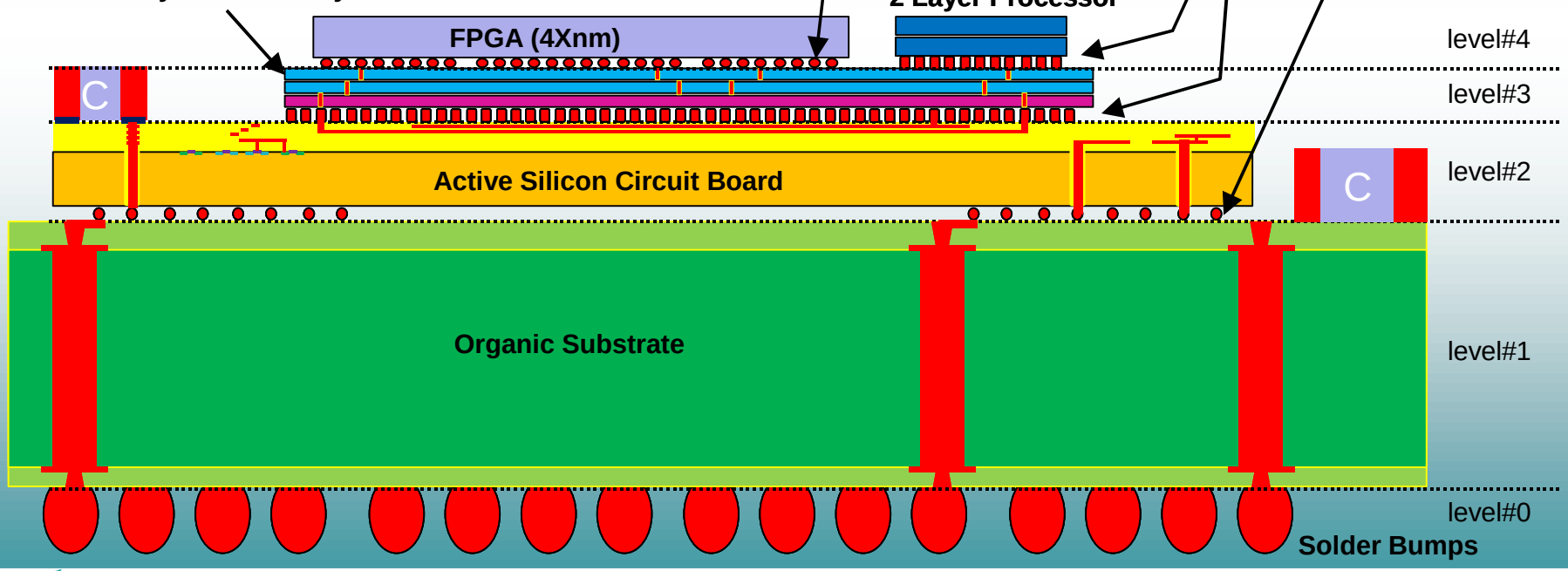
IME A-Star / Tezzaron Collaboration



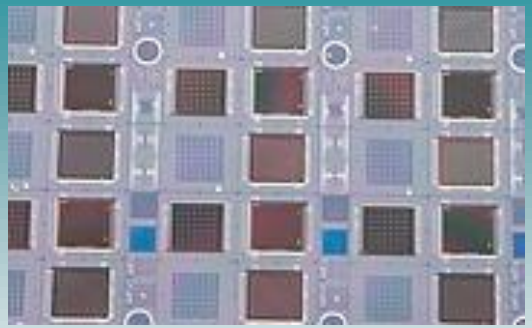


IME A-Star / Tezzaron Collaboration

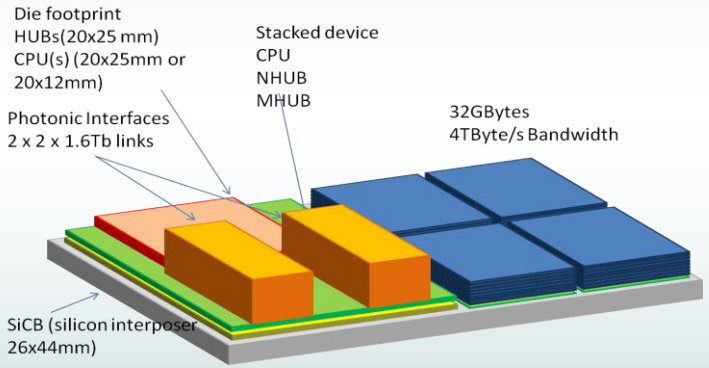


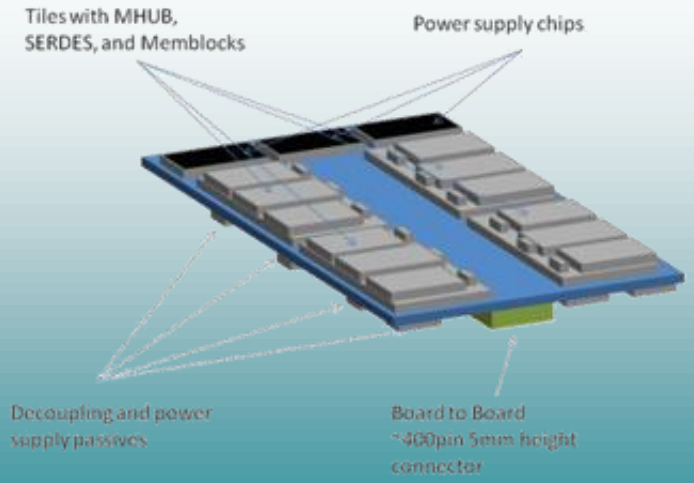


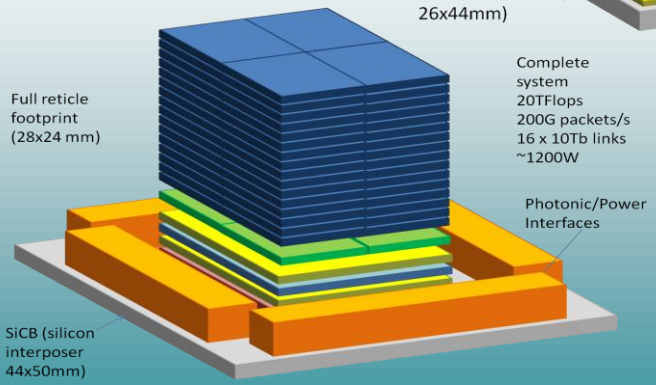
Interposer Systems



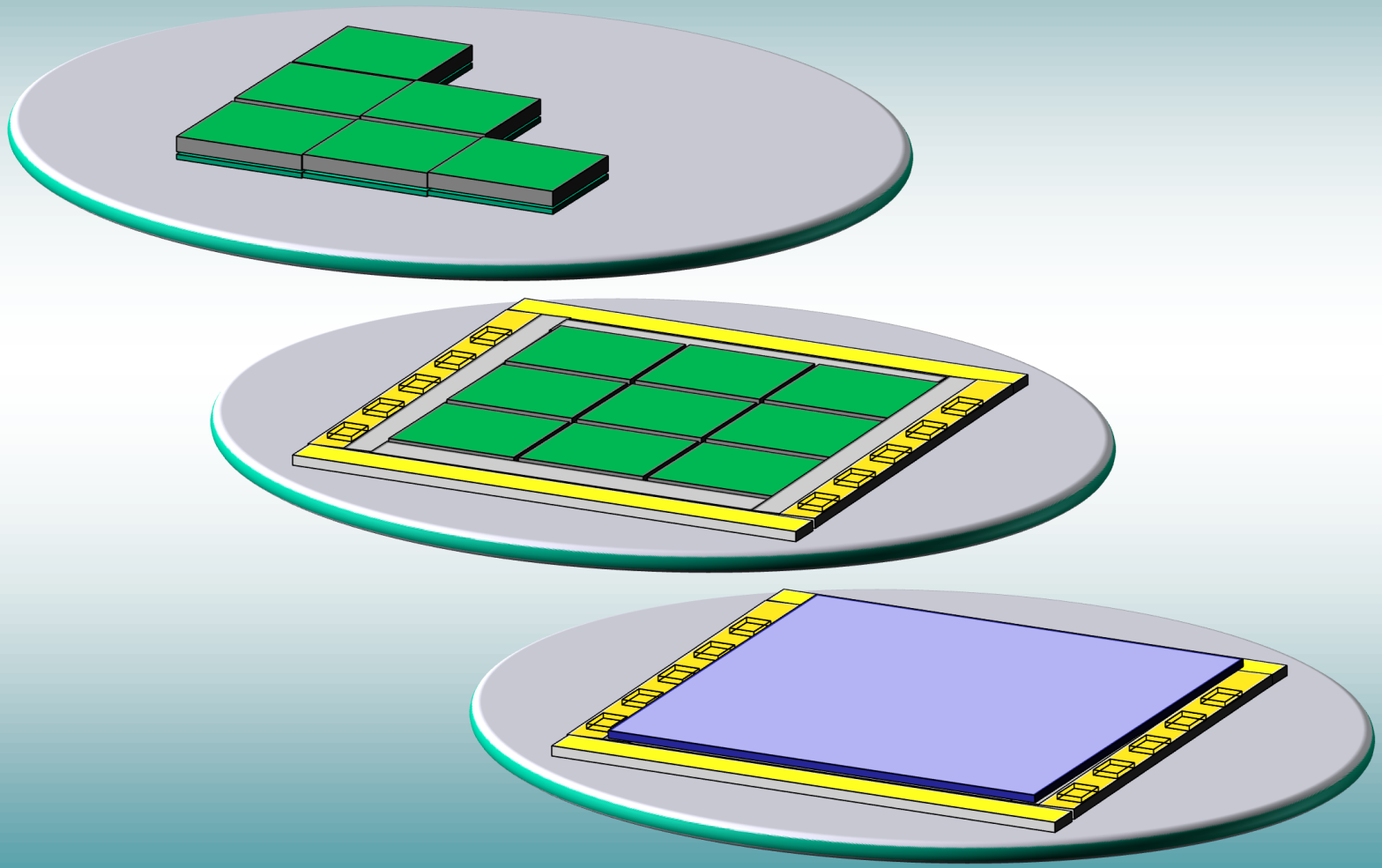
- SIP/SSIP
  - Power Conversion
  - Cooling
  - Photonics
- Optimization
  - Extending to power
- Mixed PCB/IC Metaphor



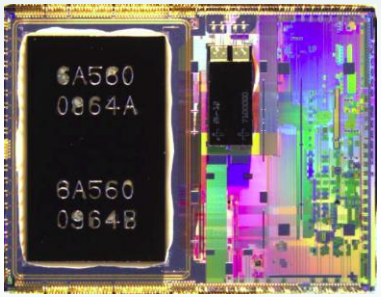


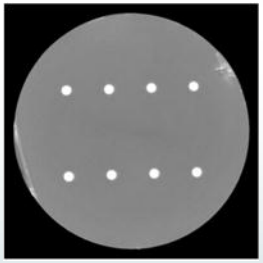


Wafer-scale FPA

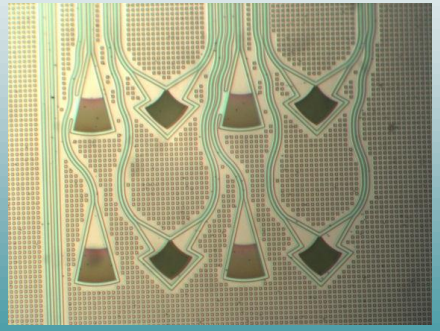


Luxtera 2.5D Photonic Data Pump

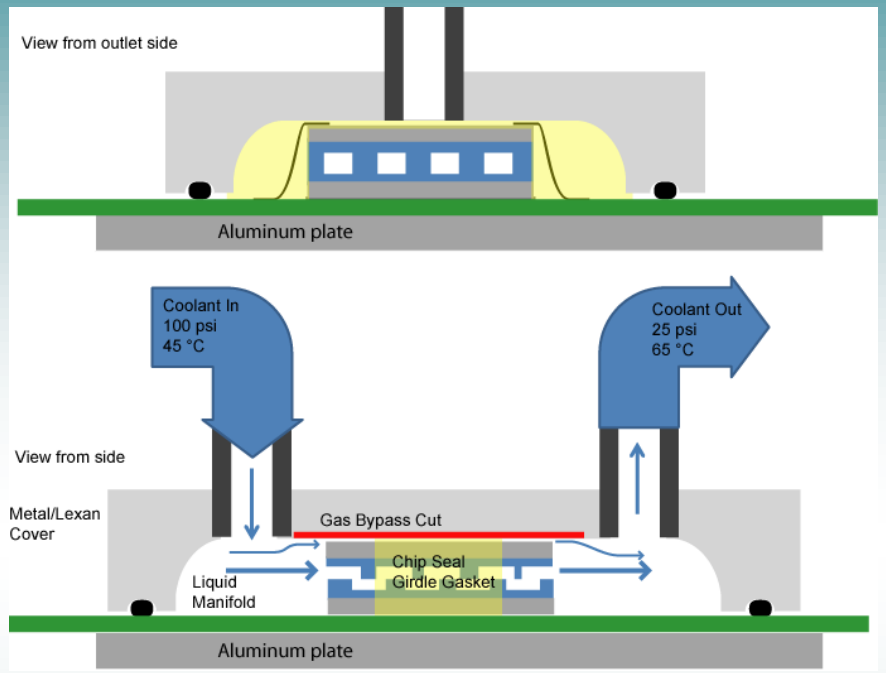


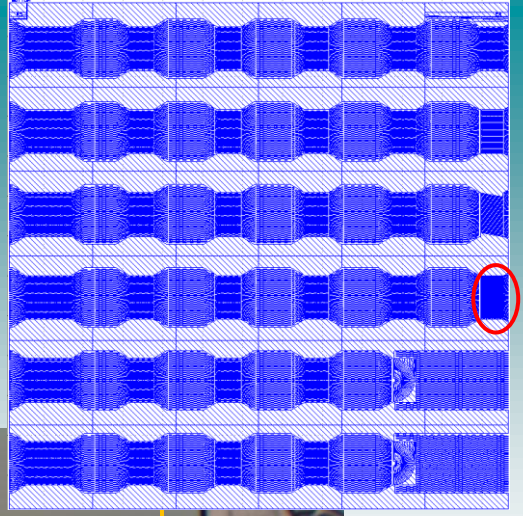


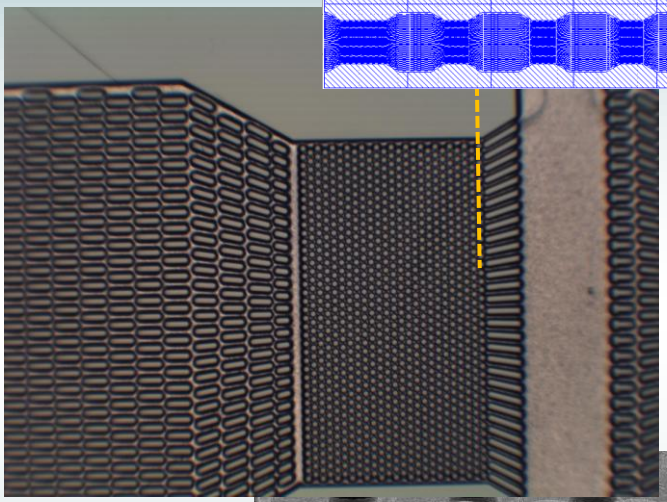
- 2.5pJ/bit power target
- Bare metal protocol
  - Ultra low latency
  - Protocol agnostic
- 8 core Fiber
- 28Gb SERDES or 2.5Gb low-swing interface
- Self-calibrating self-tuning
- >1.6Tb/s payload

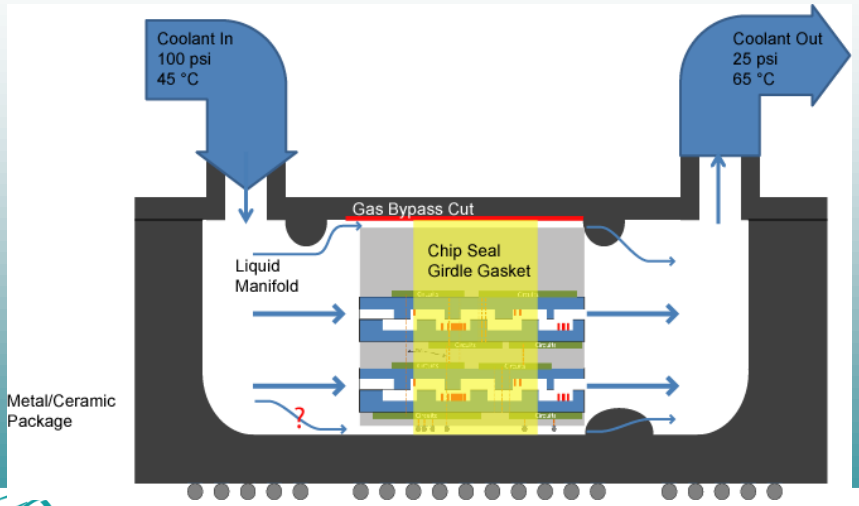


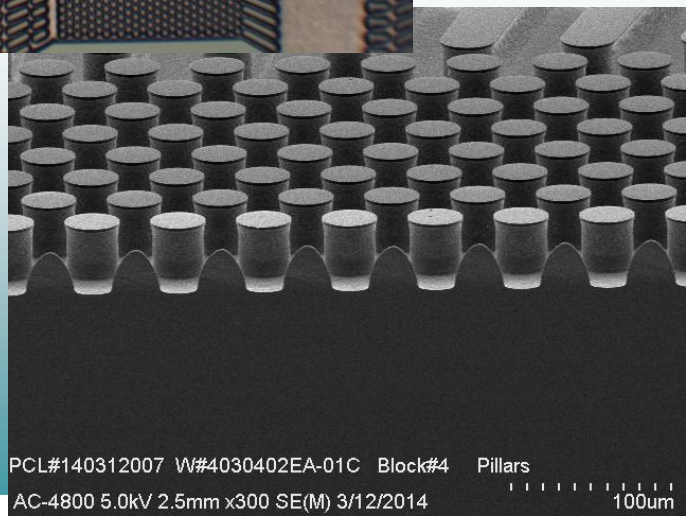
Cooling Block Illustrations











Tezzaron/Novati 3D Technologies

- "Volume" 2.5D and 3D Manufacturing
- Interposers
  - High K Caps
  - Photonics
  - Passives
  - Power transistors
- ReRAM
- Development of More than Moore Technologies
  - Microfluidics
  - Integrated sensors
  - Image enhancement technologies
- Cu-Cu, DBI®, Oxide, IM 3D assembly

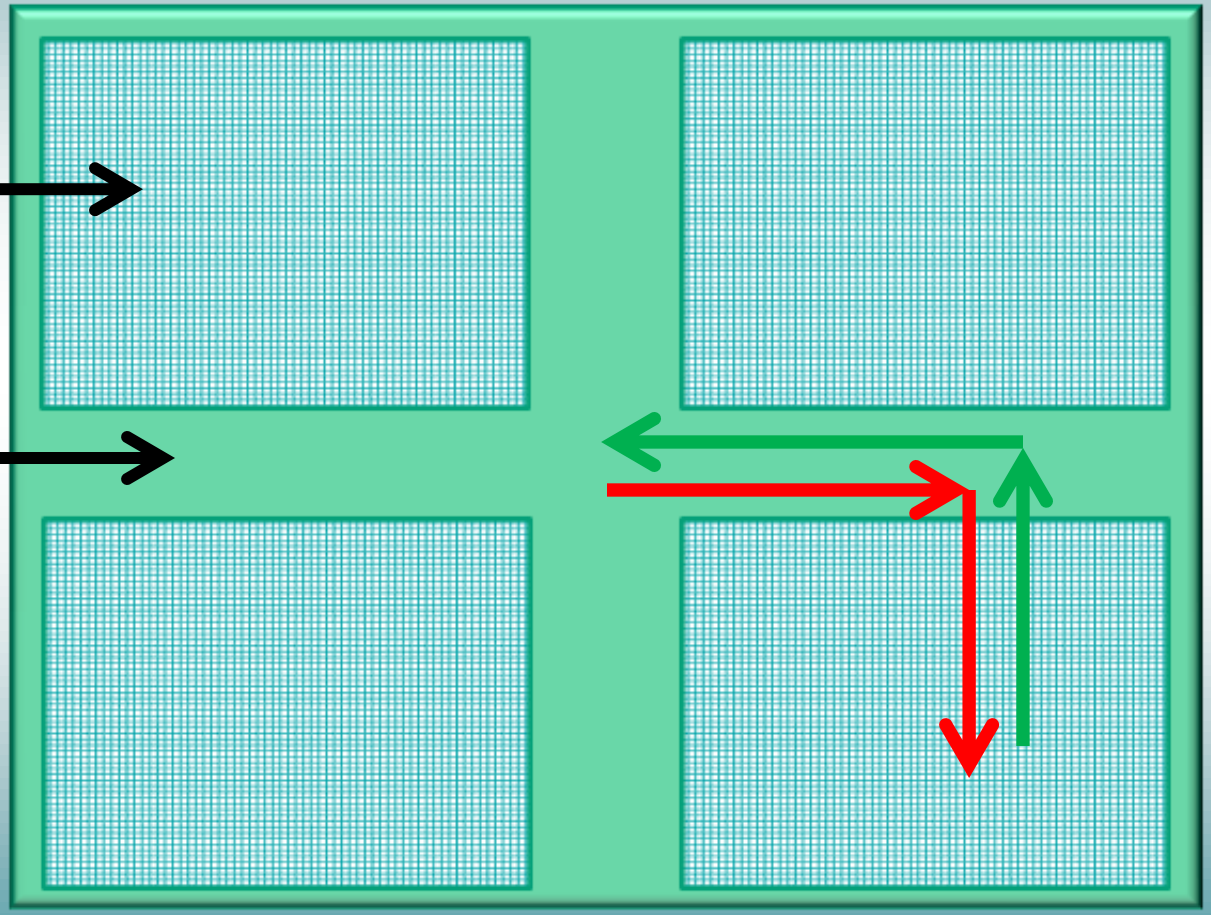
MEMORY AS AN EXAMPLE

Conventional RAM Architecture

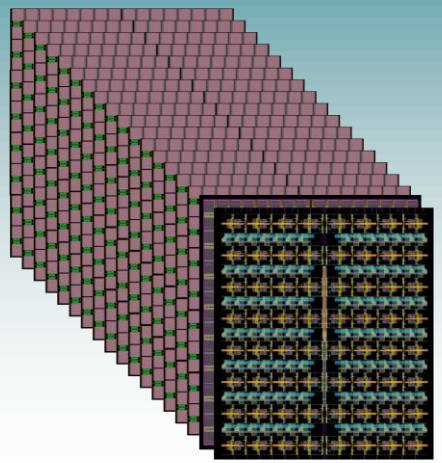
Memory Bits

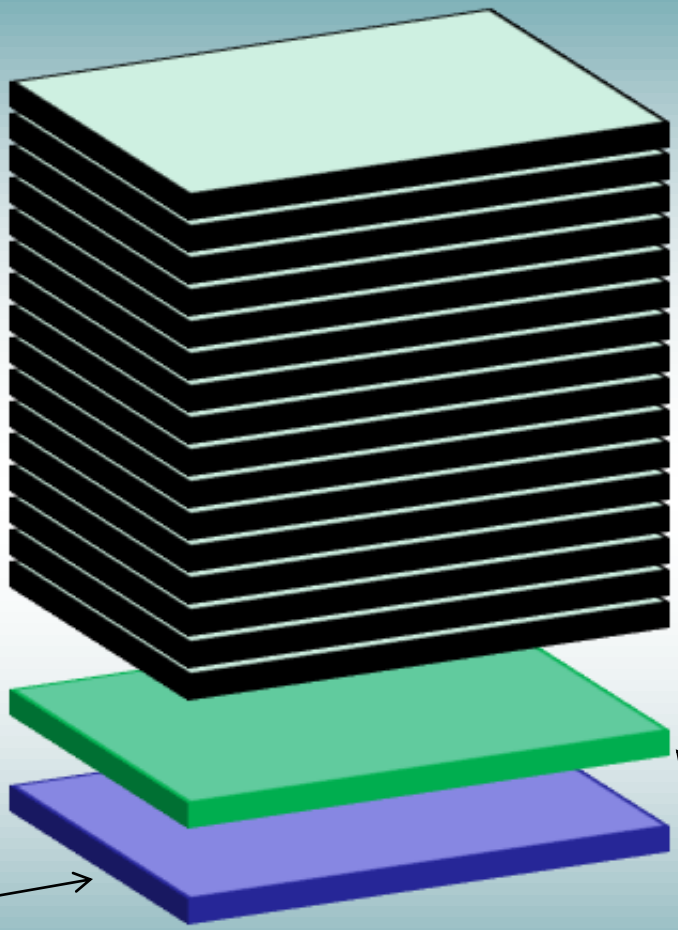
Periphery

- Decoders
- Amps
- Drivers
- etc.



Gen4 “Dis-Integrated” 3D Memory





DRAM layers
4xnm node

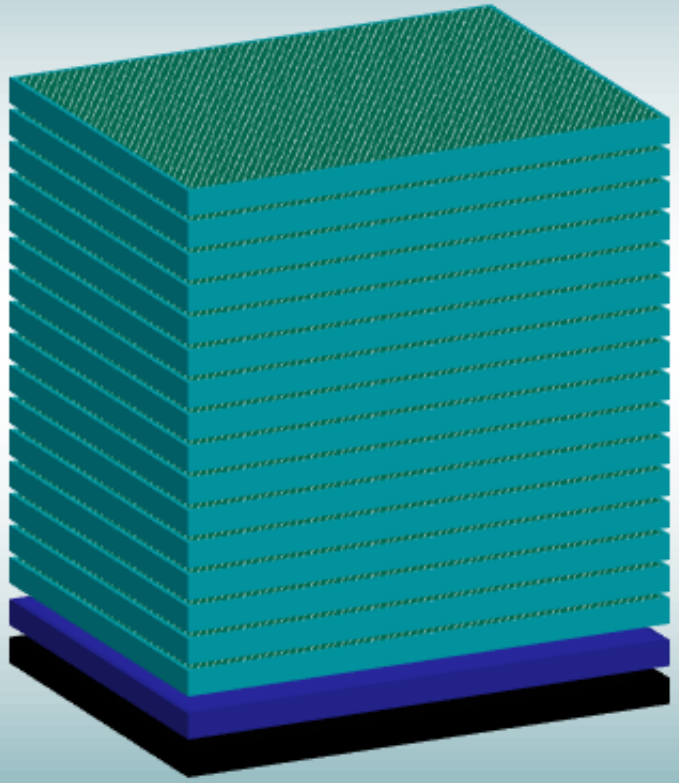
2 million vertical connections per lay per die

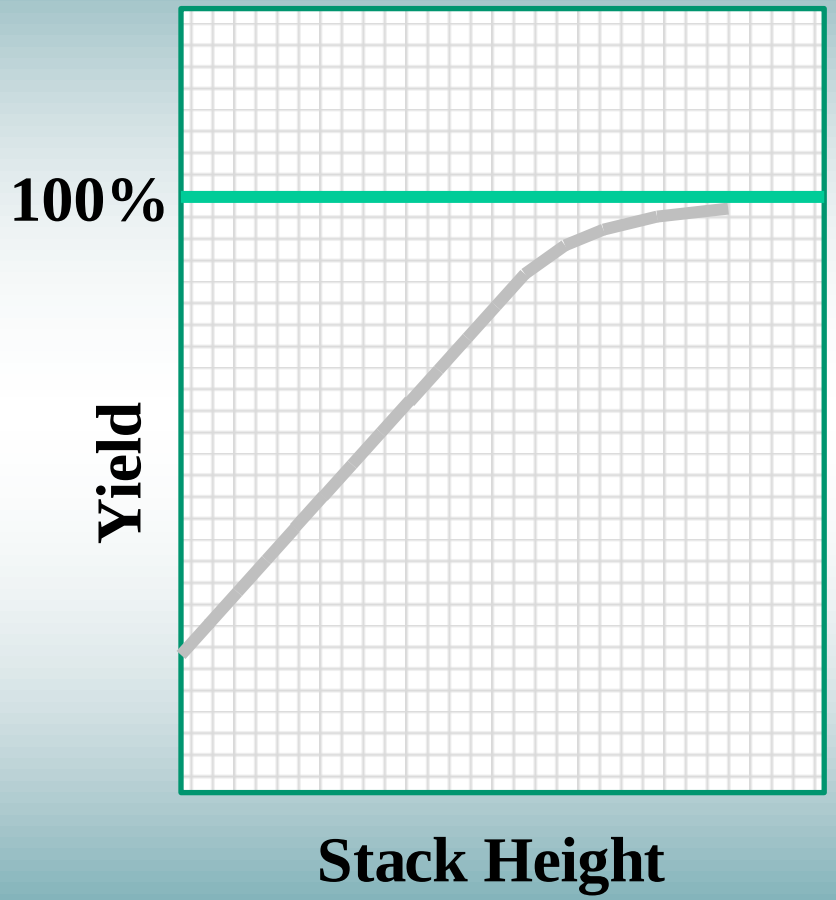
I/O layer contains: I/O, interface logic and R&R control CPU. 65nm node

Controller layer contains: sense amps, CAMs, row/column decodes and test engines. 40nm node

Better yielding than 2D equivalent!

Bi-STAR Repair Improves Yield





3D as Lego…

Photonic I/O

- Lowest Power
- Highest Performance

Pico-SerDes I/O

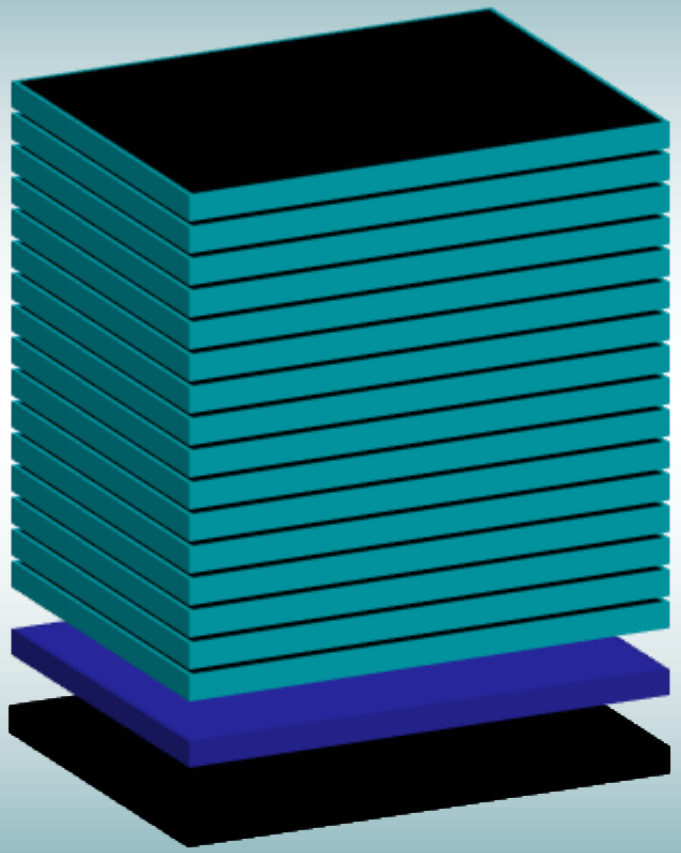
- Lower Power
- Moderate Performance

SerDes I/O

- Highest Power
- Moderate Performance

2.5D Si or Organic

- Low Power
- High Performance



What Does 3D Do for Memories?

- Stack many thin layers
  - 16x density
- Optimized processes and shorter wires
  - 75% reduction in latency
  - 40% lower power
- Memory layers are almost all memory
  - ~50% less silicon per bit
- On-board intelligence in a logic process
  - Higher yield
  - Higher reliability
- Easier to customize

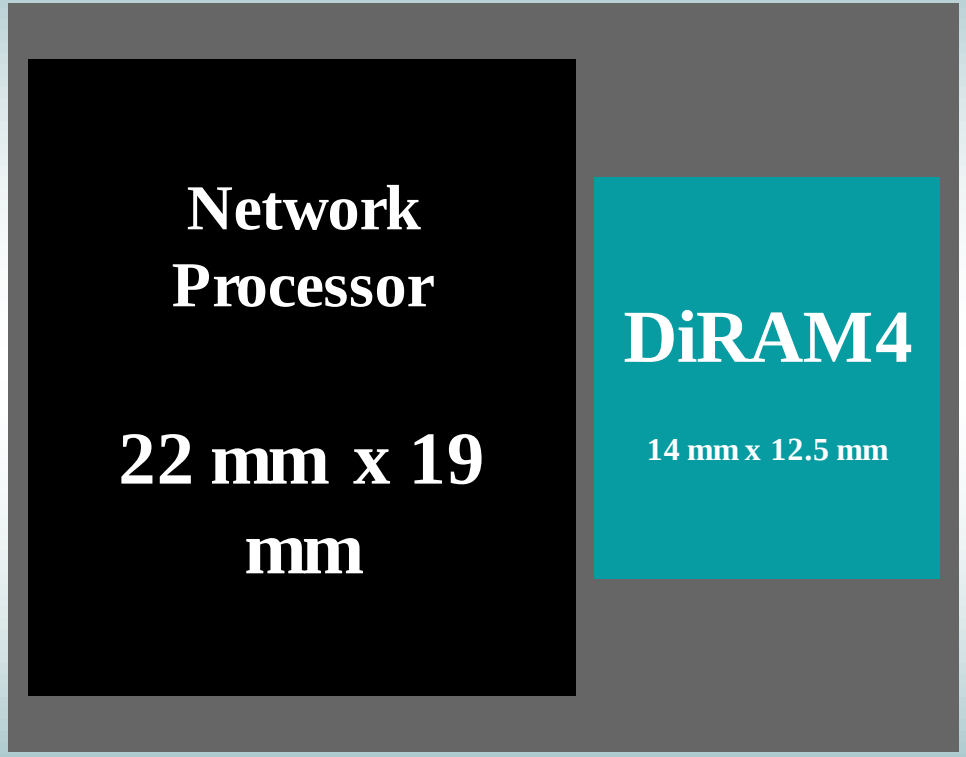
400Gb NP Standard RAM BOM

(30) 4 Gb DDR3 DRAMs = 1 Tb/s Packet Buffer

(12) 576 Mb RLDRAM3 DRAMs = 12 BT/s Tables

(4) 576 Mb SigmaQuad-IIIe SRAMs = 5 BT/s Stats

400Gb Routing with DiRAM4



- $^1/_6$ the size
- $^1/_3$ the power

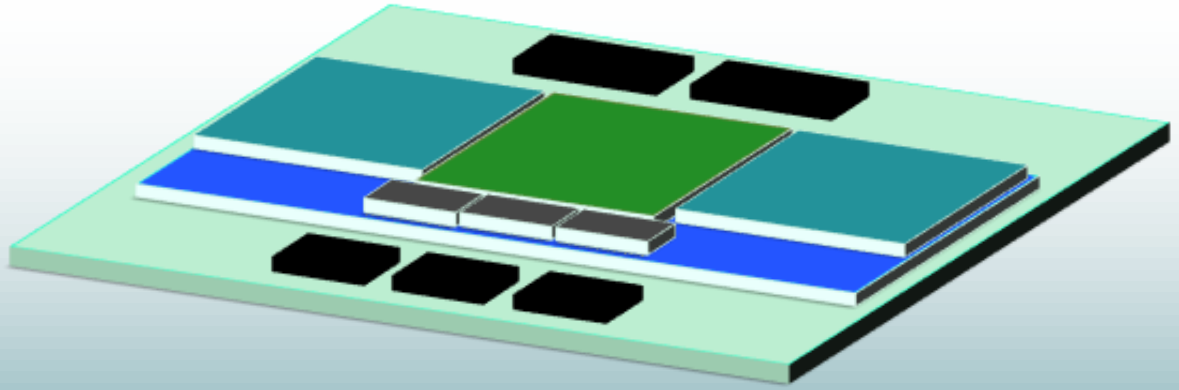
2.5D Assembly Flow

Si Interposer

Memory Hub

Memory Stack

SERDES

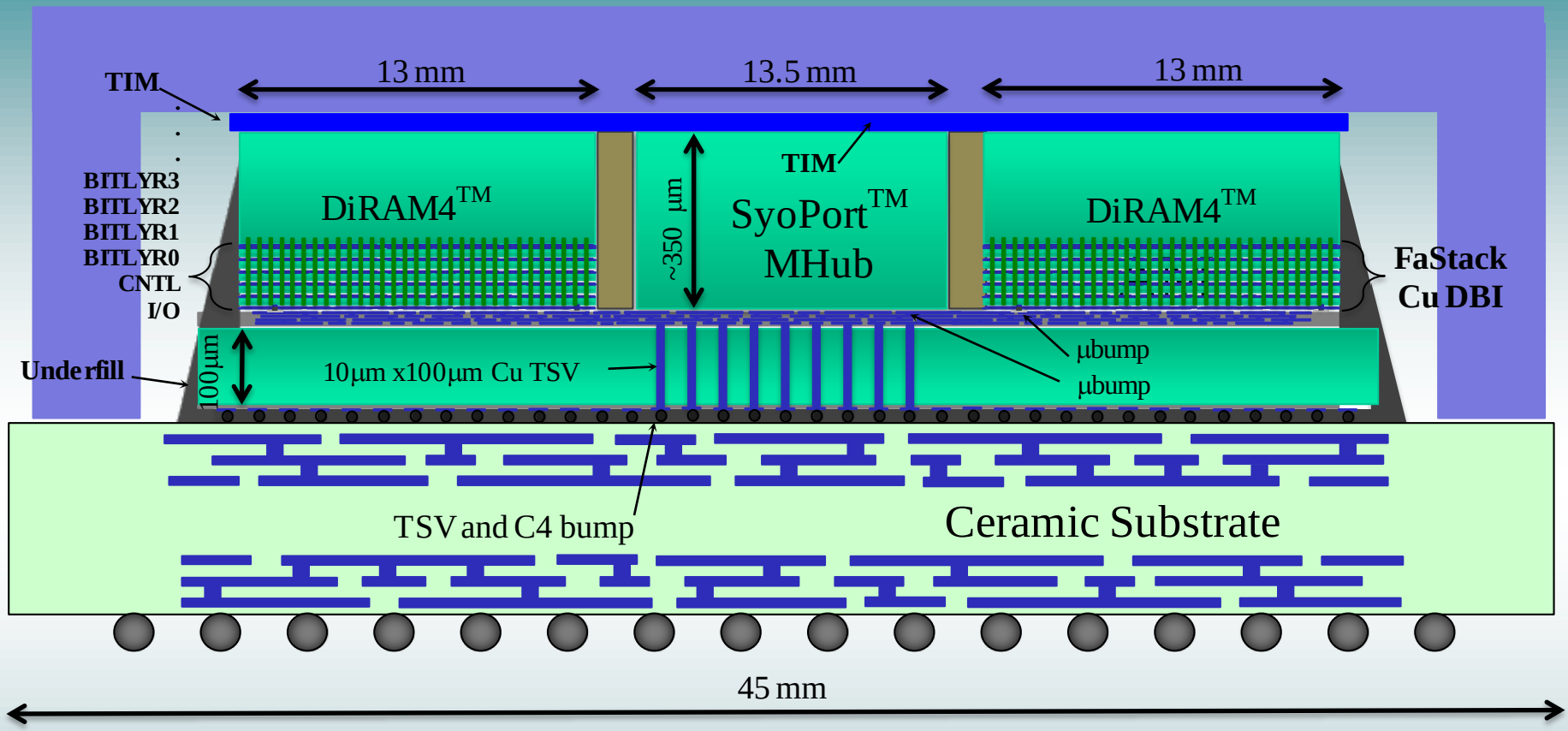


Power Supply 1

Power Supply 2

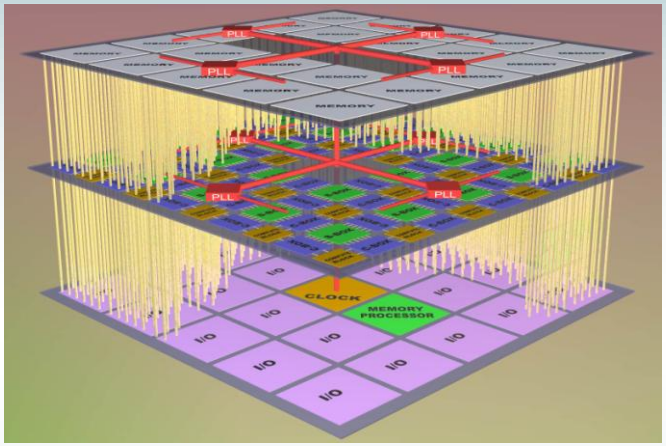
NAND Memory

Memory Block Package



Summary

- Moore's Law is about economics
  - The end is not an if but a when
- The realms of integrated circuits and packaging are overlapping and unifying
- 3D and 2.5D will be pervasive
  - Heterogeneous integration is key benefit
- Numerous opportunities
  - It's all about design!



Sensors

Computing

MEMS

Communications