

Laser Driver Development at SMU, Status and Plan

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For the SMU Group

Outline

1. Single channel VCSEL driver LOCI1
2. Dual channel VCSEL driver LOCI2
3. Open drain 4-channel array VCSEL driver
LOCI4
4. Future plan

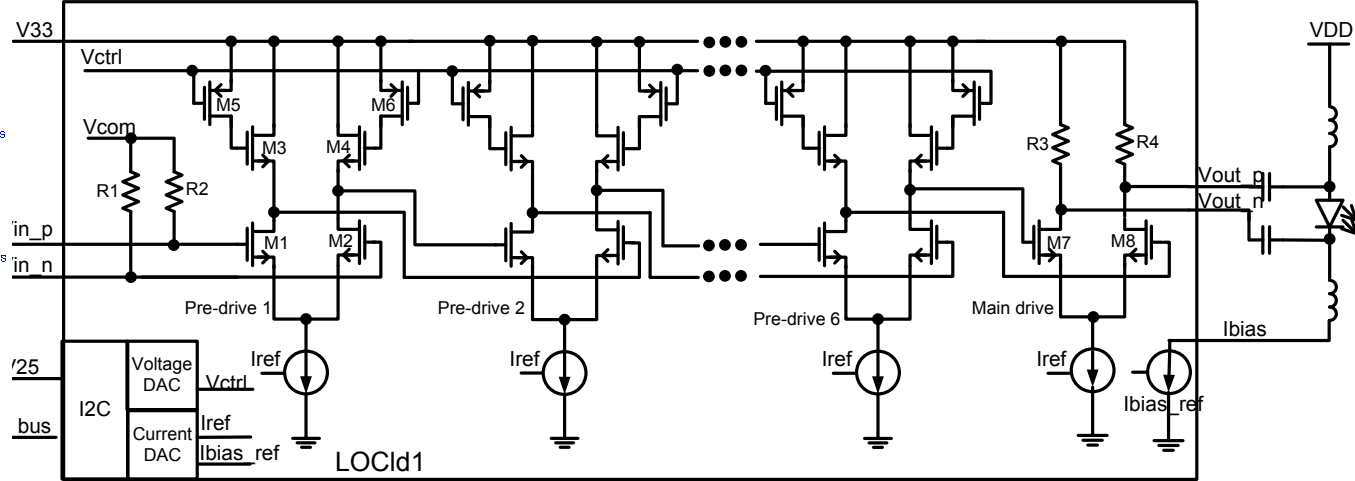
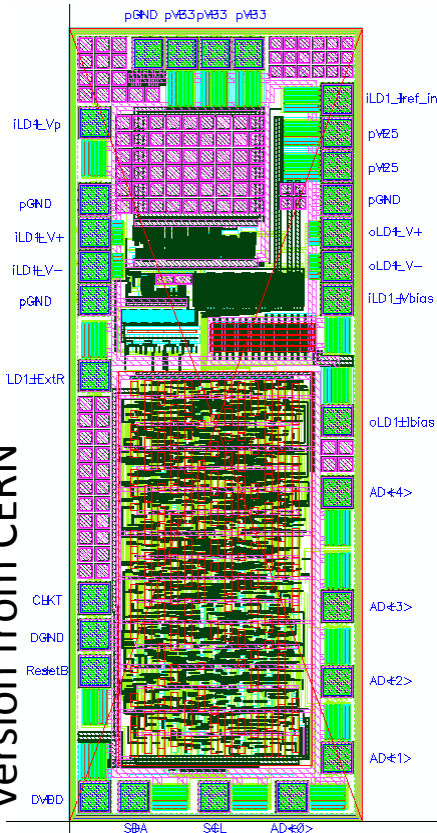
LOC ASICs

1. LOC, Link-on-Chip, was an idea for the optical link ASICs for ATLAS LAr upgrade. This idea is no longer pursued but the name is still used.
2. LOC ASICs are based on a commercial Silicon-on-Sapphire 0.25 μm CMOS process that has been evaluated for operations in the environment where the LAr front-end electronics crates are.
3. LOC ASICs consist of a serializer, VCSEL drivers and an interface circuit LOCic (framing, scrambling data) between the serializer and the ADC.
4. LOCI1 is a single channel VCSEL driver in the LOC ASIC family.

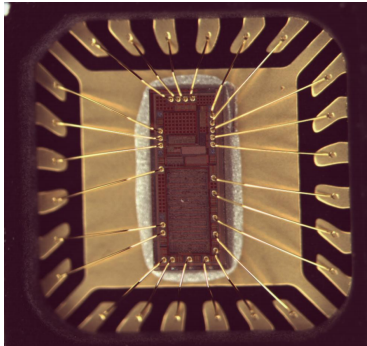
LOClD1

Driving stages

I²C, a modified version from CERN

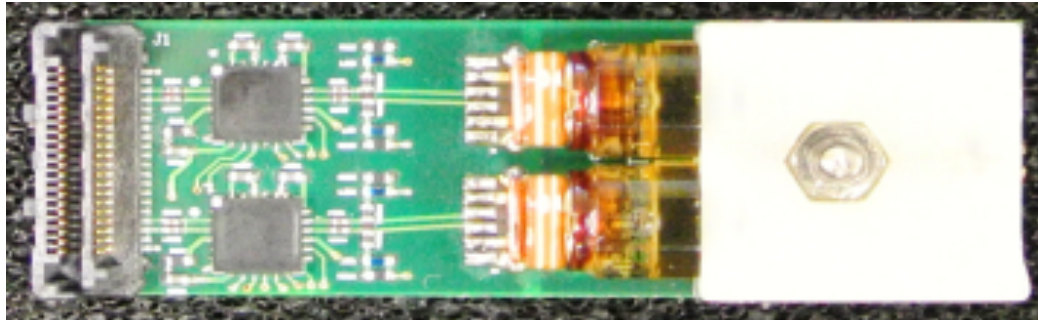


- Single channel VCSEL driver with active shunt peaking. Design speed 8 Gbps.
- I²C slave (from a modified CERN code) and DAC module for remote configuration.
- Programmable: VCSEL bias and modulation currents; peaking strength.
- VCSEL bias and modulation currents refer to a constant current source, not sensitive to transistor threshold voltage change caused by radiation.

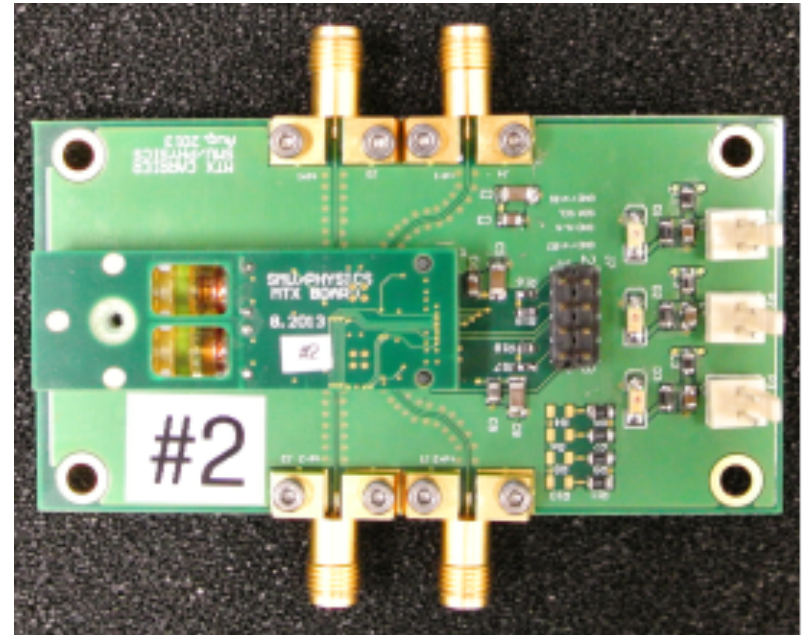


QFN-24 package, 5 x 5 mm²

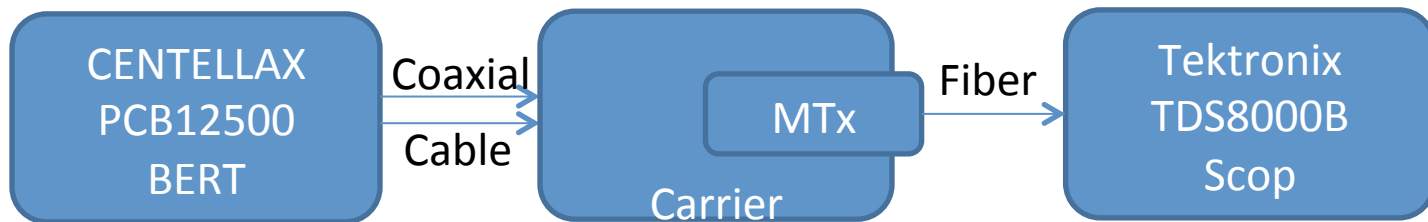
LOCId1 Test



MTx with LOCId1 and Truelight
10G VESEL TTF-1F59-427,
component side view



Carrier board with MTx, top view



Test setup

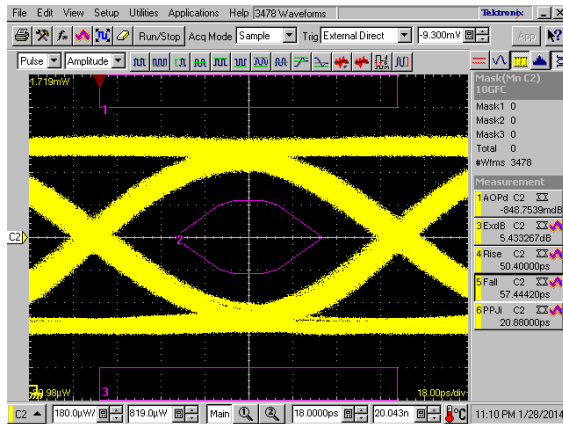
LOCI1 Test Results

Input : **8Gbps** PRBS7, 200mVp-p

Vpk = 2.25 V, I_{mod} = 6.4 mA, I_{bias} = 6 mA

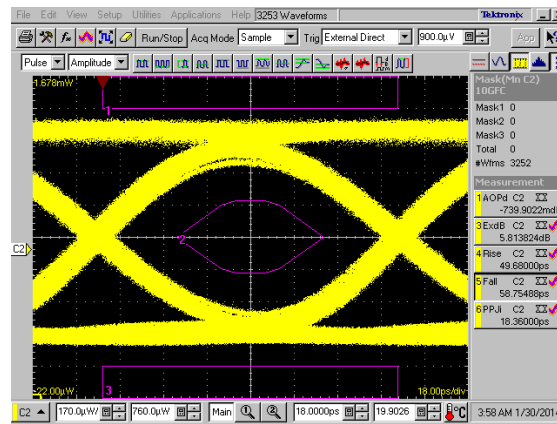
Power ~ 270 mW per channel (driver + VCSEL)

Board #1 ↓



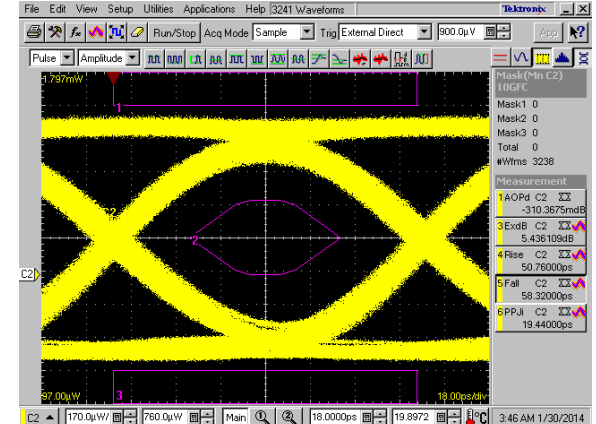
Channel #1

Board #2 ↓

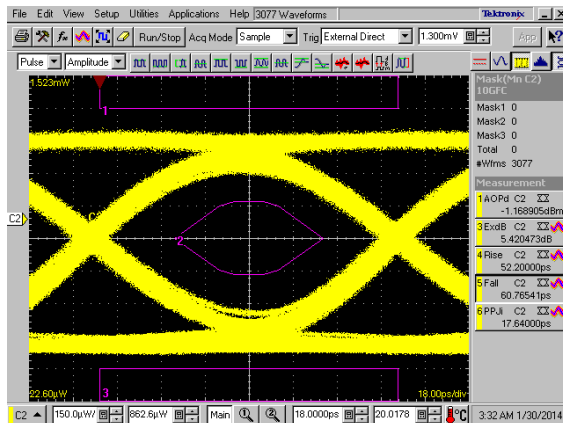


Channel #1

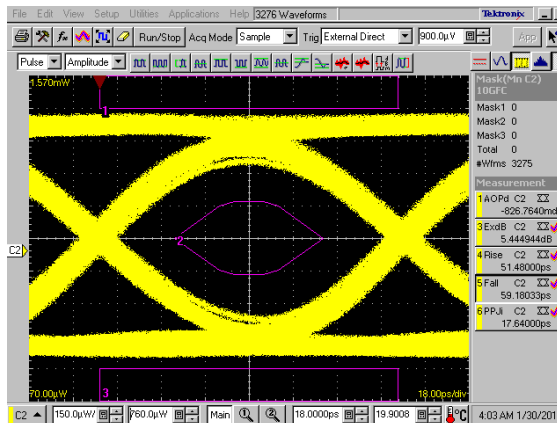
Board #3 ↓



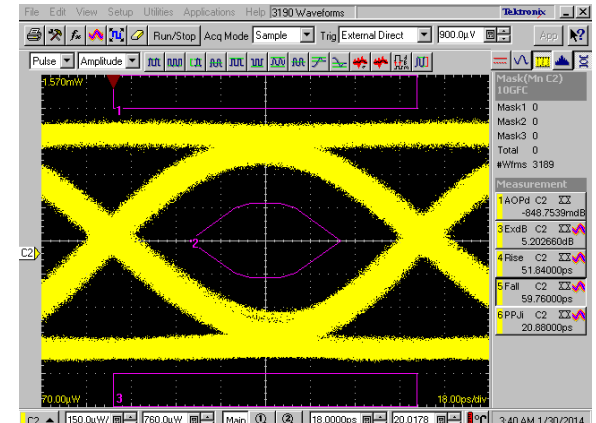
Channel #1



Channel #2



Channel #2



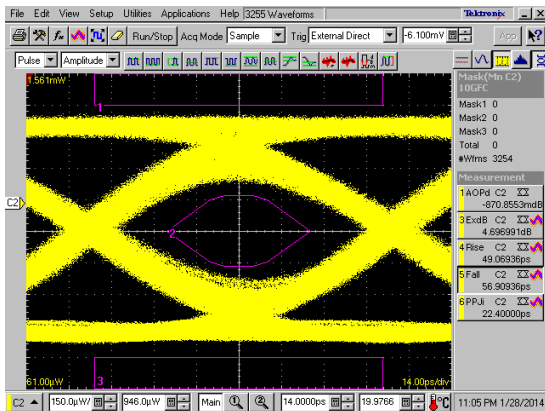
Channel #2

LOCId1 Test Results

Input : **10Gbps** PRBS7, 200mVp-p

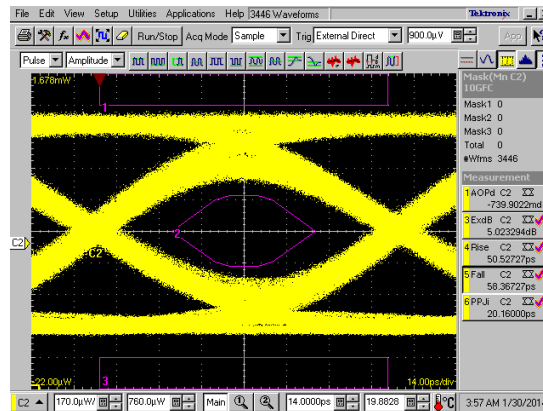
Vpk = 2.25 V, I_{mod} = 6.4 mA, I_{bias} = 6 mA

Board #1 ↓



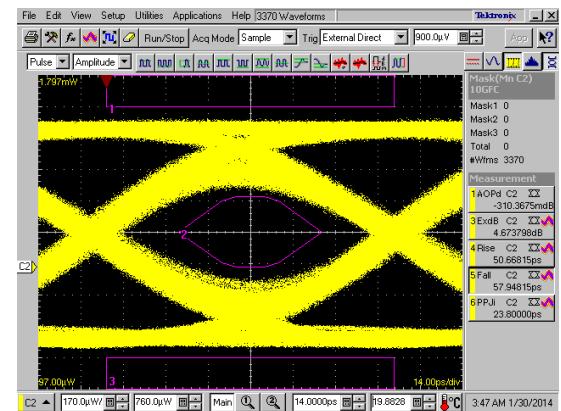
Channel #1

Board #2 ↓

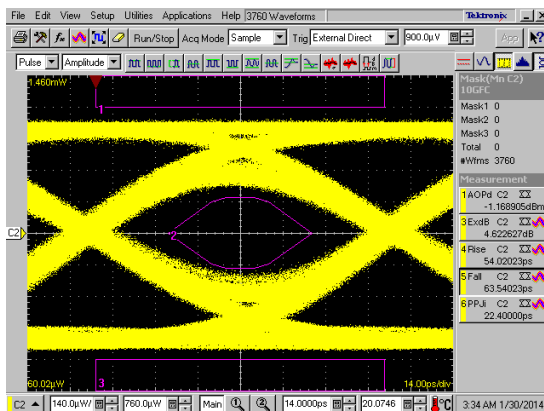


Channel #1

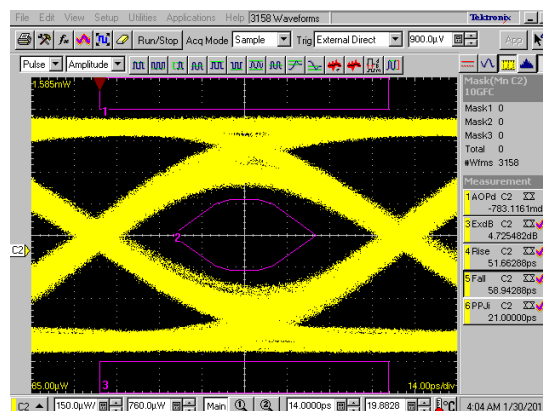
Board #3 ↓



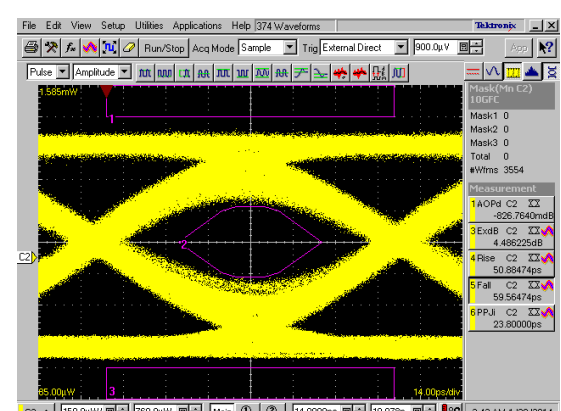
Channel #1



Channel #2



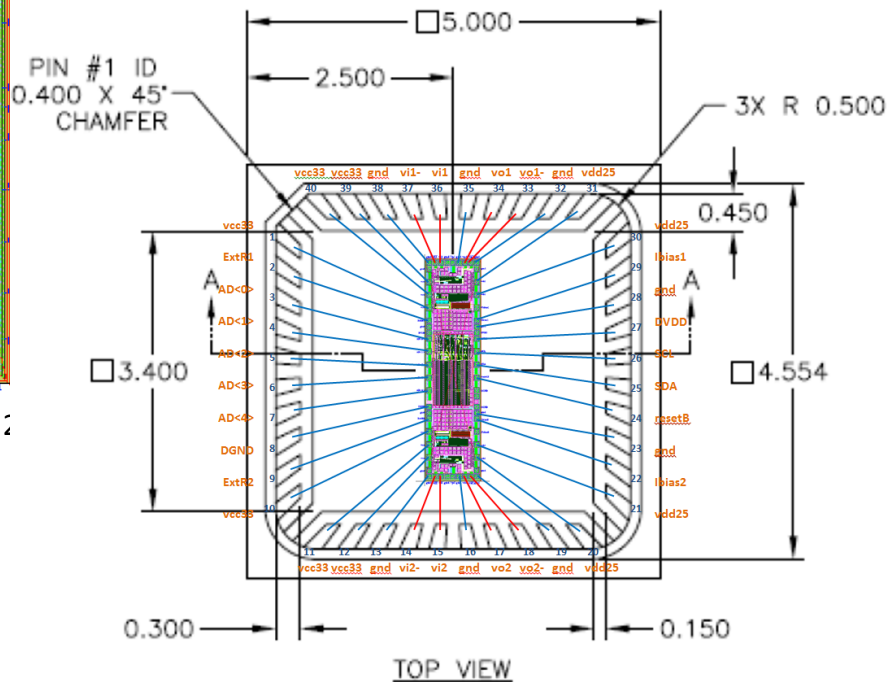
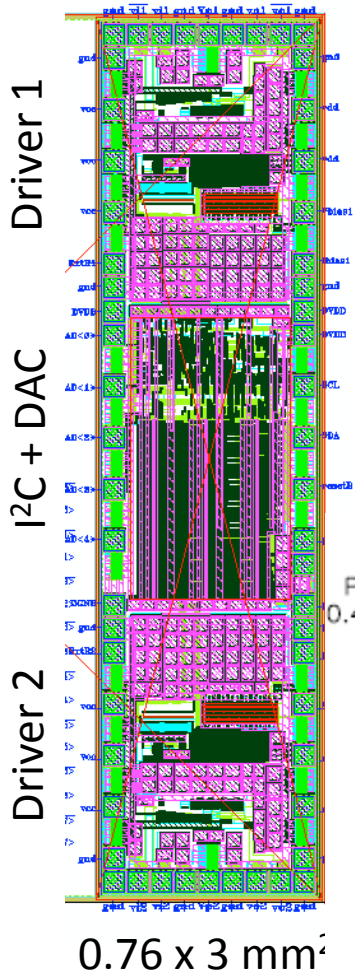
Channel #2



Channel #2

LOCI2

A “copy&paste” of LOCI1 to build a two channel VCSEL driver sharing the I²C part (improved layout). Especially designed for MTx to match with LOCs2 (the two channel serializer).

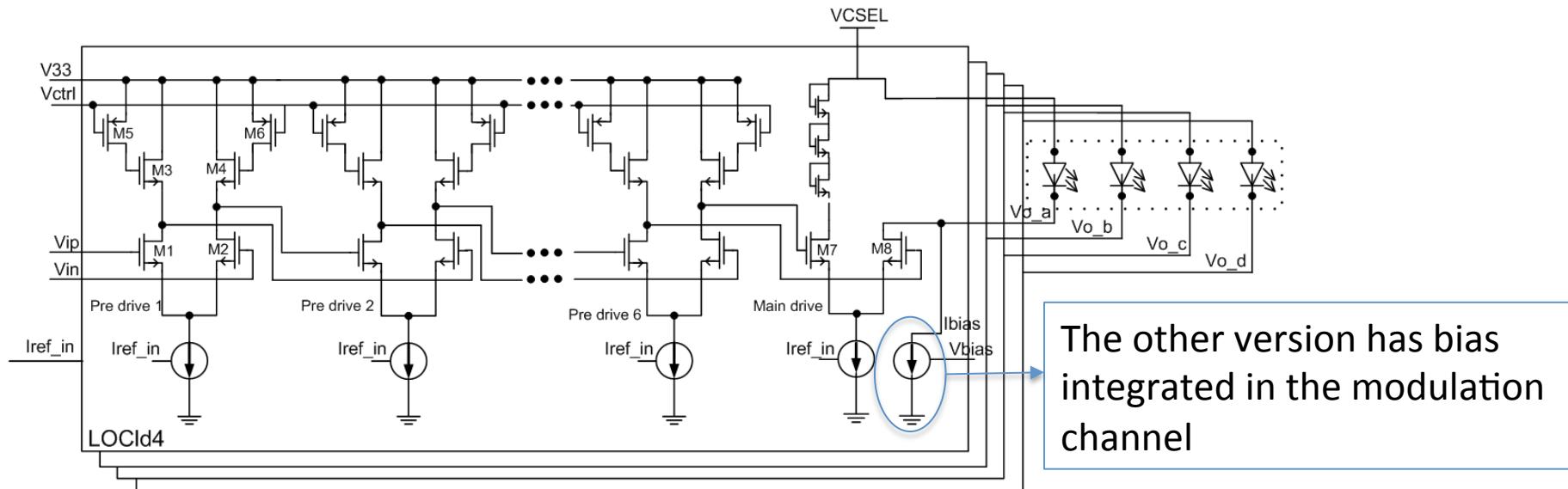


Dec. 2013 submission. Chips to be tested in April – May. Production will be in 2015 – 2016 time frame. We will decide if we still need to produce LOCI1.

QFN-40 with short wire for fast signals

LOCId4 Design

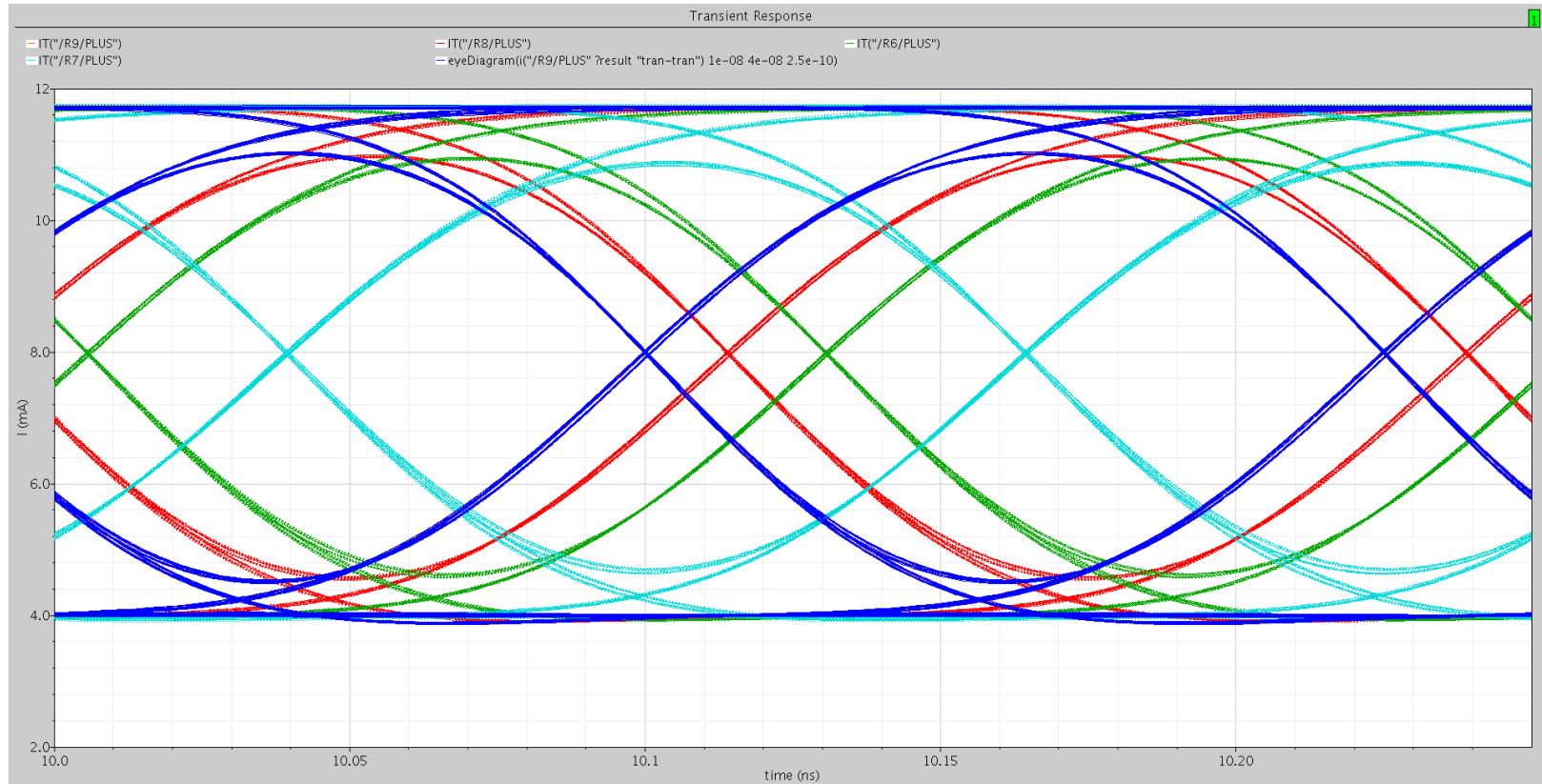
Design based on an earlier attempt on an open drain 4-channel array VCSEL driver. This is not a “copy&paste” of LOCId1. Two versions with different biasing scheme. No I²C yet. Controls are “local” for the moment.



- Six driving stages with active shunt peaking circuits. They do not share power with the last stage, which has individual power connection for each channel.
- Last driving stage: open-drain, left branch is designed to match with the right (output) branch, bonding wire and a simple VCSEL model included in the design.

LOCId4 Post Layout Simulation

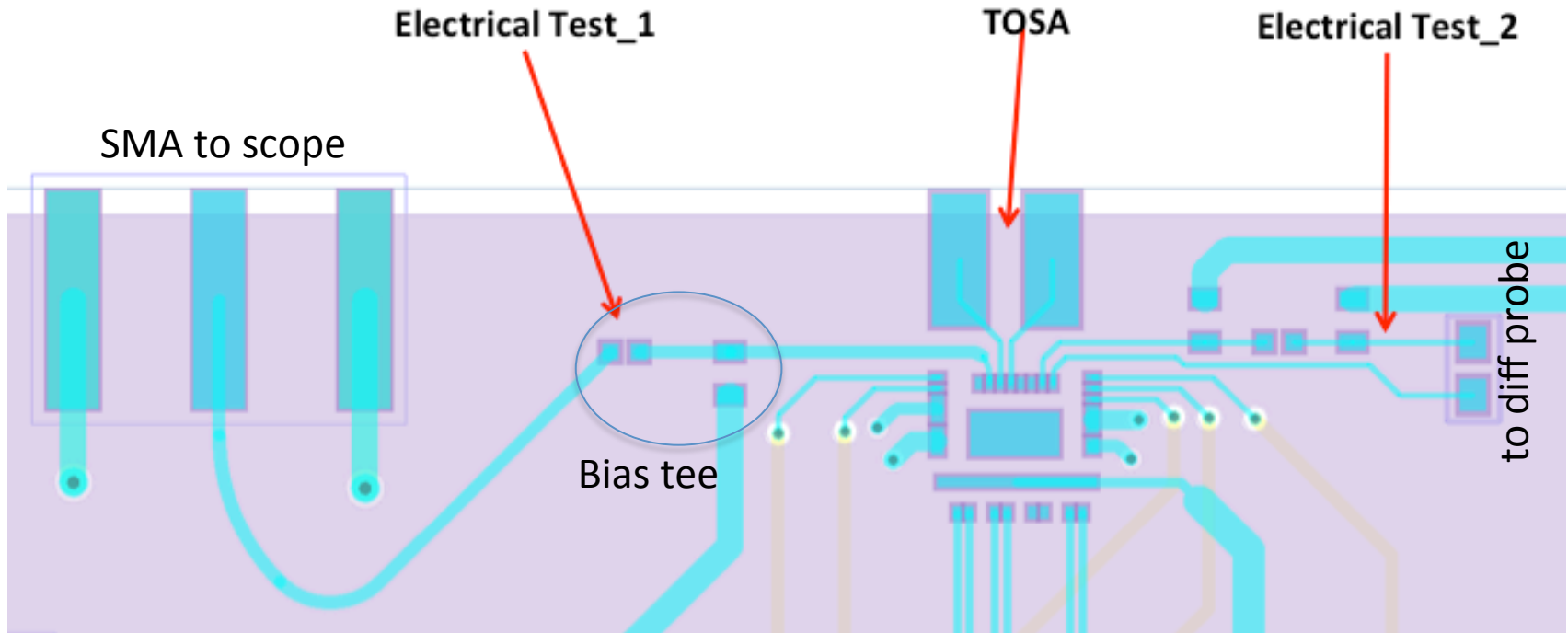
Input: PRBS: 10 Gbps & 10 ps rise time, differential $V_{p-p} = 200$ mV;
Set peaking = 1.9 V; $V_{vcSEL} = 3.8$ V; $I_{ref} = 1.3$ mA; Nominal at 27 C.
Bonding wires and a simple VCSEL model included. Total power
(including the four VCSELs) is estimated to be 425 mW.



LOCI4 Test Plan

Trying to avoid the difficulty in light coupling, here're the steps we plan to take in the test in April – May.

1. Electrical test_1 with a “bias tee” structure.
2. Electrical test_2 using differential probe.
3. Single channel optical test using TOSA.



Future Plan

1. LOCI1 and/or LOCI2 will go into production in 2015 – 2016 time frame as QFN chips. They are ATLAS LAr phase-I deliverables. We are working on a QA stand to screen each chip. We are interested in collaboration on the QA, including a life test stand.
2. If these drivers are of interest to the community, we would like to know the quantity of chips needed so that more wafers can be produced in the engineering run.
3. LOCI4 needs more R&D in 2014 – 2015. Will collaborate in VL+ to design for the VCSEL array chosen in VL+.
4. Once successful, there maybe a LOCI12 version for the CDRD project with FNAL. We need a 12-lane VCSEL driver that matches with the VCSEL array we have.
5. Array drivers may go into production for a small quantity if they are ready before the engineering run of the other LOC ASICs. Otherwise they will remain as R&D objects with MWP quantities.