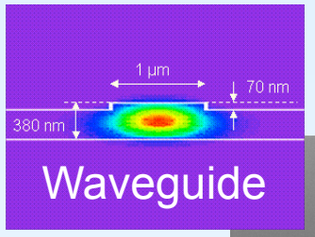
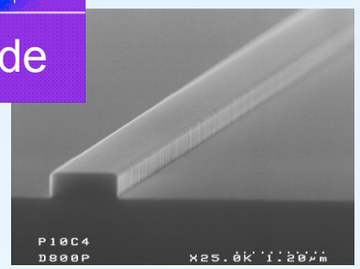
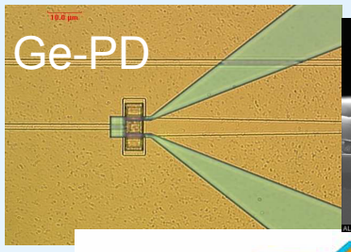
Silicon Photonics

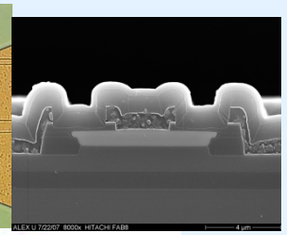
- Use of silicon substrate and ASIC production techniques to pattern waveguide and optical field manipulating structures
  - Allows the fabrication of optical modulators and high level of integration of optical circuits like couplers and gratings
- Promise of lower power & cost modulation of light
  - But still need a source of optical power (that could be located remotely)
- Sparked major interest in the optical communications industry
  - For chip-to-chip interconnects up to telecom long-haul applications
  - Heavy weights like IBM, Intel, as well as smaller specialist companies like Luxtera (Molex), Kotura (Mellanox) are very active in the field

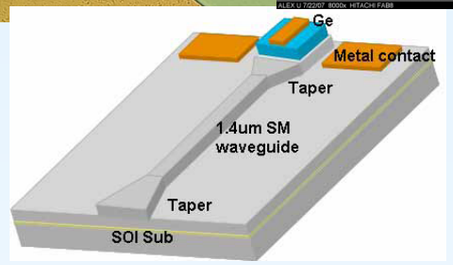
Silicon Photonics II

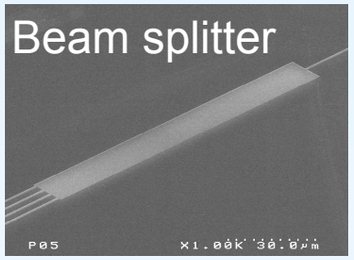


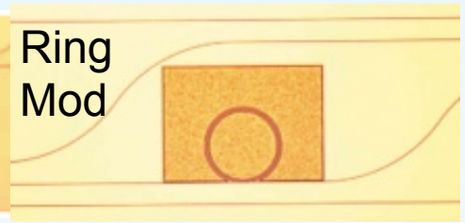


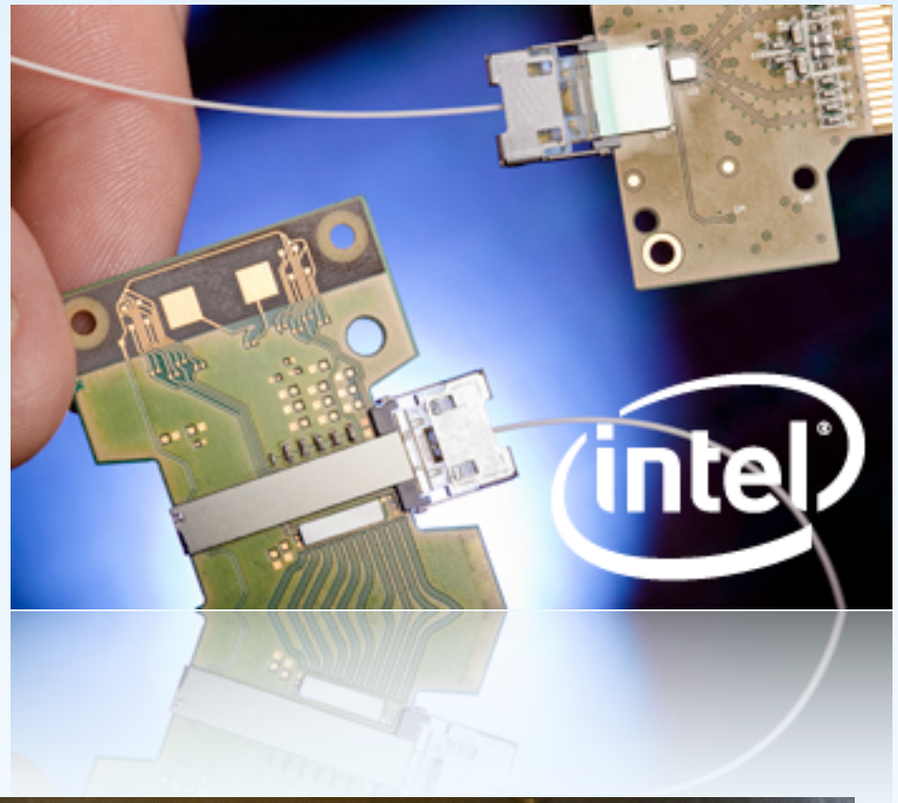


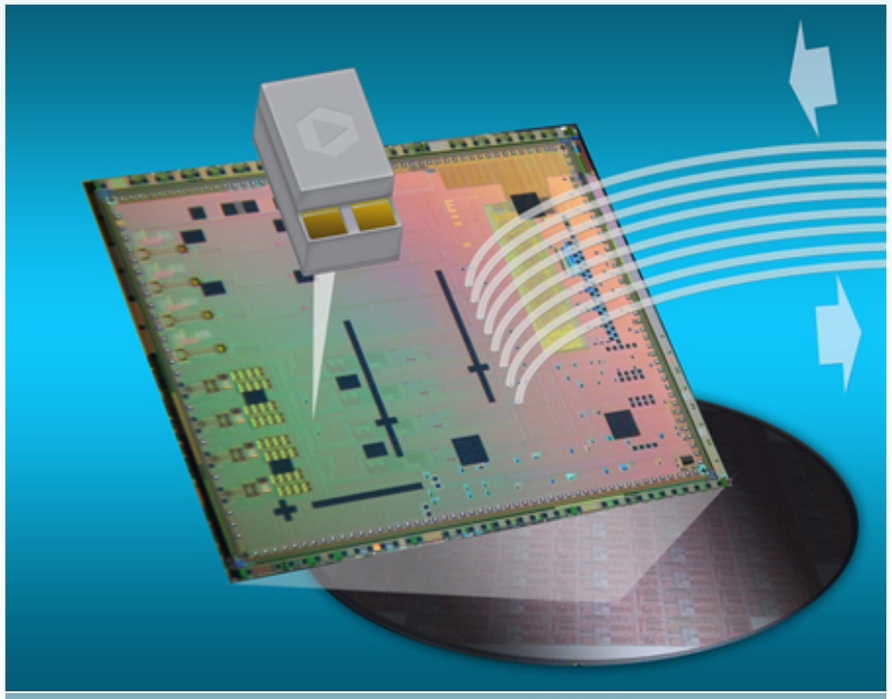


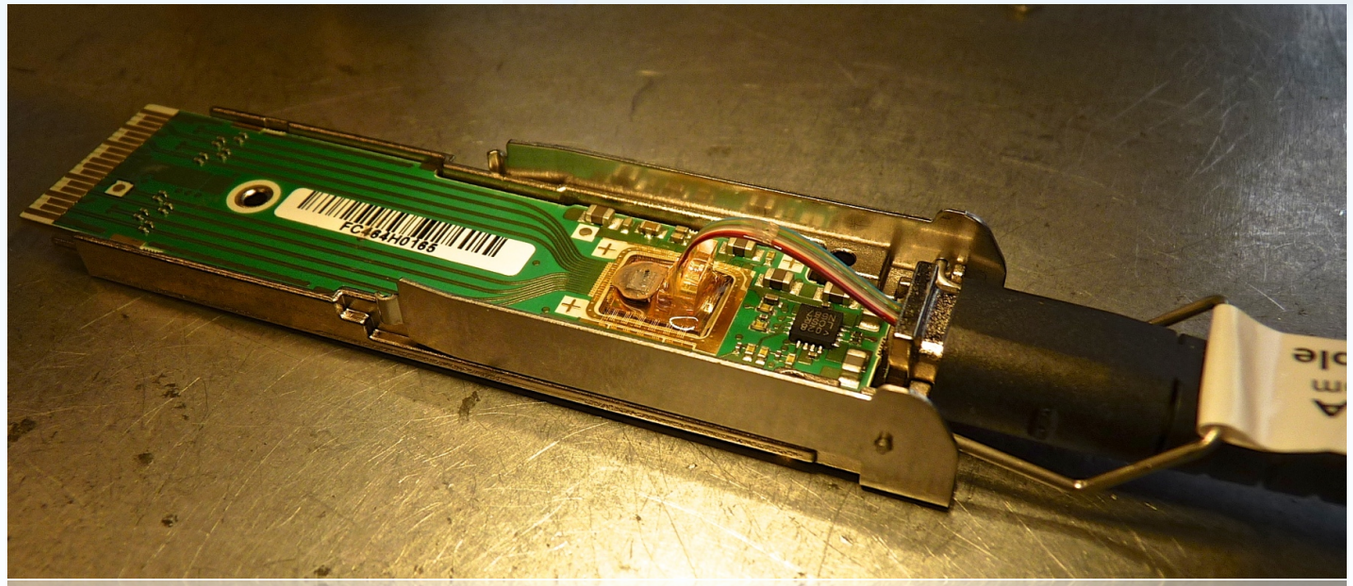












LUXTERA
ILLUMINATING THE PATH TO TERABIT IC CONNECTIVITY

Silicon photonics for HEP?

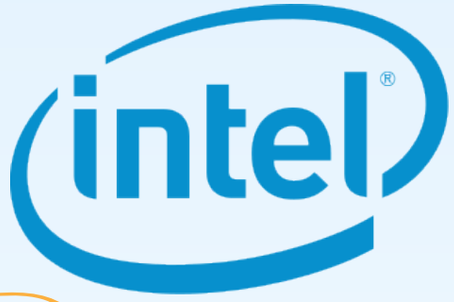
- Basic questions come up again
  - e.g. Radiation resistance
- Have been working on assessing some basic aspects of the technology
  - Using devices obtained from Industrial partner and Academic partner
    - Sarah will present some irradiation results later today
  - Also keen to assess how easy it is to design own structures
    - Using MPW services similar to what we're used to for ASICs
- EU funded fellow appointed for a three-year study of basic technology
  - Joint CERN-Intel programme
  - Assess feasibility of use of Silicon photonics technology in HEP

ICE-DIP overview

- Intel-CERN European Doctorate Industrial Program
  - European Industrial Doctorate scheme hosted by CERN and Intel Labs Europe.
- ICE-DIP offers research training to 5 Early Stage Researchers (ESRs) in advanced Information and Communication Technologies (ICT).
- The technical goal of this program is to research and develop unparalleled capabilities in the domain of high throughput, low latency, online data acquisition.
  - Many-core processors for data acquisition
  - Future optical interconnect technologies
  - Reconfigurable Logic
  - Data Acquisition Networks.

ICE-DIP overview (2)

- Partners:



NUI MAYNOOTH
Ollscoil na hÉireann Má Nuad

- Start Date: 1 February 2013
- Duration: 48 Months
  - ESR contracts are for 36 months each
- EU Funding: 1.25 M€
  - For people (training,travel), not equipment

ICE-DIP work packages

1. Use of silicon photonics technology in data transfer systems

2. A data pre-processing system closely integrating both microprocessors and reconfigurable logic (FPGA)

3. High speed networking for data acquisition systems

4. Optimizing the latency and energy characteristics of data transfer in computing platforms and accelerators

5. Enabling efficient data processing on accelerators – optimization, parallelization, vectorization

ICE-DIP WP1: Silicon Photonics

- Investigation of applicability of silicon photonics technology in data transfer systems for future generations of high-energy particle physics detector systems
  - Systems aspects, Radiation hardness investigation
- Partners are DCU and Intel Labs Santa Clara
- Foreseen to spend a large fraction of the 36 months away from CERN
  - DCU: 4 months
  - Intel Labs Santa Clara: 16 months
- Major practical goal is the design of a silicon photonics circuit to be tested in a radiation environment

Plans for 2014

- Pigtailing
  - Further trials for vertical- and butt-coupling
  - At least two device families
  - At least two packaging institutes
- Radiation hardness evaluation
  - X-rays (CERN, April/May), Neutrons (UCLouvain, June/July)
  - At least two device families
  - Device-level simulation of damage
- Modulator design, fabrication, and characterization
  - Fellow Secondment at Intel Labs, Santa Clara starting ~June
  - Target submission to ePIXfab in November
    - Test chip containing basic structures and a modulator
  - Lab equipment to be acquired to enable chip-level characterization
    - High-speed probing, fibre alignment