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CMOS MAPS with pixel level sparsification and time stamping capabilities for applications at the ILC

This paper is intended to discuss the features of a novel kind of monolithic active pixel sensors (MAPS) in deep submicron CMOS technology (130 nm minimum feature size) for use in charged particle trackers and vertex detectors. As compared to conventional MAPS with 3-transistor readout scheme, the design approach proposed here, where a deep N-well (DNW) is used as the collecting electrode, lends itself to pixel-level sparsified processing and is expected to provide the ability to manage the large data flow of information anticipated for future, high luminosity colliders. Lately, the applicability of the DNW-MAPS concept to the design of the vertex detector for future high luminosity colliders, like the International Linear Collider, has been investigated. This paper will discuss the design and performances of a recently submitted DNW monolithic sensor, the SDR0 (Sparsified Digital Readout) chip, including different test structures, where both analog (charge amplification and threshold discrimination) and digital (sparsification, time stamping) functions have been integrated inside the elementary sensor, as large as 25 μm× 25 μm. Also results from physical device simulations, aiming at evaluating the properties of the DNW sensor in terms of charge collection efficiency and cluster size, will be presented.

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