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Development of a triple well CMOS MAPS device with in-pixel signal processing and sparsified readout capabilities

The SLIM5 collaboration has already designed fabricated and tested two prototypes of CMOS MAPS sensors. The new key feature of these devices with respect to previously developed MAPS sensors is to include at the pixel level a full signal processing chain. By exploiting the triple well option offered in 130nm CMOS technology, the pixels have been designed with a signal processing chain that includes charge preamplifier, shaper, discriminator and latch, while retaining a fill factor of the sensitive area close to 90%. The criteria underlying the design of the pixel level analog processor are presented, along with some preliminary experimental results on the first devices fabricated. The very first prototype APSEL0 proved the feasibility of the proposed solution. A second prototype, namely APSEL1, improved the S/N ratio and introduced the pixel matrix. The key features of four new prototype chips, now in production, will be presented. In particular, to overcome the readout speed limit of large-matrix state-of-the-art MAPS chips, for the proposed solution, a dedicated readout data sparsification has been investigated. This is carried out both in-pixel, via a first-level pixel architecture, already fabricated and tested, and via a full system digital readout circuit, which was just designed, fabricated on the last prototype, and whose test are ongoing. The paper describes the latest version of the chip, namely APSEL2D, submitted again on a multi-project-wafer in a 0.13µm CMOS technology on Q4 2006.

Author: GABRIELLI, Alessandro (INFN Bologna)

Presenter: GABRIELLI, Alessandro (INFN Bologna)