

# Development of CMOS Sensors for Future High Precision Position Sensitive Detectors

Wojciech Dulinski, IPHC

on behalf of CMOS Sensors Development Group

IPHC/IN2P3/CNRS (Strasbourg), DAPNIA/CEA (Saclay), GSI (Darmstadt) and IFK (Frankfurt)

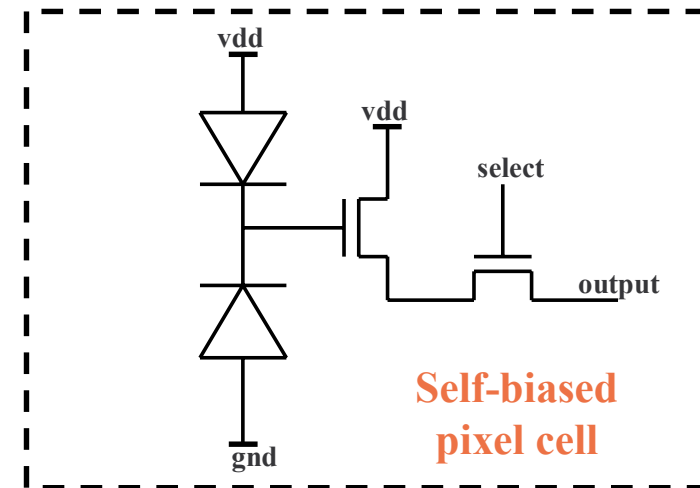
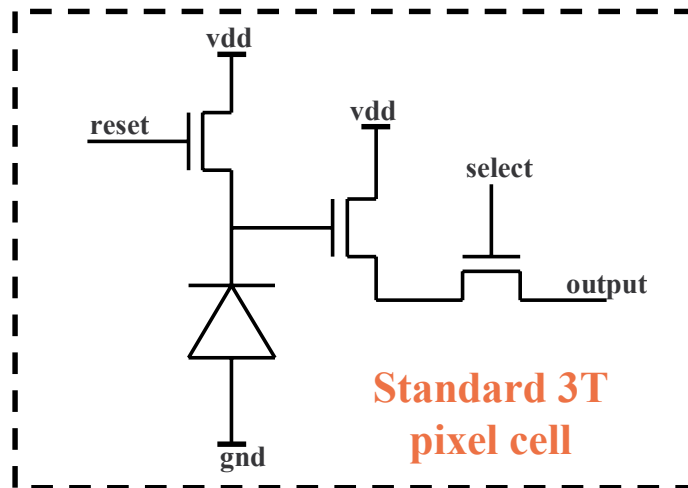
## Outline

- **Introduction: MAPS generalities**
- **Review of some important results**
- **“Slow readout” application**
  - STAR (first upgrade)
  - EUDET beam telescope (the demonstrator)
- **“Fast readout” application**
  - STAR (second upgrade)
  - EUDET (final version)
  - CBM (FAIR/GSI)
  - ILC
- **Summary and conclusions**

**Basic problems,  
limitations and  
some solutions**

# CMOS Active Pixel Sensors for radiation (light) imaging, as a competitor to CCD: late 80's

E. R. Fossum, "CMOS image sensors: electronic camera-on-a-chip", IEEE Trans. On Electron Devices 44 (10) (1997)

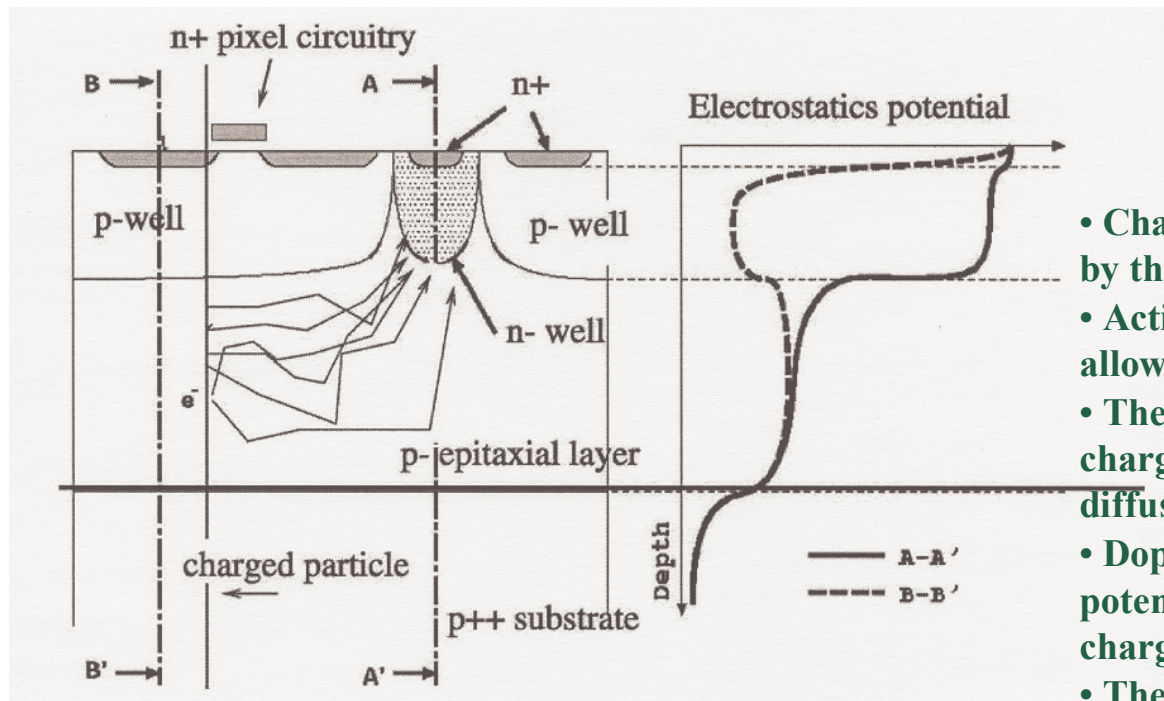


Basic pixel electronics schemes (photodiode, 3 or 4 transistors, transfer gate...) : all this elements are still bases of today's digital cameras

Strasbourg (IREs/LEPSI) invention, well suited for particle tracking application

## From digital cameras to particle tracking: use of an epitaxy layer as a detector active medium

B. Dierickx, G. Meynants, D. Scheffer “Near 100% fill factor CMOS active pixel sensor”,  
Proc. of the IEEE CCD&AIS Workshop, Brugge, 1997

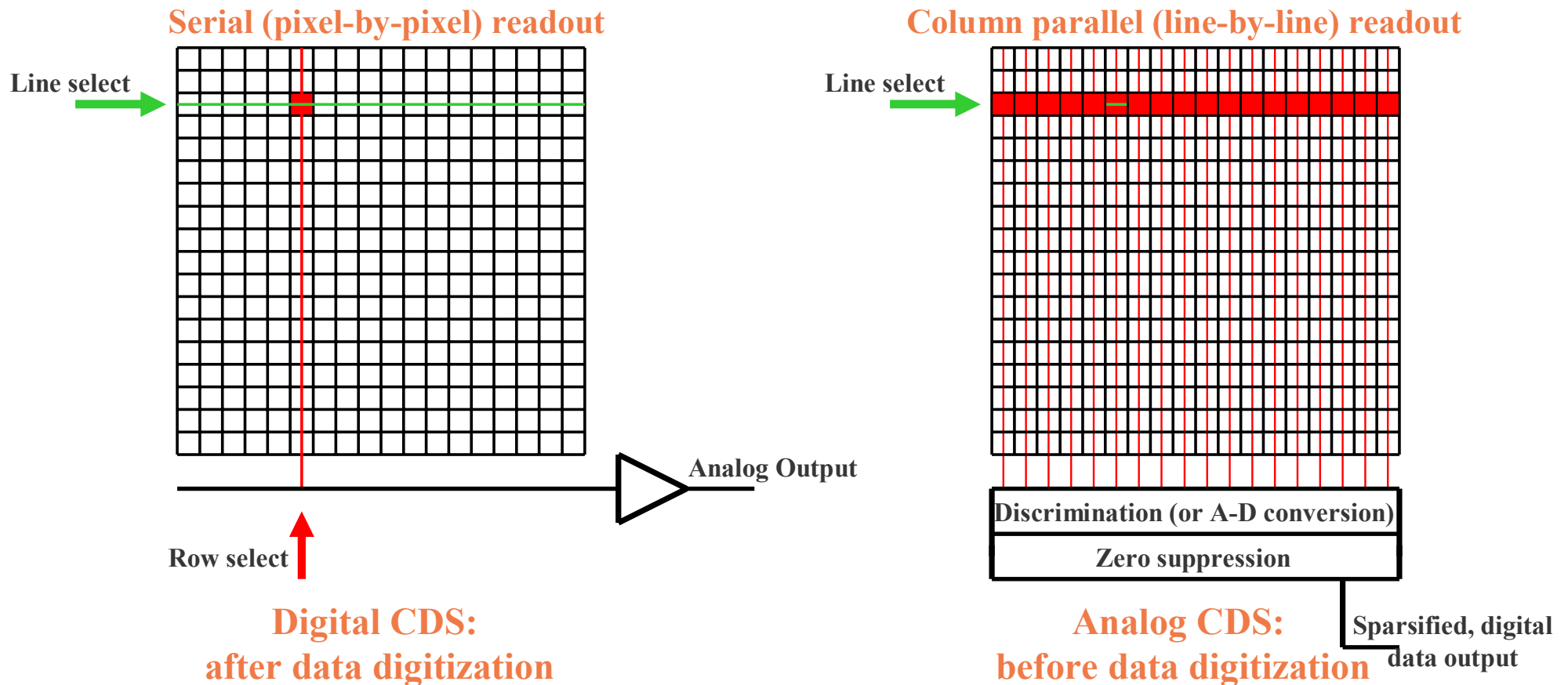


### Twin - tub (double well), CMOS process with epitaxial layer

- Charge generated by the impinging particle is collected by the n-well/p-epi diode.
- Active volume is underneath the readout electronics allowing a 100% fill factor.
- The active volume is NOT fully depleted: the effective charge collection is achieved through the thermal diffusion mechanism.
- Doping gradient ( $P^{++}_{\text{substrate}} - P^{-}_{\text{epi}} - P^{+}_{\text{well}}$ ) results in a potential minimum in the middle of epitaxy layer, limiting charge spread (2D instead of 3D)
- The device can be fabricated using almost any standard, cost-effective and easily available CMOS process

## Signal processing: Correlated Double Sampling in case of serial (slow) and column-parallel (fast) readout

CDS:  $\text{Signal} = \text{Sample}(t_1) - \text{Sample}(t_0)$ ;  $t_1 - t_0$  is the integration time

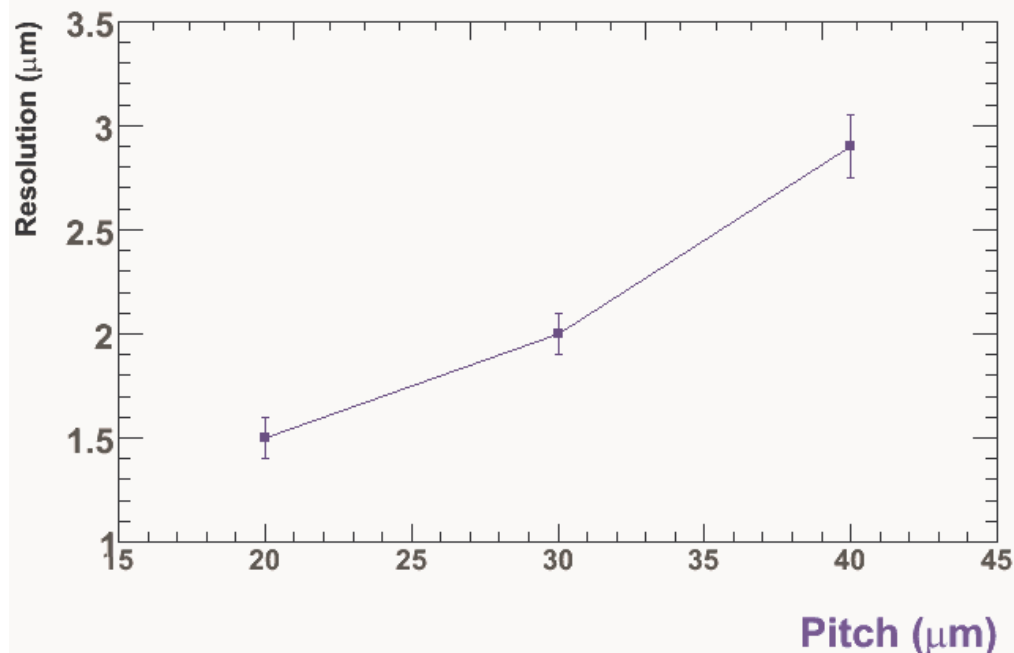


CDS is very efficient (and the only effective?) way of removing the inter-pixel pedestal spread, which is at least order of magnitude higher than the signal

## Mimosa9 (various pitch) beam tests results (THE reference)

### AMS 0.35 $\mu\text{m}$ CMOS OPTO process

- Advanced mixed-signal polycide gate CMOS: 4 metal, 2 poly, high-res poly, 3.3V and 5V gates
- Optimized N-well diode leakage current
- 14  $\mu\text{m}$  epi substrate (20  $\mu\text{m}$  possible)
- Availability through multi-project submissions, with a reasonable pricing (< 1 k€/mm<sup>2</sup>). In production, the price is of few k€ per 8 inch wafer.



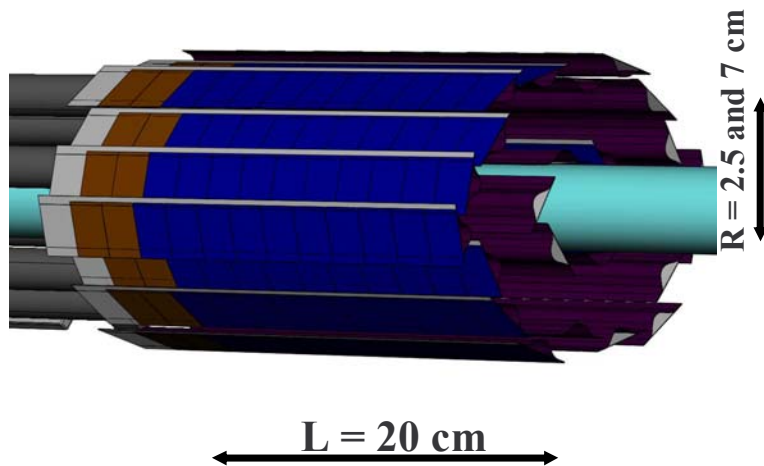
**Signal in the seed pixel: down to few tens of electrons**

**But: ENC ~10 electrons, so S/N comfortable**

**Efficiency >99.5%, for the fake hit rate ~10<sup>-5</sup>**

**Excellent spatial resolution!**

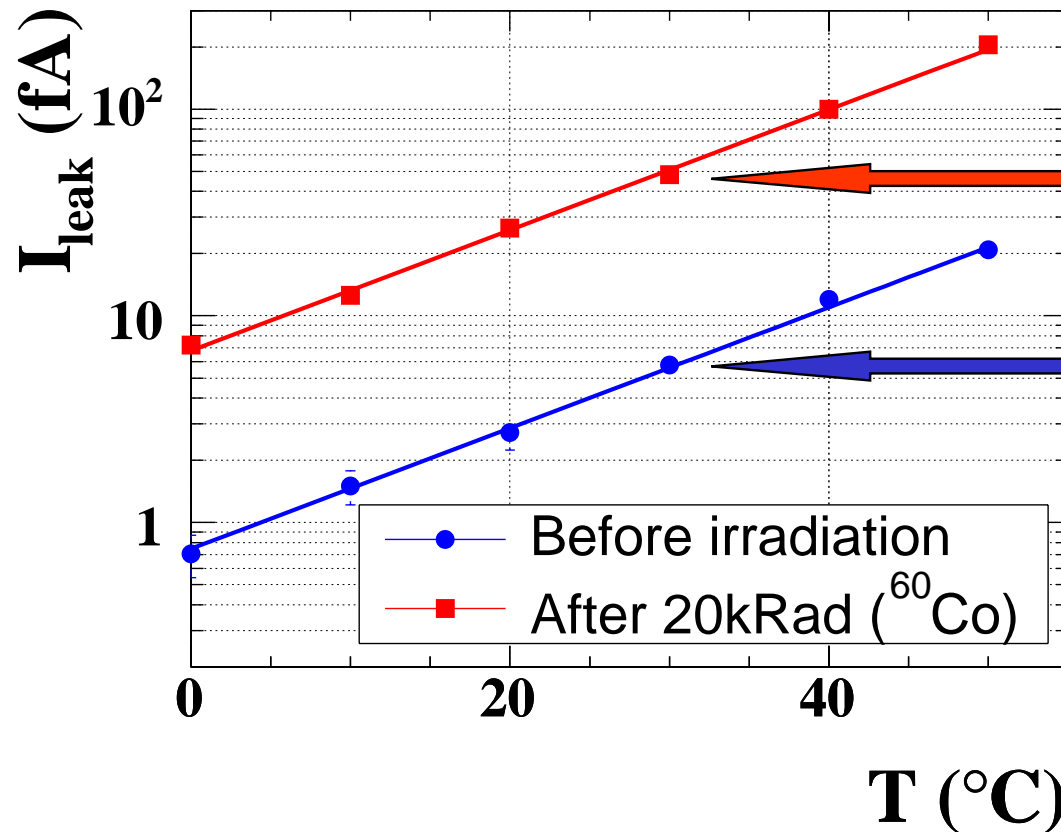
## Applications of MAPS in particle physics experiments: slow (serial, analog) readout



### STAR VxD upgrade 2008: 9+24 ladders

- (analog) readout time = integration time = 2 - 4 ms
- Room temperature operation (chip at  $\sim \leq 40^\circ\text{C}$ )
- Air cooling only
- Ionizing radiation dose:  $\sim 8 \text{ krad/year}$  ( $3 \cdot 10^{11} \text{ p/cm}^2/\text{year}$ )
- The Ultimate Upgrade: luminosity up, dose accordingly higher, integration time  $\sim 10\text{x}$  shorter.
- Considered solution is based serial readout for the first upgrade and on column-parallel binary readout for the Ultimate Upgrade

## Radiation tolerance for integrated ionizing dose: dark current increase



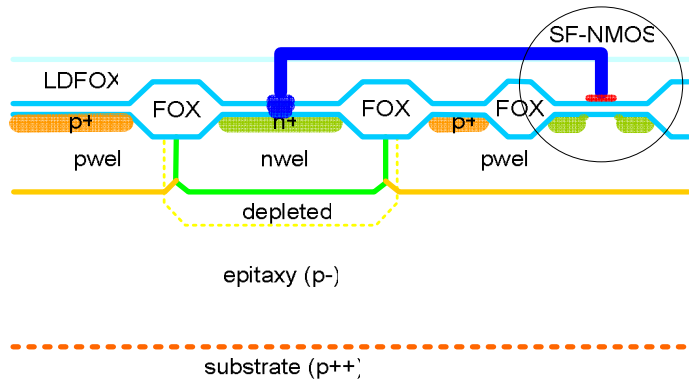
Shot Noise Contribution @ 30°C  
and @4 ms integration time

$ENC_{shot} = 39$  electrons

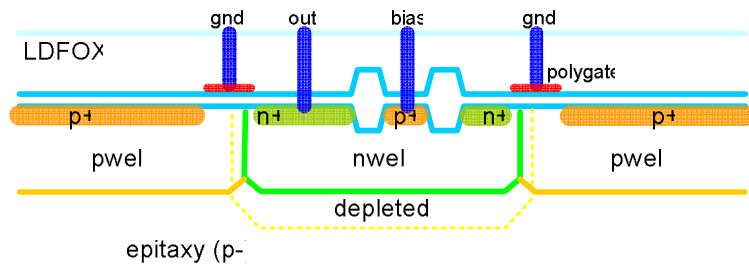
$ENC_{shot} = 12$  electrons

Standard N-well/p-epi diode dark current increase  
after irradiation with a <sup>60</sup>Co γ source (Mimosa9)

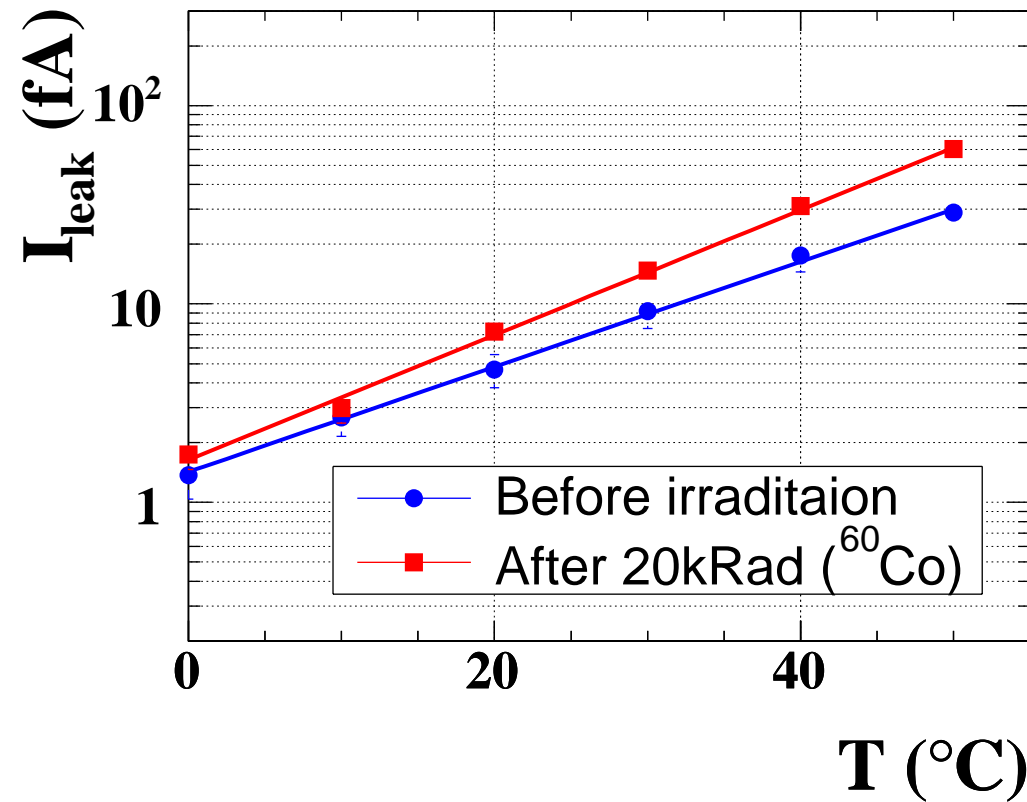
# “Thin-oxide” diode dark current increase after irradiation with a $^{60}\text{Co}$ $\gamma$ source



**standard diode layout**



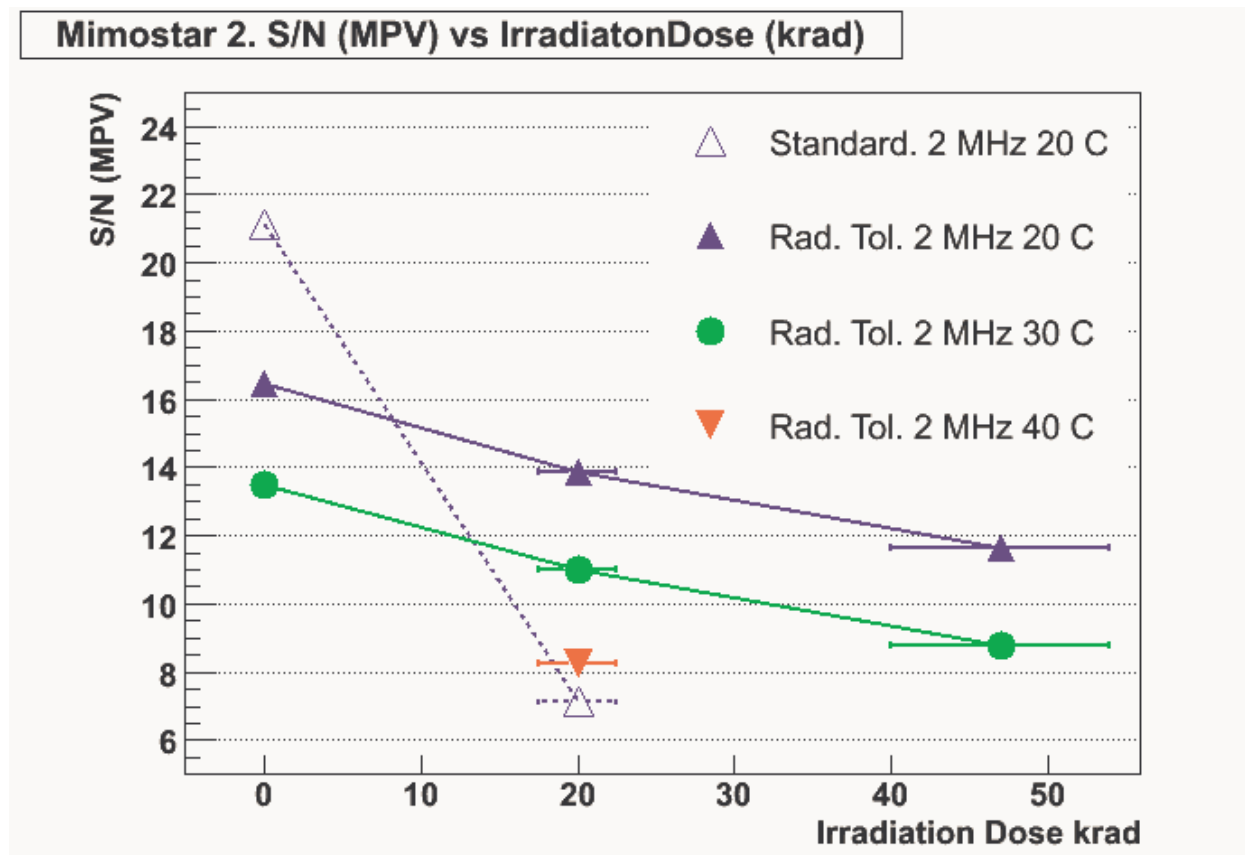
**thin-oxide diode layout**



**Recent results (Mimosa15): x10 current increase after 1Mrad. Compatible with ILC requirements.**

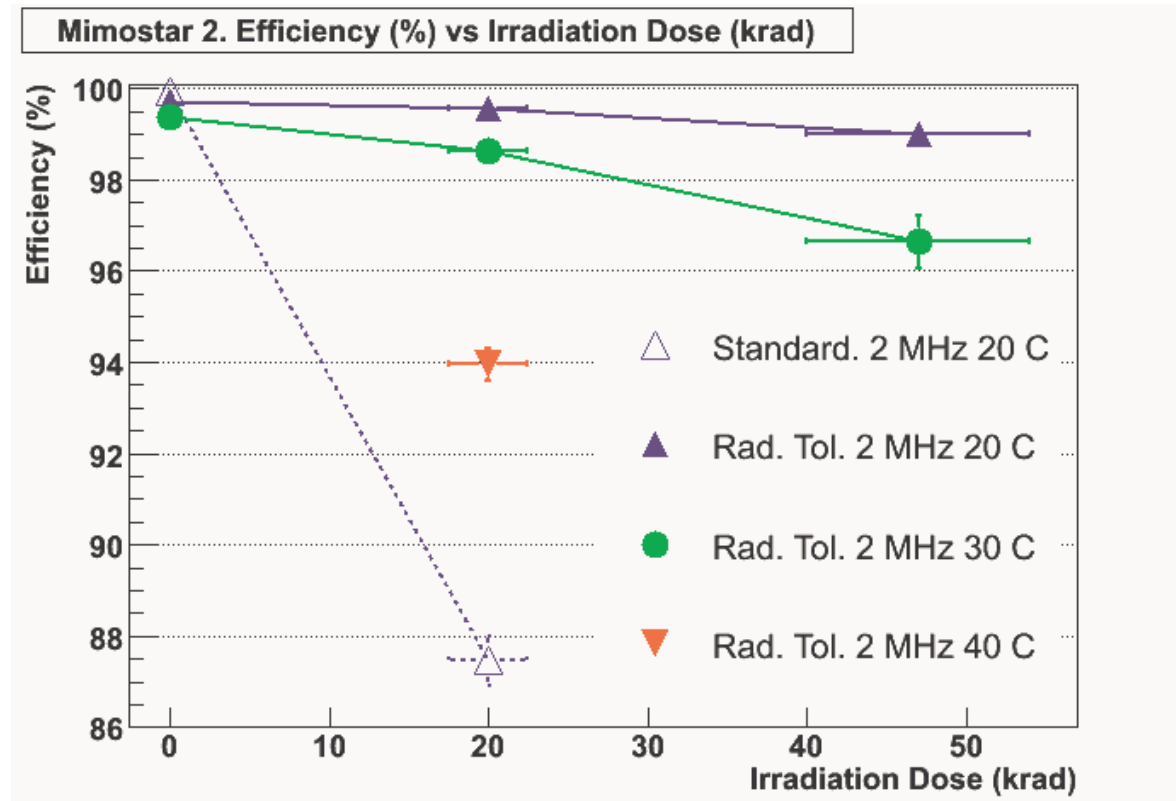


**MimoSTAR-2 (30  $\mu\text{m}$  pitch): the demonstrator for STAR experiment microvertex upgrade. Based on radiation tolerant N-well collecting diodes. JTAG based control and bias setting.**



**S/N vs. dose**

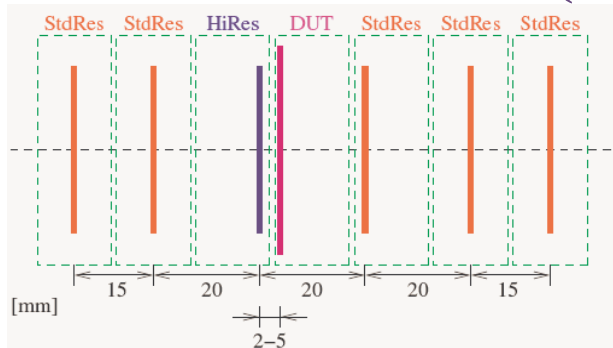
## Mimo\*2 beam tests: efficiency after irradiation



Efficiency vs. dose, for S/N cuts = 5 (seed) and 2 (crown)

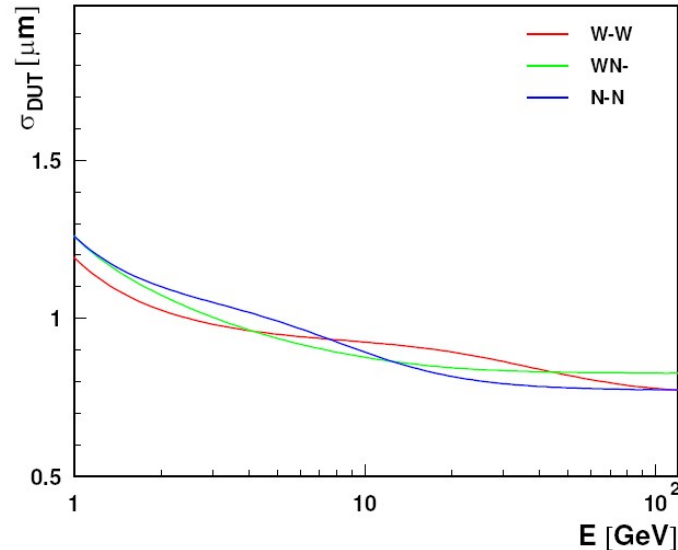
After 47 kRads, efficiency >99 % at room temperature AND long (4ms) integration time, for the fake hits rate <math>10^{-4}</math>

# Applications of MAPS in particle physics experiments: slow (serial, analog) readout



Optional high-precision plane: 1  $\mu\text{m}$  resolution

$$\Delta_{DUT} = 800 \mu\text{m}$$



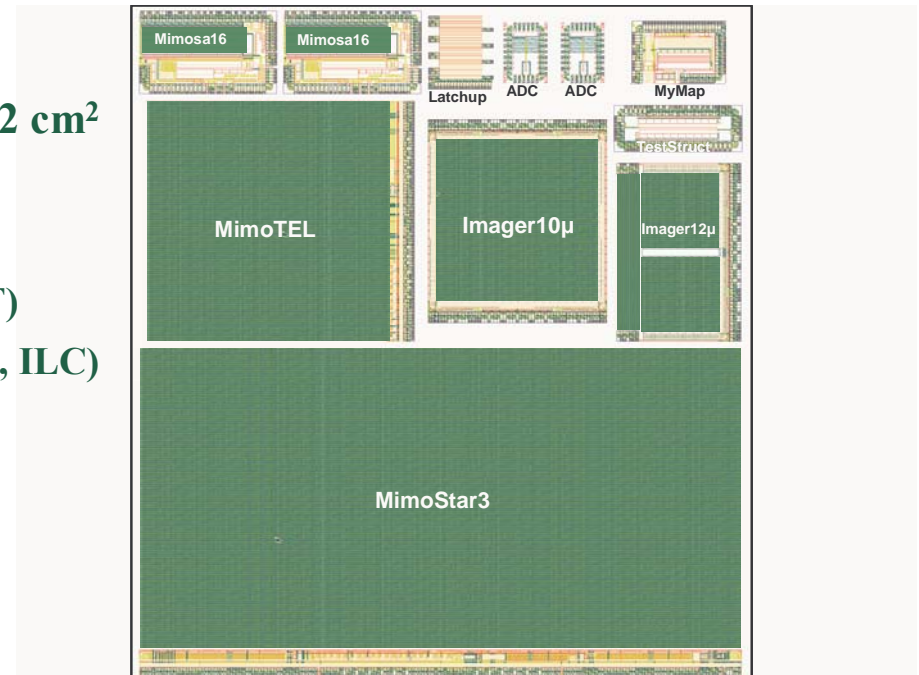
## EUDET General Purpose Beam Telescope

- **Compact:** to be mounted inside existing magnets, transportable
- **User friendly, easy to run AND to interface with various users**
- **Sensitive area:** few. sq. cm (at least 2 cm in one direction)
- **High precision tracking:** down to  $\sim 1 \mu\text{m}$  in the center, also at medium energy beams ( $\sim$  few GeV)

Telescope resolution study: Analytical Track Fitting Method with Multiple Scattering,  
verified using GEANT 4 (credit to A.F.Zarnecki, Warsaw University)

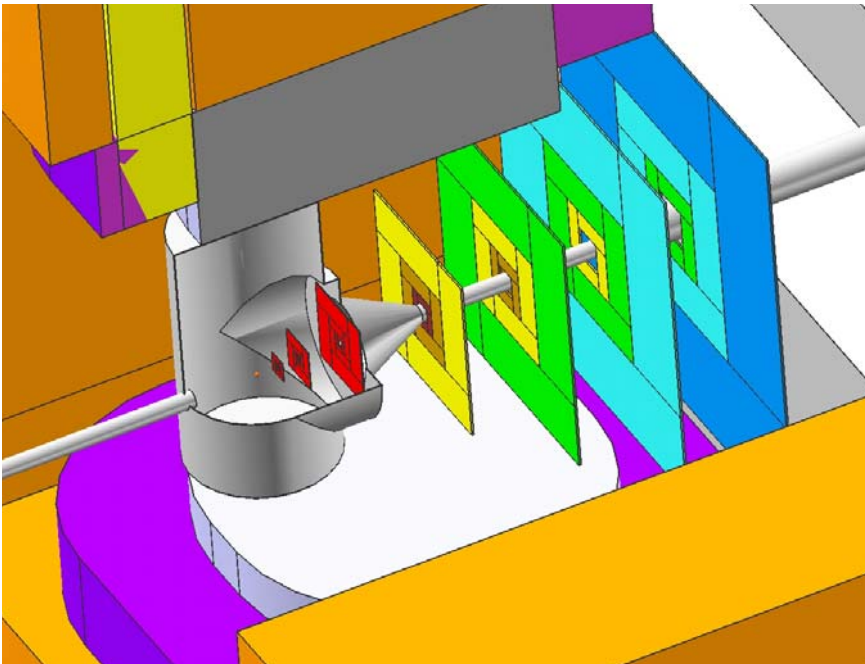
## Sensor fabrications in 2006: engineering run in AMS-0.35 OPTO

- Motivated by MIMOSTAR-3 : 200 kpixels,  $t_{r.o.} = 2 \text{ ms}$ ,  $2 \text{ cm}^2$
- Other chips:
  - MIMO TEL:  $0.8 \times 0.8 \text{ cm}^2$ , rad.tol.,  $800 \mu\text{s}$  (EUDET)
  - IMAGER-10 $\mu$  (M-18): expected resolution  $< 1 \mu\text{m}$  (EUDET)
  - MIMOSA-16: binary readout architecture (EUDET, CBM, ILC)
  - Imager-12 $\mu$  (M-19): charge-spread reduction
  - Low resolution, low power ADCs
- Epitaxy thickness: 14 and 20  $\mu\text{m}$



**Almost all sensors have been tested and are working with promising performances, waiting for the beam tests in 2007...**

## Applications of MAPS in particle physics experiments: fast, column parallel, digital readout



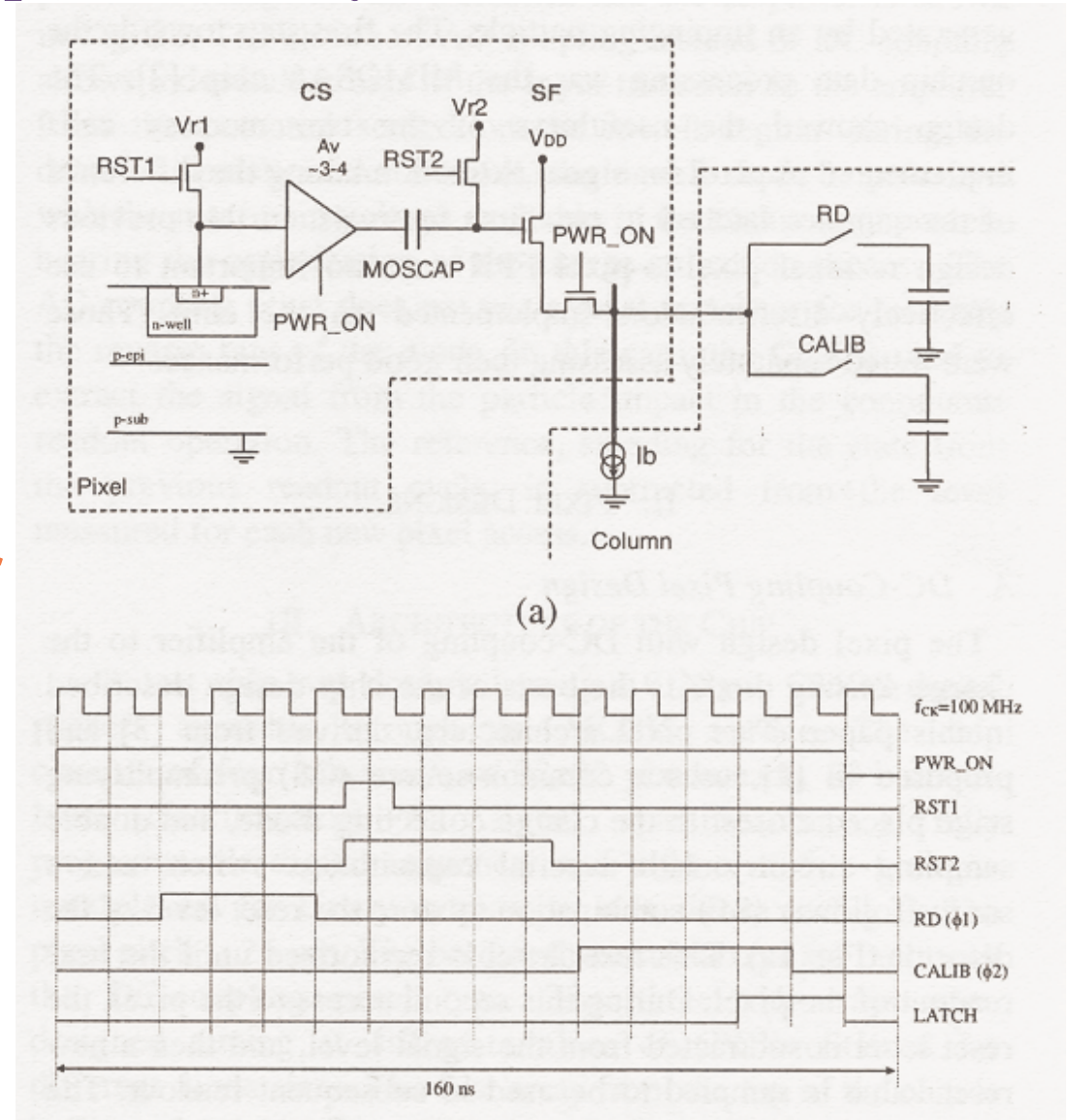
### CBM vertex detector (FAIR/GSI)

- Readout time = integration = time resolution:  $<10 \mu\text{s}$
- Binary readout, no zero suppression
- Vacuum operation
- Ionizing radiation dose:  $>2 \text{ MRad}$
- Neutron fluence (1MeV eq.):  $>10^{13} \text{ n/cm}^2$
- Total single layer thickness:  $<150 \mu\text{m (Si)}$

Extremely demanding application, but no alternative solution candidates...

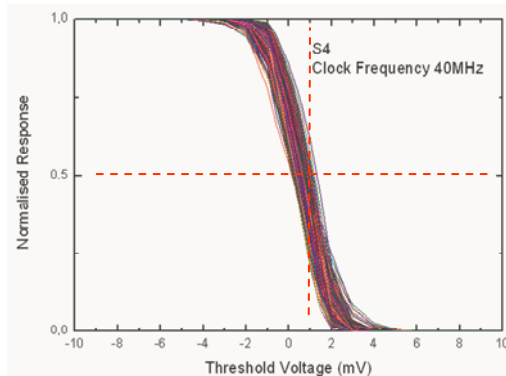
# Mimosa8 (TSMC-0.25 $\mu$ , 8 $\mu$ m epi) – a binary readout demonstrator

- CDS in pixel, based on “clamping” circuit solution
- On-chip FPN suppression
- Offset compensated comparator at the end of each column
- Pixel pitch 25 x 25  $\mu$ m<sup>2</sup>



Prototype in collaboration with Dapnia/Saclay

## Mimosa8 beam tests results

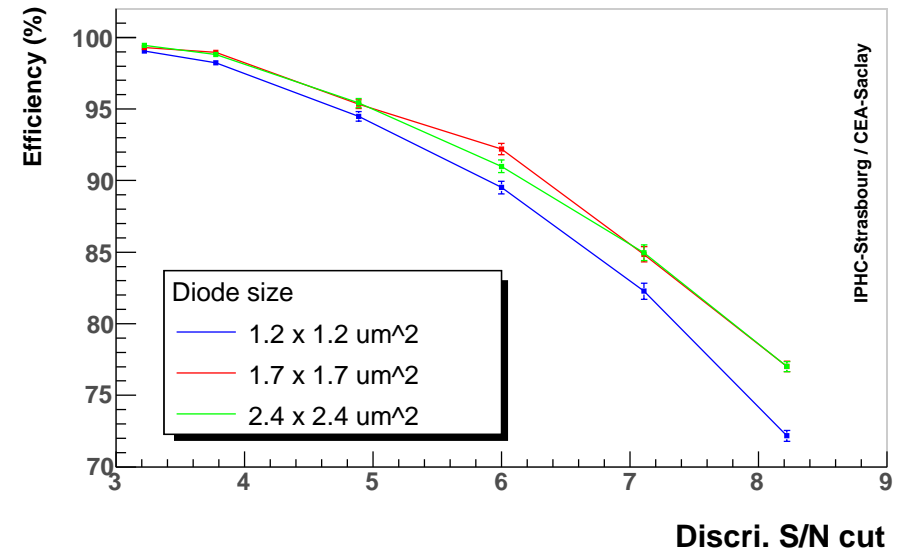


Comparator voltage scan (all pixels)

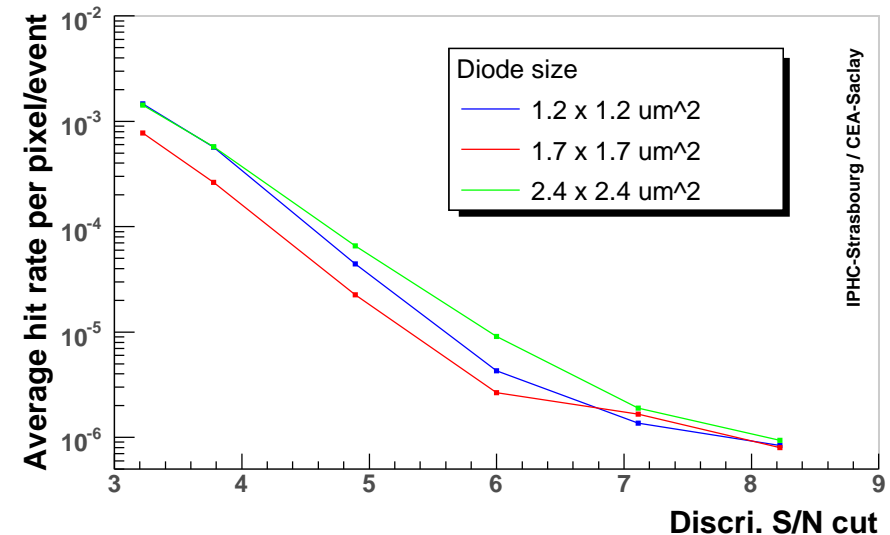
- Output noise: 0.9 mV (ENC = 15 electrons)
- Pixel-to-pixel FPN: 0.45 mV (7.5 electrons)
- Spatial resolution:  $\sigma_r = \sim 7 \mu\text{m}$

- First demonstration of feasibility of FPN correction using on-chip real time circuitry
- The design goal confirmed by the beam tests results: efficiency > 99 %
- Second version (Mimosa16) in AMS-035 OPTO with 14 and 20  $\mu\text{m}$  epi under test

M8 digital. Efficiency (%) vs S/N cut

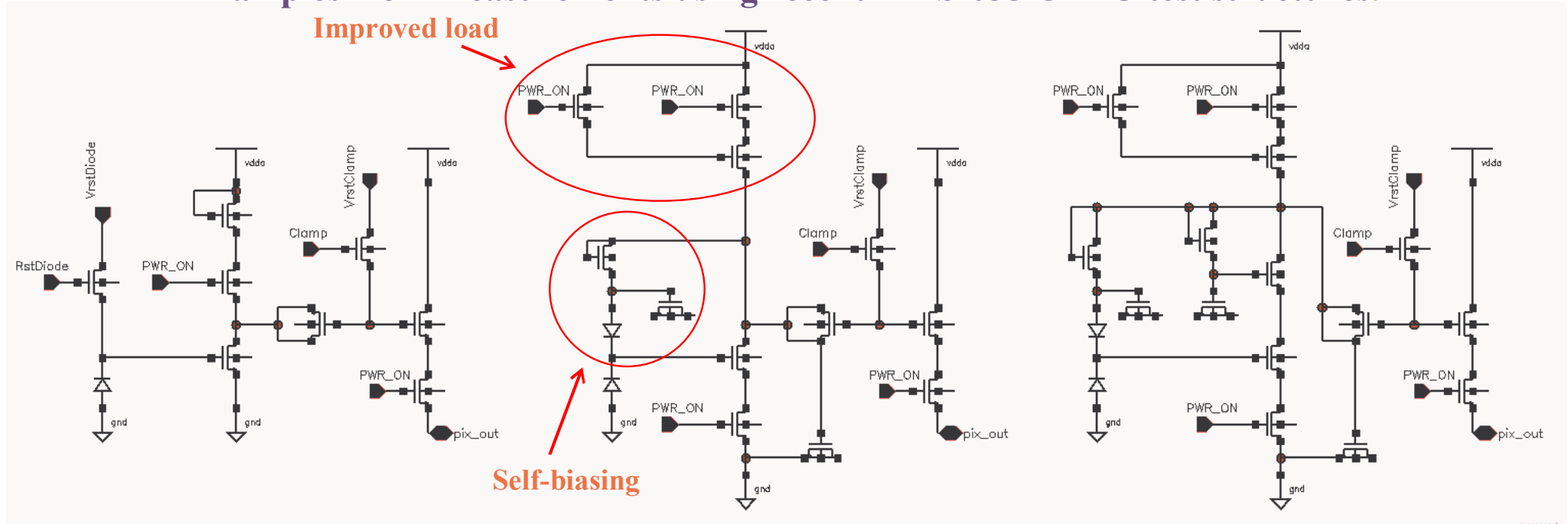


M8 digital. Max fake hit rate per pixel vs Threshold



**Pixel optimization: diode size ↑ , charge collection ↑ but also parasitic capacity and ENC ↑ !**

Examples from measurements using recent AMS-035 OPTO test structures.



CS, 2.4x2.4  $\mu\text{m}$  diode  
ENC = 12 e,  $G = 65 \mu\text{V/e}$   
Charge coll. eff. <25%

CSFb, 4.5x4.5  $\mu\text{m}$  diode  
ENC = 15 e,  $G = 45 \mu\text{V/e}$   
Charge coll. eff. >50%

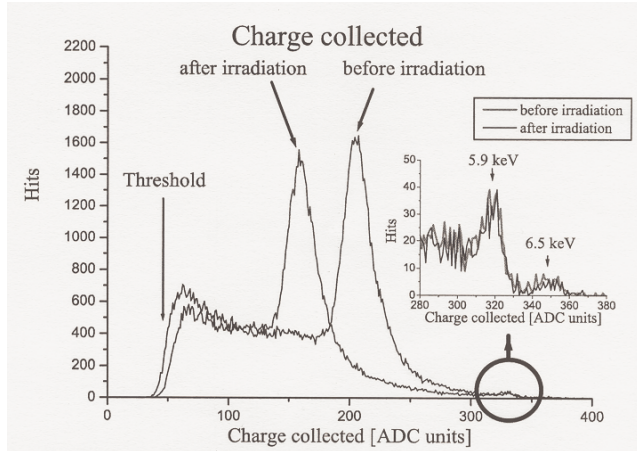
CAFb, 4.5x4.5  $\mu\text{m}$  diode  
ENC = 12 e,  $G = 65 \mu\text{V/e}$   
Charge coll. eff. >50%

\* Collection efficiency: charge collected in 3x3 cluster, measured on 20  $\mu\text{m}$  thick epi wafer and 25  $\mu\text{m}$  pixel pitch



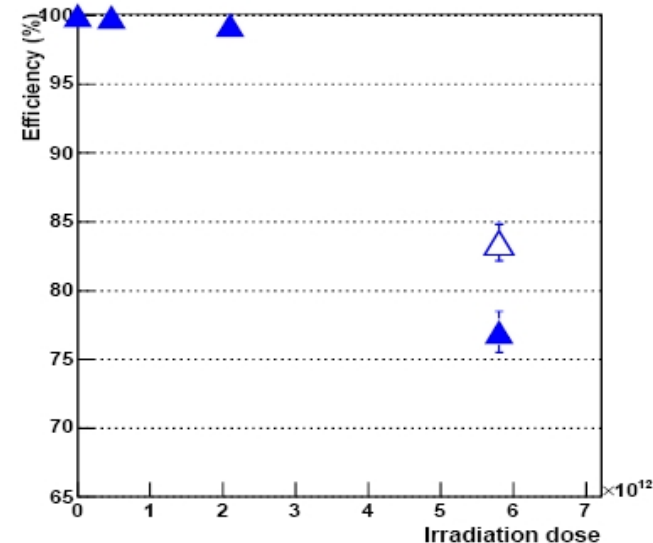
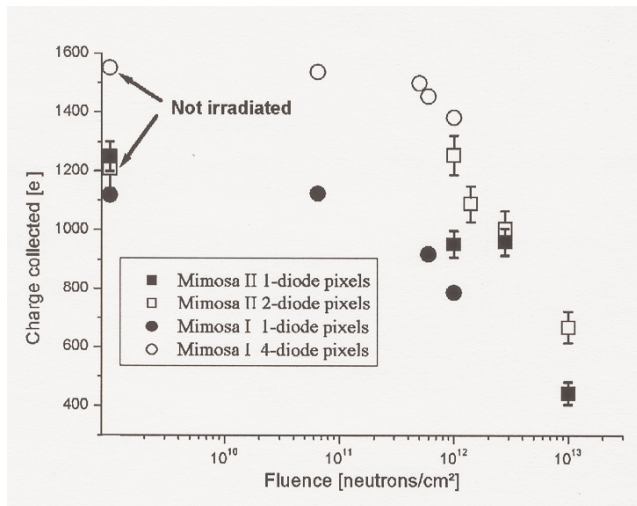
# Radiation tolerance for the bulk damage: neutron irradiation

## Mimosa15 (AMS-035 OPTO), rad-tol diodes



Fluence	0	0.47	2.1	5.8 (5/2)	5.8 (4/2)
	( $10^{12} \text{ n}_{eq}/\text{cm}^2$ )				
Noise ( $e^-$ )	9.0 $\pm 1.1$	9.2 $\pm 1.2$	9.3 $\pm 1.2$	9.6 $\pm 2.0$	9.6 $\pm 1.9$
S/N (MPV)	27.8 $\pm 0.5$	21.8 $\pm 0.5$	14.7 $\pm 0.3$	8.7 $\pm 2.$	7.5 $\pm 2.$
Det. Eff. (%)	100.	99.9 $\pm 0.1$	99.3 $\pm 0.2$	77. $\pm 2.$	84. $\pm 2.$

○  $5.8 \cdot 10^{12} \text{ n}_{eq}/\text{cm}^2$  values derived with **standard** and with **soft** cuts



Mimosa15 MIP detection efficiency

Charge loss observed after  $\sim 10^{12} \text{ n}/\text{cm}^2$ , correlated to the diode/pixel area ratio, seems to be rather basic and process independent. Going to smaller pitch and larger diodes (L-shaped) may bring some improvements (factor of two or three).

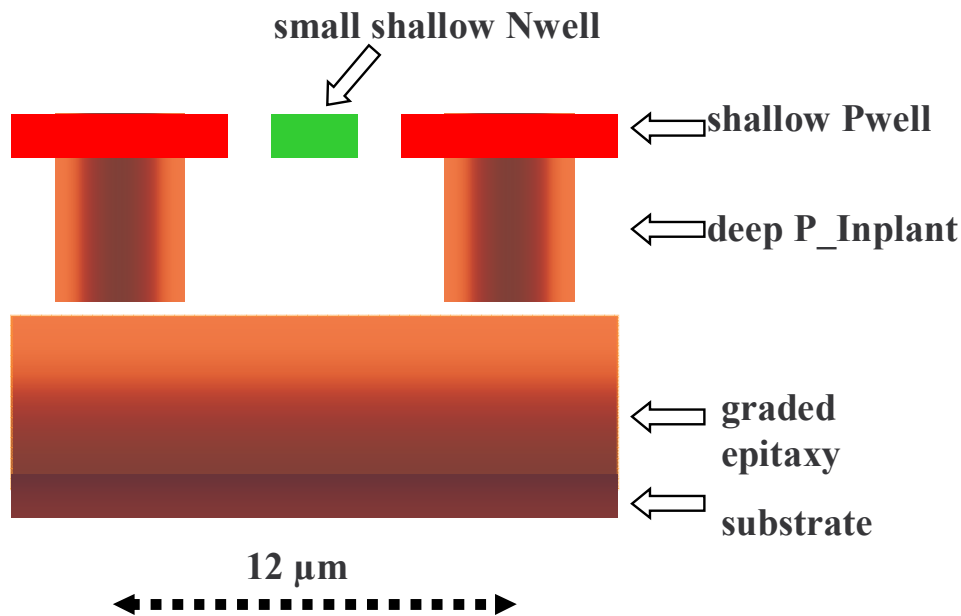
## Possible (substantial) improvement

B. Dierickx “Multiple or graded epitaxial wafers for particle or radiation detection”,  
US Patent 6,683,360 B1, Jan. 2004

*PLUS deep implants available in some BiCMOS processes*

Field shaping using doping gradient → faster charge collection → smaller sensitivity to the bulk damage

Field shaping → smaller charge spread → optimum conditions for the binary readout



Example from our simulation of novel MAPS structure (ISE TCAD, realistic doping profiles).  
In parentheses, typical standard structure.

-Charge collection time: < 10 ns (~100ns)

-Charge spread suppression:

> 60% (<30%) of charge in central pixel,  
all charge inside < 4 pixels (>9 pixels)

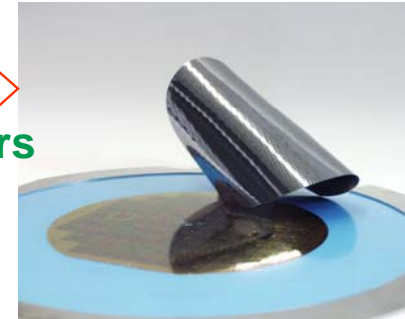
**Prototypes in construction!**

## Exploring new possibilities for MAPS performance upgrade, based on Vertical Integration (3D Electronics) industrial process.

### Vertical Integration ingredients:

- Wafers thinning down to 10-20  $\mu\text{m}$  ( $\rightarrow$  flexible sheet!)  $\Rightarrow$
- Precision alignment and molecular bonding of several layers
- Through-wafer vias formation for electrical interconnection

Result: 3D, monolithic circuit (or a sensor system)



### Possible applications in tracking systems:

1. Construction of monolithic ladder, integrating two active silicon layers (one full plane, stitched MAPS, plus one signal processing and transmission layer) bonded to heat dissipation, diamond layer. Total thickness  $< 150\mu\text{m}$   $\rightarrow$  **proposal for CBM application**
2. Increased flexibility for wafer choice: post-processing step. Back-thinning and back-contact re-implementation at low temperature is possible, allowing an optimized use of thick, high-resistivity wafers available in many RF deep-submicron CMOS processes

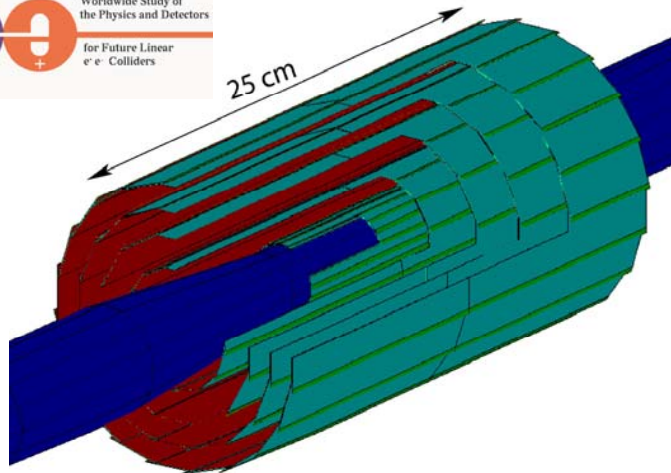
Thick metal for interconnection (busing)

SOI CMOS or BiCMOS, digital processing @ data transmission, 10  $\mu\text{m}$  thick

Graded epitaxial wafer, MAPS layer, 20  $\mu\text{m}$  thick

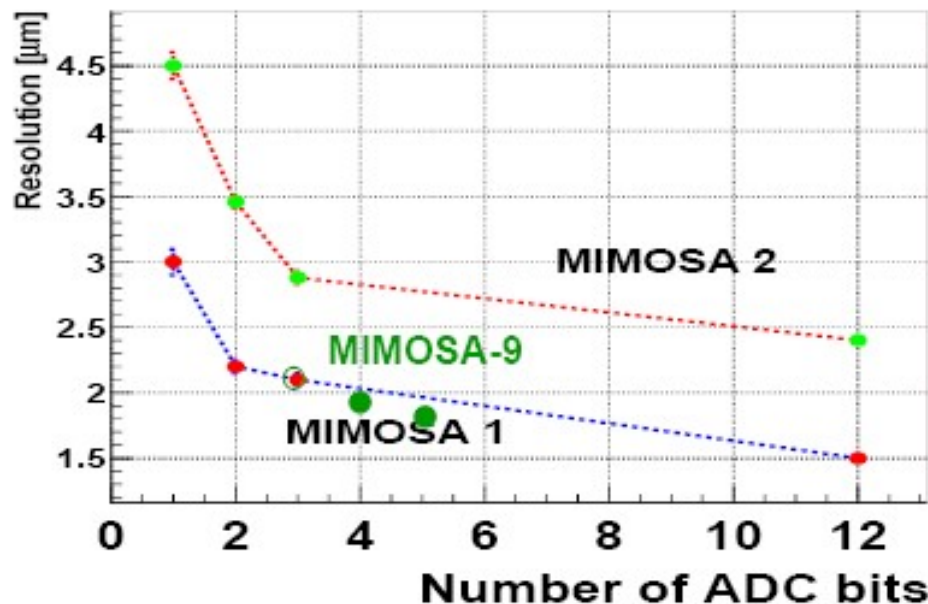
CVD diamond, heat dissipation to periphery, 50 to 100  $\mu\text{m}$  thick

# Applications of MAPS in particle physics experiments: fast, column parallel, digital readout with low resolution ADCs



## ILC VxD

- Beam train: ~1 ms every ~200 ms
- Outer layers integration time: < ~200  $\mu$ s
- Inner layers integration time: < ~25 - 50  $\mu$ s
- Neutron eq. fluence: < ~ $10^{10}$  n<sub>eq</sub>/cm<sup>2</sup>/year
- Ionizing dose: < 50 krad/year (~10 MeV electrons)



Real data based simulation of MAPS tracking performance versus end-of-column ADC resolution, supposing efficient (analog) FPN suppression

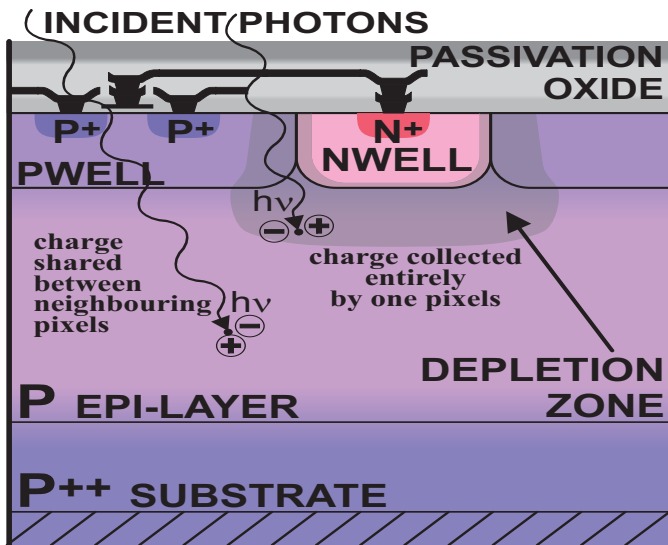
## Conclusions

- **Monolithic CMOS Pixels Sensors**, after several years of development, starts to reach certain maturity level. However, there is still a room for substantial improvements within existing technologies. In particular, deep-submicron, triple-well CMOS (or BiCMOS) processes should be better explored and evaluated. **The use of commercial, easily available and cheap technology is a great thing not only for prototyping but also for large scale production!**
- **For applications requiring ultra-thin sensors and ultra-high spatial resolution in relatively large area, MAPS are the leading candidates.**
- **First applications in physics experiments are expected soon and will be (probably) crucial for this technique. Each application requires careful optimization, but this is possible – MAPS are ASICS!**
- **Commercial technology advances, like apparition and availability of Vertical Integration, may also allow for important upgrade of MAPS performances and increase flexibility of system aspects.**

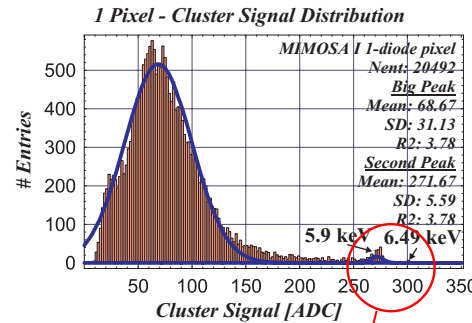
# Back-up slides: Calibration of the conversion gain - with soft X-rays

## • Calibration methods:

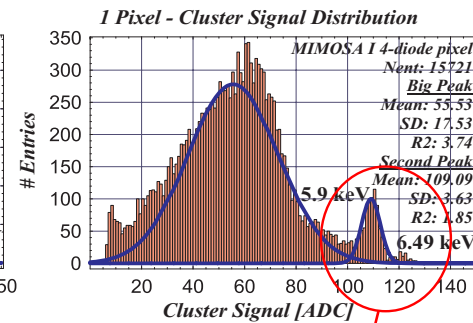
Emission spectra of a low energy X-ray source e.g. iron <sup>55</sup>Fe emitting 5.9 keV photons. very high detection efficiency even for thin detection volumes -  $\mu = 140 \text{ cm}^2/\text{g}$ , constant number of charge carriers about 1640 e/h pairs per one 5.9 keV photon



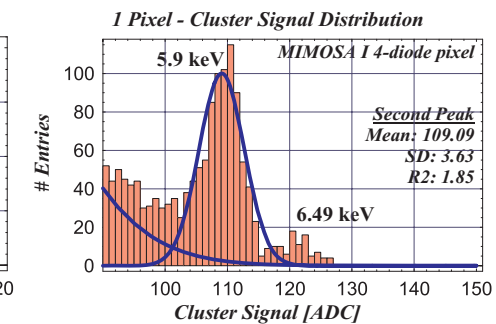
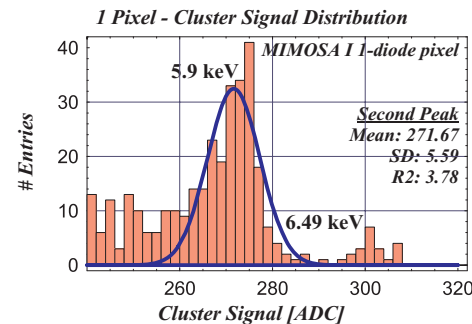
The ' warmest ' colour represents the lowest potential in the device



MIMOSA I (14  $\mu\text{m}$  EPI) configuration with single diode in one pixel

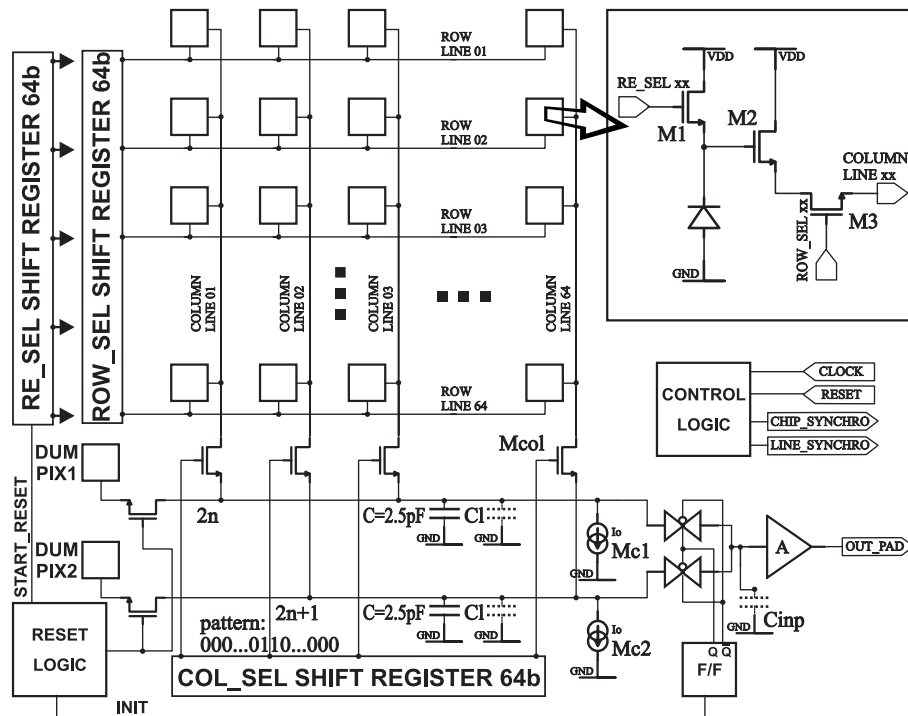


MIMOSA I (14  $\mu\text{m}$  EPI) configuration with four diodes in one pixel



MIMOSA I CMOS 0.6 $\mu\text{m}$	1 diode - 14.6 $\mu\text{V}/\text{e}^-$	4 diode - 6.0 $\mu\text{V}/\text{e}^-$
	ENC = 14 $\text{e}^-$ @ 1.6 ms f. rate	ENC = 30 $\text{e}^-$ @ 1.6 ms f. rate
MIMOSA II CMOS 0.35 $\mu\text{m}$	1 diode rad. tol. - 22.9 $\mu\text{V}/\text{e}^-$	2 diode rad. tol. - 17.5 $\mu\text{V}/\text{e}^-$
	ENC = 12 $\text{e}^-$ @ 0.8 ms f. rate	ENC = 14 $\text{e}^-$ @ 0.8 ms f. rate

## Back-up slides: The simplest readout electronics: diode + 3 transistors/pixel

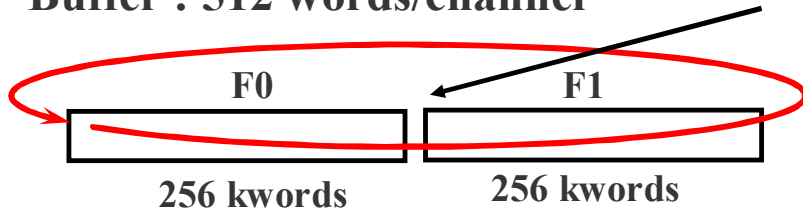


1. Reset in order to inverse bias
2. Continuous serial addressing and readout (digitisation) of all pixels
3. Keeping two successive frames in external circular buffer
4. Following reset when needed (removing integrated dark current)
5. After trigger (or in a real time), simple data processing in order to recognise hits

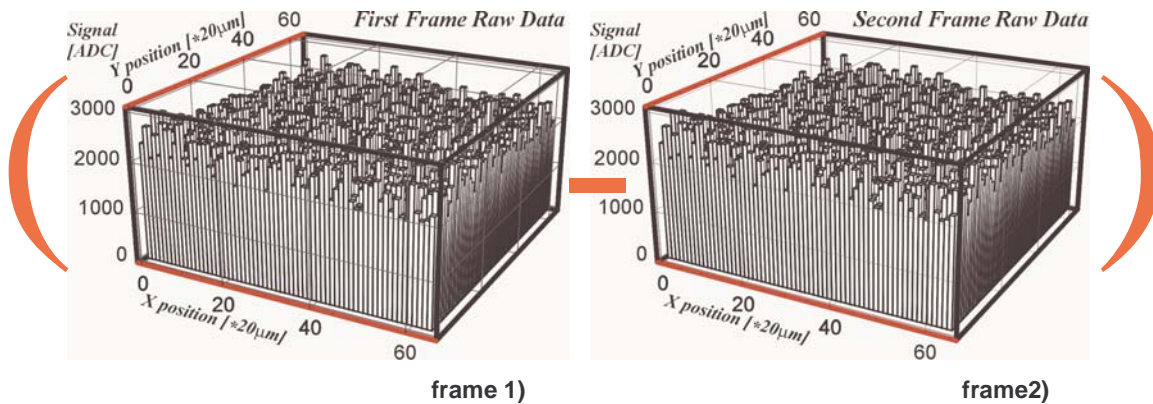
Fast ADC 12 bits

Buffer : 512 words/channel

trigger !

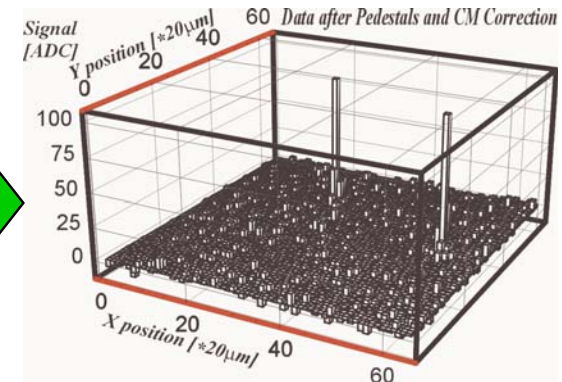
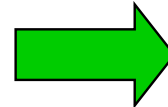
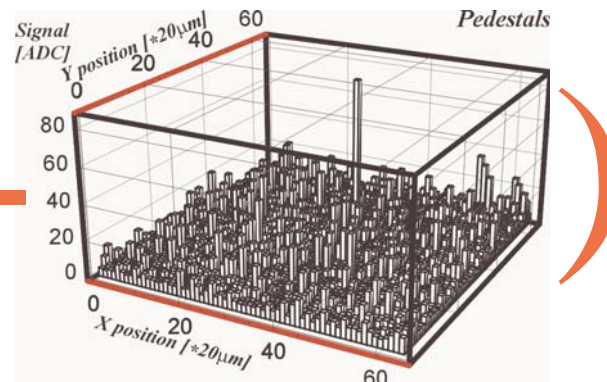
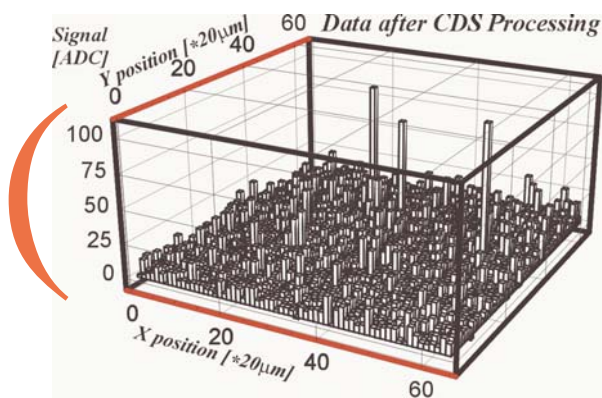


**Back-up slides: Data processing: (Digital) Correlated Double Sampling**



Useful signal on top of  
Fixed Pattern DC level  
Fixed Pattern dispersion: ~100 mV  
Typical signal amplitude: ~1mV

(frame2 - frame1) subtraction



frame2 - frame1) Pedestal (dark current) subtraction

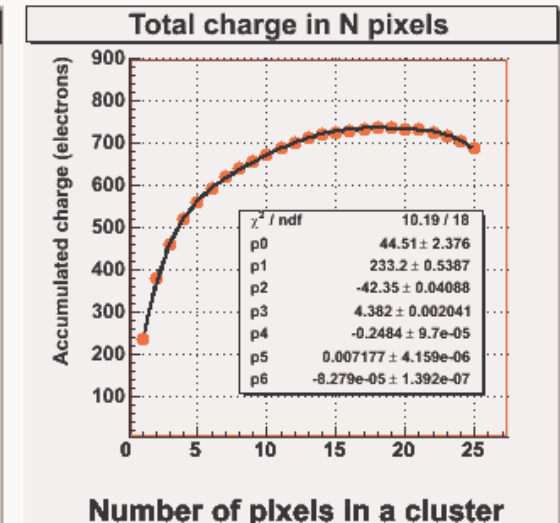
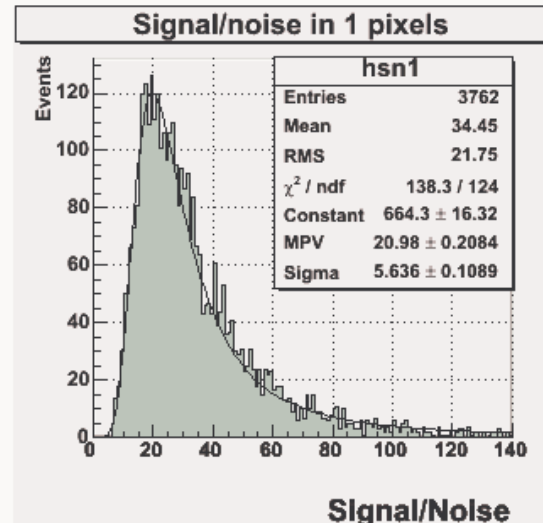
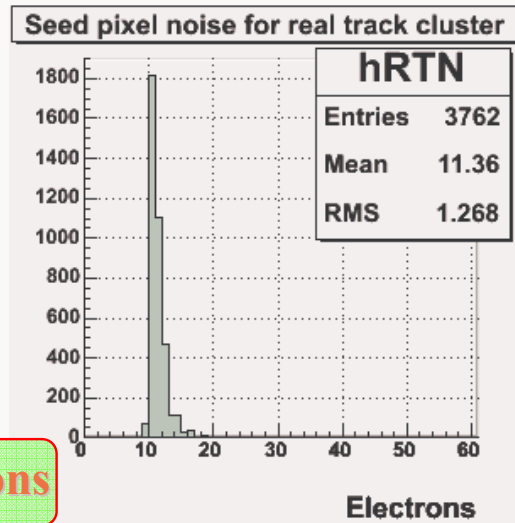
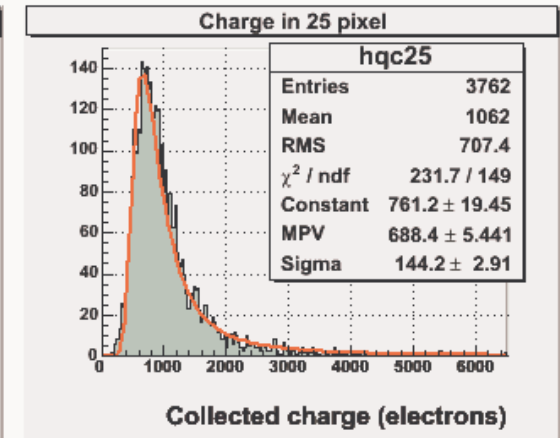
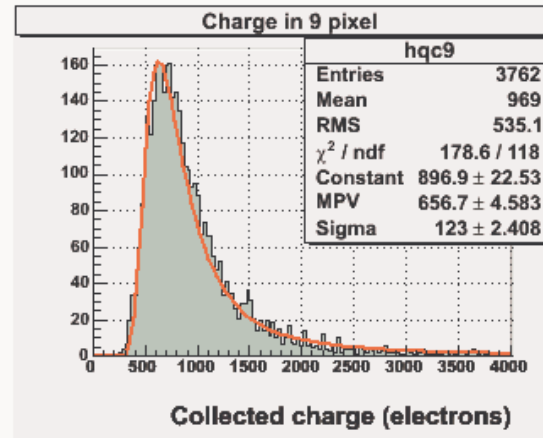
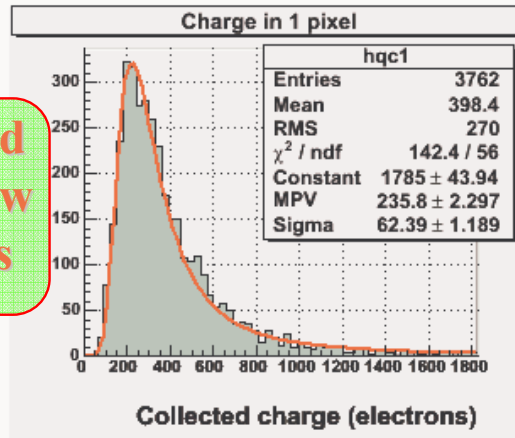
**Hit candidates!**



Back-up slides: A “typical” example from the beam tests: 30 $\mu$ m pitch array, 20°C

M9 ; run 9534; Pl 10, dist 90; Gain 7.200; eff 99.810 +/- 0.070; Seed 6.0; Neigh 4.0

Signal in the seed pixel: down to few tens of electrons



ENC: ~10 electrons

Efficiency >99%, spatial resolution: down to 1.5  $\mu$ m

**Back-up slides:  $\text{Fe}^{55}$  spectrum before (red) and after (green) 1 Mrad of X-rays @40°C (200  $\mu\text{s}$  integration) : prove of principle for ILC**

