Electronics Contributions to the Belle Silicon Vertex Detector by HEPHY Vienna



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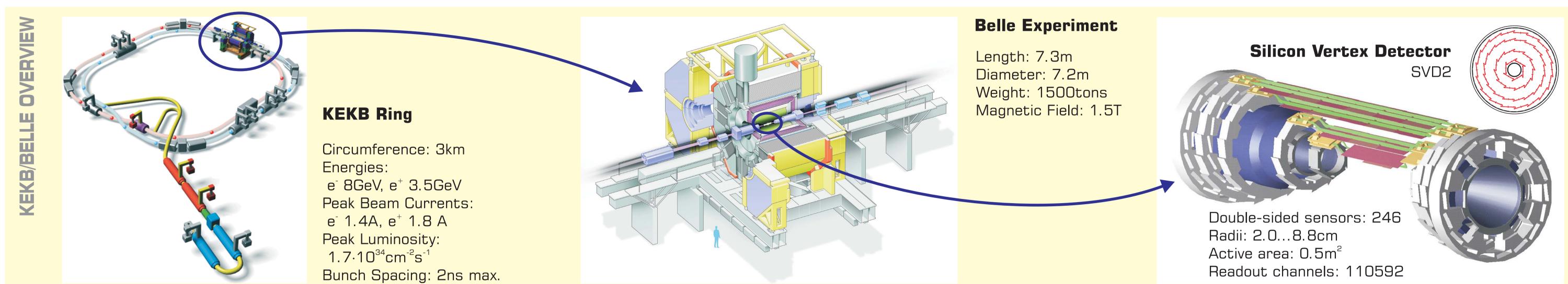
ABSTRACT

BELLE

The Belle experiment at KEK (Tsukuba, Japan) studies CP violation in B meson decays by measuring the sides and angles of the unitarity triangle. Some of these measurements require the reconstruction of the vertices of the two decaying B mesons in an Y(4S) event, making the Silicon Vertex Detector (SVD) a critical device for the experiment. The initial SVD1 was in operation from 1999 until 2003, suffering from radiation levels beyond expectation. The current SVD2, installed in 2003, introduced several improvements, like radiation tolerance and a higher accuracy due to an additional fourth layer. Over the years, the occupancy levels grew along with luminosity especially in the innermost layer (\sim 10%), compromising tracking precision and data acquisition throughput. This leads to another upgrade called SVD2.5, where the two inner layers will be equipped with faster and dead-time-free front-end amplifiers.

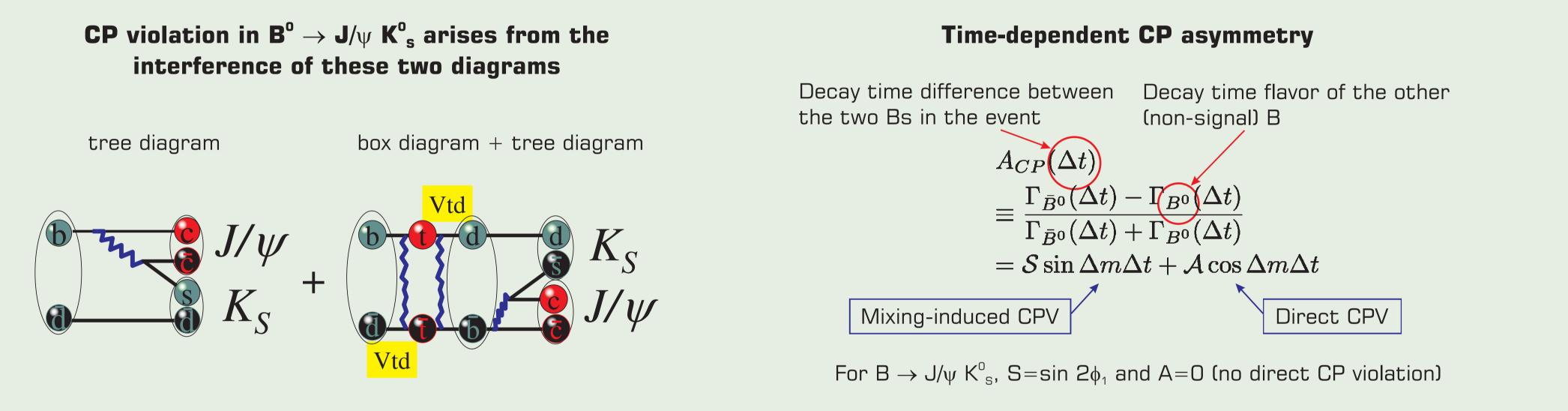
The Electronics-2 group at HEPHY Vienna designed and built the SVD2 FADC VME modules which digitize the analog data from the front-end, extract the first-level trigger using combinatorics between layers and present binary hit data to the L1.5 trigger electronics. Due to our experience from CMS, we suggested the APV25 front-end chip for the SVD2.5 upgrade and built several

prototype systems including various front-end modules, repeaters, VME controllers and FADCs with hardware data processors performing pedestal subtraction, common mode correction and zero suppression within FPGAs. Moreover, multiple samples along the shaping curve of the APV25 can be used to reconstruct the particle timing with a precision of a few nanoseconds, which will also be implemented in FPGA firmware using look-up tables, in order to reject off-time hits and thus eliminate the occupancy problem. Finally, we try to optimize the signal-to-noise ratio of the front-end detector module, using SVD2.5 sensors and the APV25 front-end chip.

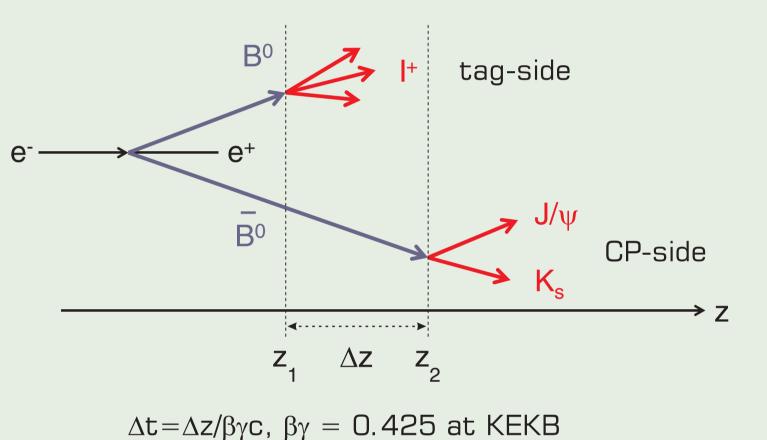


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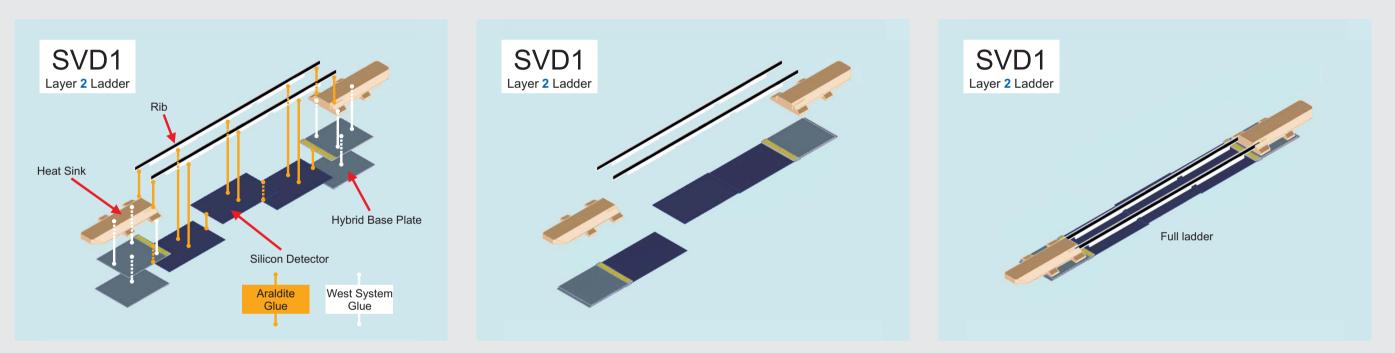


Principle of the measurement



SVD1 BELLE Ü

The first version of the Silicon Vertex Detector (SVD1) was in operation from 1999 until 2003 and performed well, delivering excellent physics results.





Unfortunately, radiation levels were higher than expected, so SVD1 suffered from radiation damage and had to be repaired/improved several times before it was finally upgraded to SVD2.

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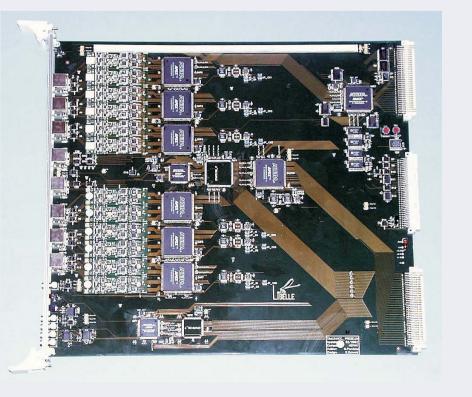
Steps of SVD1 ladder assembly performed at KEK and in Melbourne

Presented to the Electro- nics-2 group at HEPHY Vienna by J.Haba, then leader of the Belle SVD group.	The original poster contains a real SVD1 ladder here. Yes, it is a 3D poster :-) Unfortunately, this cannot be shown in a PDF	One of the first layer ladders of S V D 1 w h i c h actually measured the CP asymmetry of B-meson system for the first time in the human history.
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PRESENT: SVD2 뿓

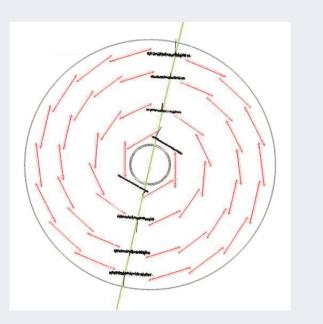


Completed SVD2 structure



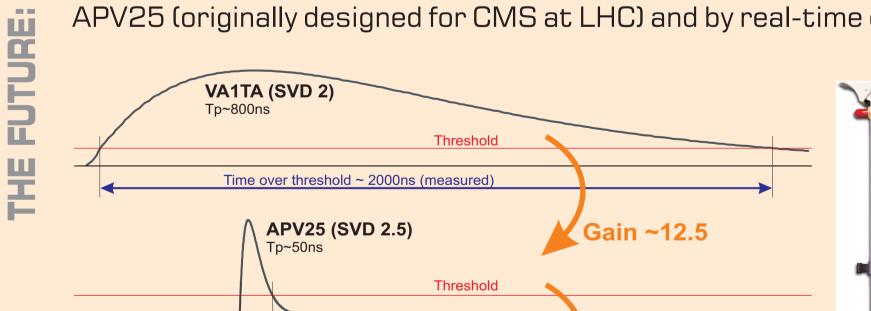
The SVD2 has many improvements compared to its predecessor and was installed in 2003.

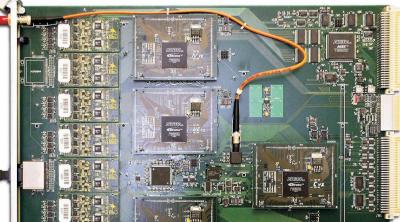
All weaknesses of the SVD1 were successfully cured and an additional (fourth) layer was added, thus improving the impact parameter resolution.



Currently, the innermost layer of the SVD2 has about 10% occupancy, which will increase together with luminosity, deteriorating the tracking accuracy. Moreover, the fraction of dead-time will grow as well.

SVD 2 These issues will be solved by replacing the front-end readout chip (SVD2: VA1TA) with the fast, pipelined APV25 (originally designed for CMS at LHC) and by real-time data processing using FPGAs.





data (20ns Prototype of an FADC with FPGA data processors

> The new SVD2.5 readout will be implemented in parallel to the existing one.

New SVD2.5 DAQ

L1-L2 ladders

APV25

APV25

repeater

FADC w/ Spars

Control

GDL

Existing SVD2 DAG

L3-L4 ladders

VA1TA

VA1TA

repeater

FADC

PC farm

L0T

FADCTF module (VME 9U)



FADCTFs in operation in Belle

Cosmic event

The FADCTF modules digitize the analog data from the front-end, extract the first-level trigger information using combinatorics between layers in both rz and $r\phi$ projections and present binary hit data to the L1.5 trigger.

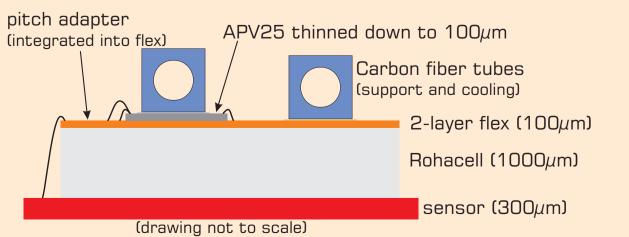
These 9U VME modules were designed and built by HEPHY Vienna. 36 units are in operation in the Belle experiment at KEK.



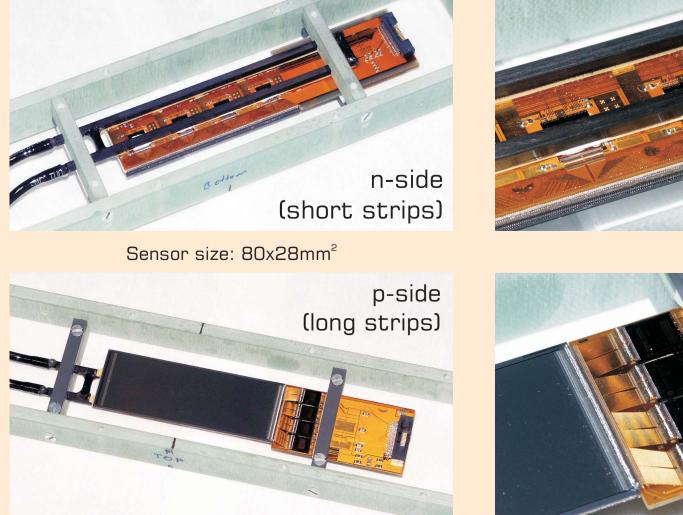


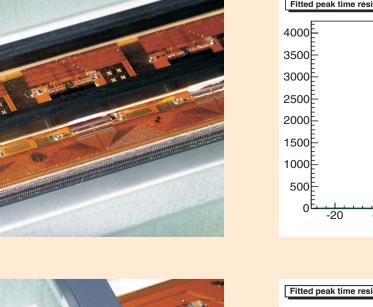
A time resolution of 2.3 and 4.0 ns was measured with the module shown below for n and p sides, respectively, at a cluster S/N of 14 and 19.

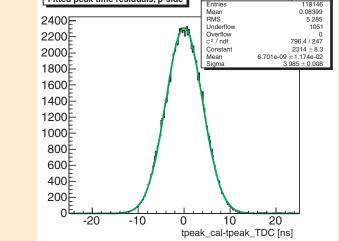




In order to achieve good S/N (i.e. low capacitance) we mounted APV25 chips directly on the detector using a 2-layer flex "hybrid" circuit and Rohacell for insulation. The APV25 chips are thinned to 100μ m to minimize the radiation length budget.







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