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Electronics Contributions to the Belle Silicon Vertex Detector by HEPHY Vienna

The Belle experiment at KEK (Tsukuba, Japan) studies CP violation in B meson decays by measuring the sides and angles of the unitarity triangle. Some of these measurements require the reconstruction of the vertices of the two decaying B mesons in an Y(4S) event, making the Silicon Vertex Detector (SVD) a critical device for the experiment.

The initial SVD1 was in operation from 1999 until 2003, suffering from radiation levels beyond expectation. The current SVD2, installed in 2003, introduced several improvements, like radiation tolerance and a higher accuracy due to an additional fourth layer. Over the years, the occupancy levels grew along with luminosity especially in the innermost layer (10%), compromising tracking precision and data acquisition throughput. This leads to another upgrade called SVD2.5, where the two inner layers will be equipped with faster and dead-time-free front-end amplifiers.

The Electronics-2 group at HEPHY Vienna designed and built the SVD2 FADC VME modules which digitize the analog data from the front-end, extract the first-level trigger using combinatorics between layers and present binary hit data to the L1.5 trigger electronics. Due to our experience from CMS, we suggested the APV25 front-end chip for the SVD2.5 upgrade and built several prototype systems including various front-end modules, repeaters, VME controllers and FADCs with hardware data processors performing pedestal subtraction, common mode correction and zero suppression within FPGAs. Moreover, multiple samples along the shaping curve of the APV25 can be used to reconstruct the particle timing with a precision of a few nanoseconds, which will also be implemented in FPGA firmware using look-up tables, in order to reject off-time hits and thus eliminate the occupancy problem. Finally, we try to optimize the signal-to-noise ratio of the front-end detector module, using SVD2.5 sensors and the APV25 front-end chip.

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