R & D of a monolithic pixel sensor based on 0.15 μm fully depleted SOI technology

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Abstract

The R&D of a monolithic pixel detector based on a commercially available 150 nm fully-depleted SOI (silicon on insulator) CMOS technology started in 2005. The substrate of the SOI wafer is used as a radiation sensor and the signal is processed in the CMOS circuit above the oxide layer. This paper summarizes the design details of typical TEG (test element group) chips and their test results.

Key words: Monolithic pixel sensor, SOI CMOS technology, Particle detection
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1. Introduction

SOI (silicon on insulator) is a technology that fabricates CMOS circuitry atop a silicon-oxide layer (buried oxide, BOX) over a silicon wafer. As each transistor is isolated from the substrate, the circuit has smaller parasitic capacitance than a normal (bulk) CMOS LSI device, enabling faster and lower-power operation. Such an SOI device is latch-up free and less sensitive to single-event phenomena in accelerator and space environments. If we adopt a high-resistivity silicon wafer and the signal induced in the sub-

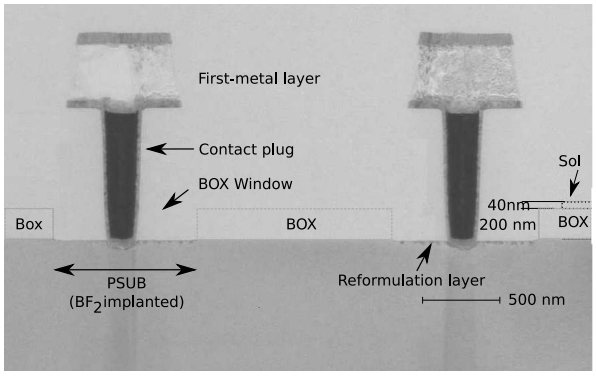

Fig. 1. Cross section of the p^+ implant and the signal contact. A typical MOSFET is also shown. Borders of BOX and SOI are emphasized with dotted lines.

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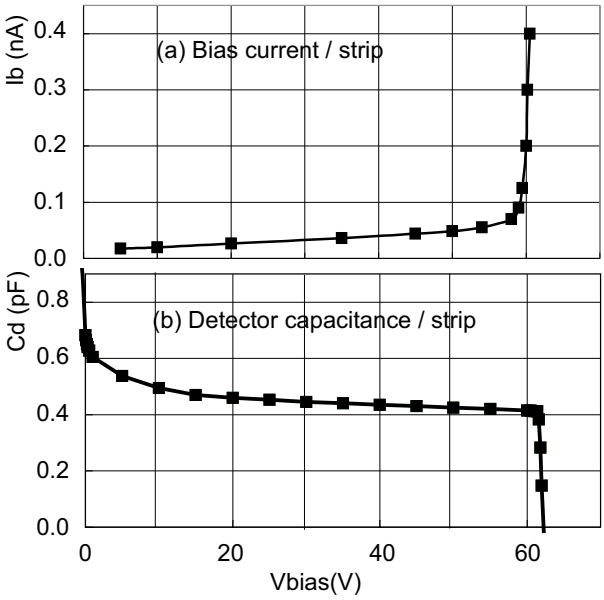

Fig. 2. The I-V and C-V curves of the strip-type TEG.

strate can be processed by the CMOS circuit, such a device can be used as a radiation sensor. Pioneering work on this concept has been done by the SUCIMA [1] project, however, the process used is not compatible with commercial CMOS technology. The monolithic-pixel detector group of KEK DTP [2] selected the 150 nm fully-depleted (FD) SOI CMOS technology of OKI Electric Co. Ltd. [3] for this purpose. The merit of collaborating with an LSI foundry is that the up-to-date technologies can be utilized in the device design.

The SOI wafers [4] are made from 650 μm thick, n-type FZ silicon (700 Ω·cm). The wafer is thinned to 350 μm after CMOS processing. The thickness of the BOX layer is 200 nm. MOSFETs are fabricated on 40-nm thick Cz crystal and with a 2.5-nm thick gate oxide. Five metal layers accommodate the complex CMOS circuits. The SOI silicon is fully depleted at low gate voltage, which also permits low-power operation. Fig.1 is a SEM picture of the substrate contact. An area shown as 'BOX window' is etched out and ion implantation done. Then the area is filled with SiO_2 layer. The contact to the implant is made later by the via holes and metal plugs.

2. Evaluation of test element group chips

Several test element group (TEG) chips were submitted to OKI in 2005. The 'circuit TEG' consists of high-sensitivity preamplifiers and time-over-threshold circuits [5]. As the low-threshold FD CMOS circuit has not been widely used, this trial is important to develop analog circuits with large dynamic range. The circuits work well. Minor errors in the circuit design are understood and will be fixed in the 2006 submission. 'Radiation TEG' is an array of MOSFETs with various design parameters. Several chips were irradiated in a proton beam and radiation tolerance

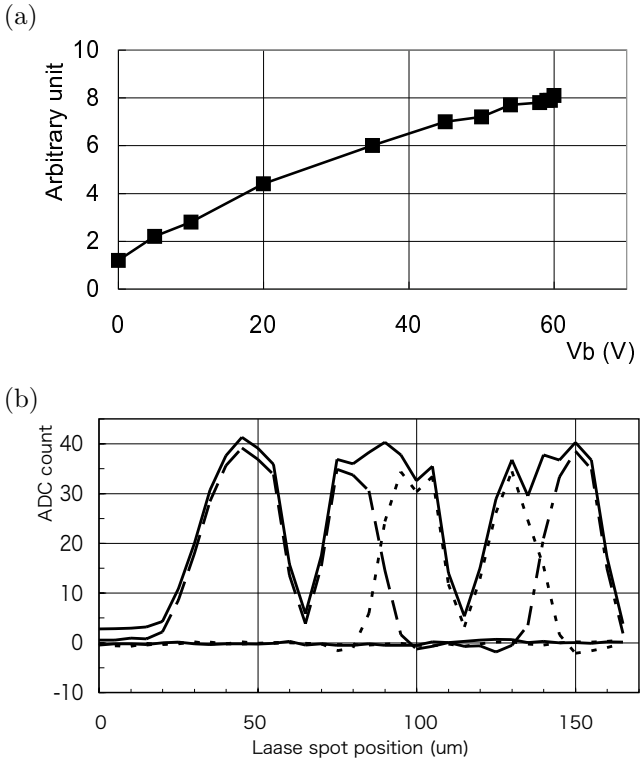

Fig. 3. Response of the strip-type TEG to a laser light. (a) The output charge as a function of the bias voltage. (b) The result of a laser-position scan. The dashed, dotted and dot-dashed lines correspond to charge from the first 3 readout channels. The solid line shows the total charge.

has been measured [6]. Another TEG is designed for use in a Compton X-ray polarimeter in space [7].

2.1. *Strip-type structure*

In order to measure the basic characteristics of the substrate, a strip-detector TEG was fabricated. The chip consists of p-type implants (460 μm long and 10 μm width) on a 50 μm pitch. The I-V and C-V curves are shown in Figs.2(a) and (b). The observed breakdown voltage, 60 V, is lower than the expected full depletion voltage ($\sim$ 200 V). Observation with an infrared camera revealed that discharge takes place at the square edges of the strip. The C-V curve is consistent with the strip area and the resistivity of the substrate.

The sensor is tested with a pulsed IR laser (λ=970 nm). Charge collected by a strip is amplified with a charge sensitive amplifier and the output voltage is plotted as a function of the bias voltage (Fig.3(a)). The curve is not saturated at the breakdown voltage as the substrate is not fully depleted. The TEG is then assembled with an APV25 readout system [8,9]. A laser spot is scanned across the strips and the charge induced in each strip is recorded. As shown in Fig.3(b), charge sharing by strips around the laser spot position is reasonable. The dips correspond to shadowing by the metal traces.

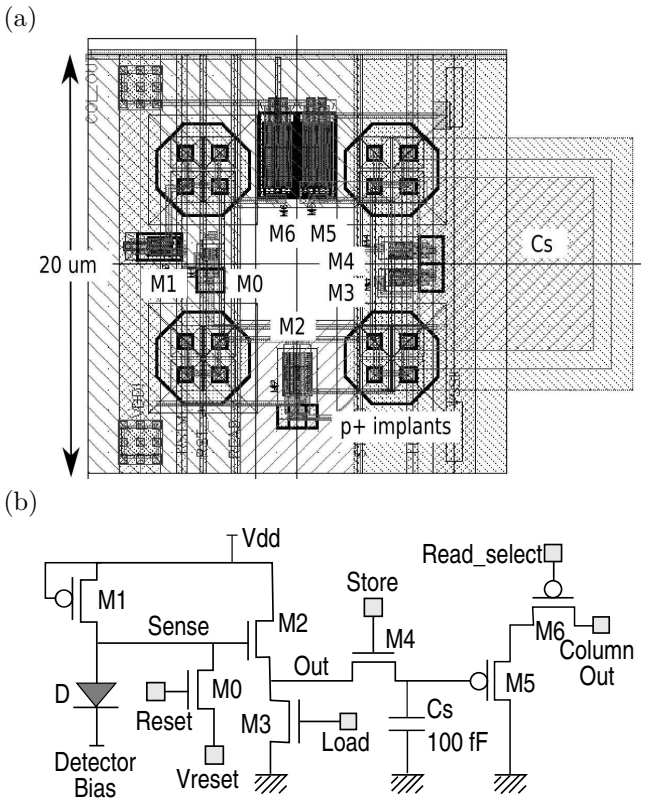

Fig. 4. (a) Layout of a pixel. (b) Circuit schematic within each pixel.

2.2. *Pixel-type structure*

A 32×32 matrix of 20×20 μm^2 pixels is designed to examine the potential of the SOI device as a radiation sensor [10]. Figs. 4 (a) and (b) show the detail of each pixel. Charges produced in the substrate are collected by four octagonal shape $4{\times}4$ μm^2 p-type implants. The breakdown voltage of the p-n junction is about 100 V, however, the test is done at 10 V bias voltage because of the back-gate effect, described later. Fig. 5(a) shows an image obtained with a 670 nm laser and a photo mask. Several channels are insensitive to light or saturated without light. The mechanism of such failures is under investigation. Fig. 5(b) shows the response of a pixel channel to a β-ray source (^{90}Sr). The size of the voltage step is consistent with the expected depletion depth (44 μm) and the detector capacitance (8 fF).

3. Back-gate effect and TCAD simulation

The detector bias voltage applied to the substrate affects the operation of the SOI transistors (back-gate effect). Since this effect can be mitigated with a guard ring, a simulation study has been performed using the ENEXSS [11] TCAD (technology CAD) system. A typical n-channel SOI FET is surrounded by a p-type guard ring in the substrate at a distance, d=2, 5 and 80 μm, as shown in Fig 6(a). Then the gate threshold voltage of the FET is simulated for $0 < V_b < 100$ V. As shown in Fig. 6(b), if we allow a threshold

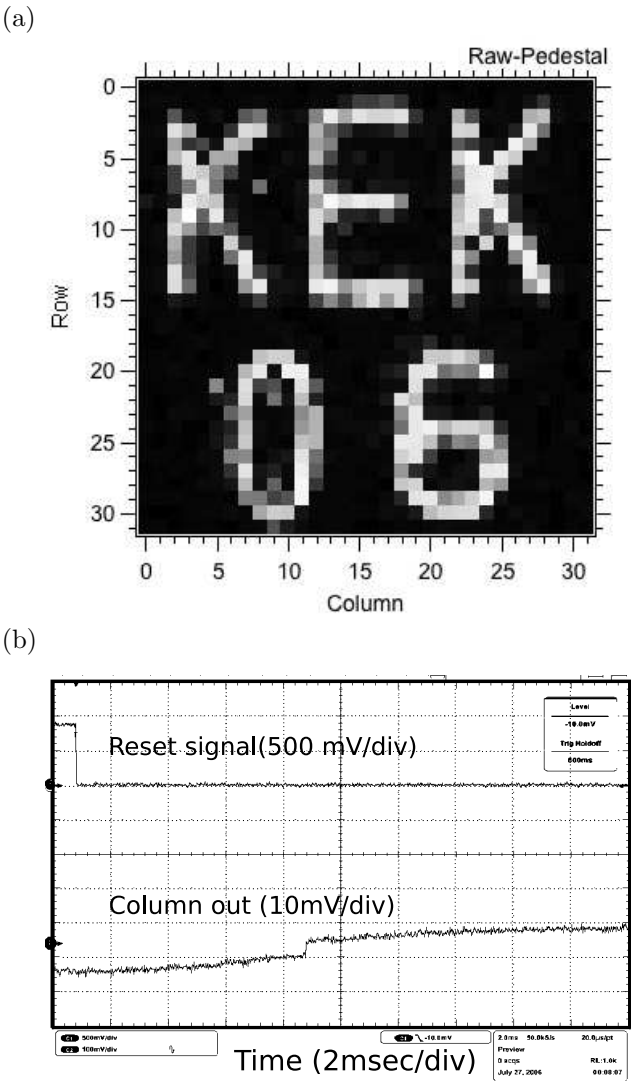

Fig. 5. (a) Image observed by the pixel sensor. A laser light (λ=670 nm) is injected to the sensor through a photomask. (b) The response of a pixel to a β source.

voltage shift of 0.1 V, a bias voltage of 90 V, 15 V and 1 V can be applied for d=2, 5 and 80 μm, respectively.

4. Summary

The R&D effort toward a pixel sensor based on 150-nm fully-depleted SOI CMOS technology started in 2005. Several TEG chips designed in 2005 are described. The 2005 TEGs demonstrate that a FD SOI device works as position sensitive detector that can detect minimum-ionizing particles. TCAD simulation shows that, with proper substrate guard rings, the SOI circuit can be operated up to 90 V substrate reverse bias voltage. The 2006 TEGs incorporate this knowledge in their design.

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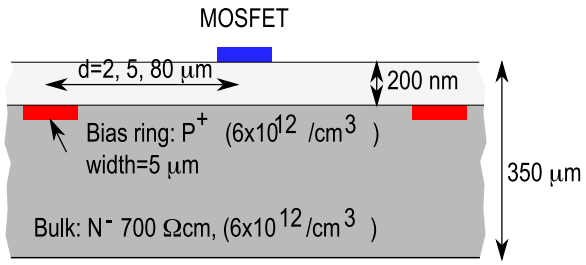
(a)



(b)

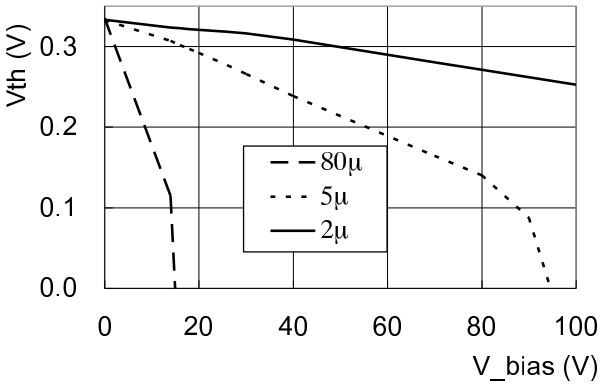


Fig. 6. (a) The geometry simulated in TCAD. (b) Result of this simulation. Solid, dotted and dashed curves correspond to MOSFET threshold voltage shifts for d=2, 5 and 80 μm, respectively.

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