High Rep-Rate CLIC Combiner Ring Kicker

SLAC/CERN Collaboration Effort

5/6/14 ALERT 2014 Workshop

Mark Kemp

U.S. DEPARTMENT OF ENERGY
Office of Science

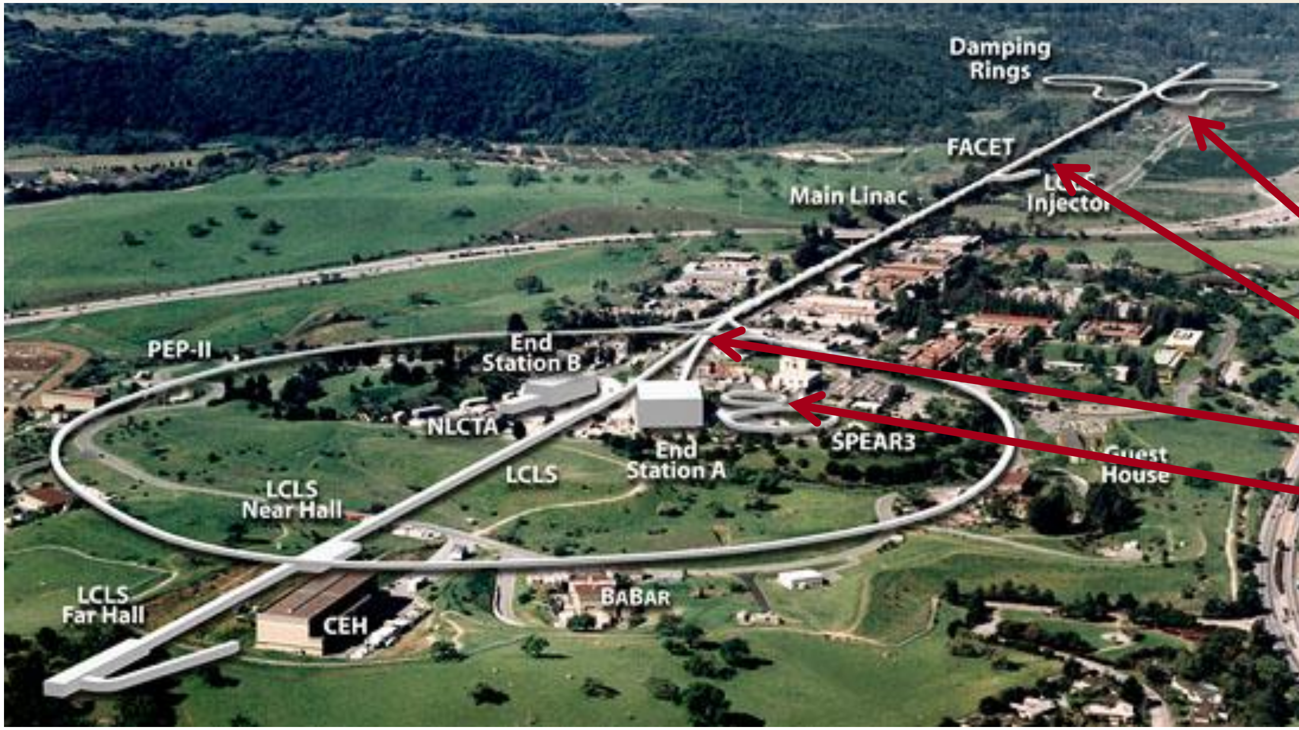
SLAC NATIONAL ACCELERATOR LABORATORY

Talk Overview

- A Bit About SLAC
- General Modulator and Kicker Discussion
- High Repetition Rate Kicker for CLIC Combing Ring
  - Kicker specifications and SLAC involvement
  - Description of general approach
  - Experimental results
  - *Note:* Talk is focused on kicker driver rather than kicker structure itself

- *March 26, 2014* Mark invited to present results at ALERT
- *March 31, 2014* Mark starts experimental work on kicker
- *May 6, 2014* Talk at ALERT on our work

SLAC Overview



Operating Kicker Systems

- Klystron gallery contains 240 RF stations
  - **Now:**
    - 1/3 to LCLS, 2/3 to FACET
  - **Future:**
    - 1/3 to LCLS I
    - 1/3 to LCLS II -> CW; super conducting

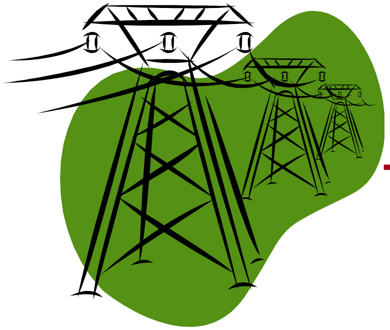
SLAC Overview- HPRF Infrastructure and Expertise

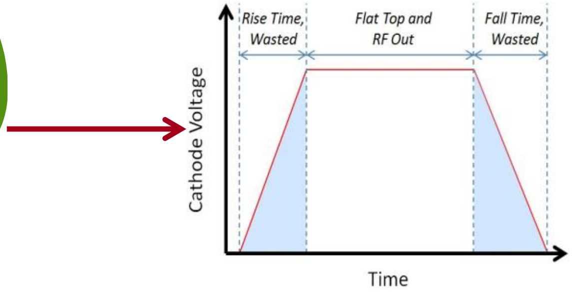
SLAC

About SLAC- Power Electronics R&D

Pulsed Power- What is it?

- Pulsed power is the technology to convert AC mains to high-power pulses





- Pulsed power R&D:
    - High Voltage/Dielectrics
    - Topologies/system integration
    - Magnetics
    - *Switching*

- Modern modulator development challenges primarily are pulse stability, efficiency, and handling component obsolescence

- Kicker development challenges are as varied as the applications

Power Conversion Systems

SLAC

- (My commentary… take with a grain of salt)

- Development on *accelerator* power conversion systems:
  - Power supplies and controls
    - Mostly commoditized. Most engineering is systems integration
  - High power RF modulators (pulsed power)
    - Many applications are commoditized. However, some challenges remain
  - Kicker systems (pulsed power)
    - Nearly no commercial vendors. One-offs and is typically challenging

High Power RF and Modulators: At a Crossroads?

SLAC

- High Power RF
  - Transition from vacuum electronics to solid state is creeping higher and higher in power and frequency

- Power Electronics (Modulator and Kicker) Systems
  - “Green” energy has stimulated large growth in solid state power electronics components
  - Downward trend in vacuum and gas switch development and commercial base

My Approach to these Issue

- *First,* realize that accelerators are not the driving force in the power electronics industry

- *Second,* come to terms with a reducing supply of non solid state switches

- *Conclusion:*
  - Wherever possible, find synergy with the large body of work being done by the “green” power electronics community
  - Think hard before including a non-solid state switch in a new system

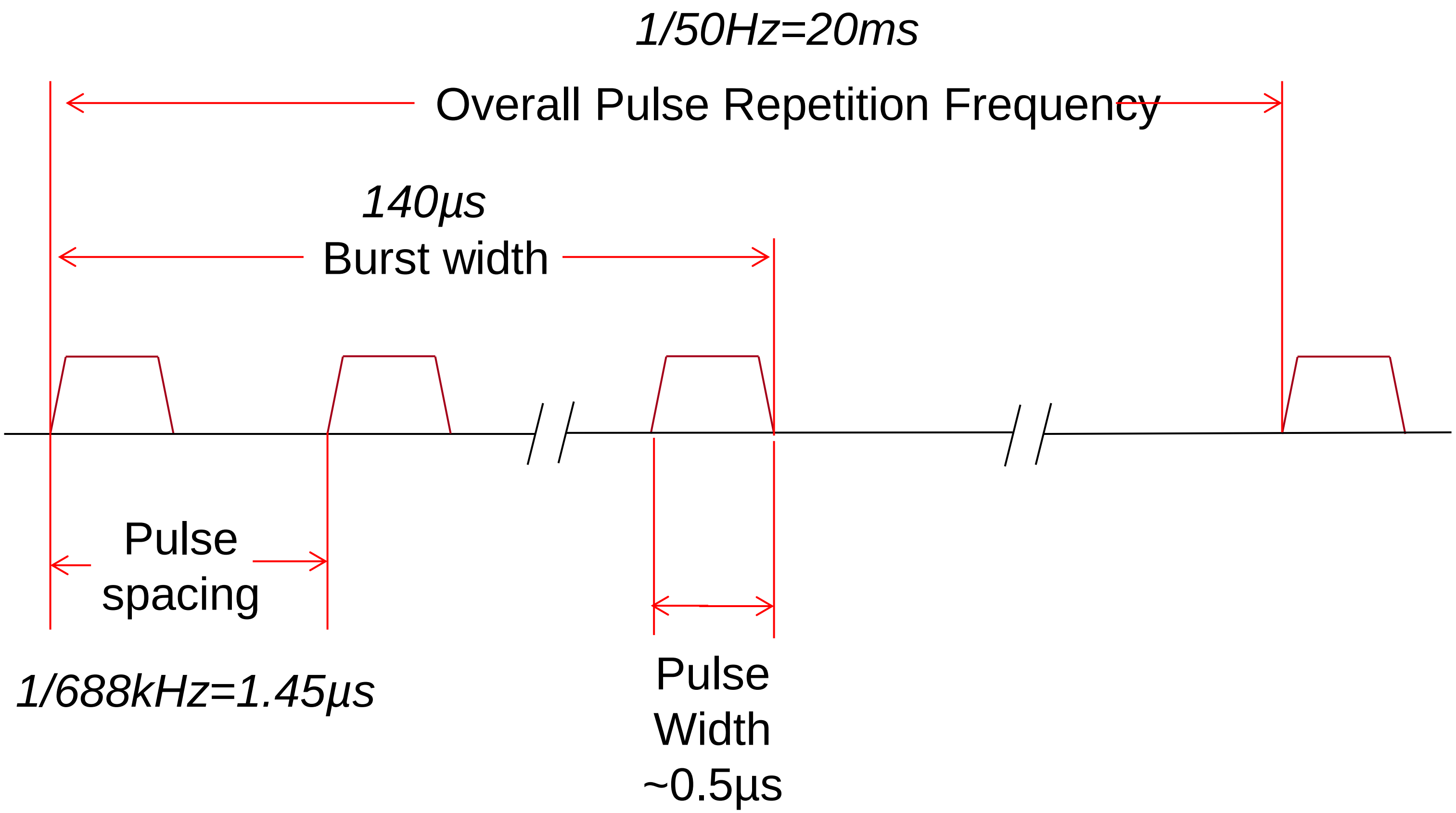
CLIC CR1 Extraction Kicker Specifications

SLAC

Pulse Voltage	10 kV
Pulse Current	200 A
Kicker Impedance	50 Ohm
Pulse Duration	245 ns (min), 450 ns (max)
Pulse to Pulse Spacing (during burst)	1.45 µs
Pulses Per Burst	96
Burst Repetition Frequency	50 Hz
Pulses per Second	50*96=4800
Pulse Reproducibility	+/-0.1%
Pulse Stability (During pulse)	+/-0.25 %
Inter Pulse Field Max	2.5% of max field

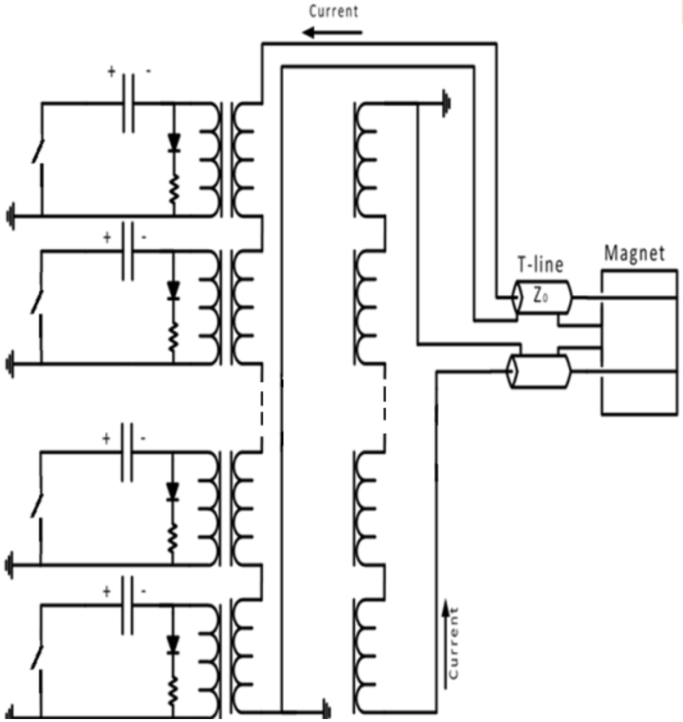
- A 3m long, 20mm separation stripline kicker is assumed
- The beam energy is 2.38 GeV and kick deflection is 2.5 mrad

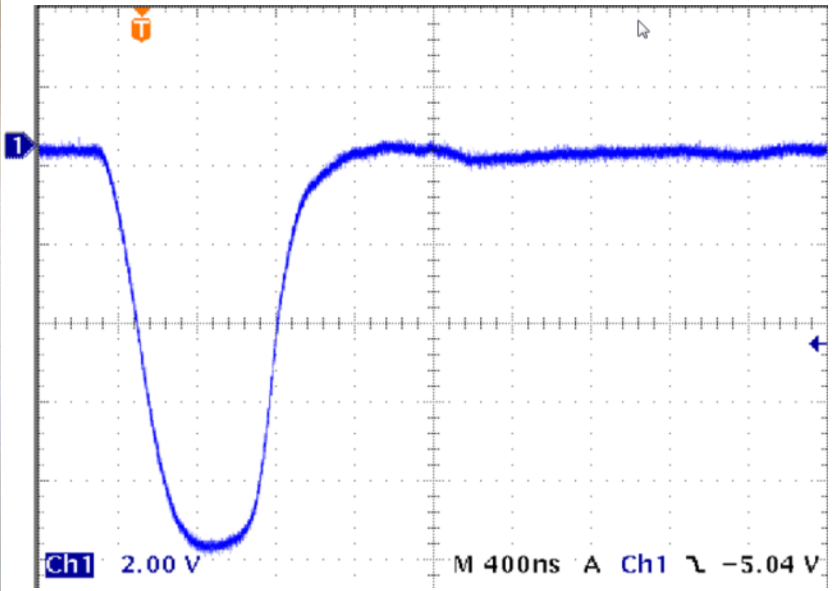
CLIC CR1 Extraction Kicker Specifications



Pulses per burst = 688kHz*140µs= ~96
Pulses per second= 96*50Hz= 4800
Duty cycle during burst= ~.5/1.5= 30%

Induction Adder Kicker Deployed @ SLAC





Current in one conductor of magnet shown (400A/div)

- Two 10-stack systems installed in 2004
- 10Hz, 20kV, Z_0=11.25Ω
- Bipolar output, IGBT driven, 2kV max on driver boards
- Magnet is an inductive short

Pappas, C., "A slotted beam pipe kicker magnet with solid state drive for SPEAR III," *Power Modulator Symposium, 2002 and 2002 High-Voltage Workshop.*

Why Is This Kicker Driver Challenging?

SLAC

- Assume a 300ns pulse with 200ns rise and 200ns fall times
- This results in about 500ns*10kV*200A=1J or 0.1mC transferred per pulse
- The energy transferred per burst is 96*1J=96J. Charge transfer is 9.6mC
- During the burst, the maximum allowable droop is 10kV*0.0025=25V
- If just a single capacitor is used to store this energy, the 10kV capacitor would need to be $96J*2/((10kV)^2 - (9.975kV)^2)$ = 384μF which would have **19.2 kJ stored energy (A LOT)**

- Depending on the pulse shape used, the duty cycle during the pulse is 30-50%. If, say, an induction adder is used, the core must either be reset in-between individual pulses, or the core must be large enough to support the whole burst
- To reset in between pulses during the burst, the reset current needed is 200A*.3/(1-.3)= 85 A. This is just about as high as the pulse current
- The total volt seconds needed is 10kV*96 pulses*500ns=0.48 V-s
- Assume a 0.5 T saturation core material, **the total core area** needed is 0.48 V-s / 0.5T = **$0.96\ m^2$ (BIG)**

Why Is This Kicker Driver Challenging?

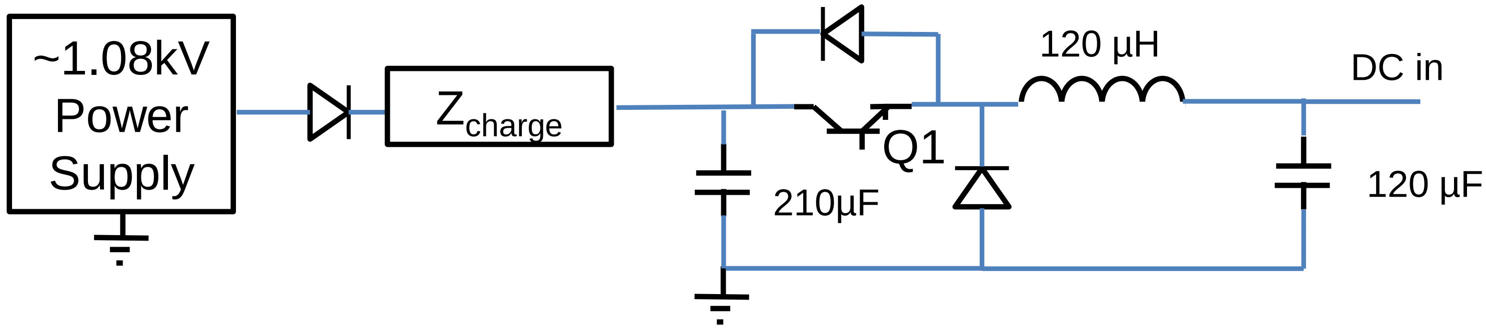
SLAC

- The flattop specification during each pulse is also difficult. However, CERN has a PhD student (J. Holma) already studying this problem

- **<u>Questions to answer at SLAC:</u>**
  - Can we produce a design to reduce the stored energy to 10% of the value calculated on the previous slide?
  - Can we produce a design to reduce the required core area to 10% of the value calculated on the previous slide?
  - Can we perform a proof-of-concept experiment validating our designs?

- *Initial Approach:* re-use as much existing hardware as reasonable. May not be ideal for the application, but should demonstrate the critical concepts

Pulse Charging Circuit During Pulse Train



- Every cell fed by a common power supply. Each cell is isolated by a charging diode and impedance

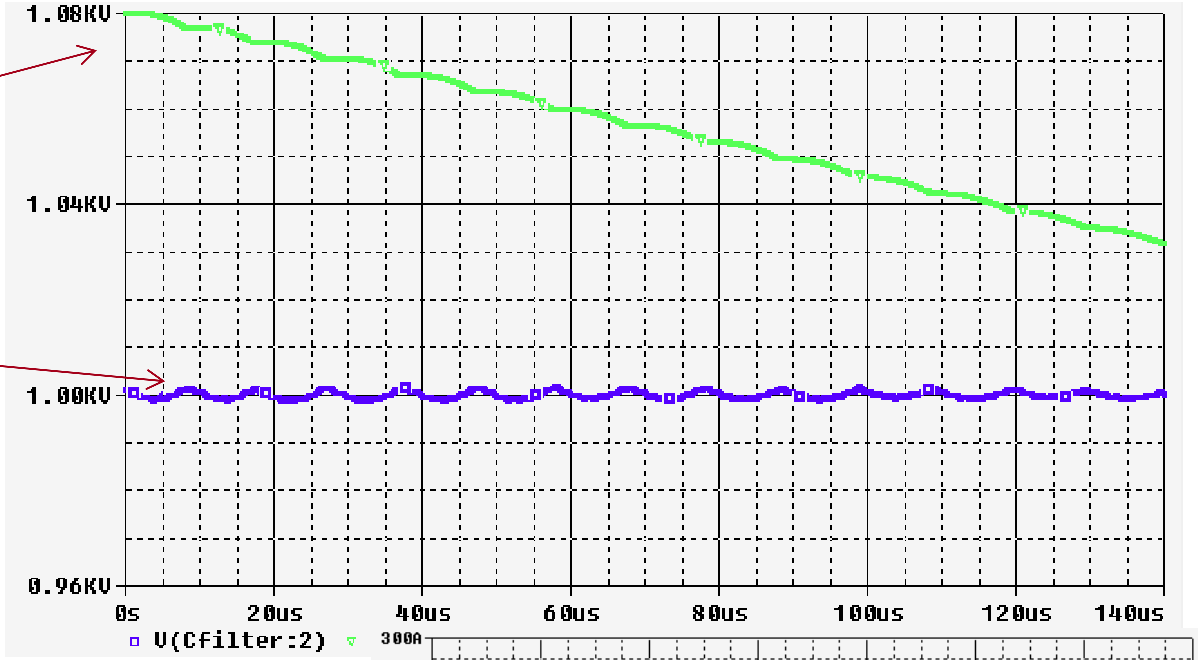
- A 100kHz chopper, Q1, transfers energy from the 210μF capacitor to the 120 μF capacitor during the burst train

- The ripple on the 120μF capacitor is kept to less than +/-2.5V

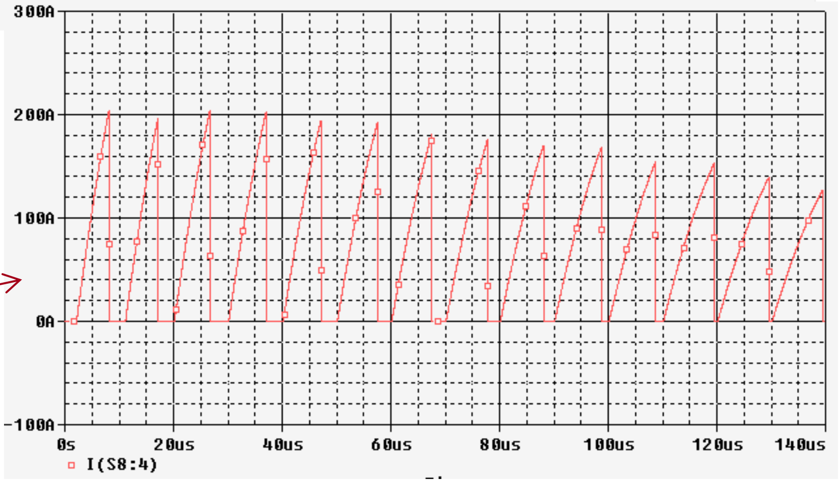
Pulse Charging Circuit During Pulse Train: Simulation

210 µF capacitor voltage

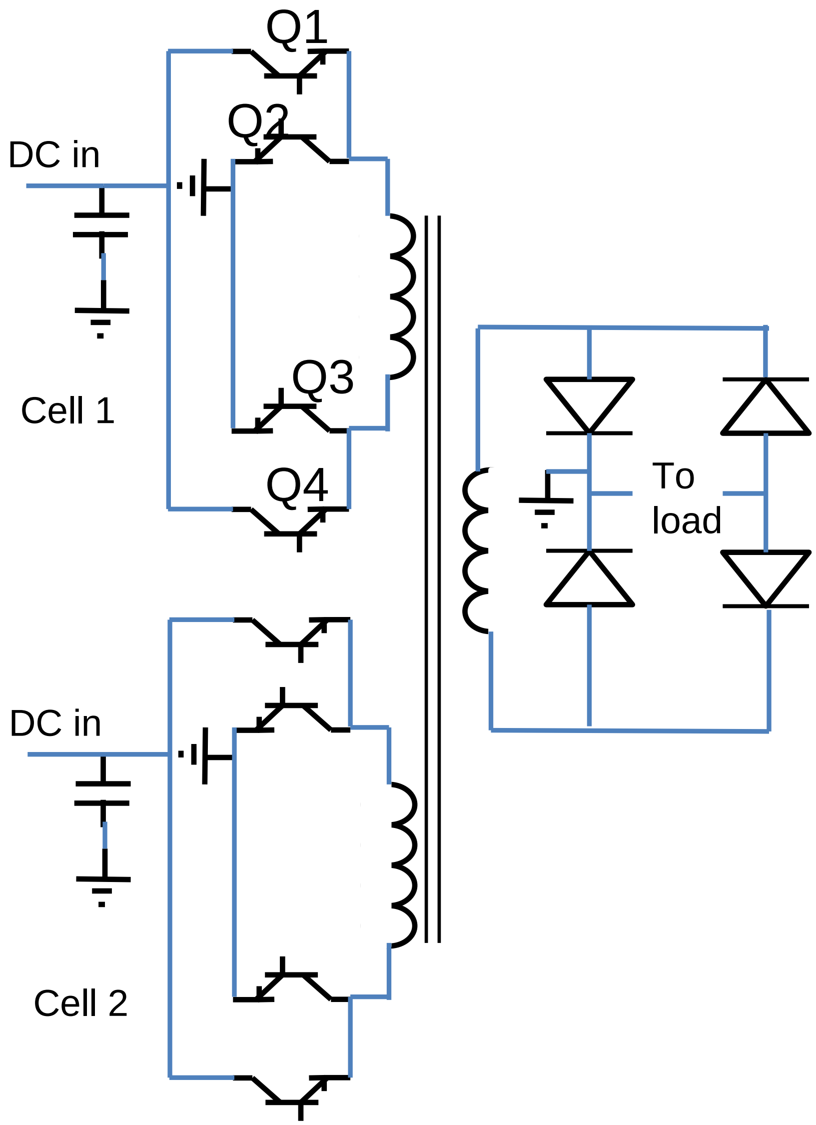
120 µF capacitor voltage



Chopper current



Burst-Mode Induction Modulator



- •A variant of the typical induction modulator topology and full bridge inverter

- •Cells produce alternating positive and negative polarity pulses, but load output is single polarity

- •Flux alternates direction in the core, enabling pulse train output

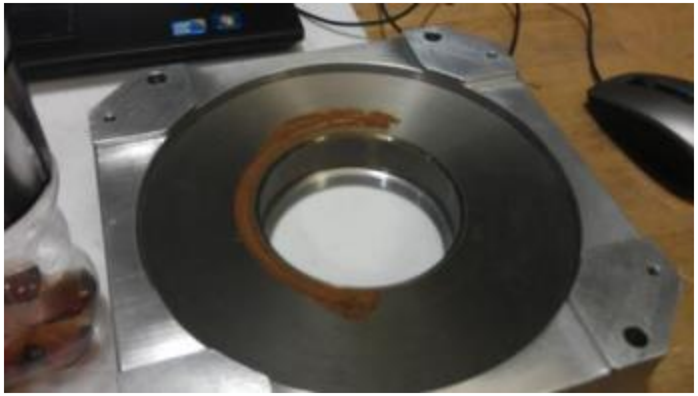
Burst-Mode Induction Modulator

- Can we produce the CLIC CR1 pulse train with this dual-polarity induction modulator?
  - The full induction modulator will be ten cells, with each cell operating at about 1kV and about 200A
  - If we construct a three-cell prototype and demonstrate the pulse shape, the conclusion will not be substantially different if we constructed the full stack.

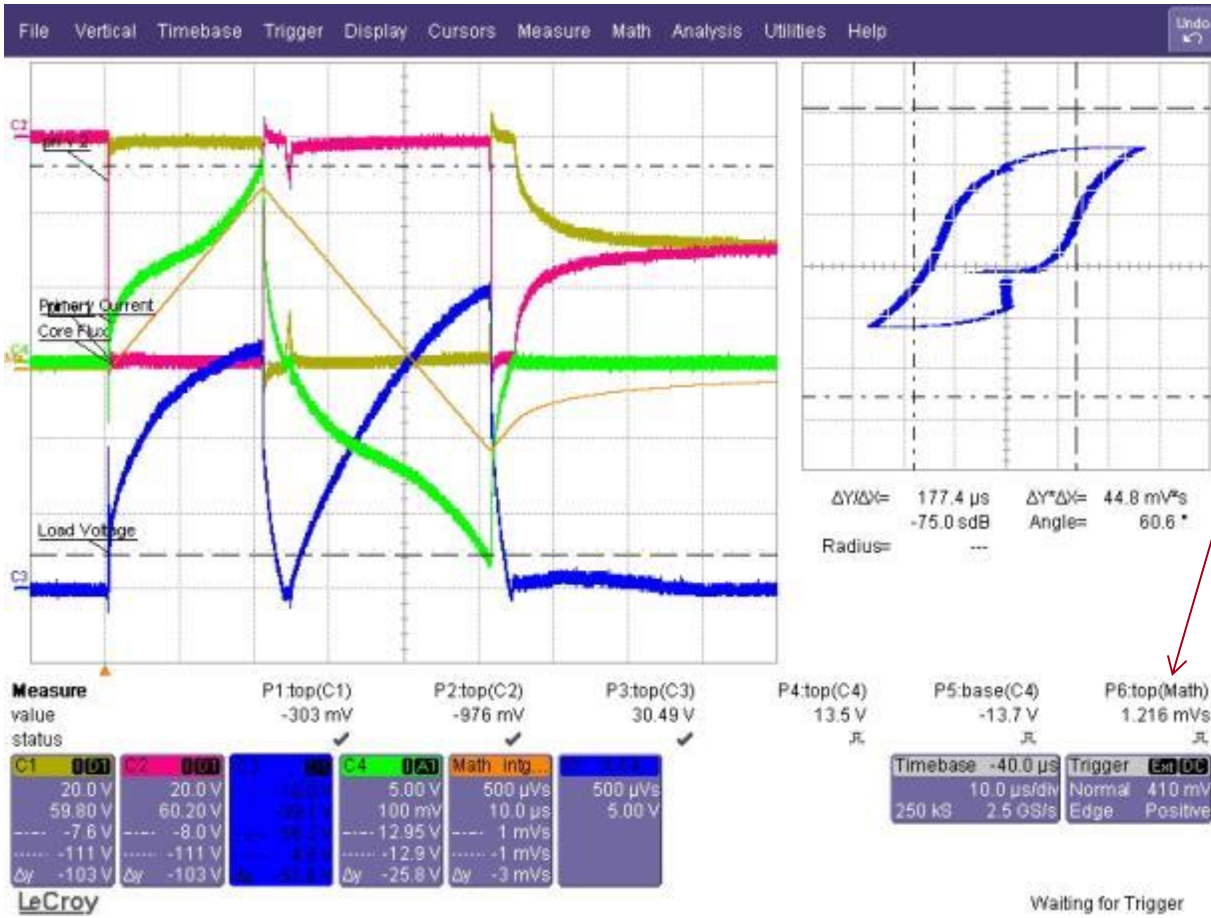
- Can we demonstrate the pulse to pulse stability specification?
  - Pulse charging circuit has been designed and mostly fabricated
  - *Future action item:* test pulse charging concept.

Components for Experimental Demonstration

- All storage capacitors are Wima 30 µF, 1.2kV film capacitors
- Switches are Infinion IGBT 1.7kV, 200A half bridges
- Cores and cases are from some unknown previous project
  - 3.875” ID
  - 8.125” OD
  - 1” Height
  - FT-1M or FT-2M Finemet tape



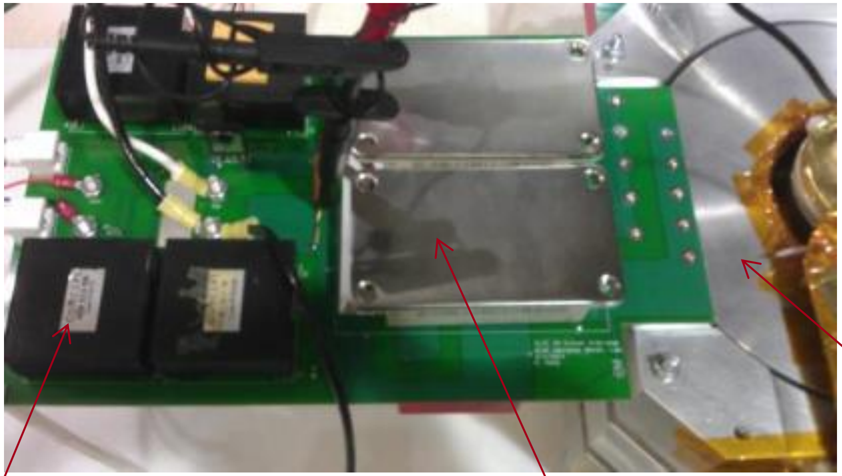
Measuring the Core Characteristics

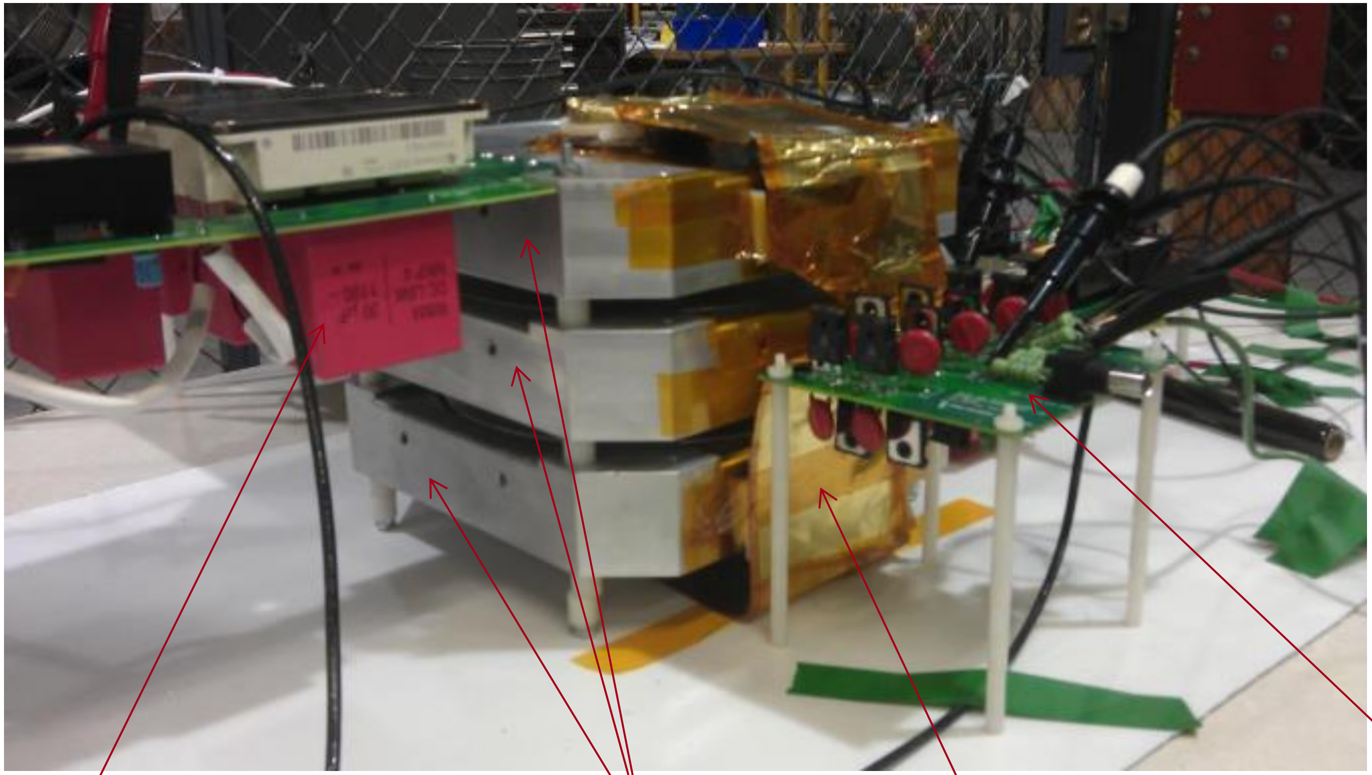


- Shown is single core
- Here, the maximum flux is 1.216 mV-s (0.087 T)
- Could likely push higher, but effects of saturation are shown
- Two cores were about the same. Third core was <0.8 mV-s

Experimental Setup

- Three induction modulator cells
- PCB construction. Bolts directly to winding
- Secondary made from pipe and brass foil shims. Insulated with Kapton tape
- Full wave rectifier on secondary with Ohmite OY array as load



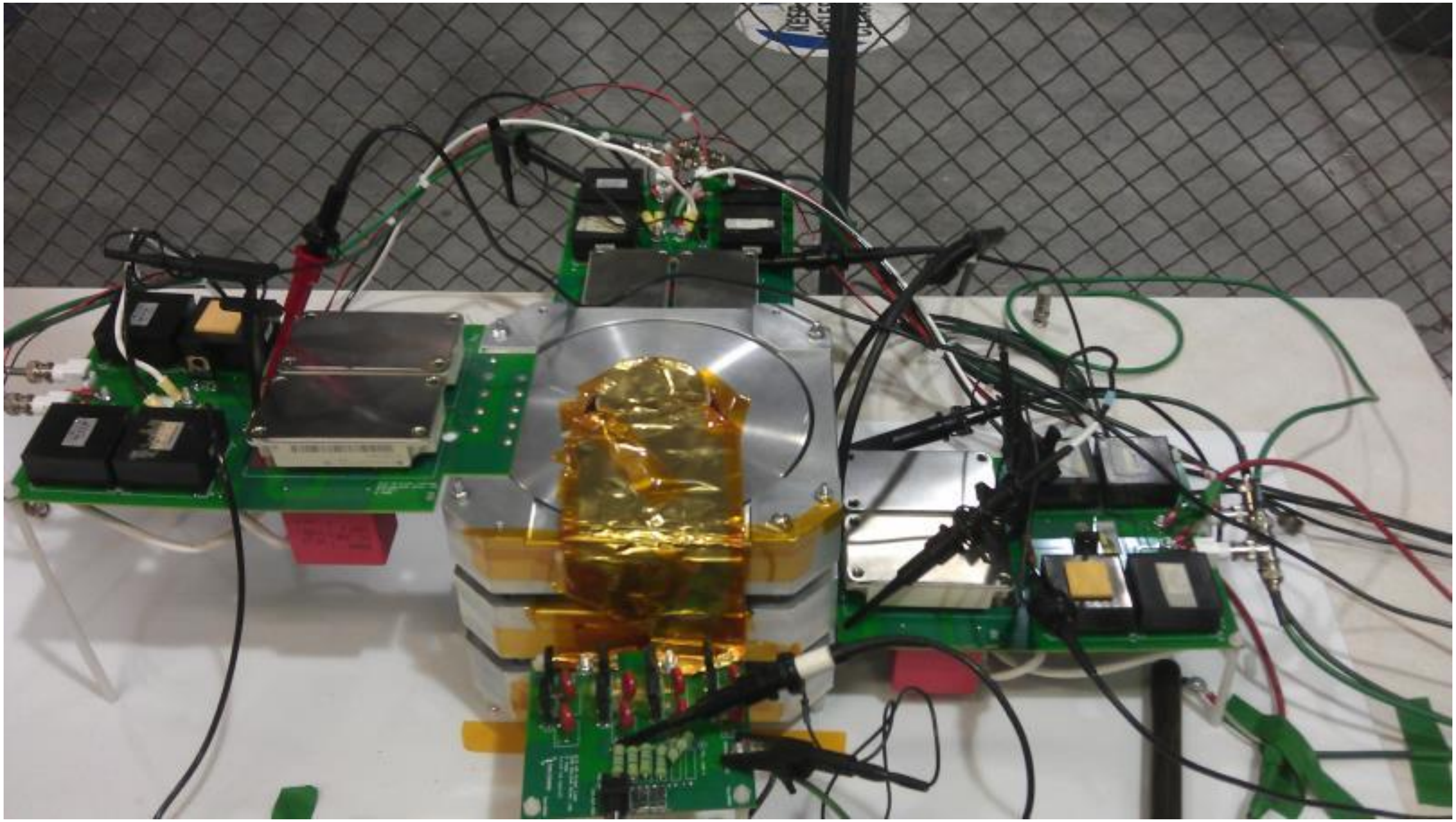


Cell storage capacitors

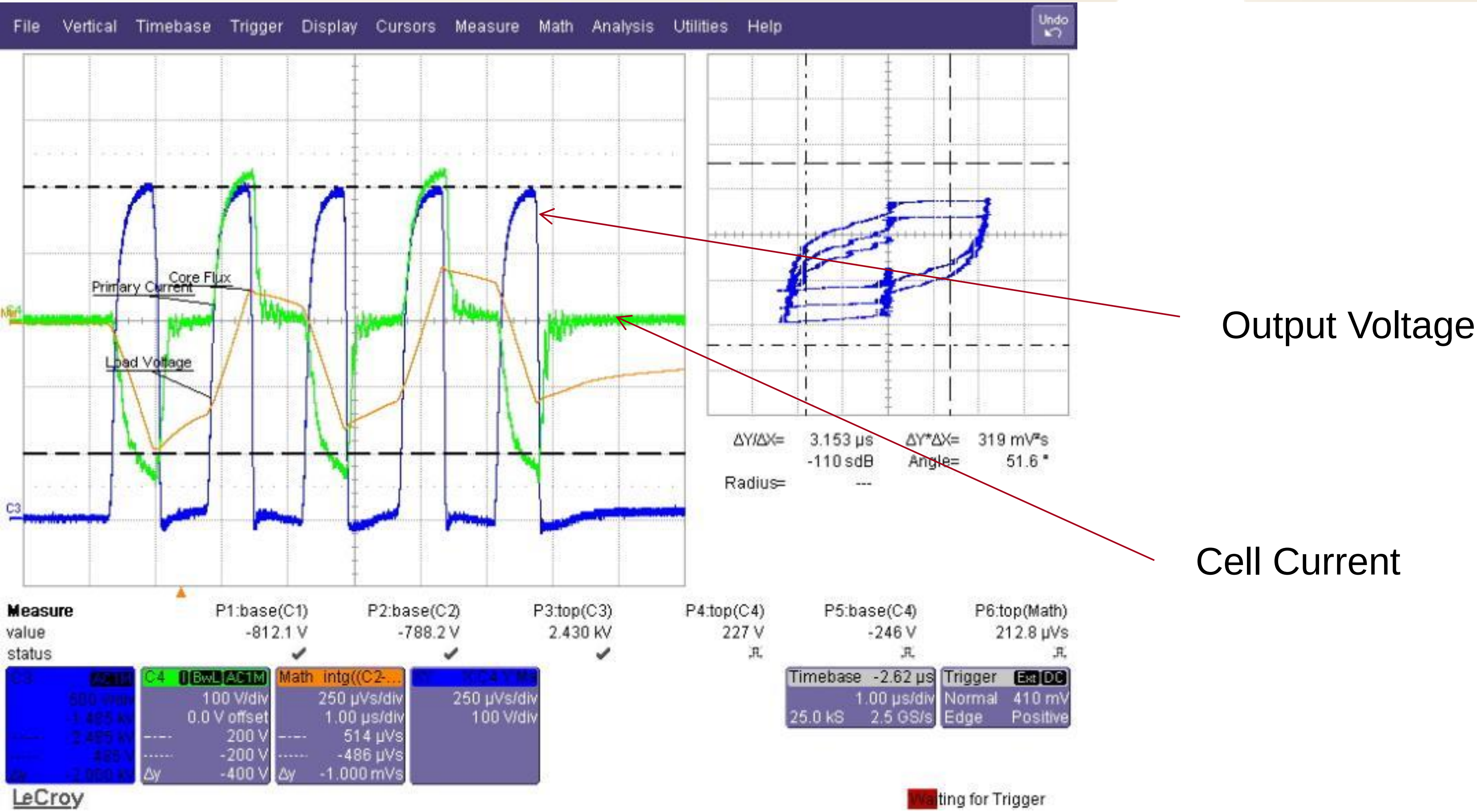
Three primary windings

Full-wave rectifier

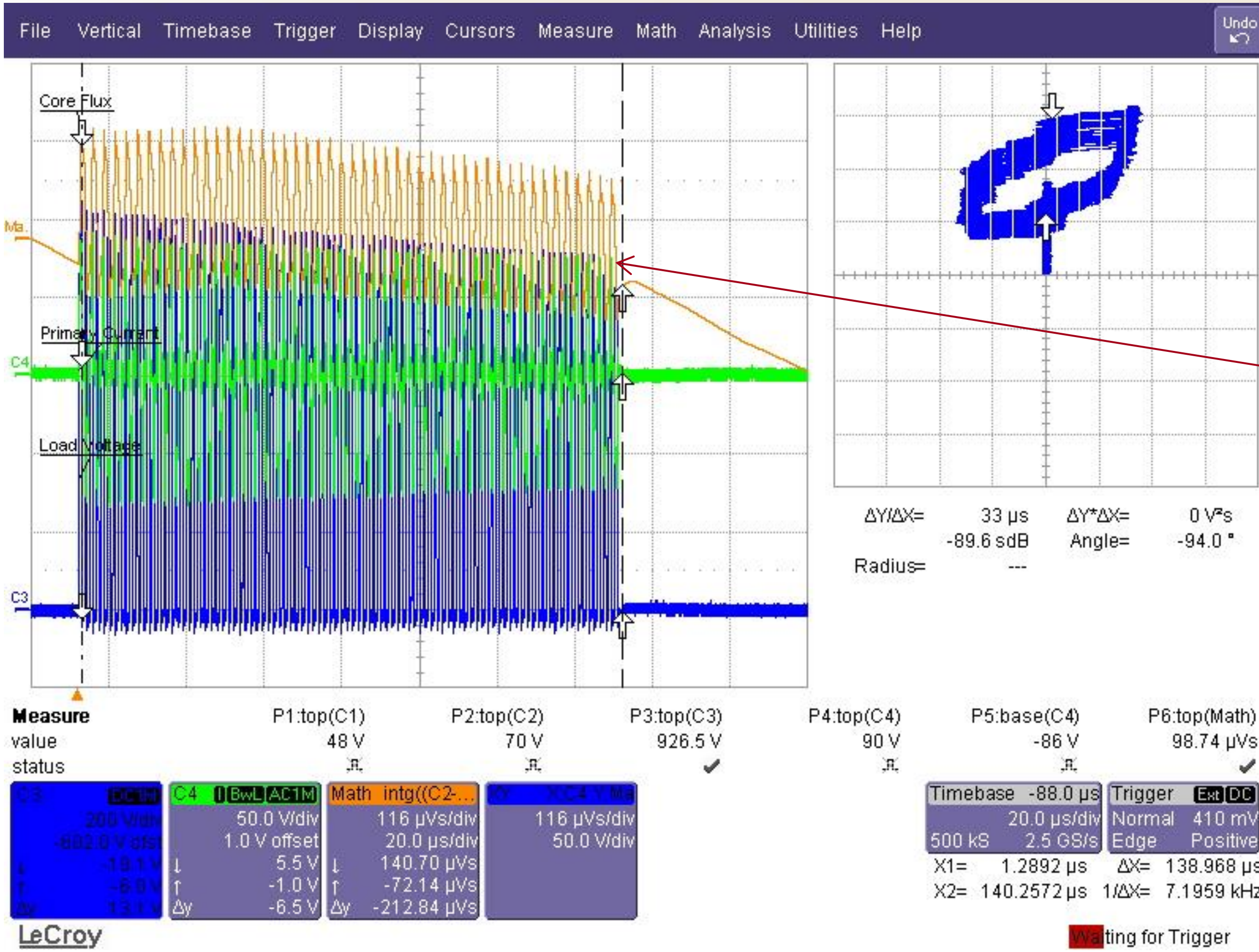
Secondary winding



Burst Mode Operation

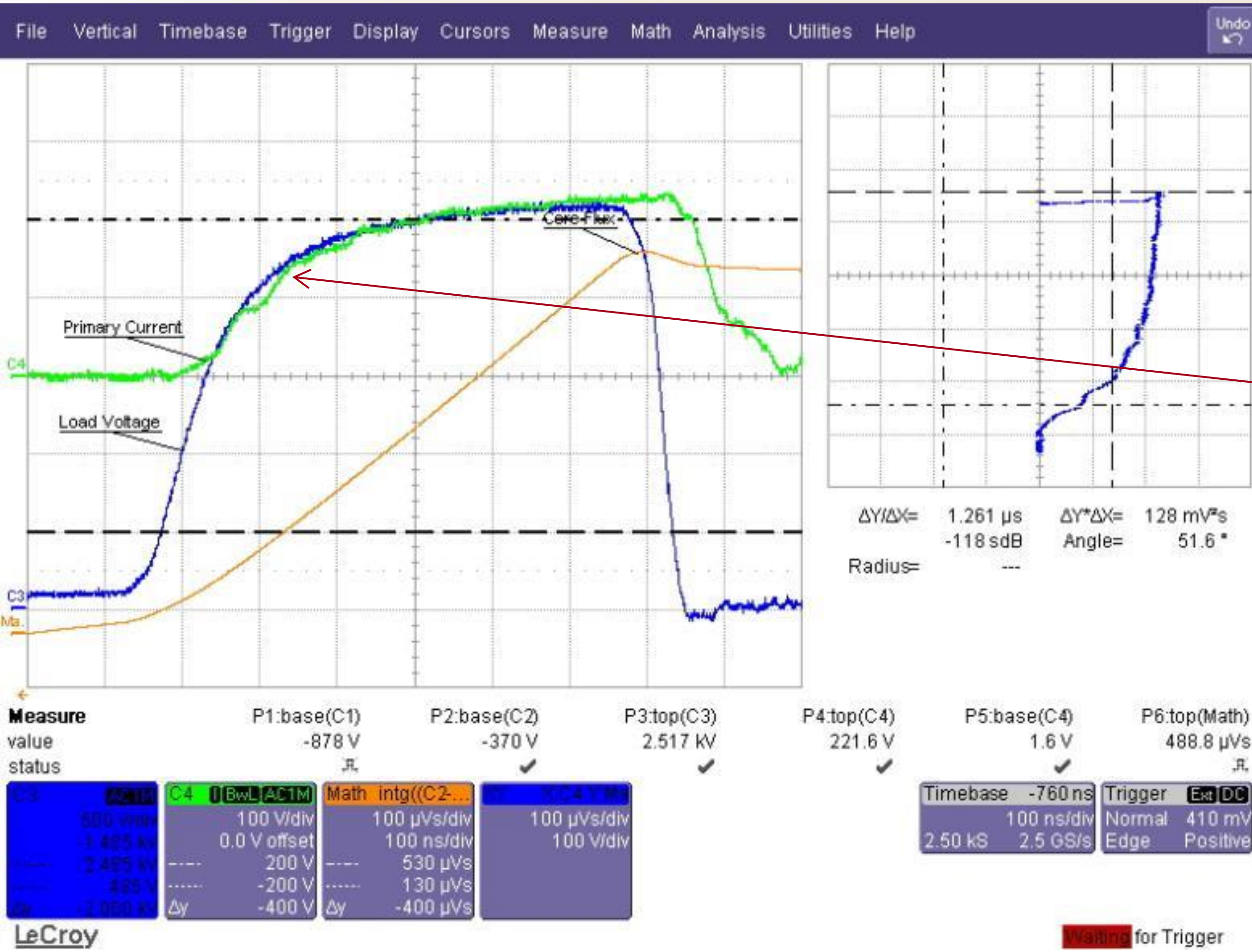


Pulse Burst Demonstration



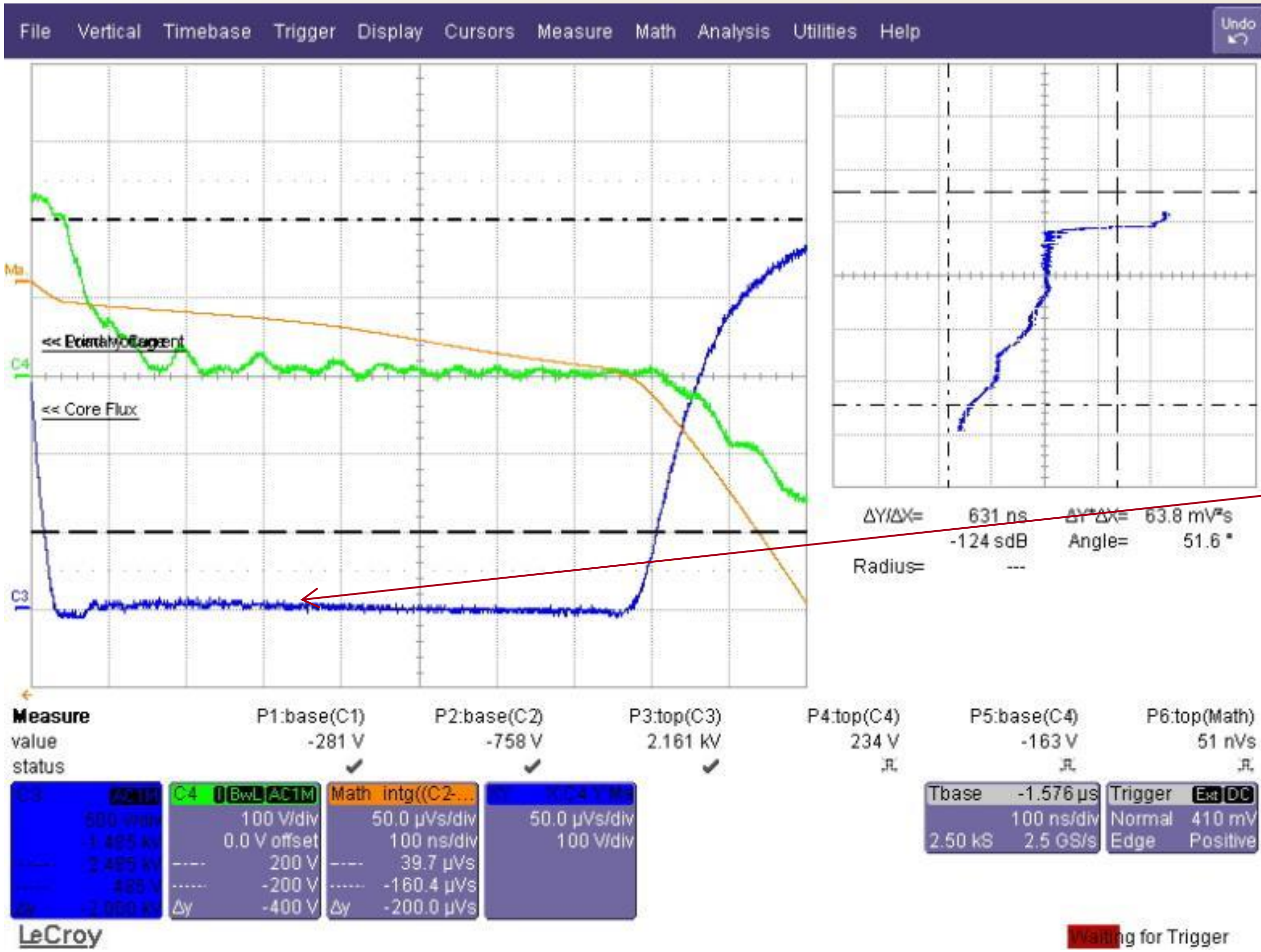
Output Voltage

Burst Mode Operation- positive cell pulse



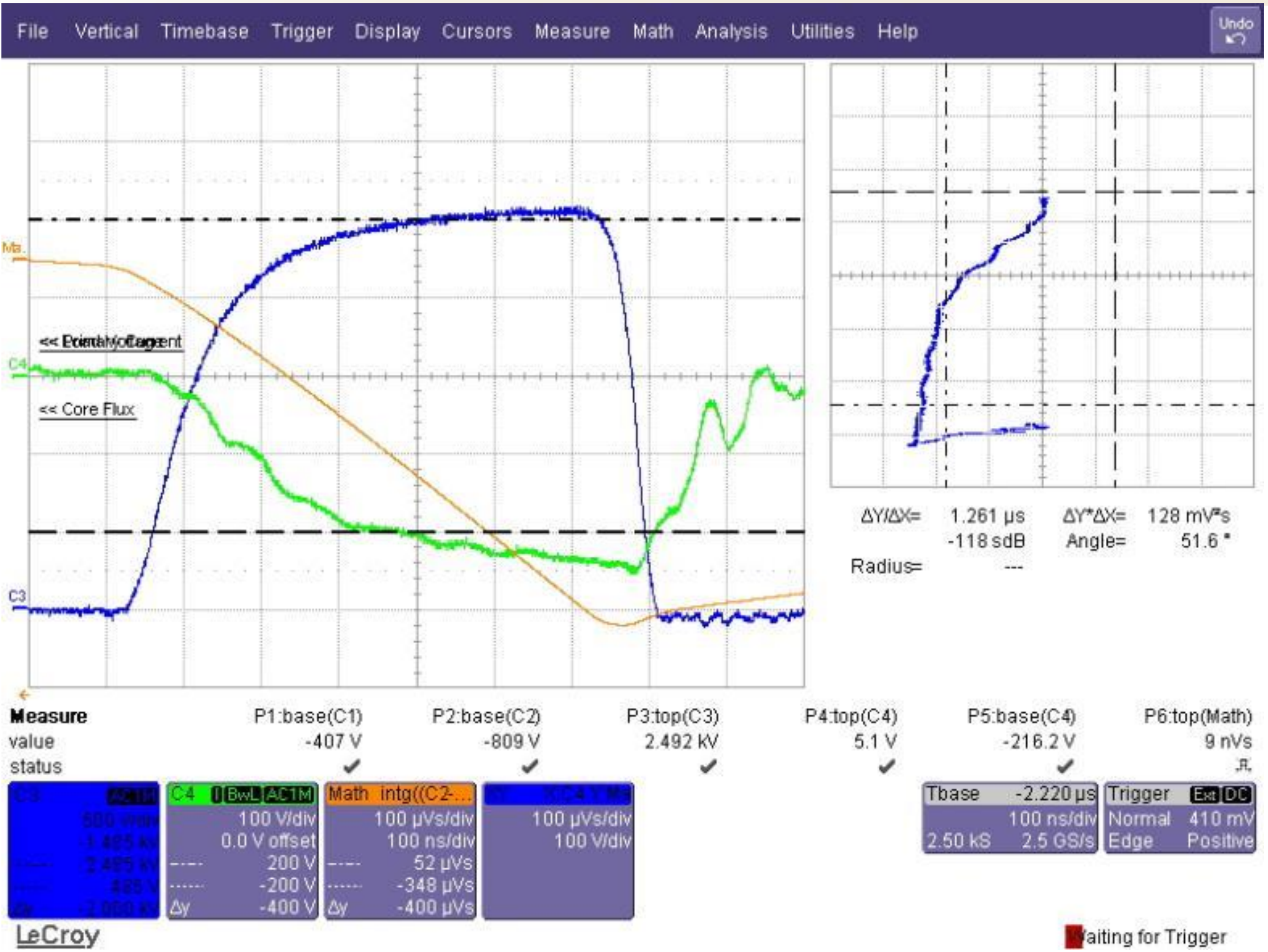
Rise time due to leakage and lead inductance

Burst Mode Operation- dead time



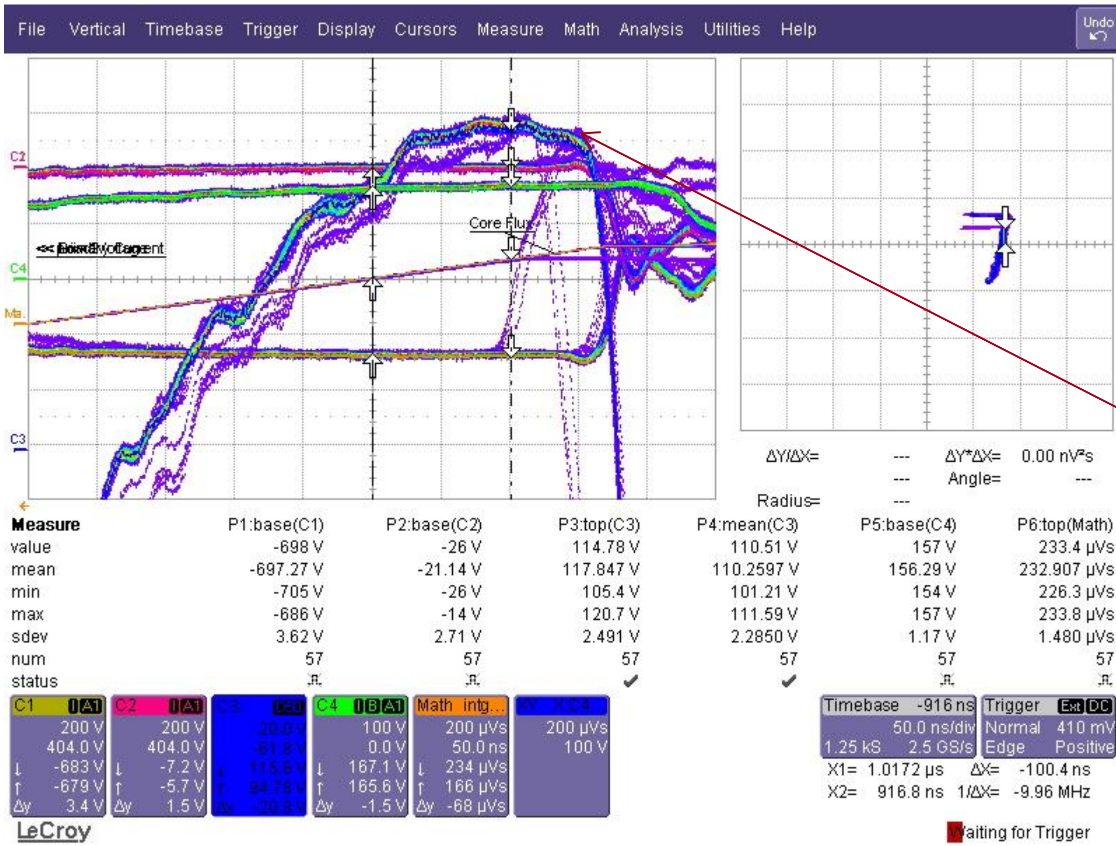
Low inter-pulse voltage

Burst Mode Operation- negative pulse



Pulse to Pulse Stability Specification

SLAC



- Zoom to top of voltage waveform
- About 1V amplitude standard deviation out of 2.5kV pulse gives about +/-0.6%
- Higher rep rate will degrade this, however effects of core won't worsen

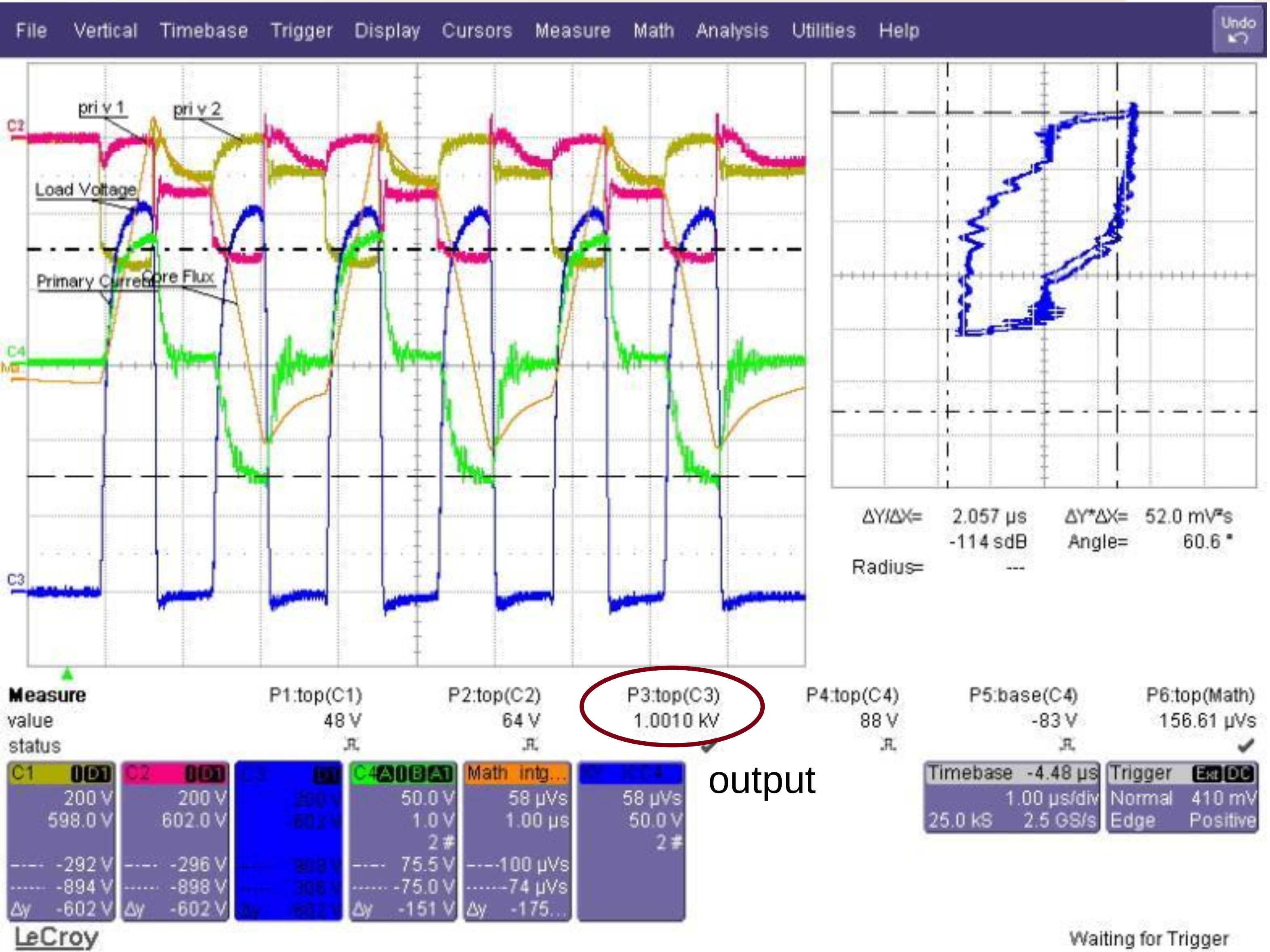
Talk Summary

- Both high power RF and pulsed power fields are presently learning how to take advantage of growing solid state device industry
- I feel within 5-10 years, we will see reliability/availability of modulators approach that of DC supplies
- On the technology side: CLIC CR1 Kicker burst rate looks doable
    - Mixture of pulsed power and traditional power electronics topologies

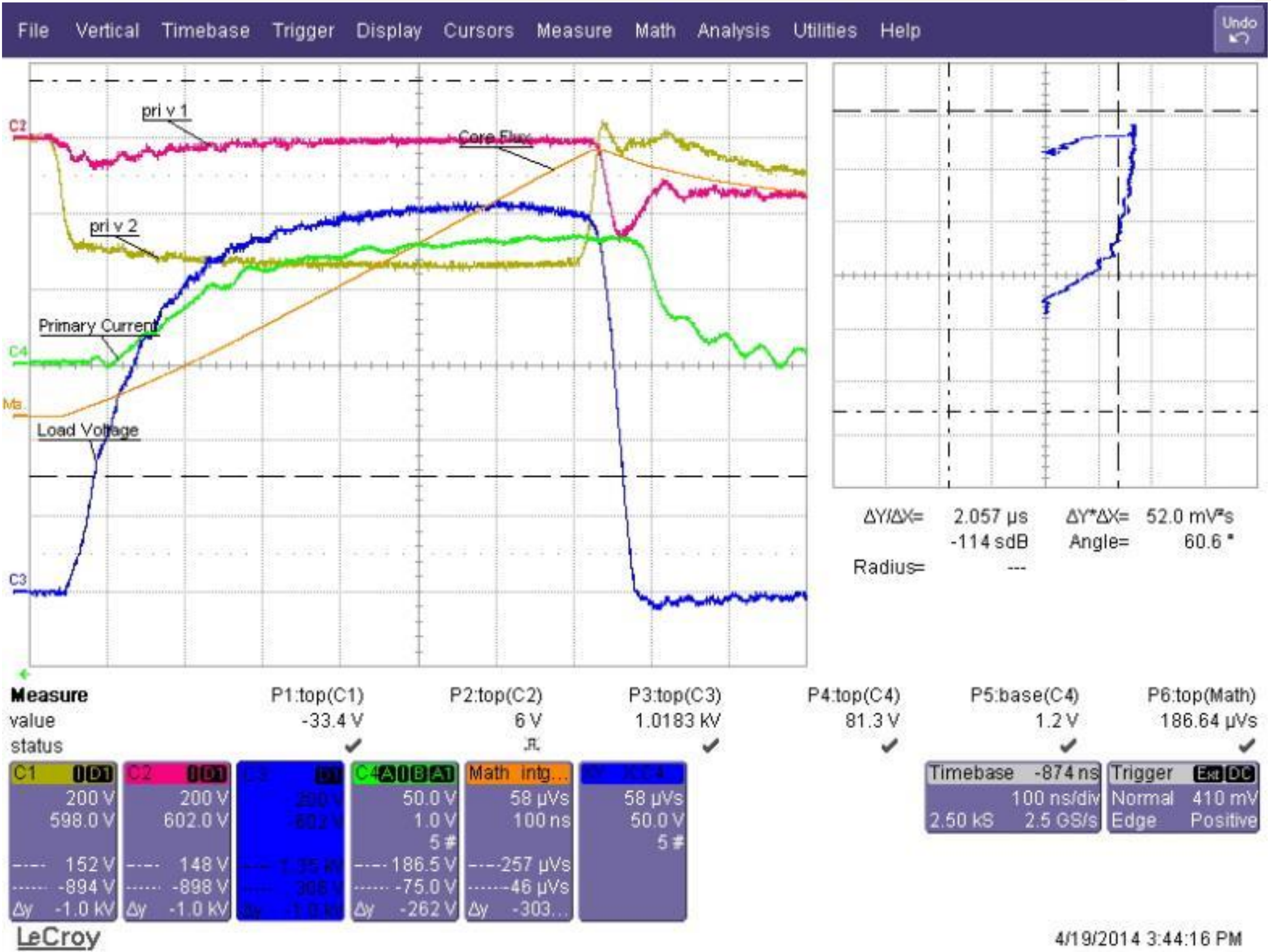
Additional Slides

Showing Burst Mode Operation

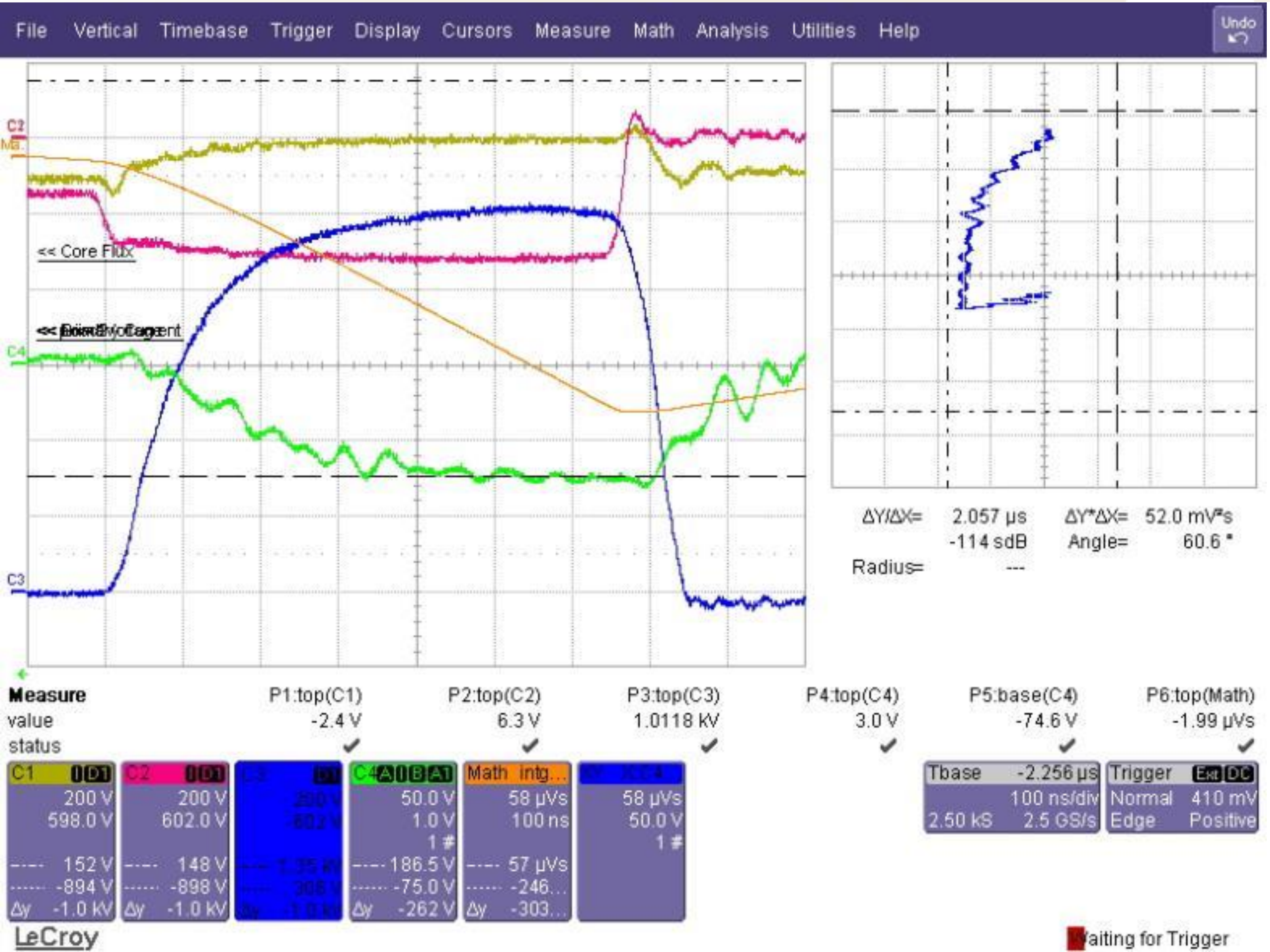
SLAC



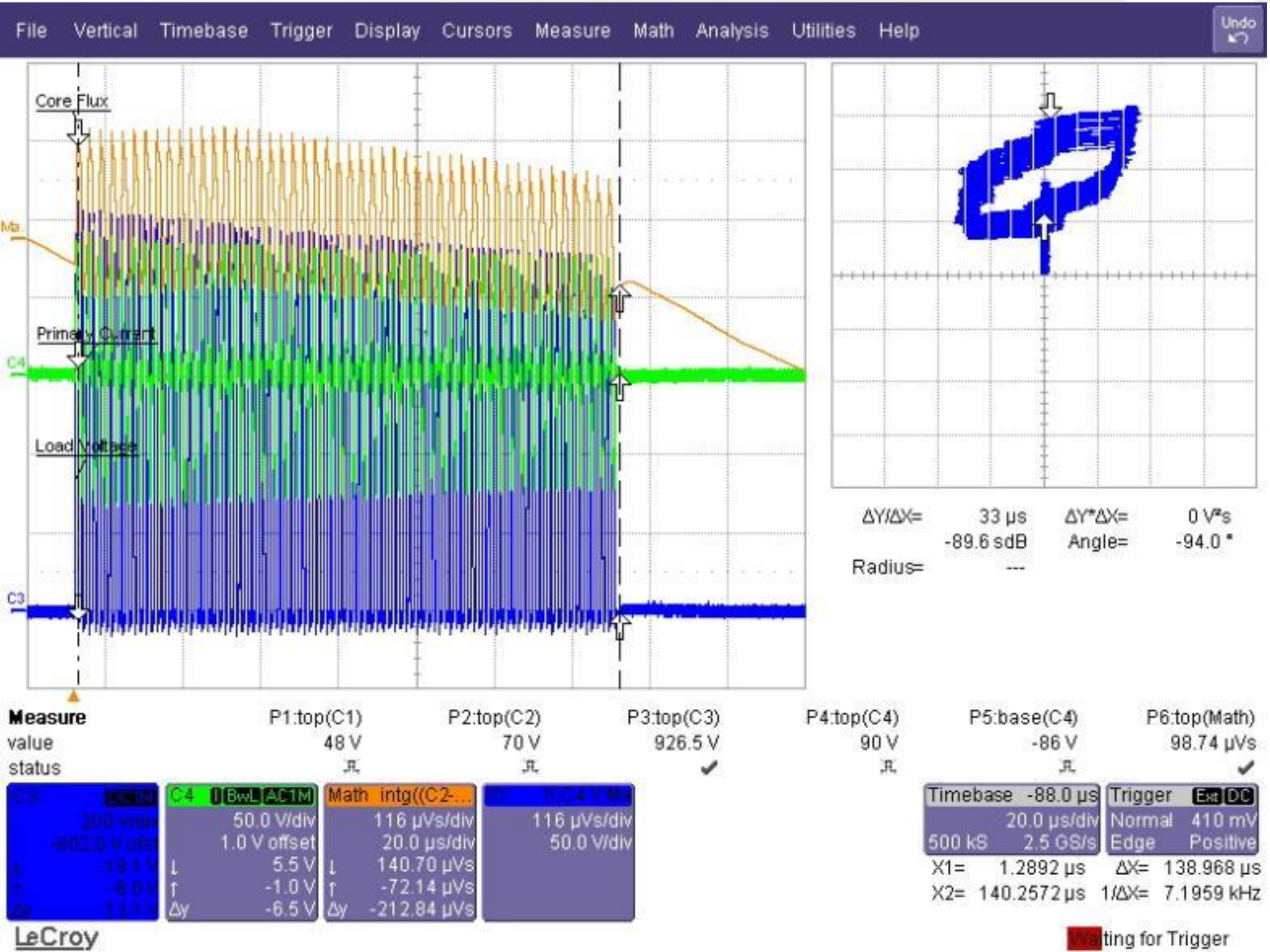
Showing Burst Mode Operation- positive cell pulse



Showing Burst Mode Operation- negative cell pulse

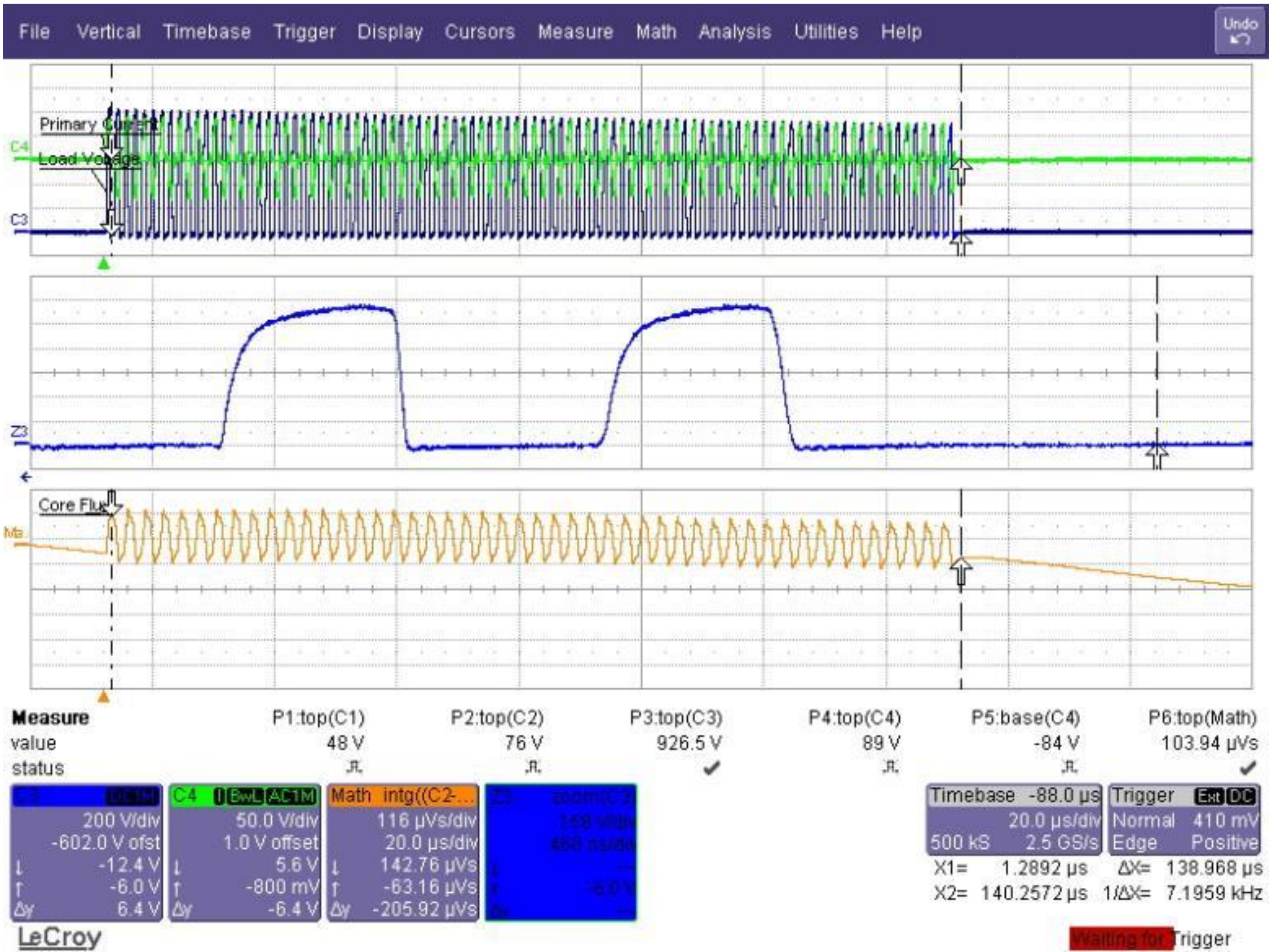


Showing Burst Mode Operation



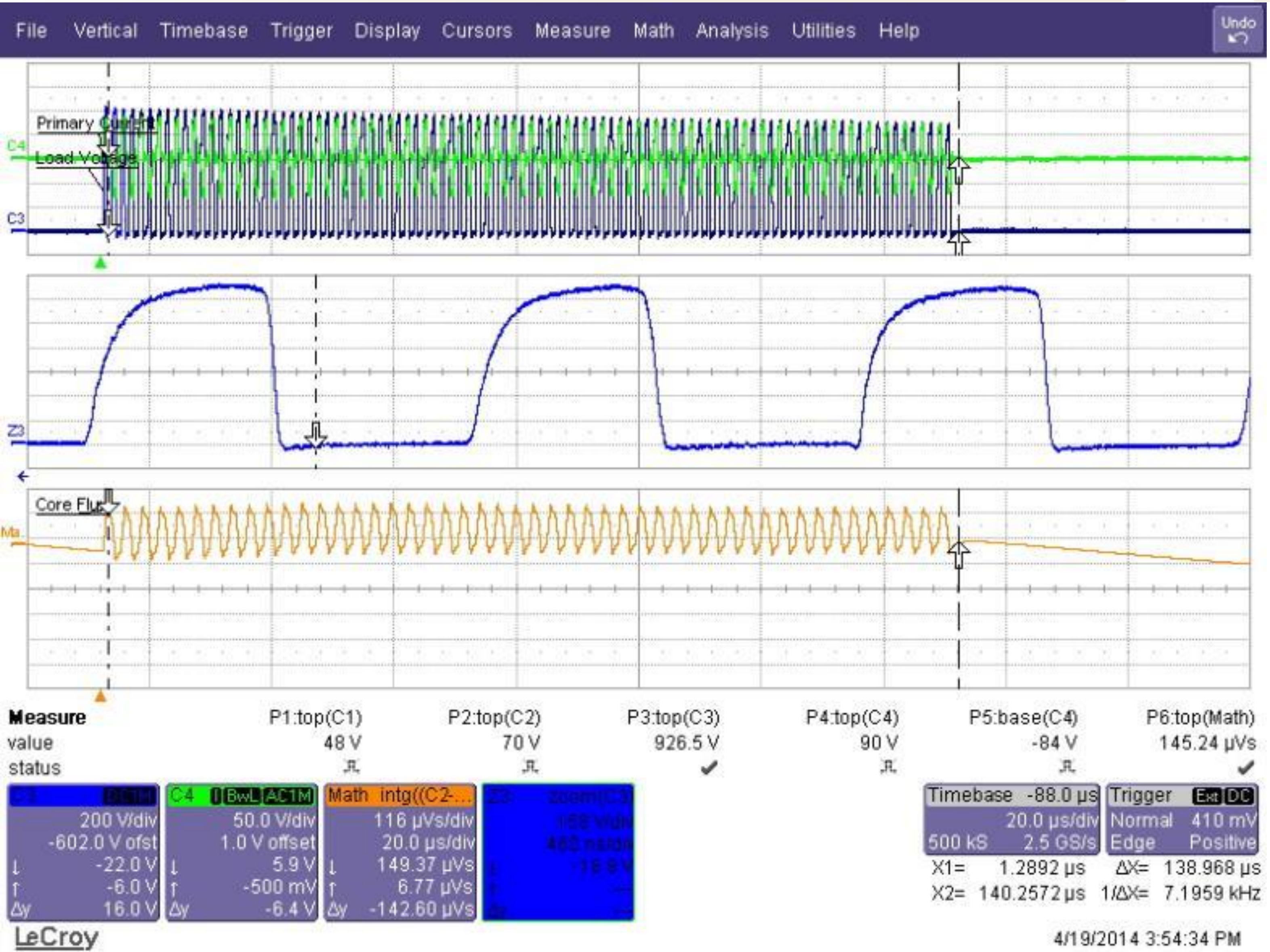
96 pulses

Showing Burst Mode Operation



Middle plot is zoomed-in load voltage at end of pulse

Showing Burst Mode Operation



Middle plot is zoomed-in load voltage at beginning of pulse