On Track Towards a Picosecond HPTDC

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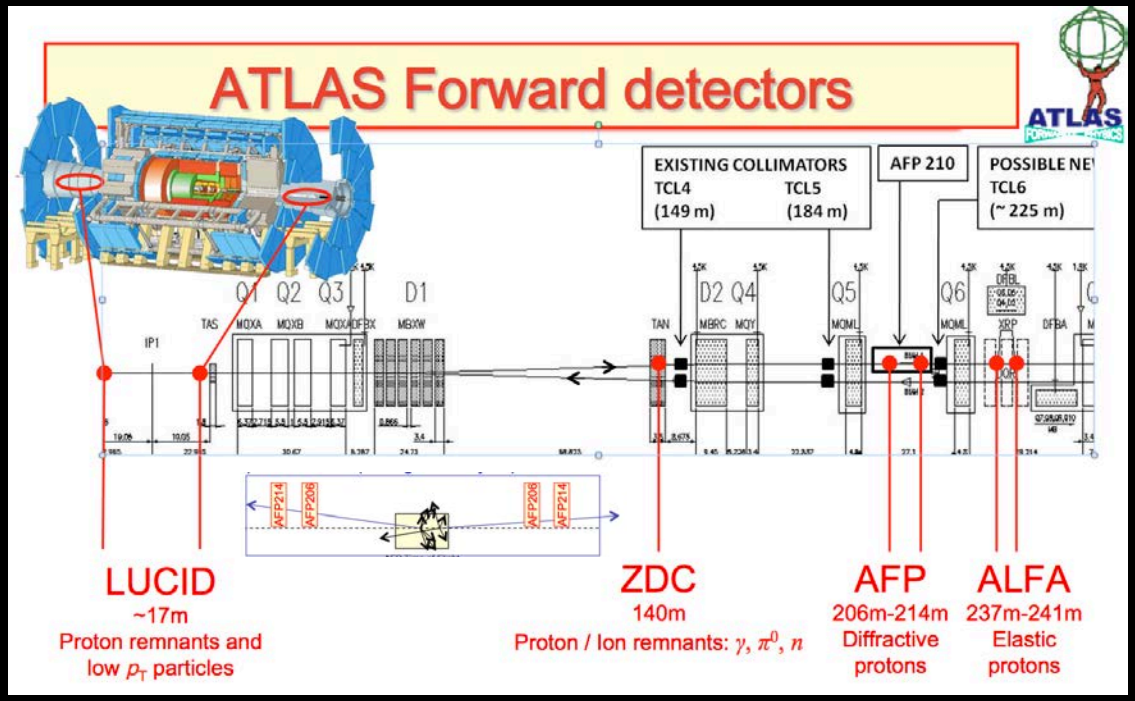
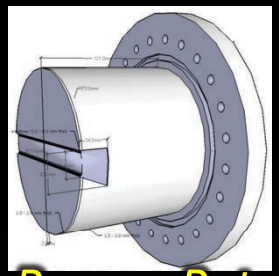
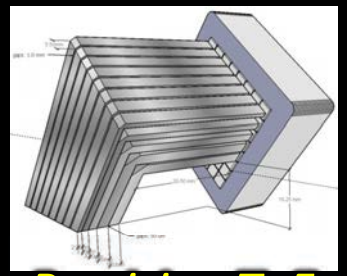
The Talk Menu

ATLAS Forward Protons (AFP)

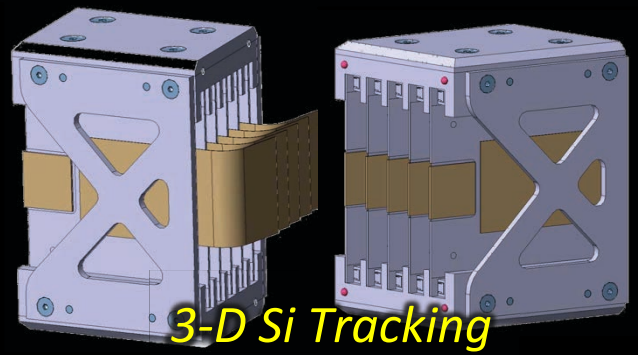




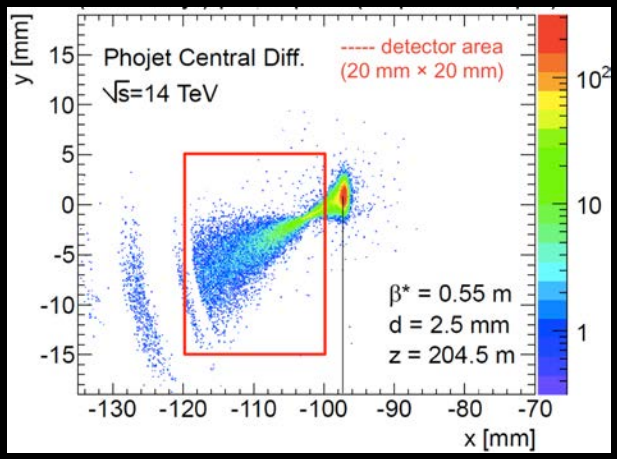
Roman Pots



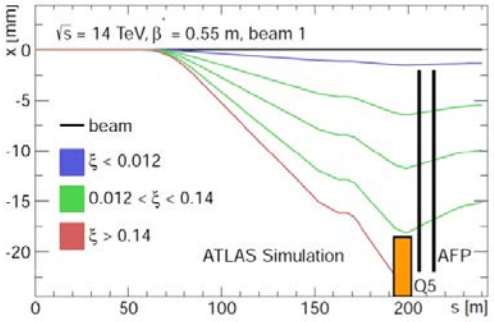
Precision ToF



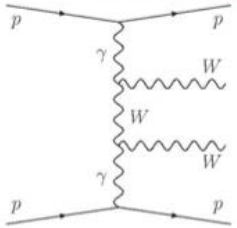
3-D Si Tracking



– Proton energy loss ξ is related to x:



– Central Mass M is related to both protons' energy losses ξ_1, ξ_2 :



$$M_{\mathrm{AFP}} = 2 p_{beam} \sqrt{\xi_1 \xi_2}$$

e.g. $\xi = 0.01$

$\Rightarrow M = 160$ GeV

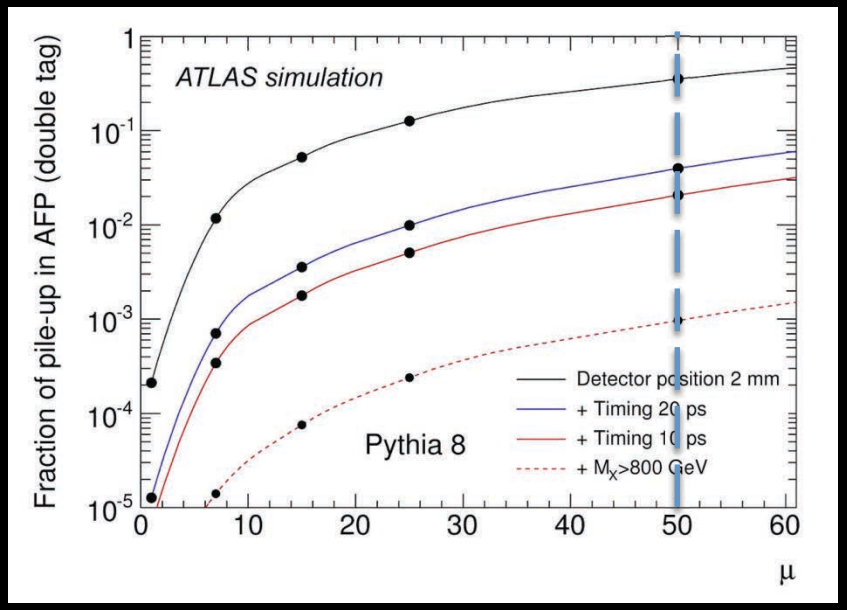
AFP – Precision ToF

Main CEP background: overlap of SD protons with non-diffractive events

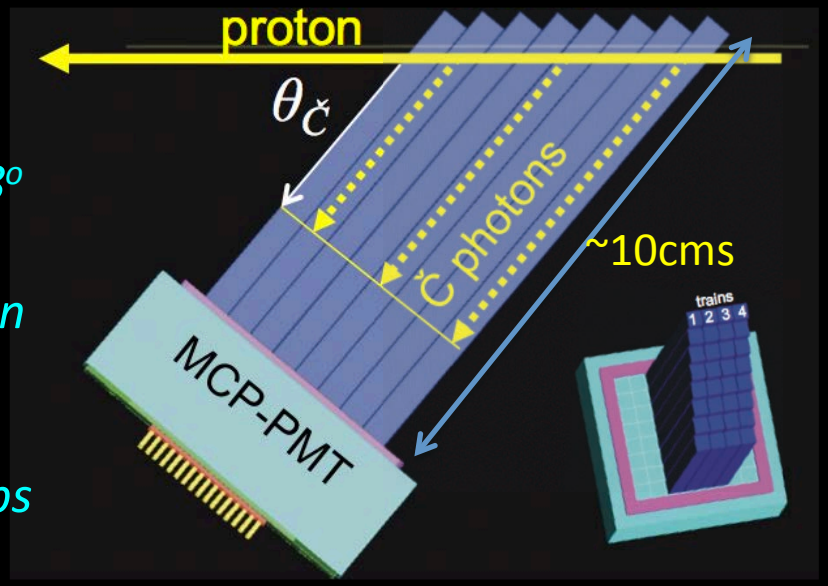
= 'pile-up' background

Reduce by:

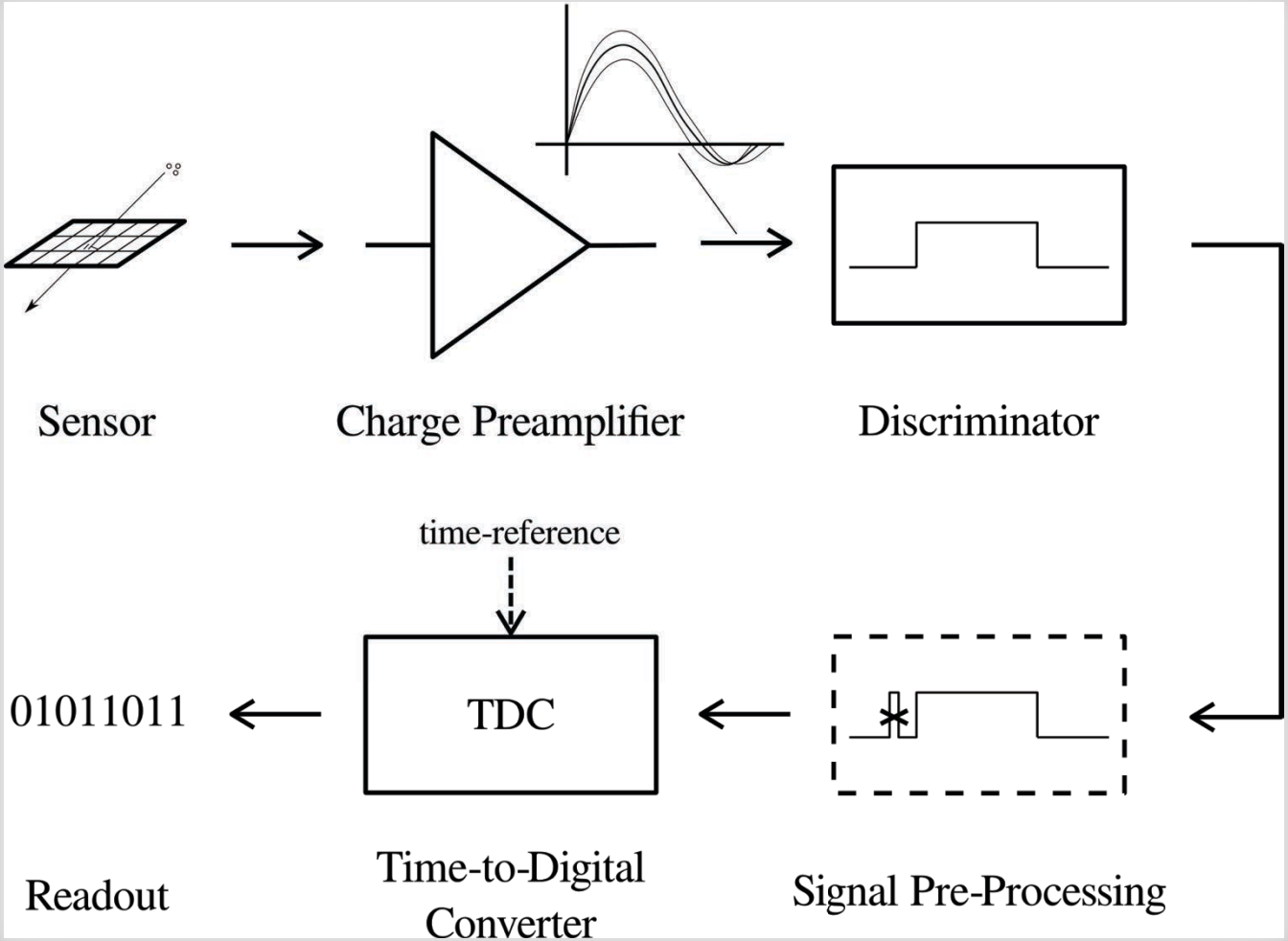
- central mass matching:
  - $M_{central} = M_{AFP} = (s\,\xi_{Left}\,\xi_{Right})^{1/2}$
- ToF:
  - $z_{vtx} = c(t_{Left} - t_{Right})/2$
  - E.g.: $\sigma_t = 10$ ps ➔ $\sigma_{zvtx} = 2.1$ mm
- not a new idea; FP420:



- *Quartic Concept:*
  - *Initial design 4 trains of 8 quartz bars*
  - *Mounted at the Cherenkov angles~48°*
  - *Isochronous – same time arrival of Cherenkov light at MCP for each bar in the train.*
  - *Multiple measurements improve readout resolution eg 30ps/bar →11ps for 8 bars*



Time Measurement Chain



HPTDC Based ToF System

(Designed and built at the UofA)

- *HPTDC board (9 channels)*
  - *3 HPTDC chips (16 Ch)*
  - *Capable of 15 MHz throughput*
  - *$\sigma_{Time} \approx 14$ ps with pulser*
- *5 ps resolution CFD demonstrated*
- *New version of CFD nearly ready*
  - *An improved resolution observed ~3ps*
  - *Also provides ToT measurement*

Timing System Resolution

Component	σ_t (ps) Current	σ_t (ps) Projected	Action
Radiator/MCP-PMT (~10 pe's with 10 μ pore MCP)	19	17	Optimize radiator
CFD	5	5	Larger dynamic range
HPTDC (14 ps with pulser)	17	<9	New HPTDC chip
Reference Clock	3	3	-
Total/bar	26	20	
Total/ detector (6 ch)	11	8	-

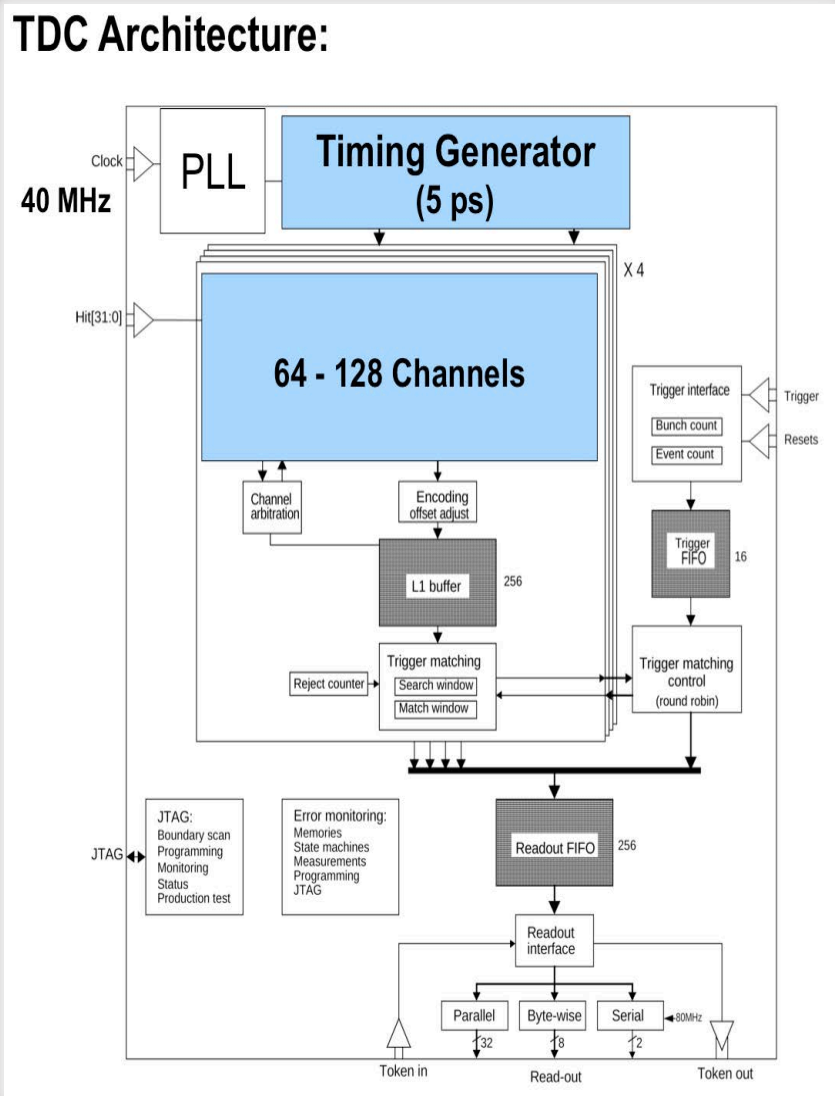
Reached and extrapolated timing resolution:

- *Currently at 11-12 ps (Fall 2012 Test beam) with 6 bars;*
- *ultimate performance of this system is probably about 8 ps*

Towards a Picosecond HPTDC

The Full PS HPTDC ASIC Design

- *Demonstrator ASIC*
  - *< 3ps-RMS resolution*
  - *< 50 mW/channel*
  - *Missing: PLL, Counter, Digital logic*
- *Full TDC*
  - *Based on HPTDC*
  - *64-128 Channels per ASIC*
  - *40 MHz input clock*
  - *< 5 ps timing resolution (power consumption opt.)*
- *Radiation tolerant*
  - *IBM 130 nm tech. - with high resistivity substrate*
  - *Error checking to counter SEU*

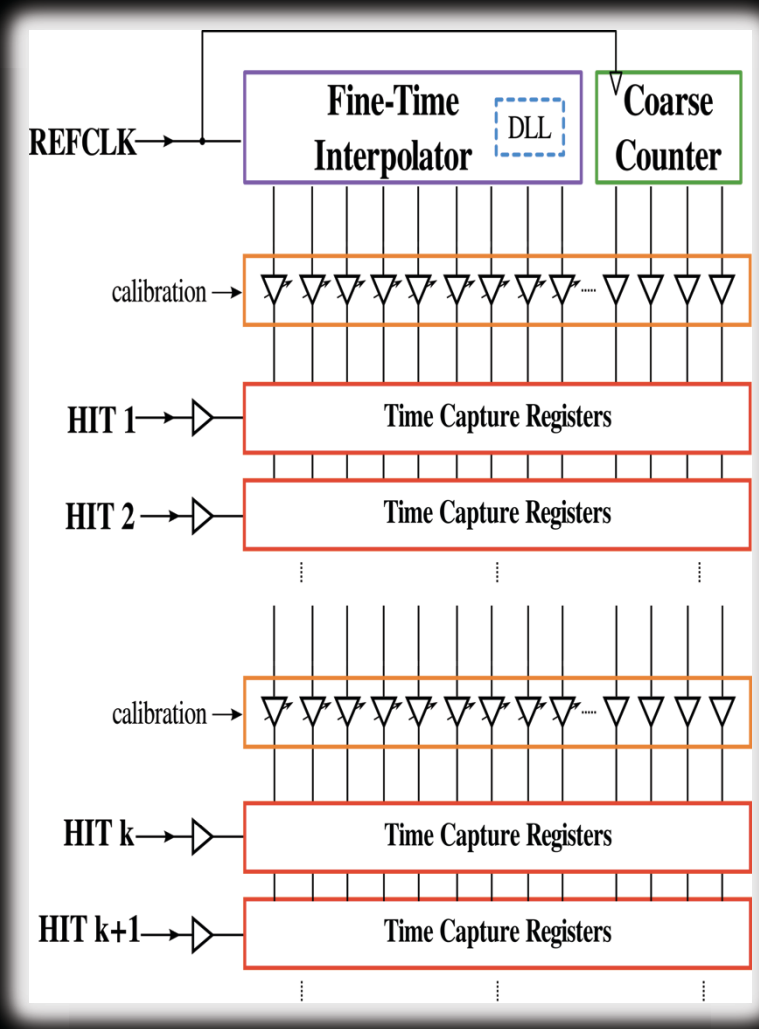


Challenges in the PS Realm

- *Device mismatch*
  - *-> Careful simulation and optimization*
  - *-> Major impact on design and performance*
- *Noise (power supply)*
  - *-> Short delays, fast edges*
  - *-> Separate power domains*
  - *-> Substrate isolation*
  - *-> Crosstalk*
- *Signal distribution critical*
  - *-> RC delay of wires*
  - *-> balanced distribution of timing critical signals*
- *Process-Voltage-Temperature variations*
  - *-> LSB auto calibration to compensate for slow VT variations*
  - *-> Global offset calibration still required*

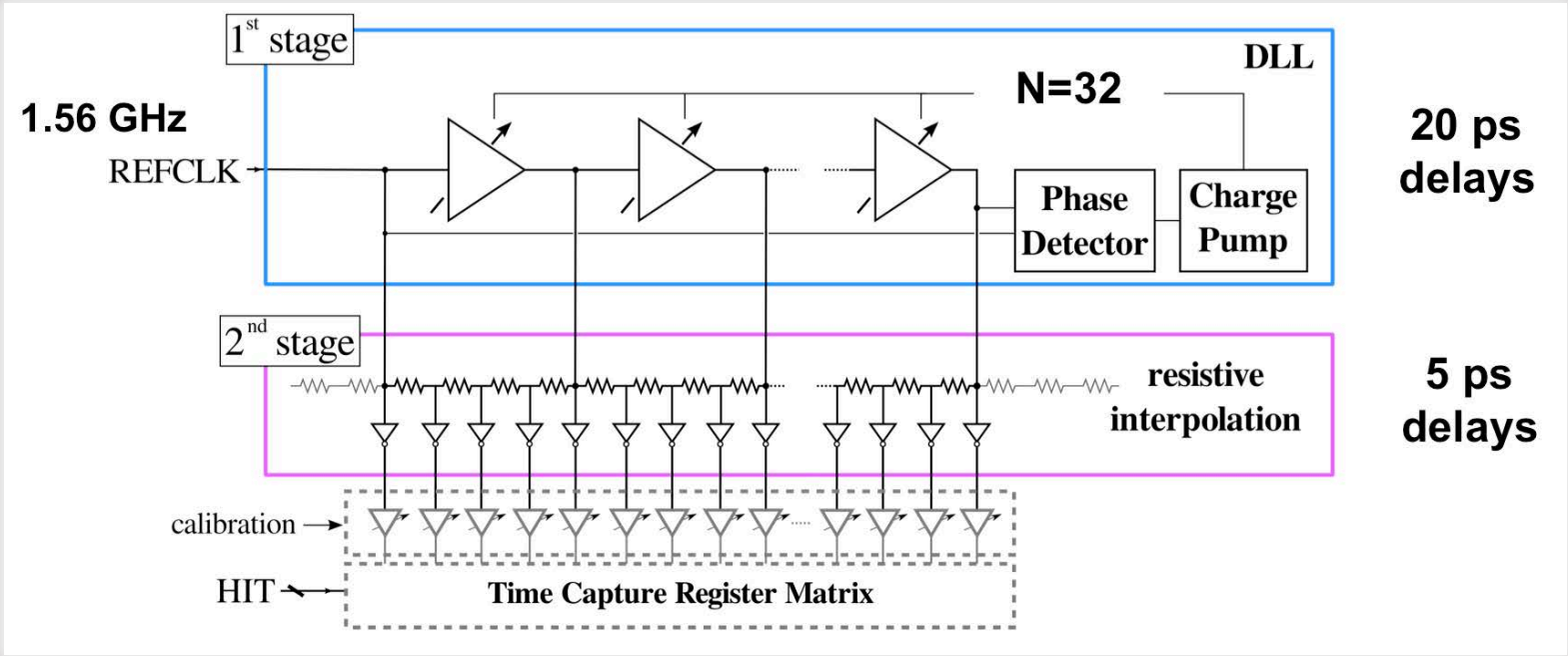
TDC Architecture

- *Central interpolator with counter to extend dynamic range*
- *Measurements are ref'd to common ref. for synch. of multiple TDCs*
- *DLL for PVT auto calibration and power consumption trade-off*
- *Short propagation delays and fast signal slopes of timing critical signals to reduce jitter*
- *Calibration applied on a group of channels to reduce circuit overhead and calibration time*
- *Relatively constant power consumption make it less sensitive to change in hit rate*



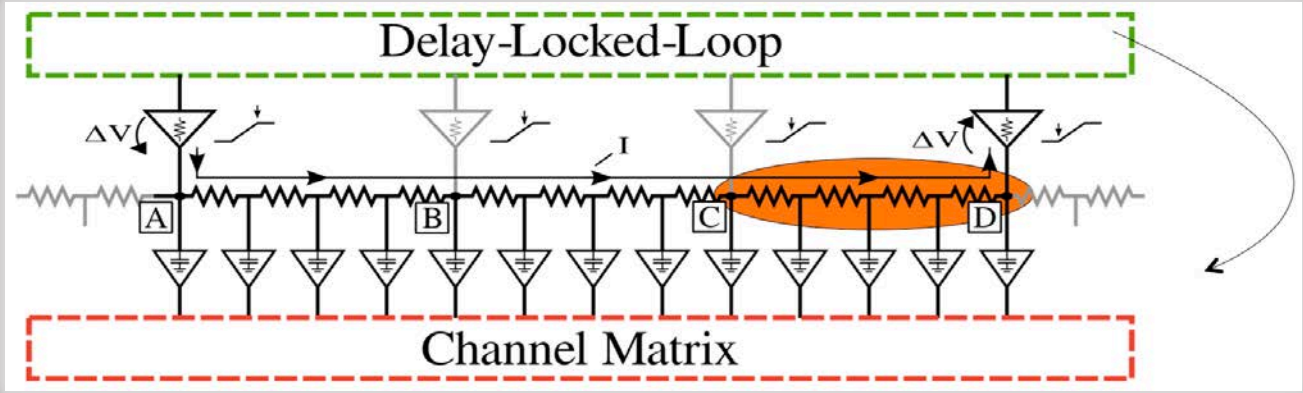
DLL – delay locked loop
PVT – process, voltage, temperature

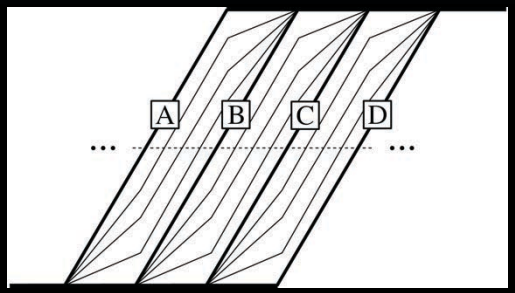
Fine Time Interpolator

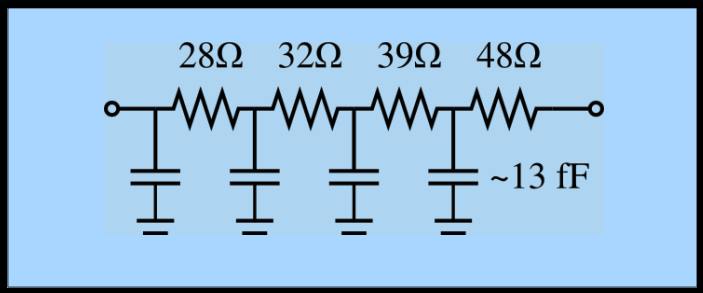


- *DLL to control LSB size*
  - *32 fast delay elements in first stage - 20 ps*
  - *Total delay of DLL 640 ps at 1.56 GHz*
- *Resistive Interpolation to achieve sub-gate delay resolutions*
  - *LSB size of 2nd stage controlled by DLL (Auto adjusts to DLL delay elements)*

Resistive Interpolation



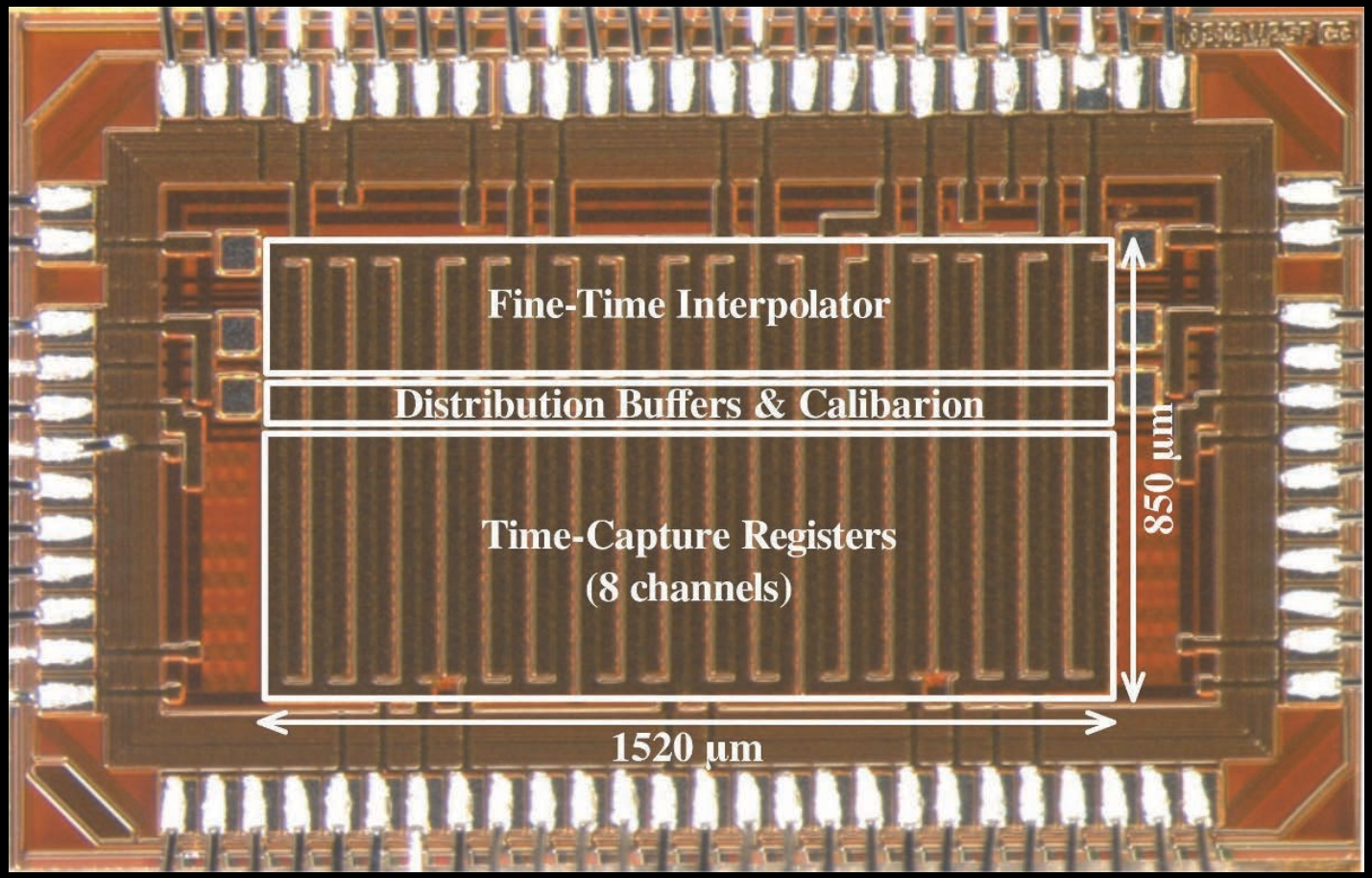




- *Resistive voltage divider →*
  - *Signal slopes > than delay, stabilized by DLL*
- *RC delay (capacitive loading)*
  - *Small resistances, small loads*
  - *Simulation based optimization of resistor values*

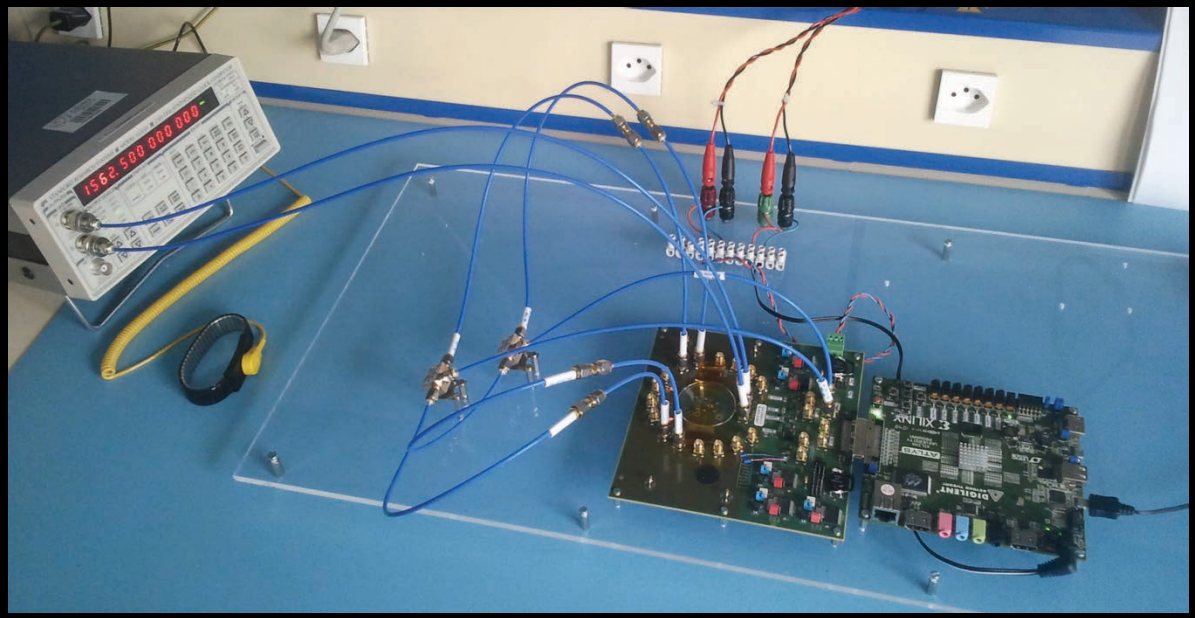
TDC Demonstrator

L. Perktold / J. Christiansen



- *130 nm IBM technology*

Test Setup



- *Tested*
  - *Interchannel cross-talk – smaller than ±*
  - *PVT variations – -0.2 ps/mV & 0.4 ps/deg*
  - *Measured double-shot precision < 2.44 ps RMS*
  - *Power consumption full 8-ch test chip*
    - *At 10 ps resolution 26mW(acquisition running) – 21mW(acquisition stopped)*
    - *At 5 ps resolution 26mW(acquisition running) – 21mW(acquisition stopped)*

Conclusion

- *Demonstrator TDC has been designed, prototyped and successfully tested.*
  - ***3ps RMS time resolution has been achieved***
  - *Device mismatch considerably affects performance*
    -> Trade off: Power, Resolution, Calibration
  - *Macro suitable for high resolution general purpose TDC*
- *Simulation of the whole ASIC has begun at UofA in order to produce complete design for first ASIC run*
  - *Radiation hard technology utilized*
  - *Switchable between high resolution (hi power) low resolution (lo power)*
  - *Working on reducing power requirements at high resolution*
  - *Larger number of channels (64-128) than initial HPTDC design*
  - *~40 MHz data throughput possible*
- *Aiming for the first trial ASICs within a year.*