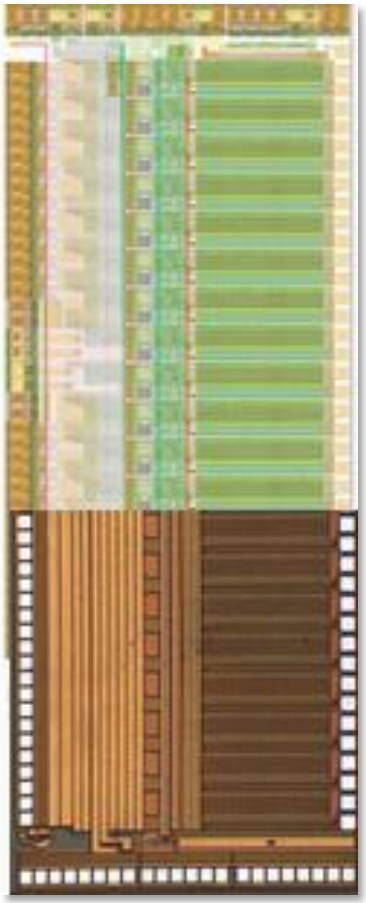
THE SAMPIC WTDC CHIP



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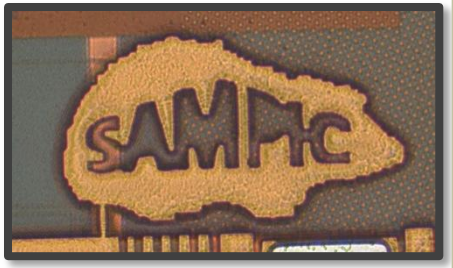

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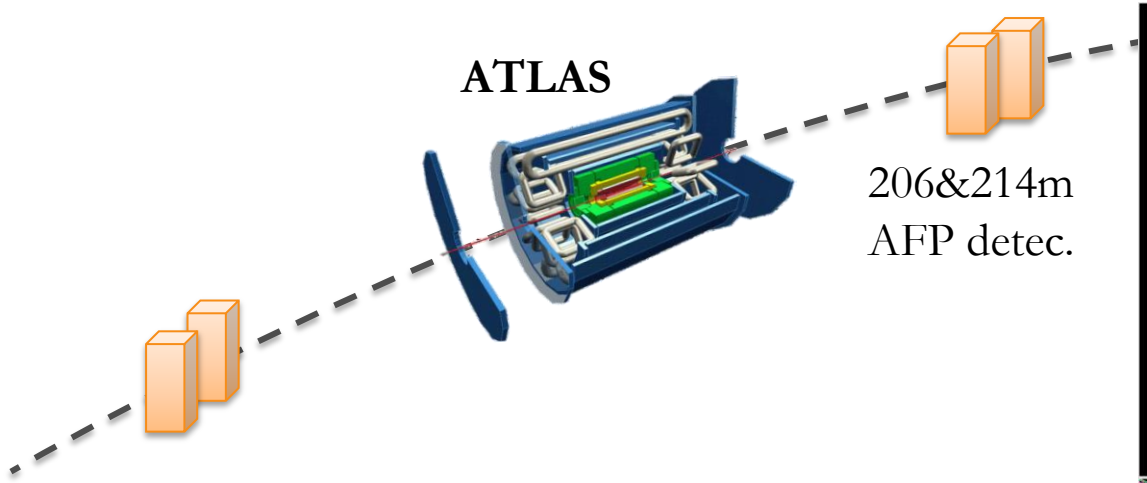
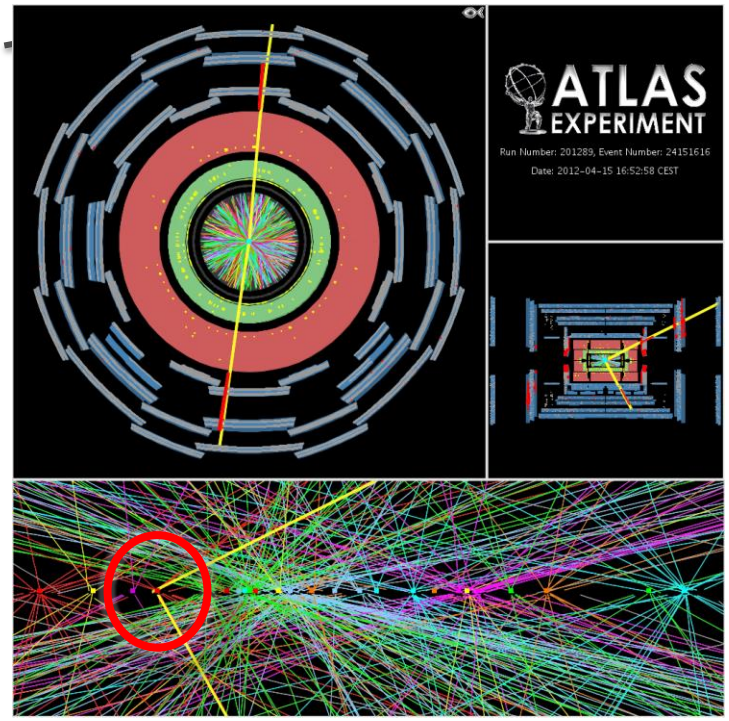
INTRODUCTION

- **Test chip** = common prototype before designing specific chips for ATLAS AFP and SuperB TOF
- R&D funded by "P2IO" grant (not by experiments)
- **Goals for the first prototype:**
  - Evaluation of AMS 0.18µm technology
  - Evaluate new design options (DLL & SCA)
  - Evaluate simultaneous R/W
  - **Multichannel Chip usable in a real environment (with detector and a real DAQ)**
- Core of a future deadtime free chip

TIMING IN ATLAS FORWARD PHYSICS DETECTORS





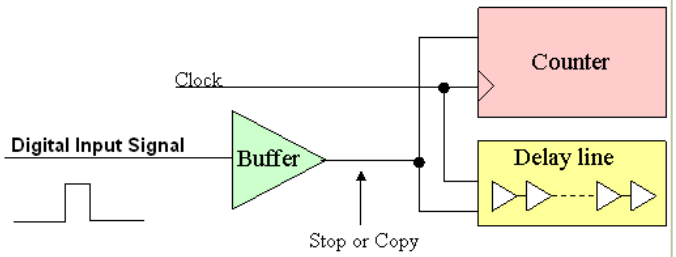
Study of diffractive protons at very low angles

- Few mm from the beam
- 2 x 2 detectors on each side of ATLAS
  each made of:
  - 5 slices of Hybrid Si pixel detectors (FEI4)
  - Timing detectors :
    - **Few ps timing resolution to:**
      - associate event to the correct vertex (3 mm precision => 10 ps)
      - reject background due to the halo
    - Careful segmentation to reduce pile-up
    - High rate (HL-LHC):Typically: 1 event/bunch crossing / 16 ch
    - 3 Solutions in competitions 2 with (Quartz + MCP-PMT) one with diamond

INTRODUCTION A FEW COMMENTS ABOUT TDCs

Current most performant TDCs use digital counters and Delay Line Loops (DLLs):

- **advantage**: they produce directly the encoded **digital value**
- **but** the resolution is at least limited by **the DLL step** (often by environmental factors)
- Actual time resolution of today's available most advanced ASICs: **~ 20 ps**
- New developments are ongoing (new HPTDC @ CERN, targetting **5 ps, 130 nm** technology)



TDC Principle

BUT a TDC needs a **digital** input signal

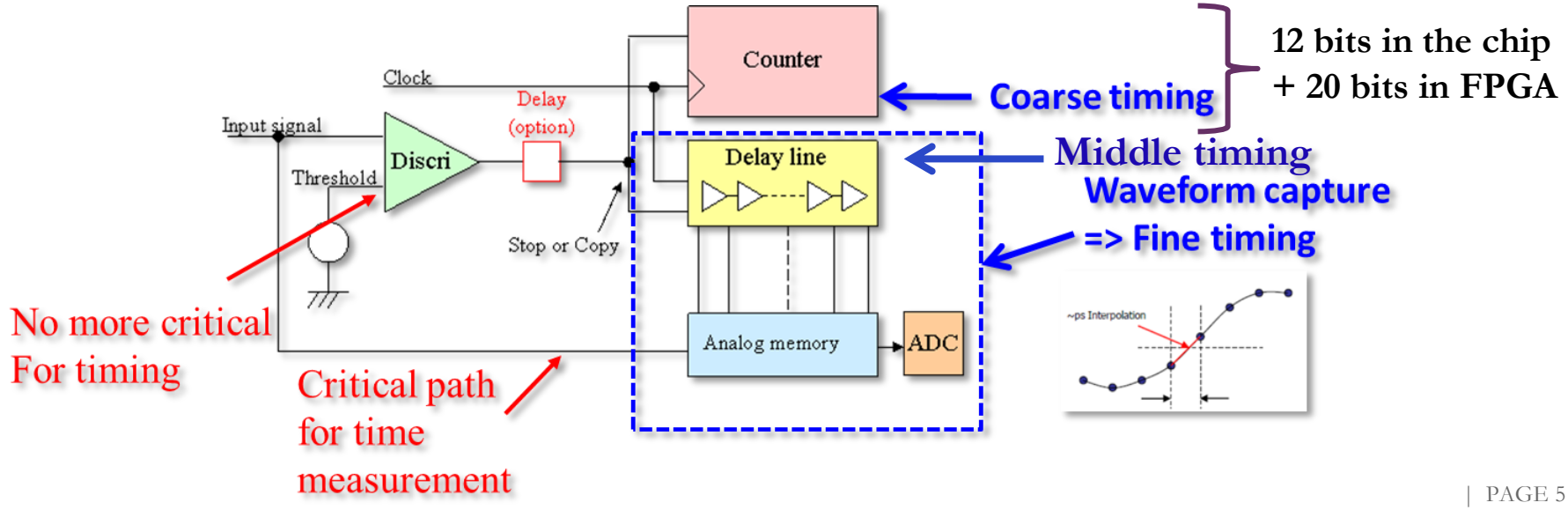
⇒ **analog** input signal has to be translated to digital with a **discriminator**

⇒ **additional jitter** and **residues of time walk** effect enter the game

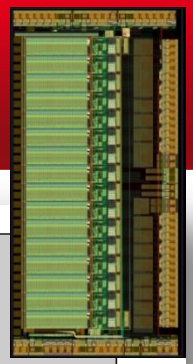
⇒ overall timing resolution is given by the **quadratic sum of the discriminator and TDC timing resolutions**

THE « WAVEFORM BASED TDC » STRUCTURE

- The Waveform TDC : a new concept based on an original principle
- Association of : **Analog Memory + Discriminator + Counter + DLL + ADC**
- Time Given by :
  - Coarse = Timestamp Gray Counter (~6 ns step)
  - Middle = DLL locked on the clock to define Region of interest (150ps step)
  - Fine = few samples in the ZOI of the waveform (interpolation will give a precision of a few ps rms)
- **Digitized Waveform Shape, Charge and Amplitude are available**
- **Discriminator used only for triggering, not for timing**



OVERALL ARCHITECTURE



- **16 single-ended Channels:**
  - ✓Self Triggerable (or Central OR Trigger, or External Trigger)
  - ✓Independent channels
  - ✓ 64 Analog Sampling Cells/Ch
  - ✓One 11-bit ADC/ Cell (Total : 64 x 16 = 1024 on-chip ADCs)

- **One Common 12-bit Gray Counter** (@160MHz) for **Coarse Timestamping**.

- **One Common servo-controlled DLL**: (from 1 to 10 GHz) used for middle precision timing & analog sampling

- **One** common **11-bit Gray Counter** running @ 1.3GHz and used for the **parallel Wilkinson Analog to Digital conversion**.

- 12-bit LVDS **Read-Out Bus** (160 – 400 MHz)
- SPI Link for Slow Control configuration

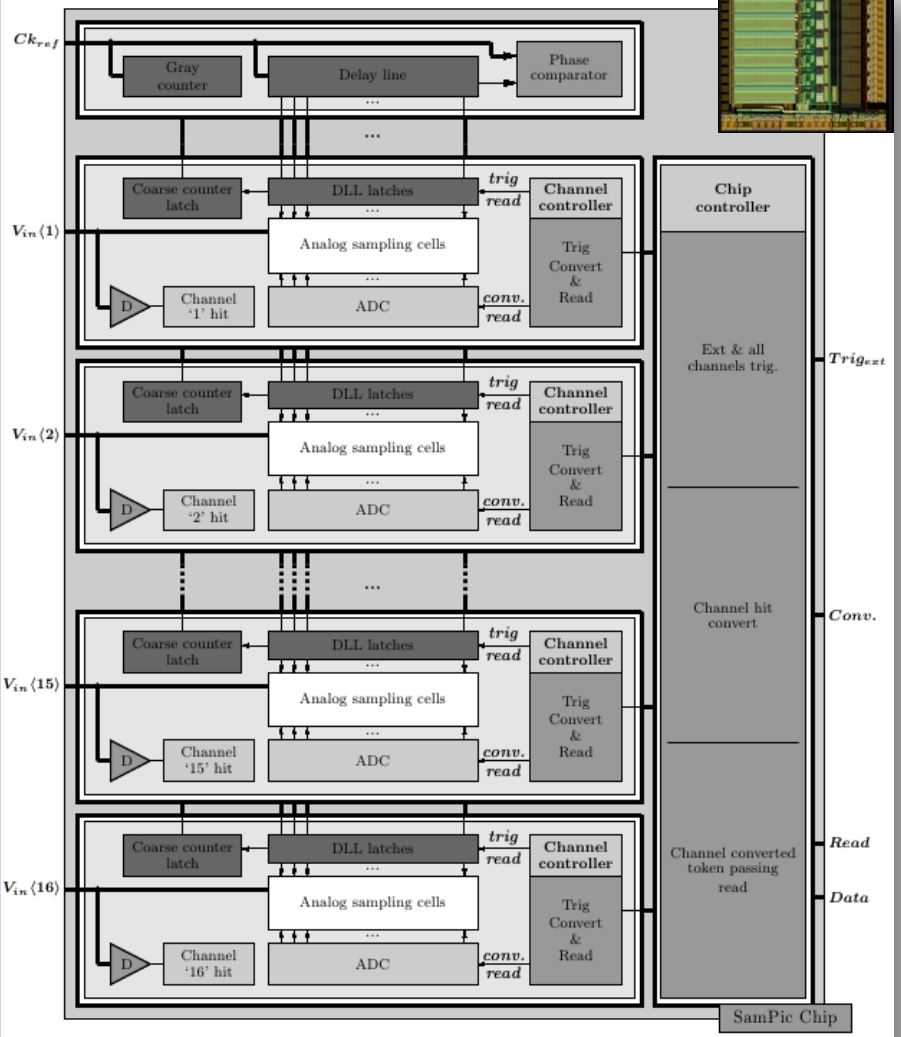
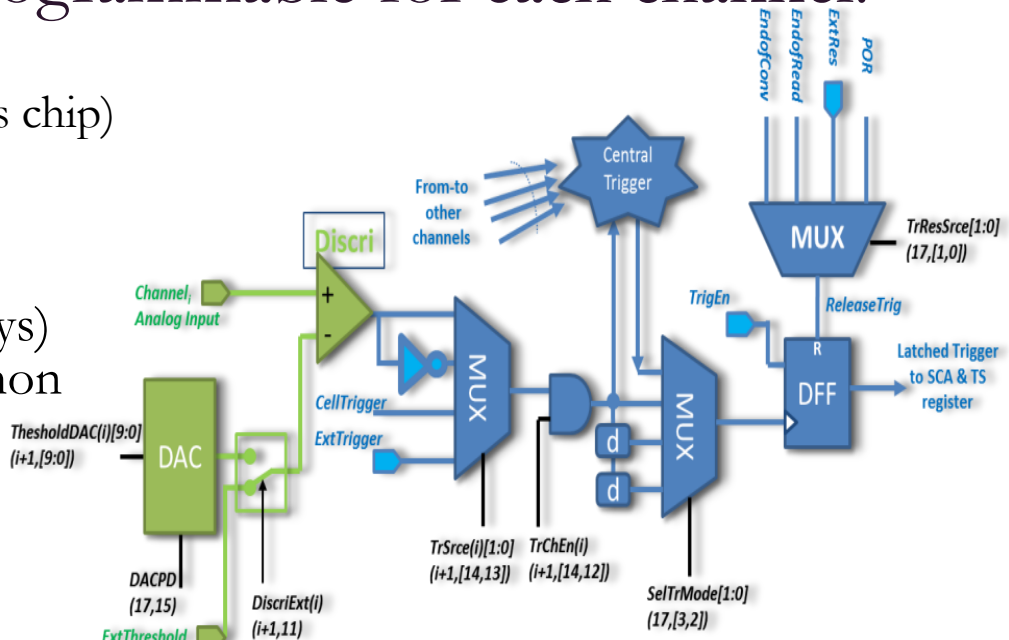


Figure 1 – Top level bloc diagram of the SamPic chip.

SAMPIC TRIGGERING OPTIONS

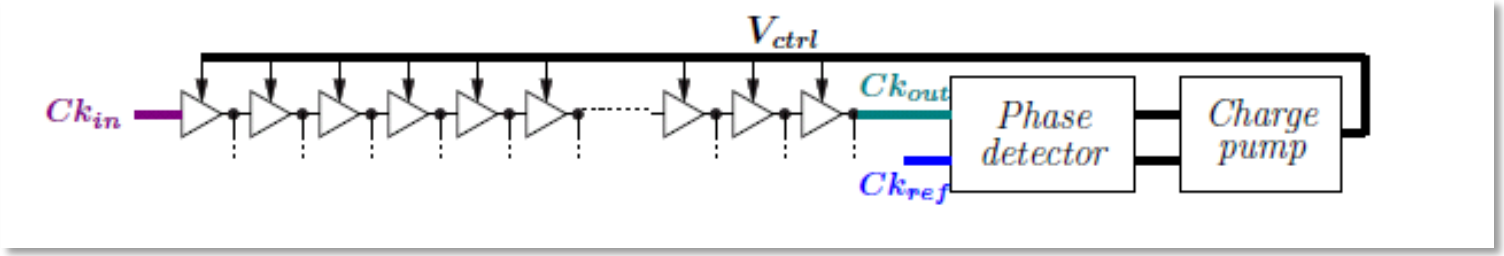
- One discriminator/channel
- One 10-bit DAC/channel for trigger (or external threshold)
- Several trigger modes programmable for each channel:
  - External
  - "Central" trigger (only OR in this chip)
  - Edge selection
  - Enable/disable
  - Internal/external threshold
  - Postrig (0,1,2 elementary delays)
  - Fast Global Enable for common deadtime



- When a trigger occurs:
  - the sampling in the analog memory is stopped and the coarse timestamp is latched
  - The chip rises then a flag for the user (FPGA) to start the ADC conversion and afterward the data

TIMEBASE

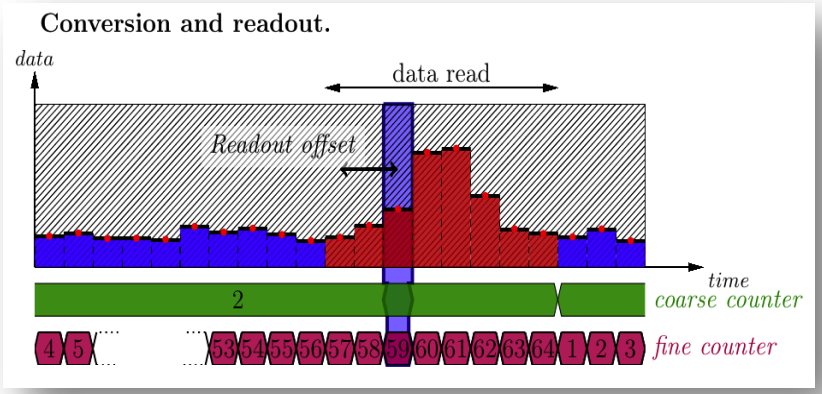
- **One single 64-step Delay Line Loop**
- Locked on the Timestamp counter clock
- On chip servo-control (Phase detector + Charge Pump)

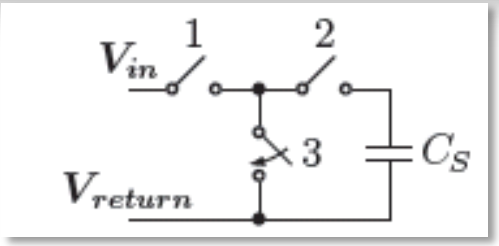


- Provides 64 incrementally **delayed** pulses **with constant width** used to drive the T/H switches of the **64 cells** for **each SCA channel**
- **'virtual multiplication'** by 64 of the TS Clock (100MHz =>6.4GHz)
- T/H signals can be disabled on each channel (stop the sampling)
- Optional low speed mode for sampling < 3 GSPS
- Special structure to ensure a perfect continuity between last & first cells

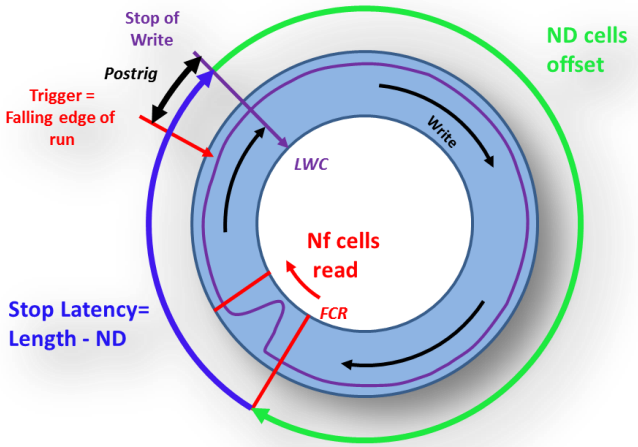
ANALOG MEMORY (SCA)

- No input buffer, Single ended
- **64 Cell-depth** trade-off between:
  - Time precision /stability (short)
  - Input capacitor (short)
  - Accommodation to trigger latency (long)
- **>1 GHz BW**
- 1V usable range
- Cell structure to avoid leakages and ghosts
- **Continuously writing** until triggering (circular buffer)
- **« TDC » like trigger position marking**
- Special design ensuring good quality (constant bandwidth and constant tracking duration) over all the 64 samples (even those after trigger)
- Optional **Region of Interest Readout** for deadtime minimization





~50fF

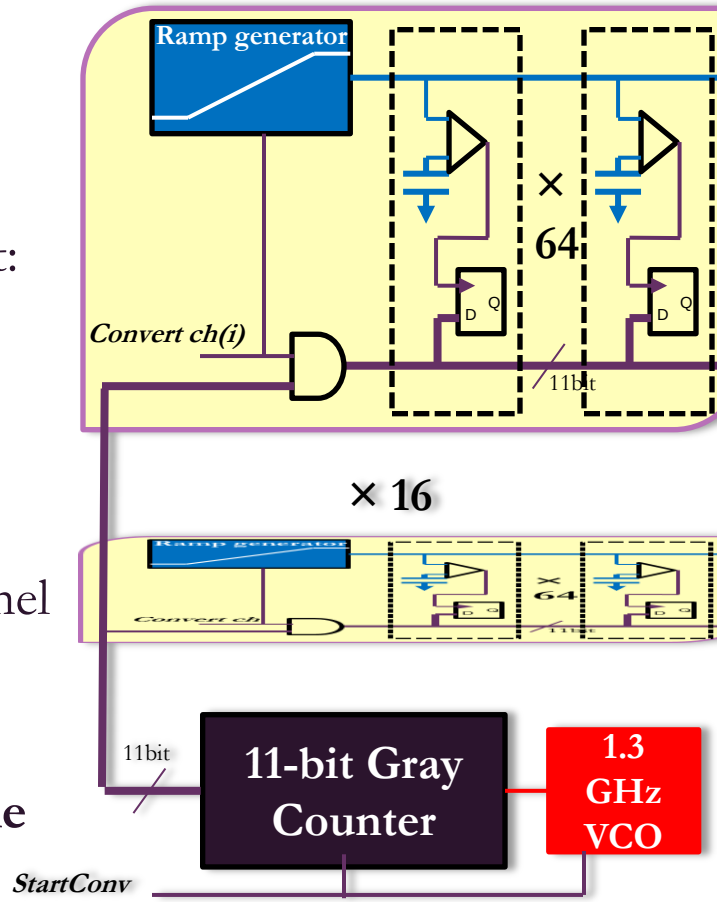


WILKINSON DIGITIZATION

Simultaneous conversion of all the cells of the triggered channels:

- Starts the on-chip 1.3 GHZ VCO
- Starts the on-chip **1.3 GHz Gray counter** and sends its outputs to the channels to convert
- Starts the ramp generators of channels to convert: tunable slope: speed/precision tradeoff
  - **1.6µs/11bit, 400ns for 9 bit…**
  - **Main contribution to the Dead Time**

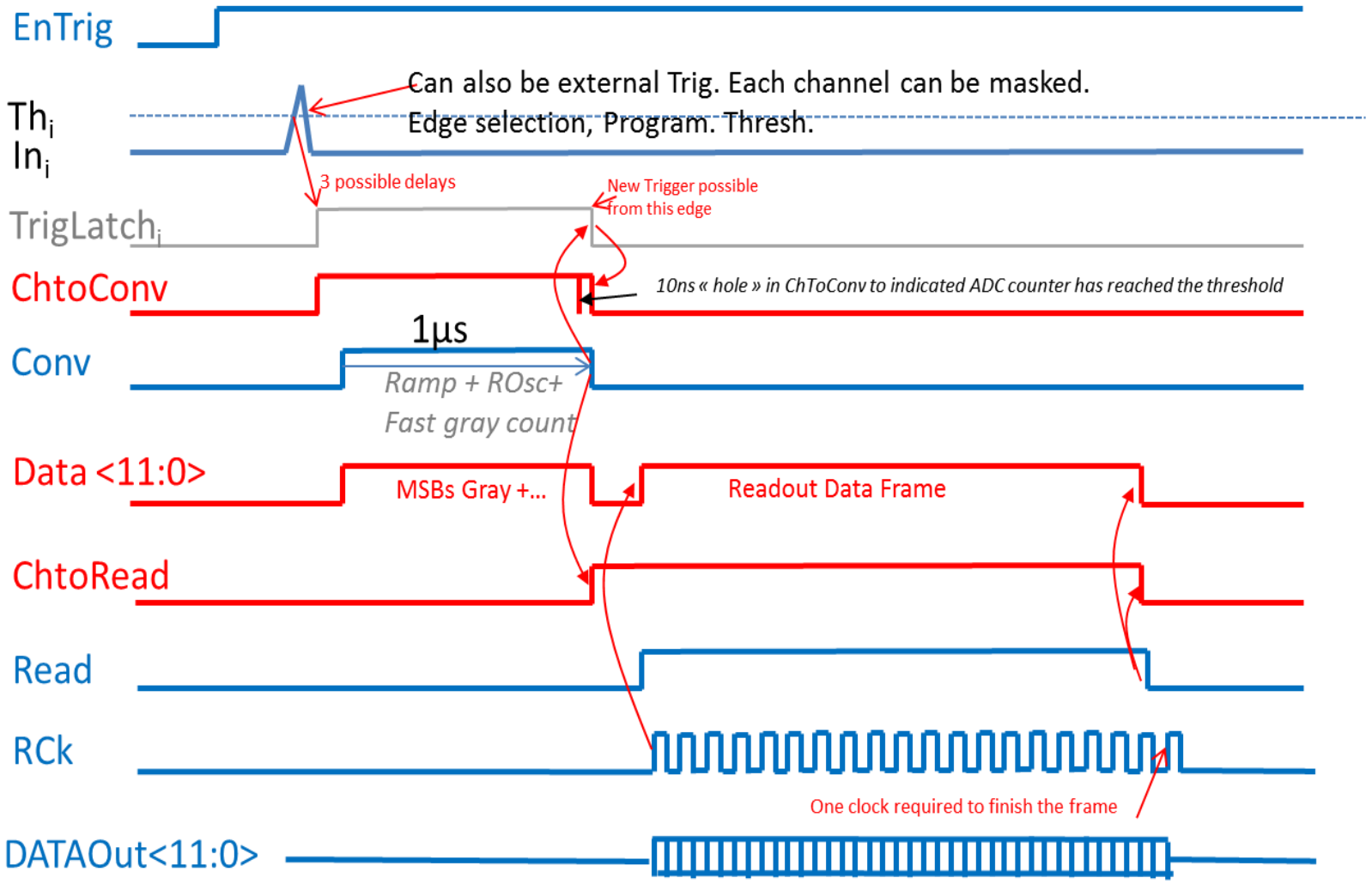
- Enable the **64 comparators** of the enabled channel
- When **Ramp crosses cell value** => the counter stored in a register
- Once converted, a channel is **immediately usable to record** a new event



READOUT

- Readout (Read and RCk signals)
- Data read **channel by channel**
- Rotating **priority mechanism** to avoid reading always the same channel
- **Region of interest readout** to reduce the deadtime (nb of cell read can be chosen dynamically)
- Readout of the converted data through a 12-bit LVDS bus:
  - Timestamps
  - Trigger Cell Index
  - Channel Identifier
  - The cells (all or a selected set) of a given channel are read sequentially
  - Up to 4.8 Gbit/s
- **Channel is not in deadtime during Readout (the data register is really a buffer stage)**

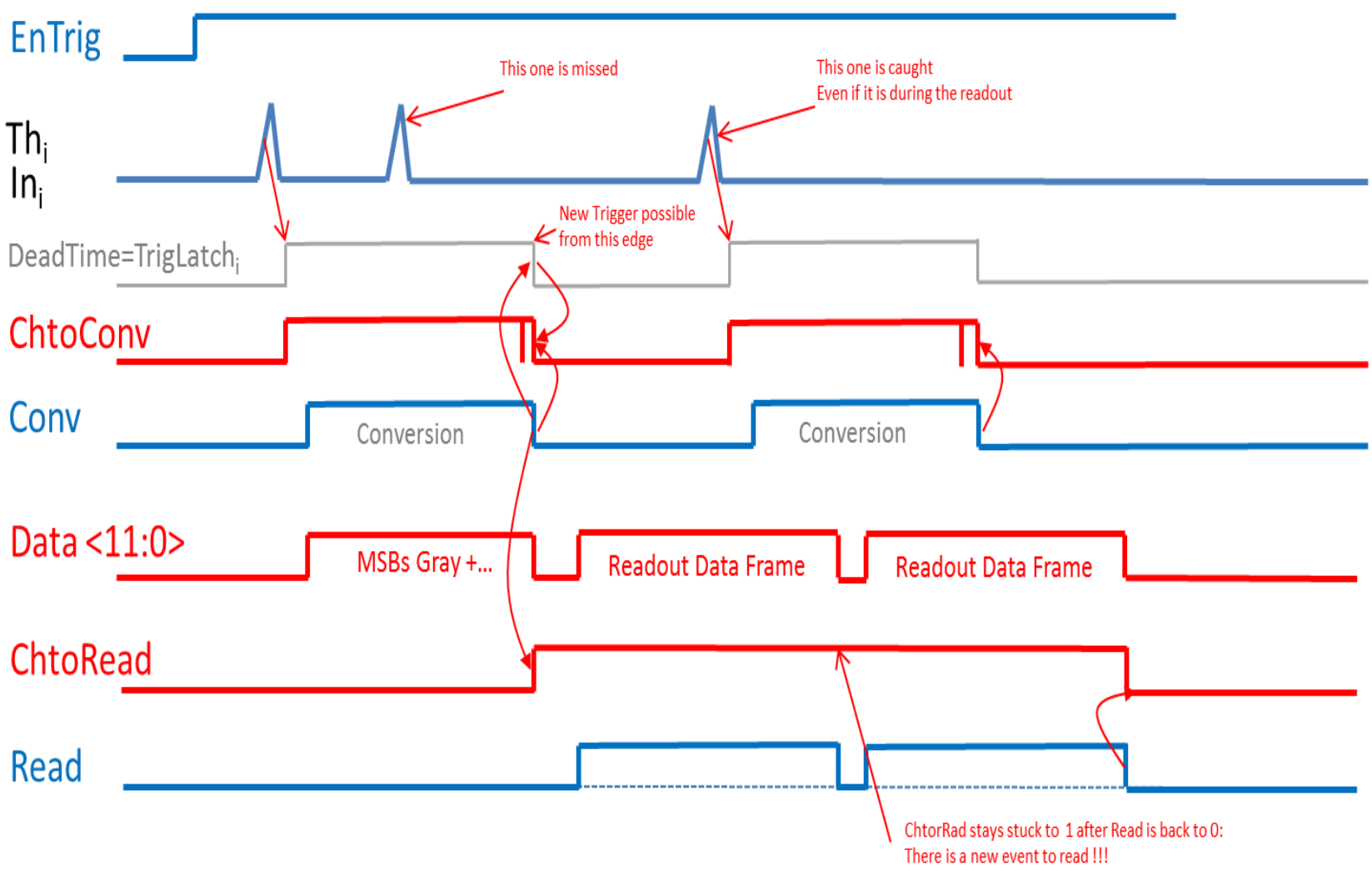
SIMPLEST OPERATION: 1 HIT, 1 CHANNEL



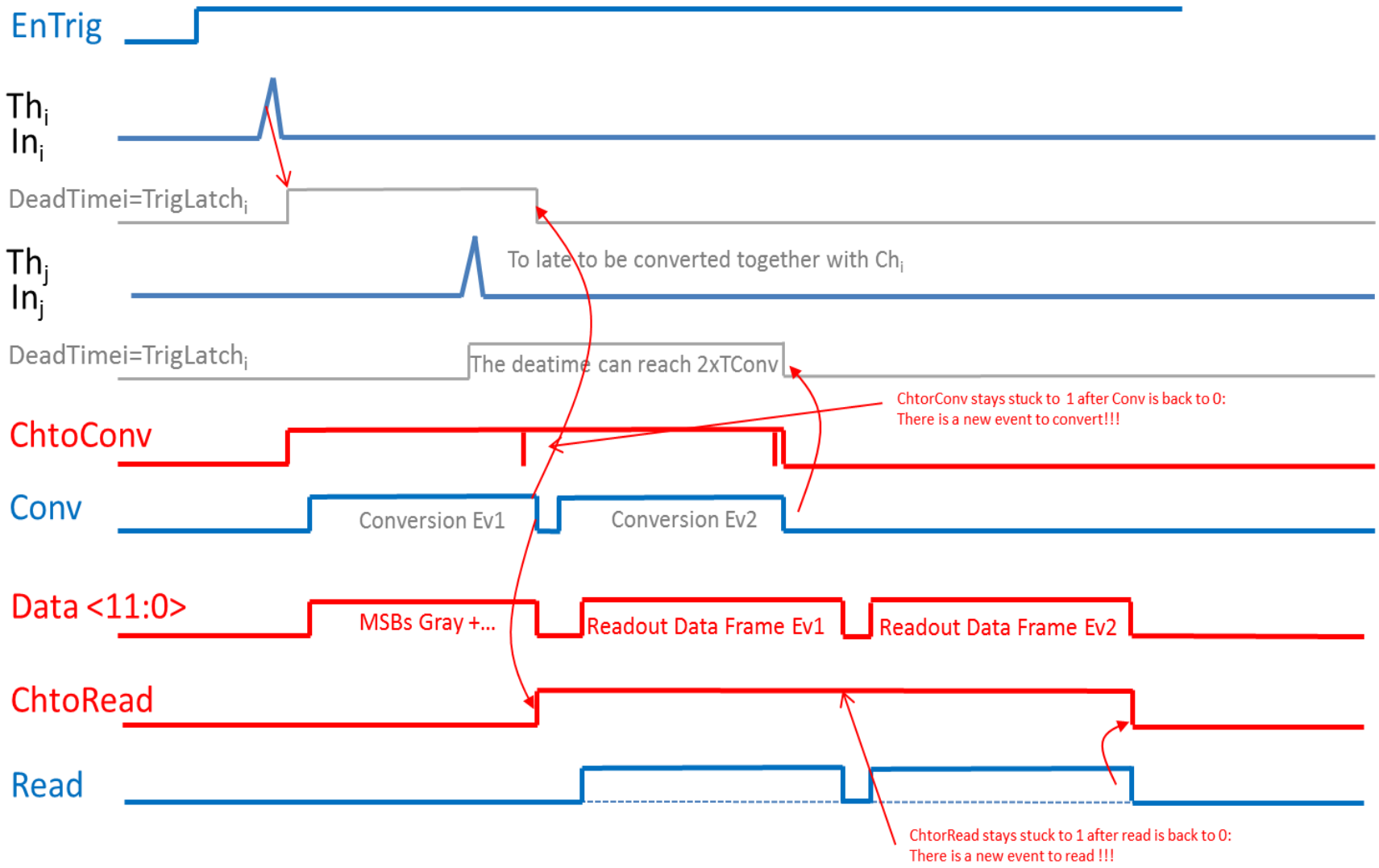
FROM SAMPIC to FPGA

TO FPGA from SAMPIC

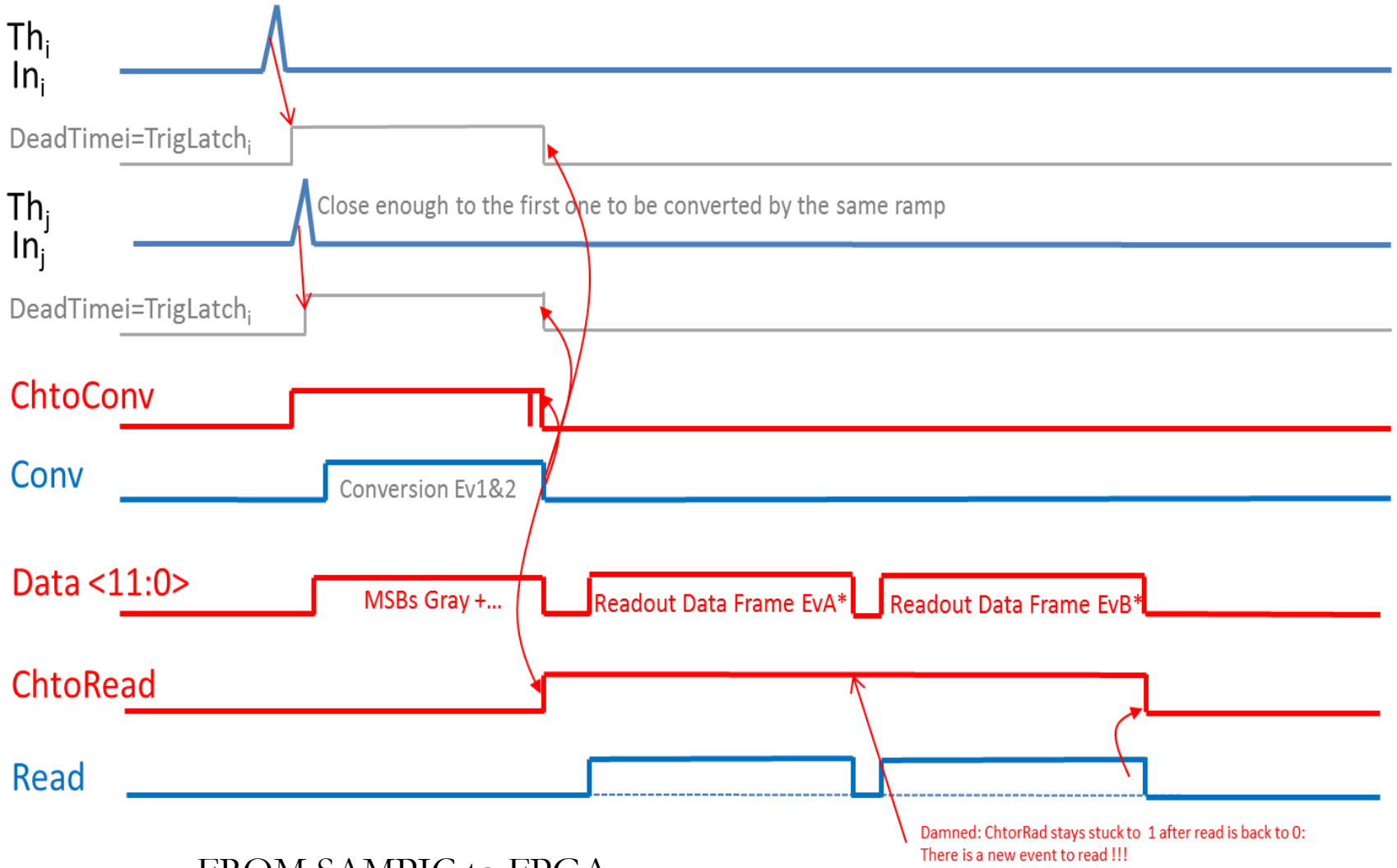
MULTIPLE HITS, 1 CHANNEL



HITS ON 2 CHANNELS, 2 CONVERSIONS



HITS ON 2 CHANNELS, SIMULTANEOUS CONVERSIONS

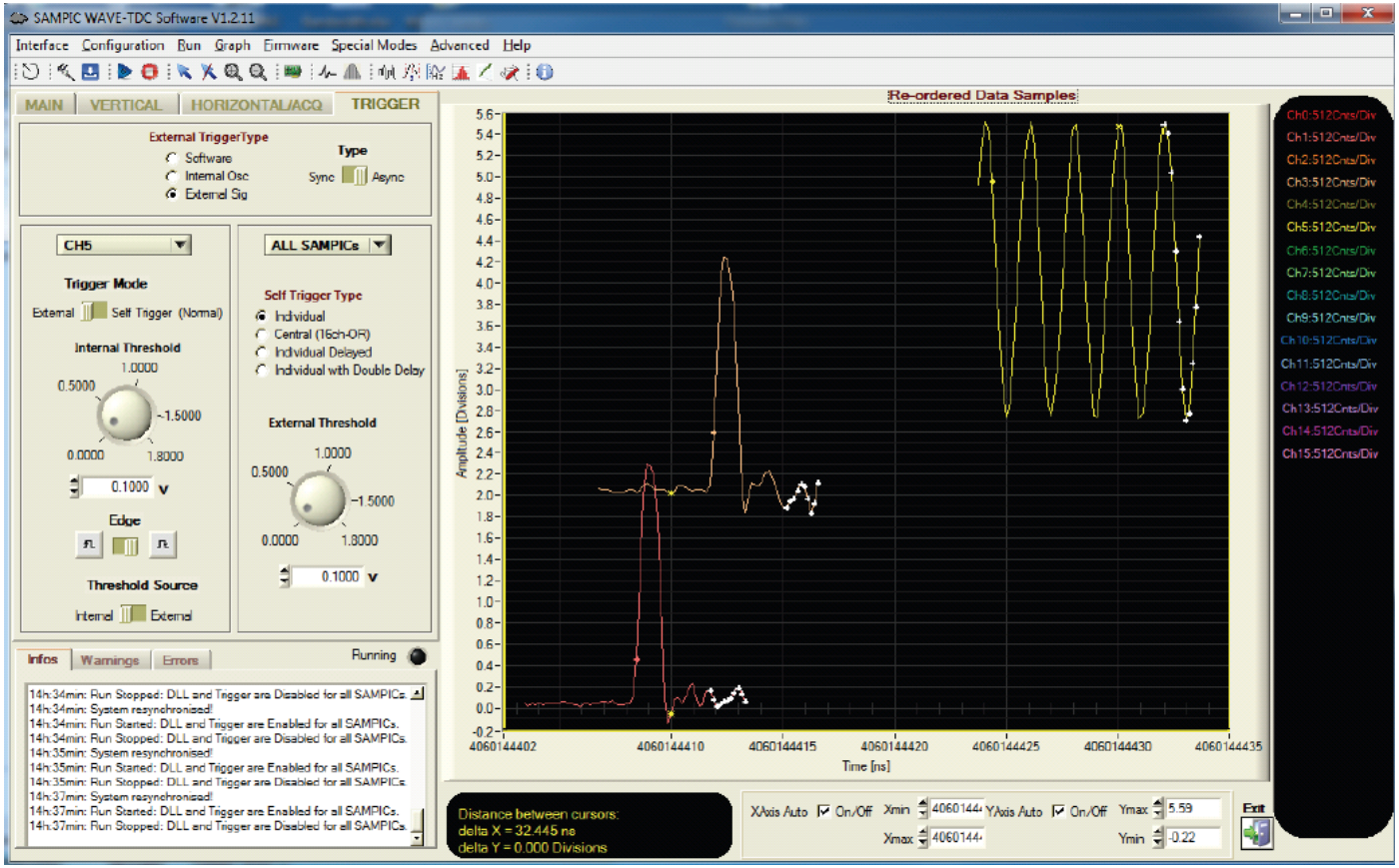


THE ACQUISITION BOARD (LAL)

- Mezzanine board for 16 channels
- Mother board can hold 2 mezzanines: **32-channel system**
- MXC connectors
- **USB** – Ethernet – Fiber Optic readout
- 5V voltage supply – 1Amp
- Windows software
- 3 modules are currently available

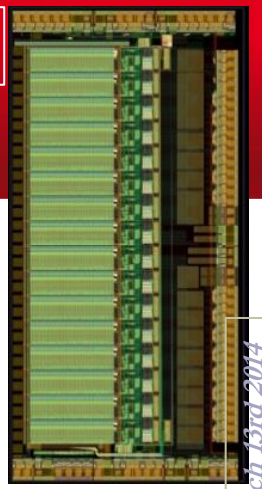
THE ACQUISITION SOFTWARE (LAL)

- Usable for test
- Already usable for small size experiment.
- Special visualization for WTDC mode



TEST STATUS

Only 10 kE prototyping !!!



AMS0.18: 7mm²

- **Everything is working well excepted**:
  - **ROI readout**: fail in some cases => we read the whole depth
  - **Central trigger**
  - These 2 features are not absolutely necessary (and can be easily corrected)
  - **The chip is usable as it is**
- Sampling is ok :
  - from 3 to 8.2 GSPS on all the channels
  - up to 10 GSPS on 8 channels
  - Not tested under 3 GSPS
- **Readout ok @ 80MHz**. To be tested at higher frequency
- No evidence of cell Leakage. **Data not damaged for storage times of few tens µs**

POWER CONSUMPTION: 0.18W @ 6.4 GSPS (1.8V SUPPLY)

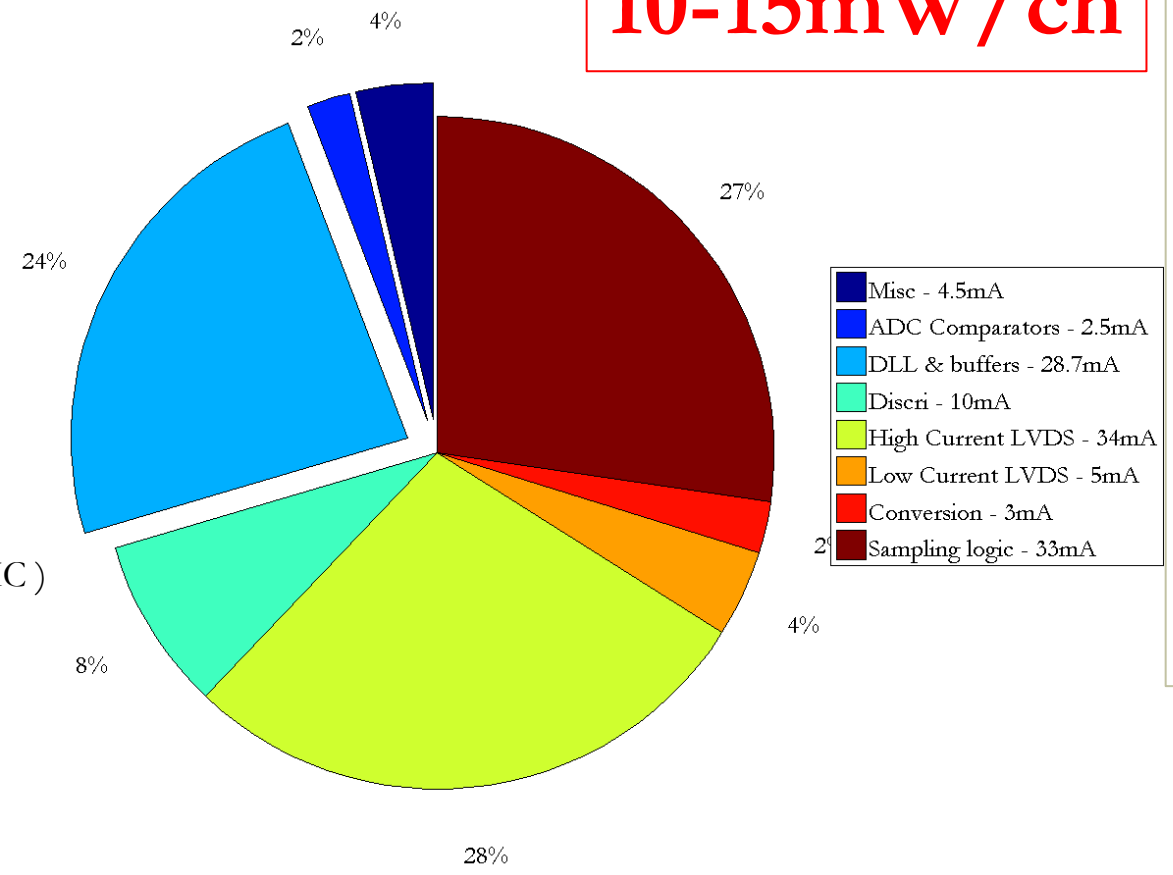
Analog (20mW):

- Discriminator: 1.1mW/ch
- ADC: 2µW/cell=> 130µW/ch

Digital: 10mW

- DLL: 51 mW
- Sampling logic & ROI : 60mW
- LVDS output: 9 mW (LC) -70mW (HC)
- Misc: 10mW

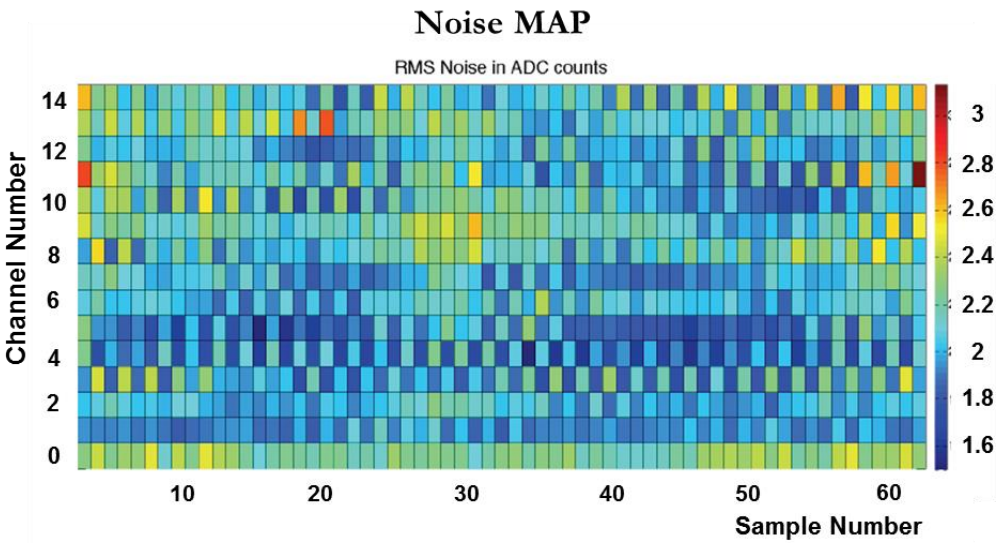
10-15mW/ch



SamPic power consumption - 120mA High Current LVDS - 84mA Low Current

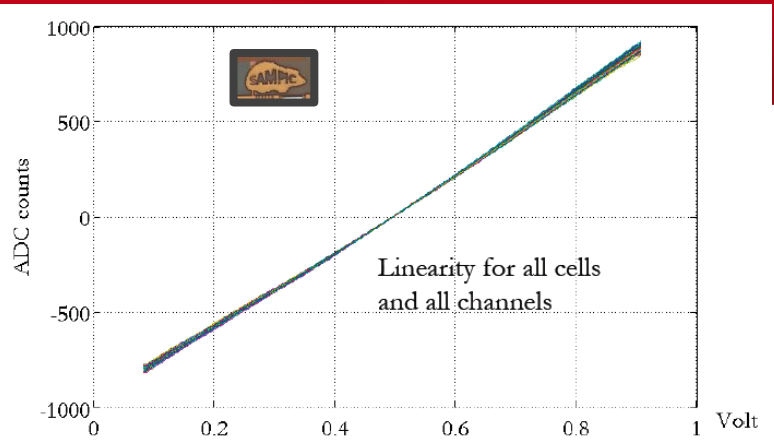
SAMPIC DIGITIZATION/NOISE

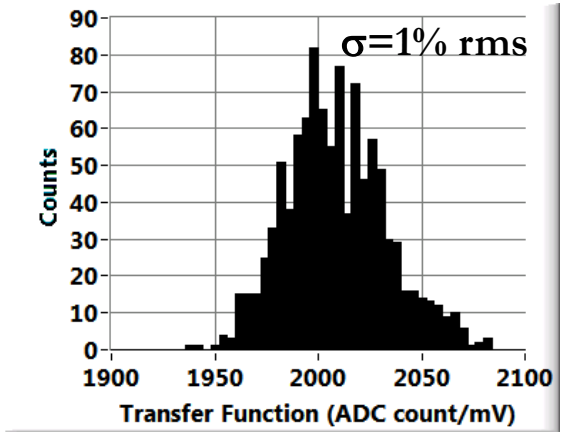
- Wilkinson conversion works as expected with 1.3 GHz clock
- 0.5mV /ADC count
- 1V dynamic/ 11bit in 1.6µs
- Cell/cell pedestal spread = 5 mV rms => easily calibrated and corrected
- After correction: average noise is 1 mV rms
- Noisiest cells are at 1.5 mV rms
- unchanged with sampling frequency
- Also tested in 9 bit mode
  - LSB = 2 mV
  - Only 15% noise increase
- **~10 bit rms range**



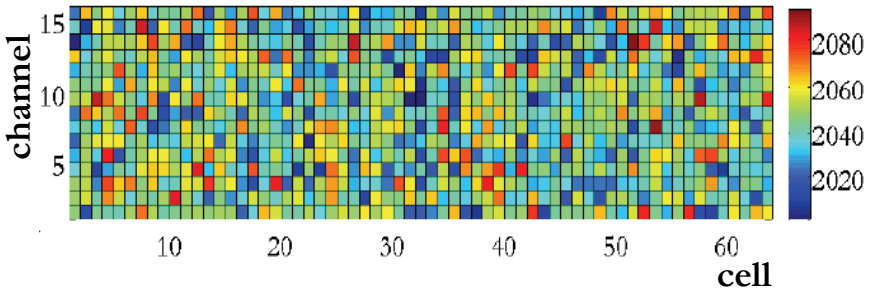
ADC TRANSFER FUNCTIONS

- Cell-to-cell spread of slopes = 1% rms with random distribution (not related to channel
- 3% peak to peak integral non-linearity
- Both effects are systematic and due to charge injection by switches
- Can be corrected after calibration. If not, it degrades the resolution to ~7-8 bit rms

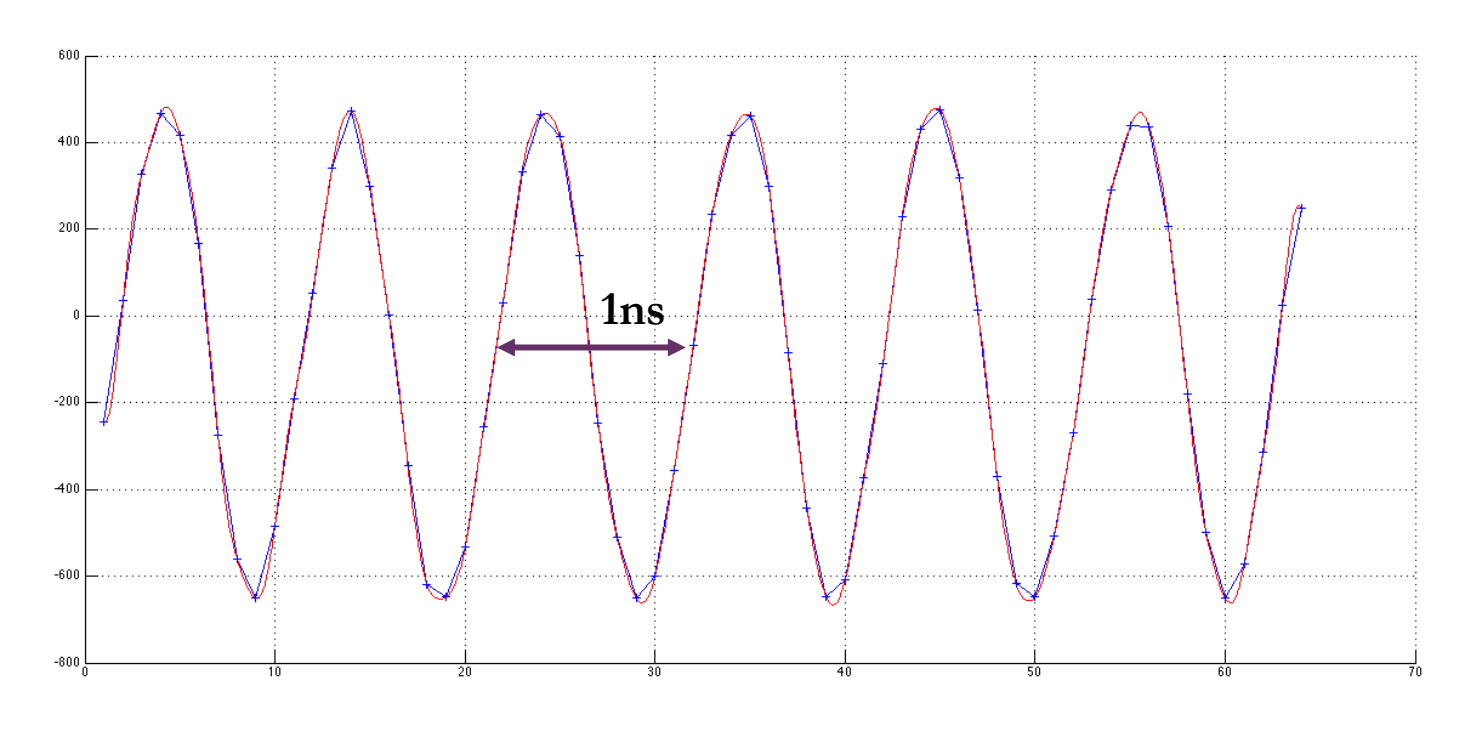




- **Already good results if not corrected**
- **Now corrected by software together with pedestals using a 2nd degree polynomial.**

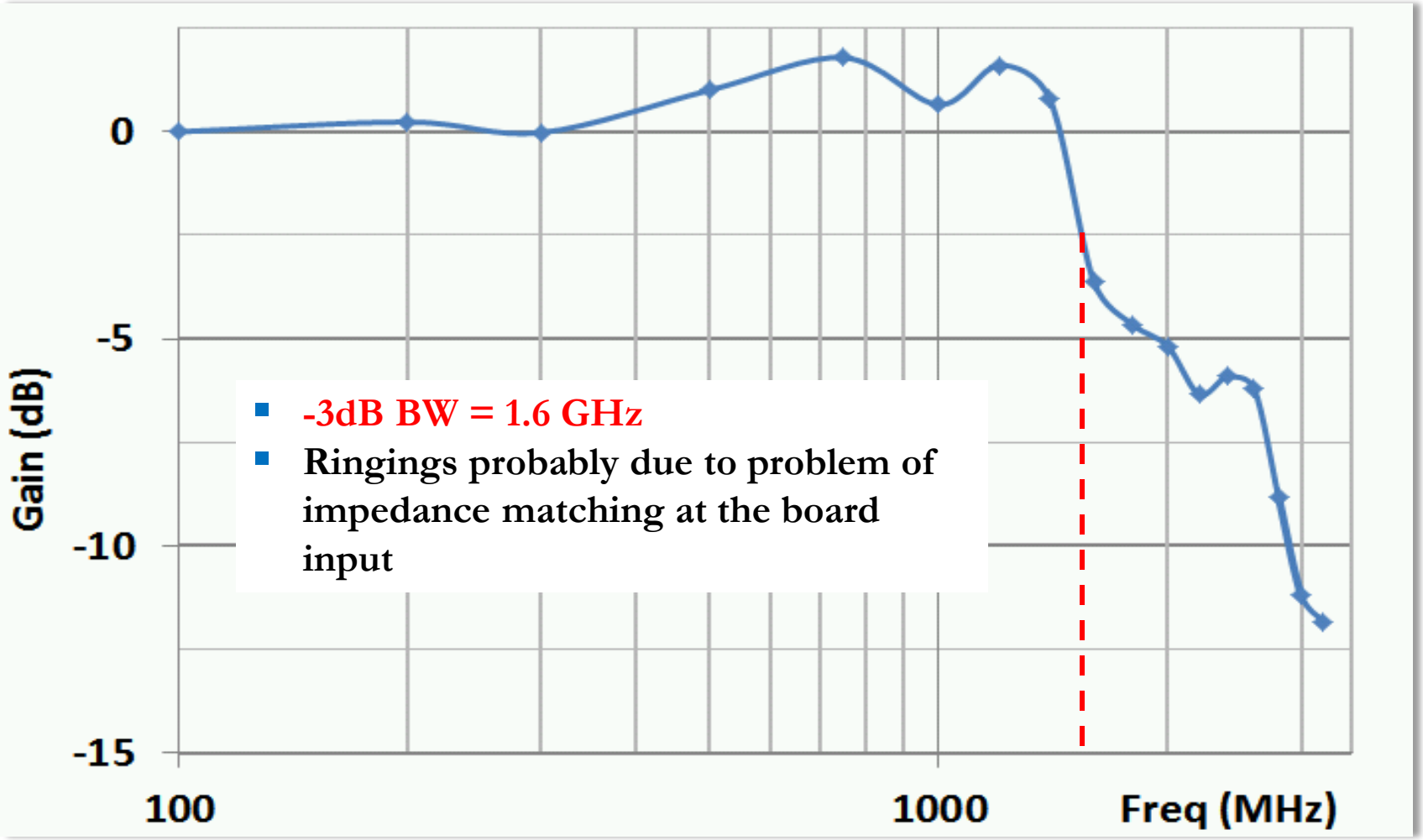


QUALITY OF SAMPLING



- 1 GHz sinewave (0.5V peak-peak) 64 samples
- 'out of the box' (only pedestal correction) @ 10.2 GSPS
- 64 usable data points
- Already looks good

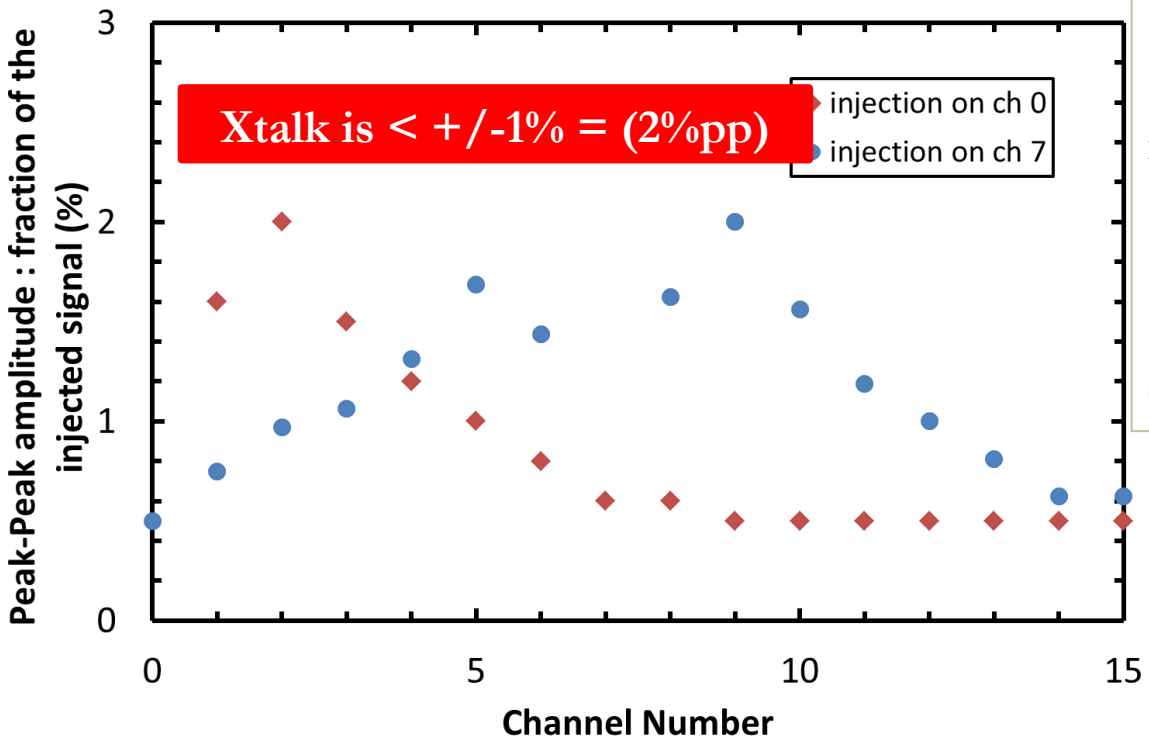
BANDWIDTH



- -3dB BW = 1.6 GHz
- Ringings probably due to problem of impedance matching at the board input

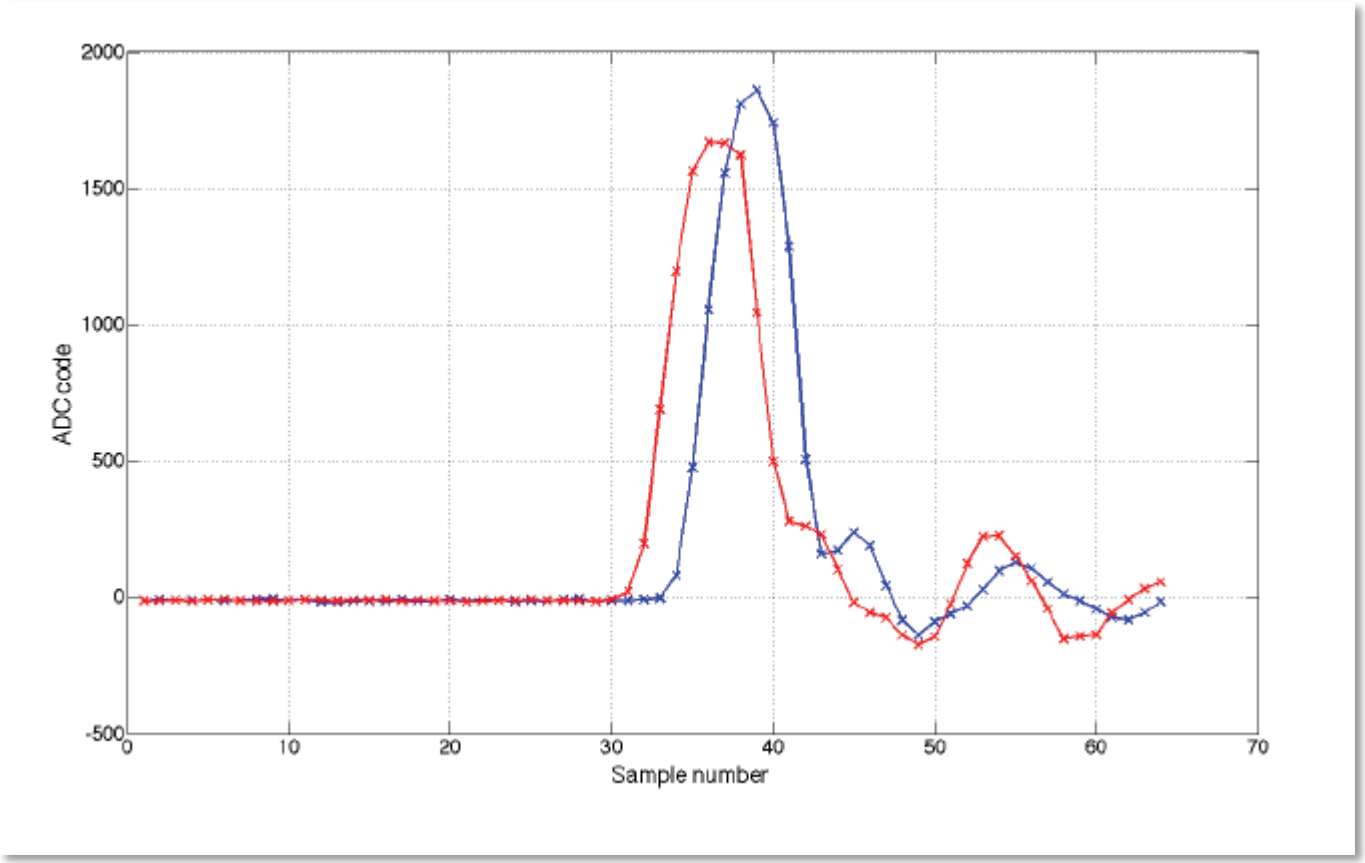
SAMPIC0: XTALK MEASUREMENT

- 800mV, 1ns FWHM, 300ps risetime and falltime injected on **channel 7(blue)**
- Signal measured on the other channels
- Xtalk = derivative and decrease as the distance to the injection channel
- Xtalk signal is bipolar with ~ equal positive and negative lobe
- Similar plot, but shifted if injection in another channel **(red)**



PULSES RESPONSE

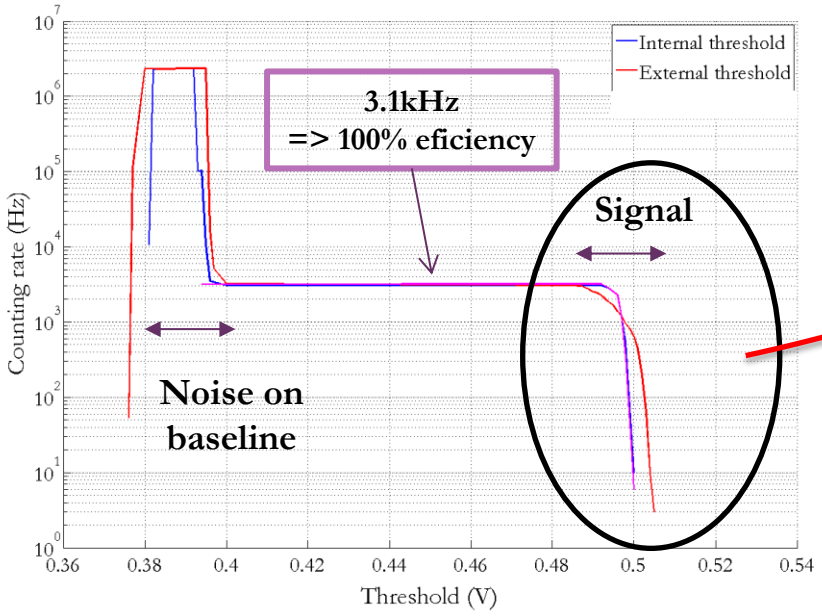
- Further tests made with **1ns-FWHM** pulse split in 2. 1 output delayed by cable => 0.9V amplitude
- 6.4 GSPS sampling
- Self triggered

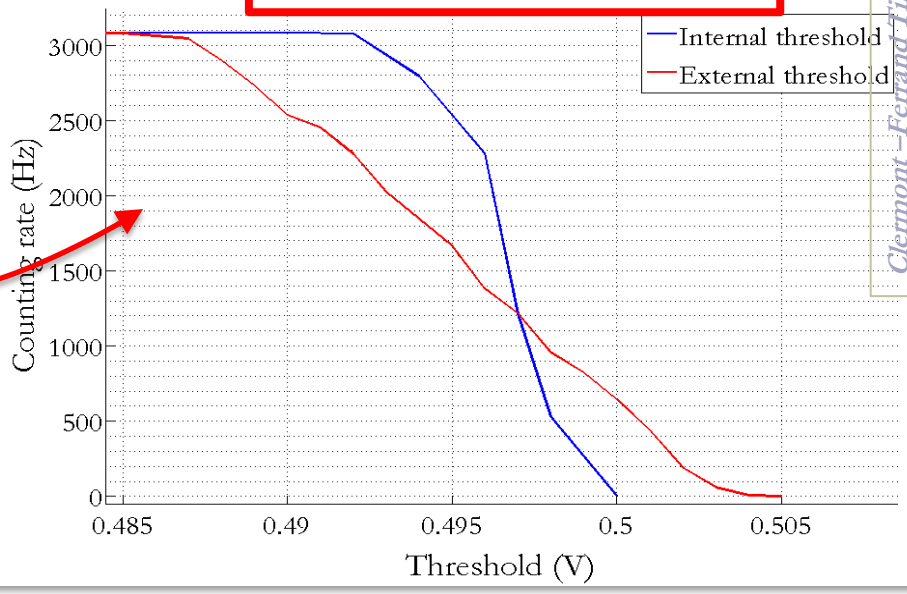


SELF-TRIGGER EFFICIENCY AND NOISE

- Input is 150 mV 1 ns wide pulses (3.1 kHz repetition rate)
- Threshold (internal or external) sweep => trigger efficiency curve
- Discriminator Noise extraction by fitting the S curve by en error function
- **Better noise if threshold internally set**

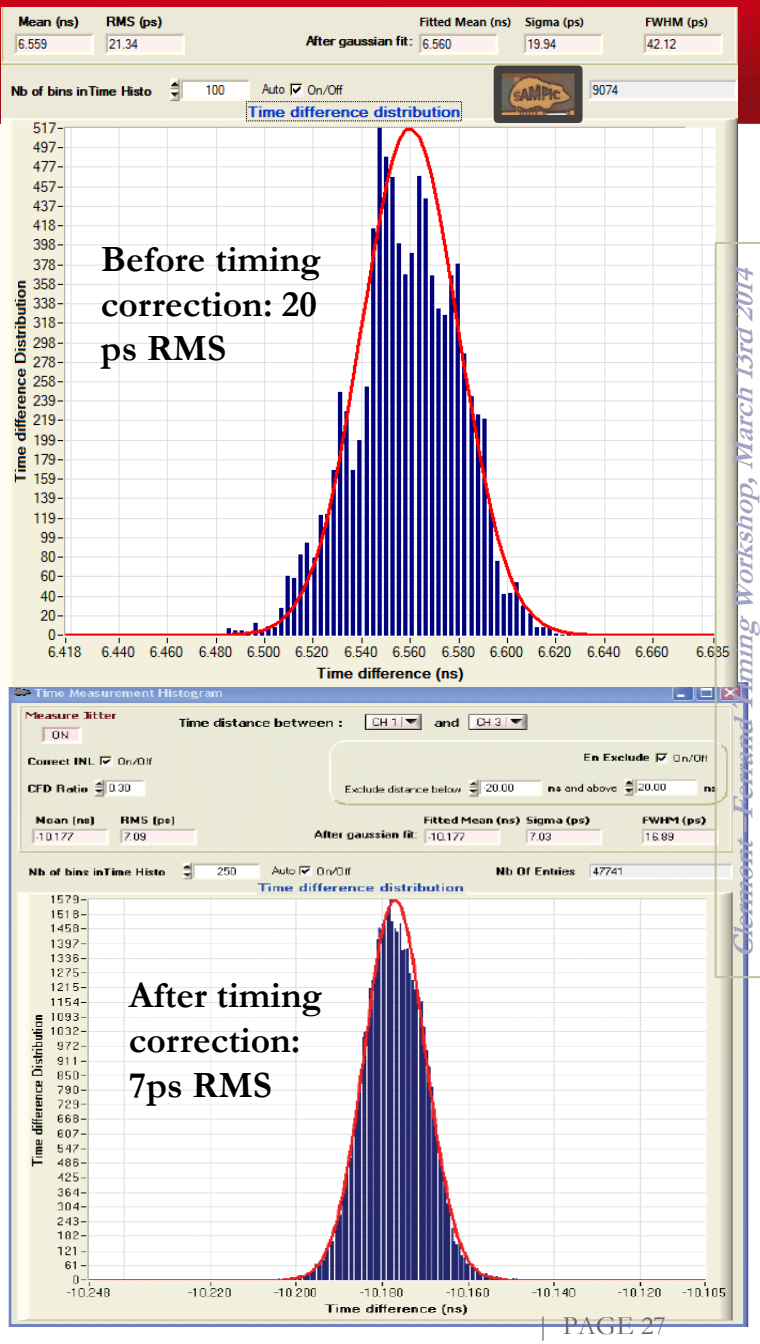
Discriminator noise:
Int threshold :2 mV rms
Ext threshold: 8 mV rms



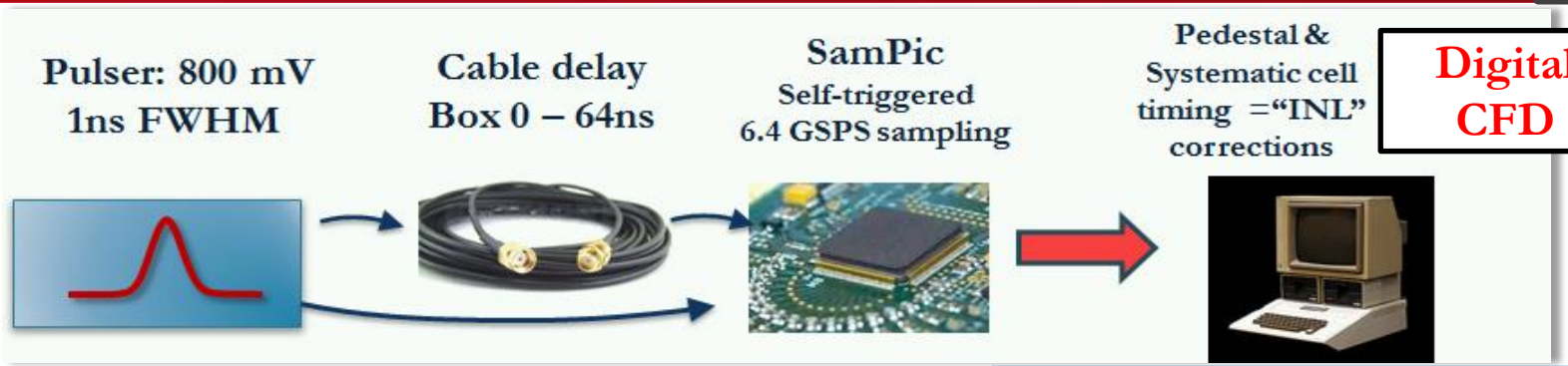


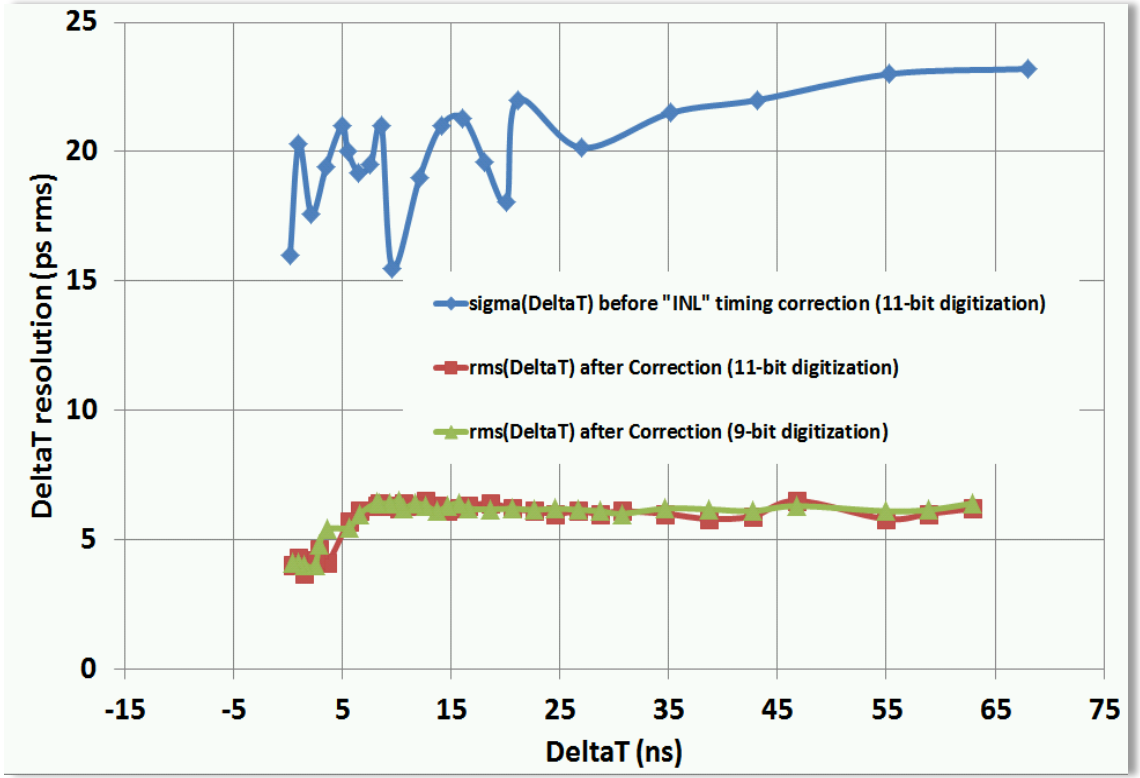
TIMING RESOLUTION (PEDESTAL CORRECTED ONLY)

- First measurement: 2 pulses with 10ns distance. ,1Ns FWHM, 800mV, 3 kHz rate
- Measurement performed for 6.4 GPSPS sampling
- **20 ps rms ΔT resolution before any correction => already not so bad.**
- **7 ps rms ΔT resolution after INL timing correction**
- No tail in the distribution.
- **No hit "out of time" due to metastabilities, problem of boundaries between ranges, …**



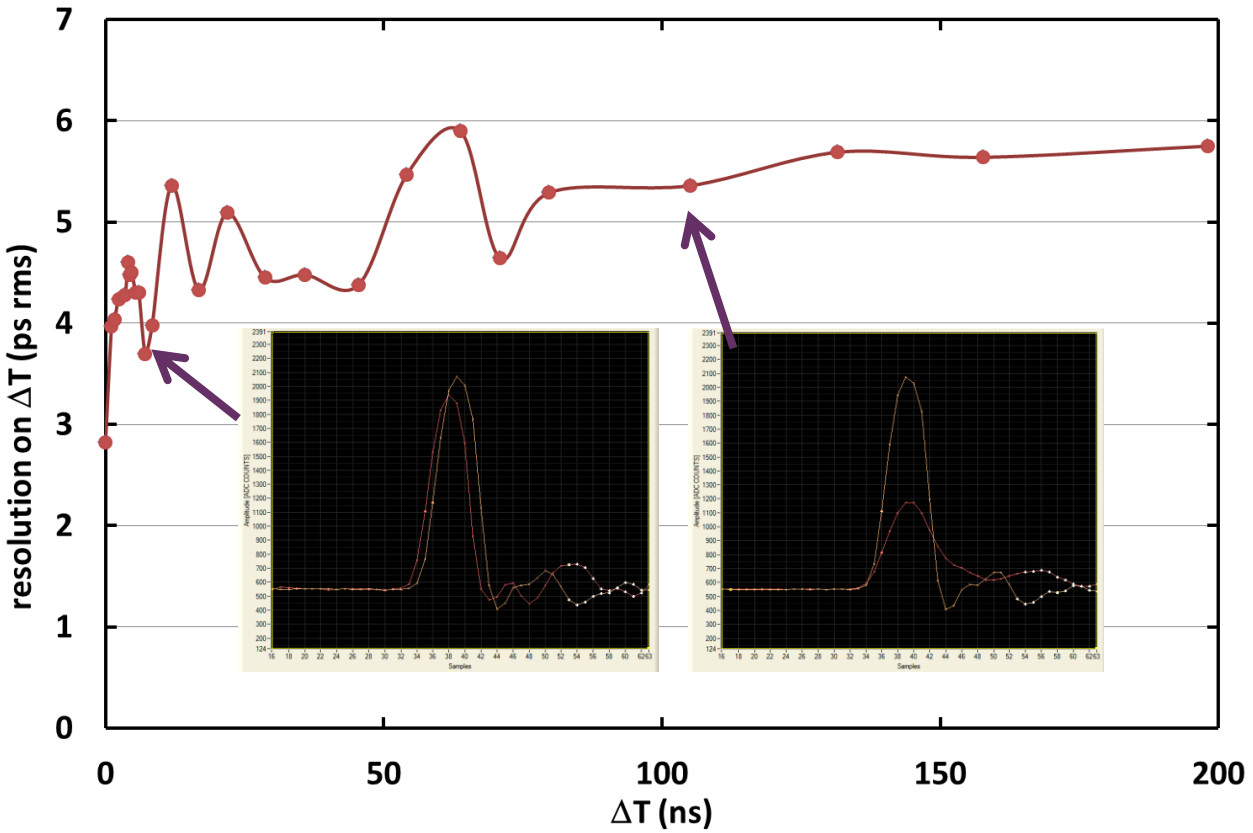
ΔT MEASUREMENTS. ONLY PEDESTAL CORRECTION





- <15 ps RMS = (22/√2) single pulse timing resolution without any timing calibration (short DLLs)
- <5 ps RMS timing resolution on single pulse after timing "INL" correction
- Resolution vs ΔT is FLAT after 10ns
- Same results in 9-bit/400ns mode
- Correction of ADC gain spread and non-linearity not applied yet

TIMING RESOLUTION, PULSER LECROY (AFTER CELL GAIN EQUALISATION)- DIGITAL CFD



- 11bit mode/6.4 GSPS
- 1ns FWHM, 400ps Tr pulses with 700mV amplitude.
- 2 identical pulses with one of them delayed by cables
- Risetime is x1.5 and amplitude /2.2 after 100ns delay !!!
- **Over all the range :**
  $\sigma(\Delta T) < 6$ps rms
  => $\sigma(T) < 4.4$ps rms

For delays > 10ns, the 2 pulses are no more recorded during the same DLL cycles !

TIMING RESOLUTION VS AMPLITUDE & RISETIME (1 NS FWHM)- CFD ALGORITHM

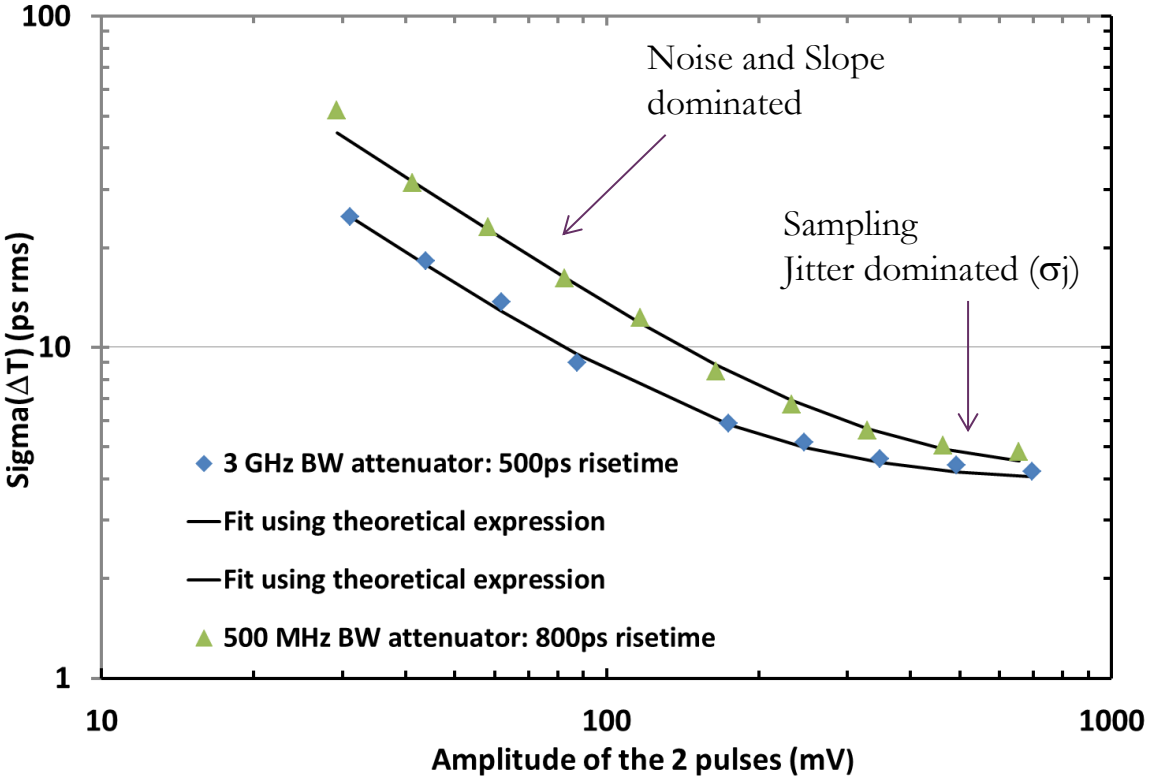
- Theoretical expression is:

$$\sigma(\Delta t) = \sqrt{2} \times \sqrt{{\sigma_j}^2 + \left(\frac{\alpha}{Amp}\right)^2}$$

with $\alpha = \frac{\sigma_n}{Nslope}$ (σ_n is the noise)

where $Nslope = \frac{1}{Amp} \times \frac{dV}{dt}$ is the normalized signal slope

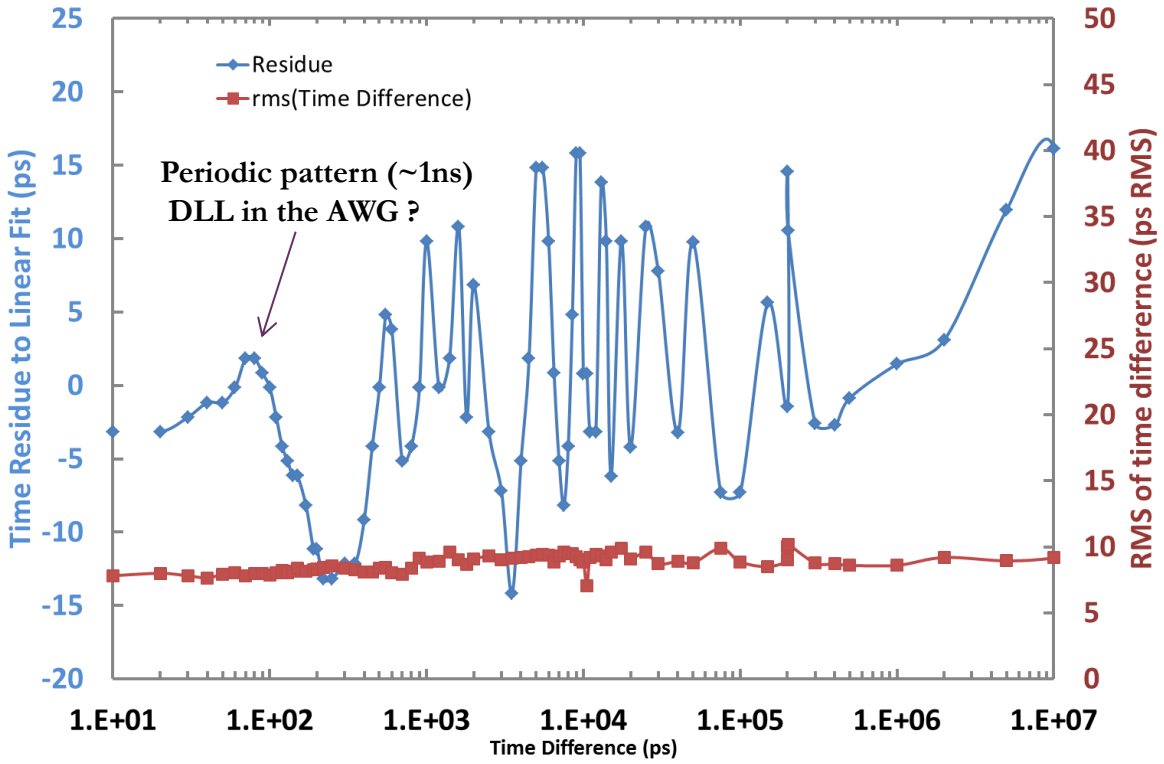
- σ_j and α extracted by fit
- σ_n extracted from α is ~ 1mV rms
- Measurements in good agreement with the theory



Atten. BW (GHz)	σj fit (ps rms)	α fit (ps.mV)	Nslope (ns^{-1})	Calc σn (mV rms)
500	2.82	919	1.33	1.2
3	2.76	538	1.88	1.0

« ABSOLUTE » TIME MEASUREMENT ?

- Now we use a TEK 3052 arbitrary waveform generator
- Slower than Lecroy one's (2.5ns risetime)
- We use the 2 channels of the pulser and program their delay (step of 10ps)
- Generator specified for few 10 ps delay precision and 100ps jitter (clearly better)



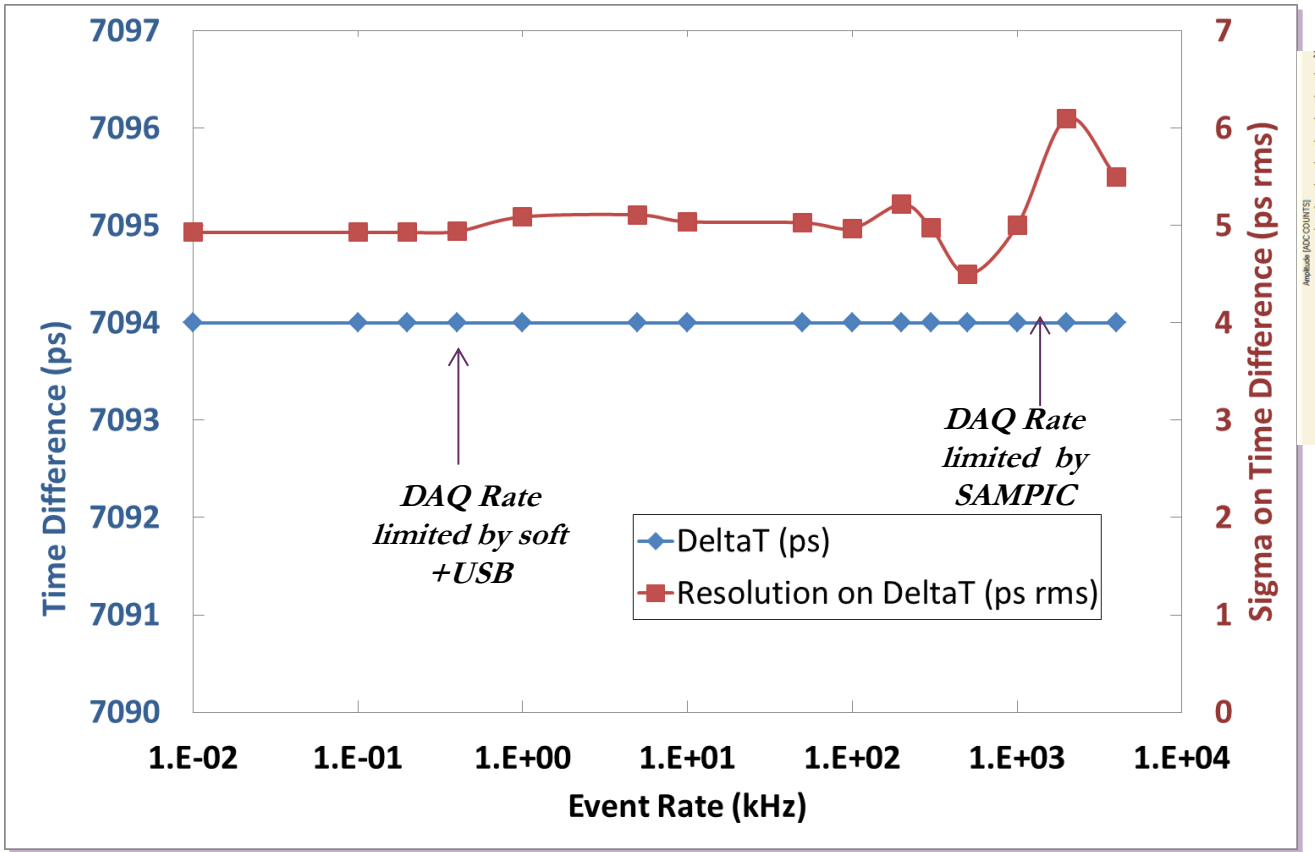
- Resolution on time difference is < 10ps RMS, even for delays up to 10 µs = 1ppm resolution
- Linear fit of the time difference vs delay programmed in the AWG:
- Slope =1 +1.3E-6 => ~ppm relative precision of the oscillators od SAMPIC and of the AWG
- Residue to the fit within +/-15ps up to 10µs delay

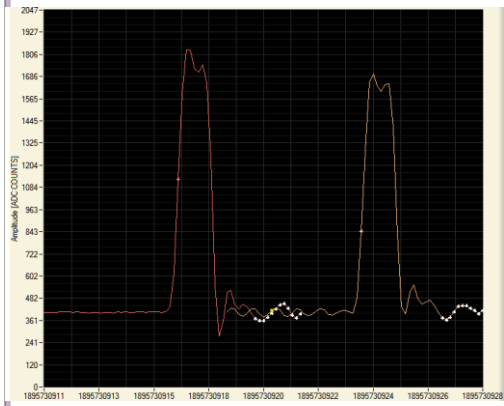
«TIMING RESOLUTION VS RATE

1ns FWHM, 0.4ns risetime, 0.7V signals sent to 2 channels of SAMPIC (splitted)

- 7.1ns delay by cable, 6.4 GSPS. 11 bit mode, 64 samples, everything corrected
- Rate is progressively increased.

No change of delay measured or of resolution up 2 MHz rate !!!





WORK PLANNED OR IN PROGRESS

- Improvements of Firmware and DAQ software in progress (daily)
- Characterization @ 8.2 and 10 GSPS => no drastic change on performance (with our test signals available)
- Characterization @ low (3GSPS or less) sampling rate "PM mode".
- Timing characterization with detectors/ test beams.

  * 3 setups are already existing., one lent to TOTEM

  * We plan to produce 3 more ones => possible collaborations for measurements
- Characterization in fastest conversion/less resolution mode
- New submission planned for Mid 2014 :
  - correction of the identified bugs
  - Nb of bits for timestamp => 18 bits
  - Improved "central trigger" (coincidence & or)
  - **channels could be merged by groups of 2 or 4 to be used as multiple buffers**

SAMPIC0: SUMMARY

		Unit
Technology	AMS CMOS 0.18µm	
Number of channels	16	
Power consumption	180 (1.8V supply)	mW
Discriminator noise	2	mV rms
SCA depth	64	Cells
Sampling Speed	<3-8.4 (10.2 for 8 channels only)	GSPS
Bandwidth	1.6	GHz
Range (Unipolar)	1	V
ADC resolution	8 to 11 (trade-off time/resolution)	bit
SCA noise	<1.3	mV rms
Dynamic range	9.6	Bit rms
Conversion time	0.2-1.6 (8bit-11bit)	µs
Readout time (can be probably be /2)	25 + 6.2/sample	ns
Time precision before correction	15	ps rms
Time precision after timing INL correction	< 5	ps rms

CONCLUSION

A self-triggered WTDC chip demonstrator has been designed and characterized:

- Works well with expected performance:
  - 1.6 GHz BW
  - up to 10 GSPS
  - Low noise (trigger and acquisition)
  - < 5ps rms timing resolution
- Already meets our initial requirements
- Already usable for tests with detectors
- Work ongoing on:
  - DAQ System (firmware + software) optimization
  - Existing chip fine characterization
  - Second prototype

THANK YOU FOR YOUR ATTENTION

BACKUP SLIDES

WHY AMS 0.18µ ?

- Based on IBM0.18µm : IBM quality & documentation
- Good Standard Cells Library
- Good lifetime foreseen (HV module, automotive)
- **1.8V power supply: nice for analog design/ high dynamic range**
- **Reasonable leakages**
- Good noise properties (already checked with IdefX chips for CdTe)
- Reasonable radiation hardness
- Less complex (and less expensive) than IBM 0.13µm
- AMS high quality Design Kit
- Easy access (CMP, Europractice, AMS)