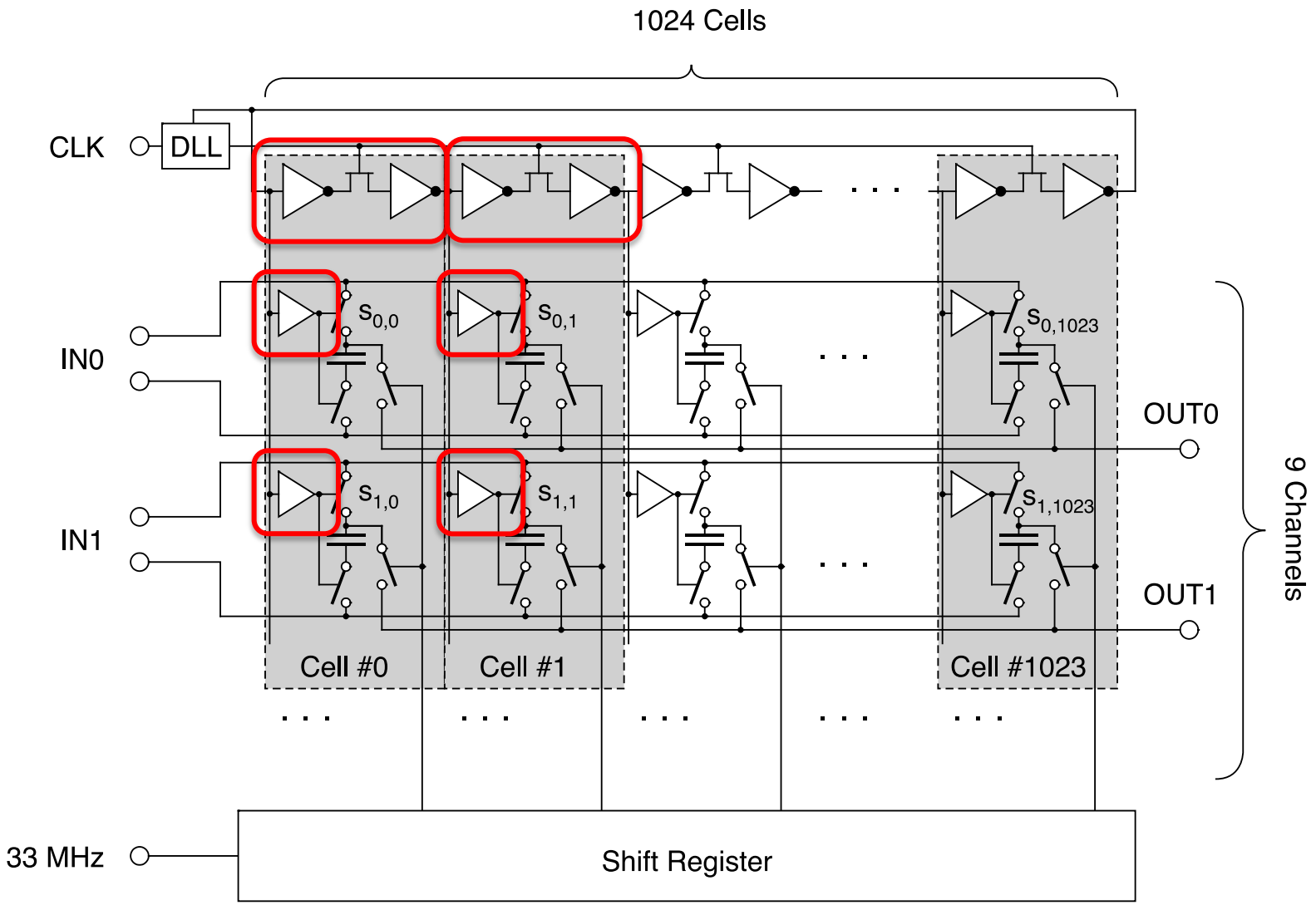
Stefan Ritt, Paul Scherrer Institute, Switzerland

A NEW TIMING CALIBRATION METHOD FOR SWITCHED CAPACITOR ARRAY CHIPS TO ACHIEVE SUB-PICOSECOND RESOLUTIONS

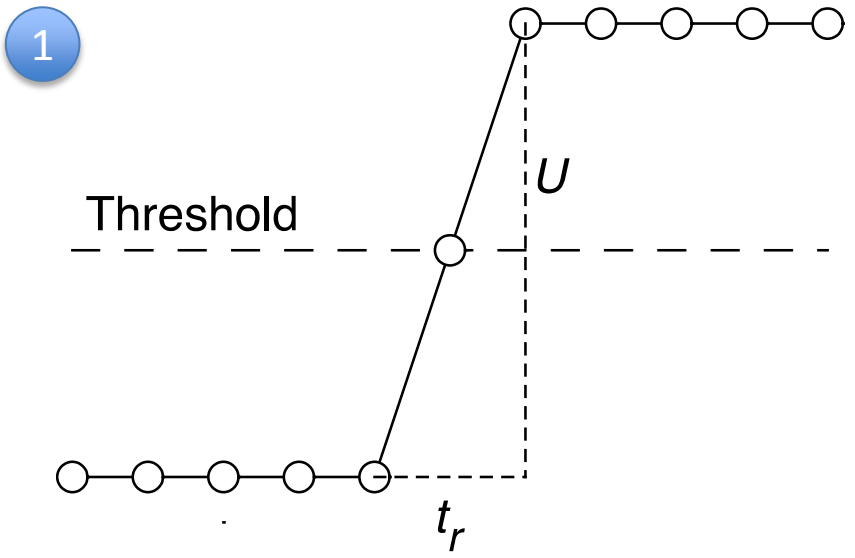
Overview

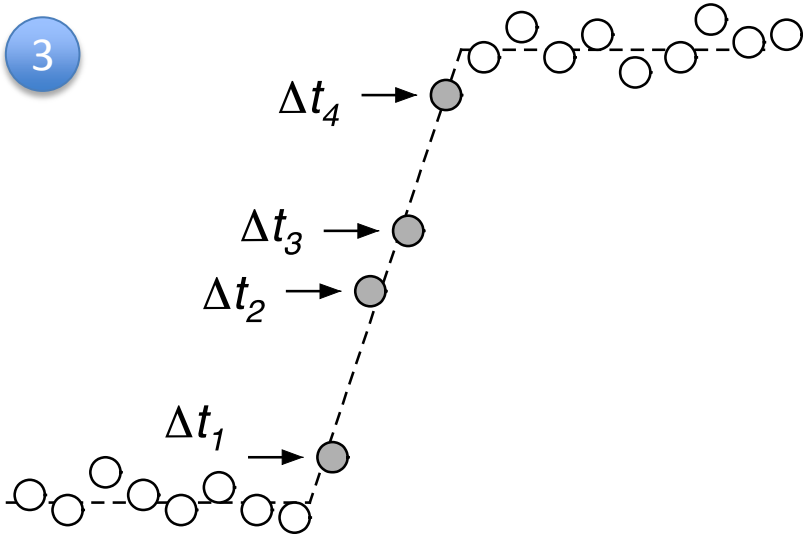
- Limitations of timing resolutions in Switched Capacitor Arrays (SCA)
- New method for SCA calibration
- Results

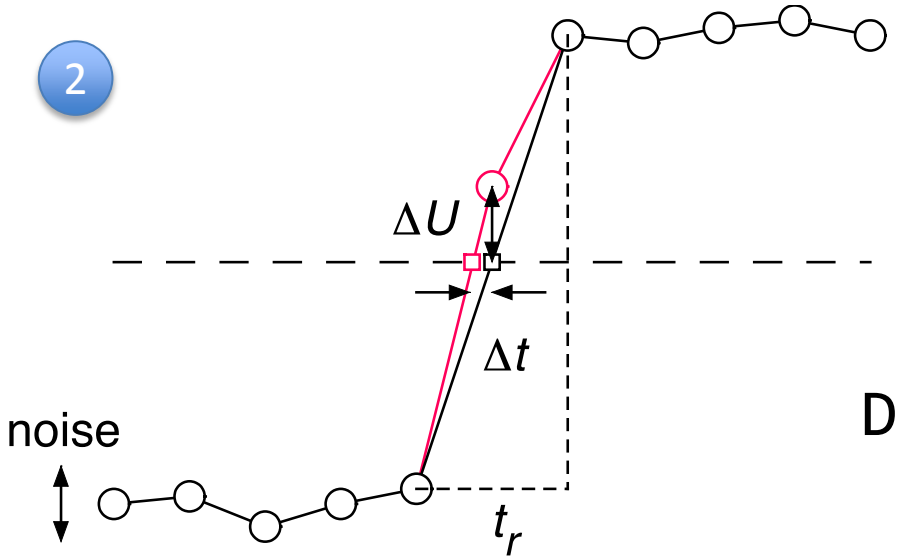
Schematic Overview (DRS4)



Noise limited time accuracy







$$\frac{\mathrm{D}U}{\mathrm{D}t} \approx \frac{U}{t_r} \longrightarrow \mathrm{D}t = \frac{\mathrm{D}U}{U} \cdot t_r$$

$$\mathrm{D}t = \frac{\mathrm{D}U}{U} \cdot t_r \cdot \frac{1}{\sqrt{n}} = \frac{\mathrm{D}U}{U} \frac{t_r}{\sqrt{t_r f_S}} = \frac{\mathrm{D}U}{U} \cdot \frac{\sqrt{t_r}}{\sqrt{f_S}}$$

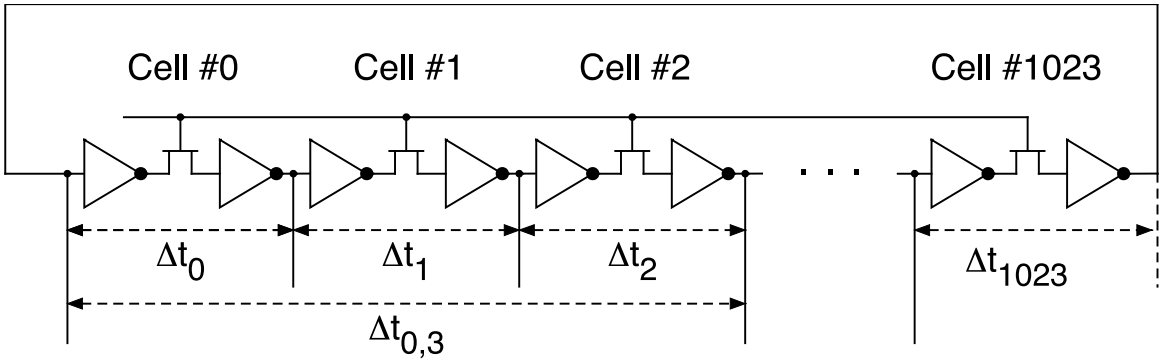
A few examples

U [mV]	DU[mV]	t_r [ns]	f_{3dB} [MHz]	f_S [GSPS]	Dt [ps]	
10	1	1	333	3	60	
100	1.8	1	333	2	13	TARGET
100	0.65	1	333	3	3.8	SAM
100	0.7	0.23	1500	10	1.9	PSEC4
100	0.35	0.36	950	5	1	DRS4

- Small (<20 mV) signals give poor timing
- Theoretical limit for TARGET/SAM/PSEC4 is reached
- Limit for DRS4 is lower than current resolution (O(20ps))

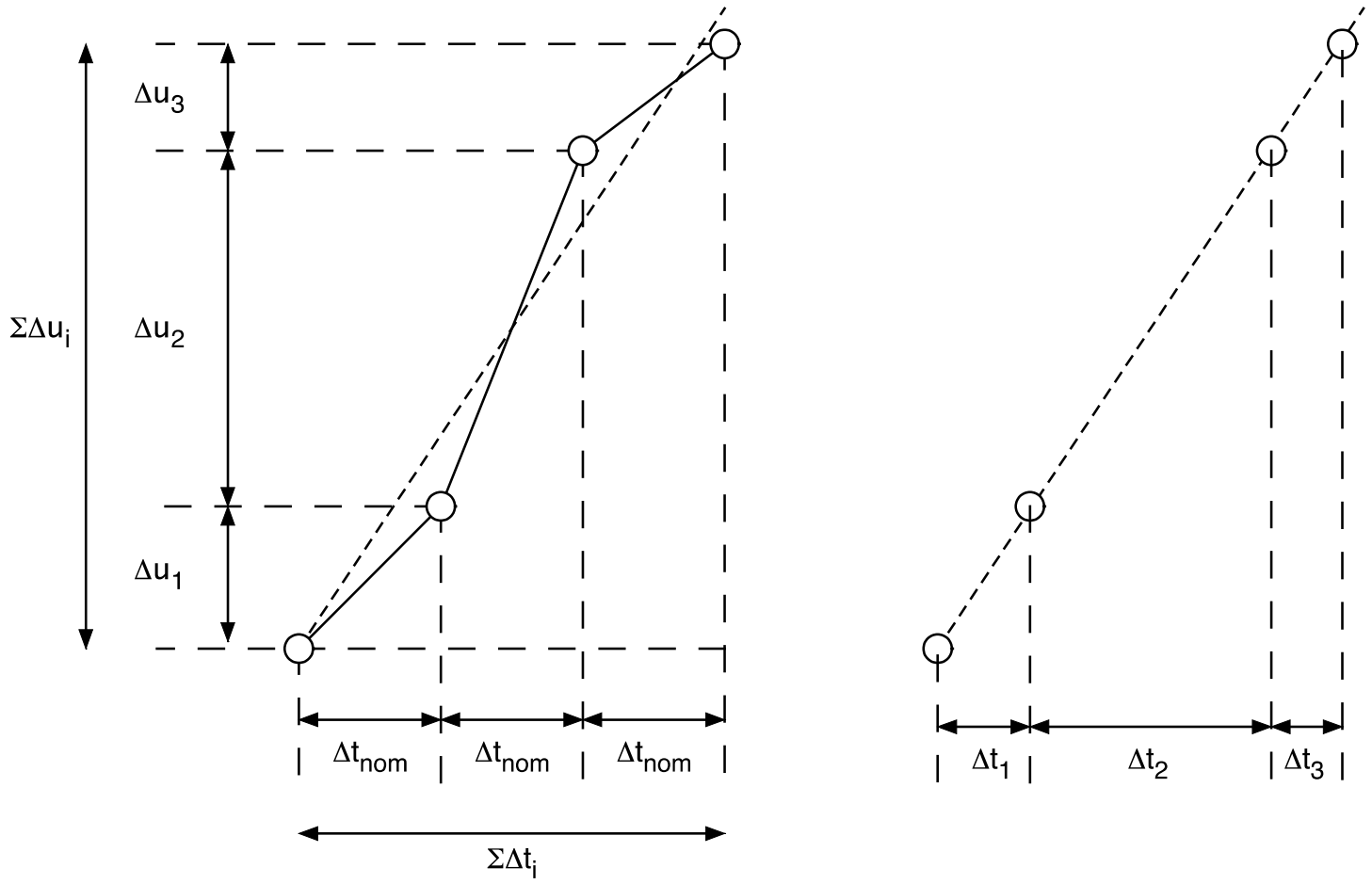
  What is the reason for this?

Time definition



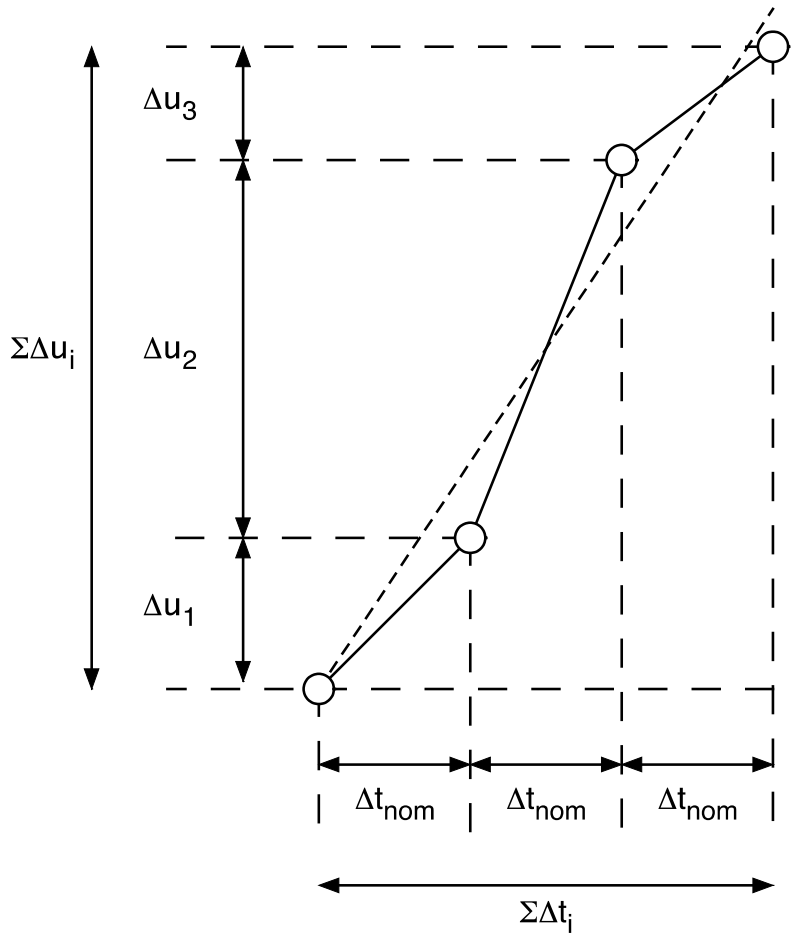
- single inverter delay: $\Delta t_i \rightarrow$ *differential* nonlinearity
- Sum of single inverter delay: $\Delta t_{a,b} = \Sigma \Delta t_i \rightarrow$ *integral* nonlinearity

Local Calibration



Credits: D. Stricker-Shaver, Univ. Tübingen, NSS/MIC 2012 proceedings

Local Calibration

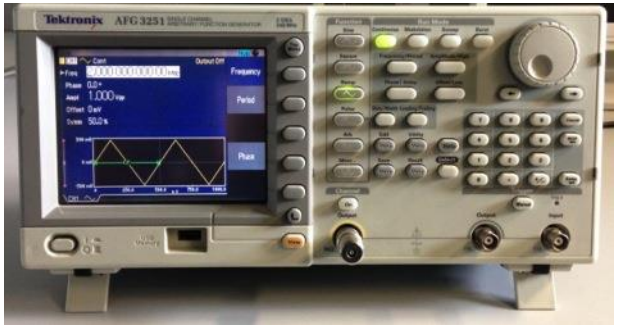


$$\frac{\mathrm{D}t_i}{\mathrm{D}U_i} = \frac{\sum \mathrm{D}t_i}{\sum \mathrm{D}U_i}$$

$$\sum_{i=0}^{1023} \mathrm{D}t_i = \frac{1024}{f_{sampling}}$$

$$\mathrm{D}t_i = \mathrm{D}U_i \cdot \frac{\frac{1024}{f_{sampling}}}{\sum \mathrm{D}U_i}$$

How to calibrate?



- External function generator
  - Not convenient for re-calibration
  - Arbitrary waveform generation has ~20 ps jitter
- FGPA: LVDS output with slew rate limitation
  - Anything coming from an FPGA has 50-100 ps jitter
- Dedicated quartz oscillator
  - Can be on-board
  - Generate sine wave via passive low-pass filter
  - Only use region around zero as linear slope

Oscillator

PERFORMANCE PLASTIC PACKAGE ULTRA MINIATURE PURE SILICON™ CLOCK OSCILLATOR

ASEMP

Moisture Sensitivity Level – MSL 1

RoHS Compliant

ASEMP Life Size 3.2 x 2.5 x 0.85 mm

FEATURES:
- Ultra Miniature Pure Silicon™ Clock Oscillator
- High Performance MEMS Technology by Discera
- Low Power Consumption for high speed communication
- Exceptional Stability Over Temp. at -40 to +85°C, ±15ppm
- Extended Automotive Grade Temp. stability at -55 to +125°C, ±25ppm
- Available in 50kG Shock Resistance Configuration upon request
- MIL-STD-883 shock and vibration compliant
- Durable QFN Plastic Compact Packaging
- Standby or Disable Tri-state function
- Low jitter (Period jitter RMS and Phase jitter RMS)
- High power supply noise reduction, -50dBc

APPLICATIONS:
- Storage Area Networks (SATA, SAS, Fiber Channel)
- Passive Optical Networks (EPON, 10G-EPON, GPON, 10G-PON)
- Ethernet (1G, 10GBASE-T,/KR/LR/SR, FCoE
- HD/SD/SDI Video & Surveillance
- PCI Express
- Display port

Low Jitter High Performance 3G MEMS Technology!

Key Electrical Specifications – CMOS

Parameters		Minimum	Typical	Maximum	Units	Notes
Supply Current (I_{dd})		-----	31	35	mA	CL=15pF, 125MHz
Output Logic Level	V_{OH}	0.9*V_{dd}	-----	-----	V	I=±6mA
	V_{OL}	-----	-----	0.1*V_{dd}	V	
Rise Time	Tr	-----	1.1	2.0	ns	CL=15pF
Fall Time	Tf	-----	1.3	2.0	ns	20%/80%*VDD
Duty Cycle		45		55	%	
Integrated Phase Jitter (J_{PH})		-----	0.30	2	ps	200kHz ~ 20MHz@125MHz
		-----	0.38	2		100kHz ~ 20MHz@125MHz
		-----	1.70	2		12kHz ~ 20MHz@125MHz
Period Jitter RMS (J_{PER})		-----	3.0	-----	ps	

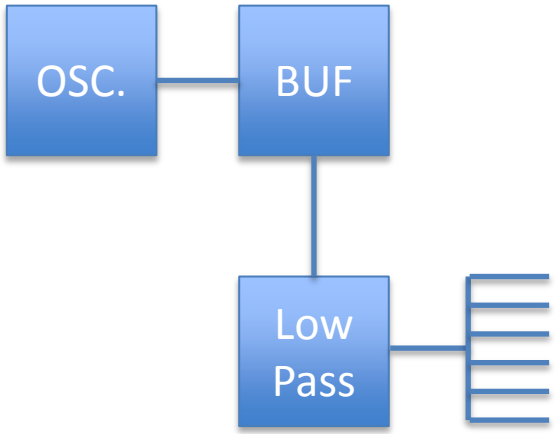
ABRACON IS ISO9001:2008 CERTIFIED

ABRACON CORPORATION

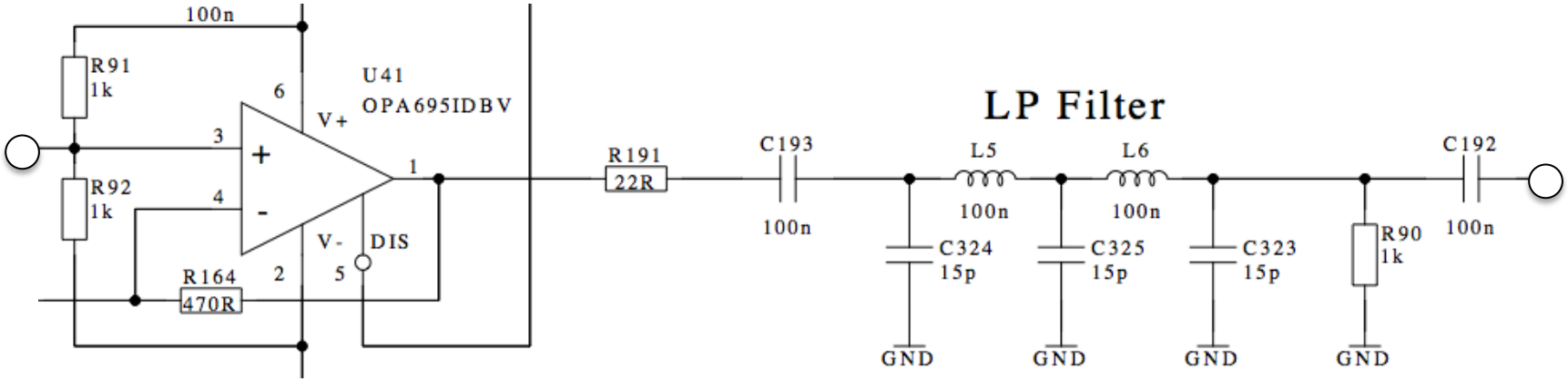
Visit www.abracon.com for Terms & Conditions of Sale **Revised: 07.16.12**

30332 Esperanza, Rancho Santa Margarita, California 92688
tel 949-546-8000 | fax 949-546-8001 | www.abracon.com

100 MHz

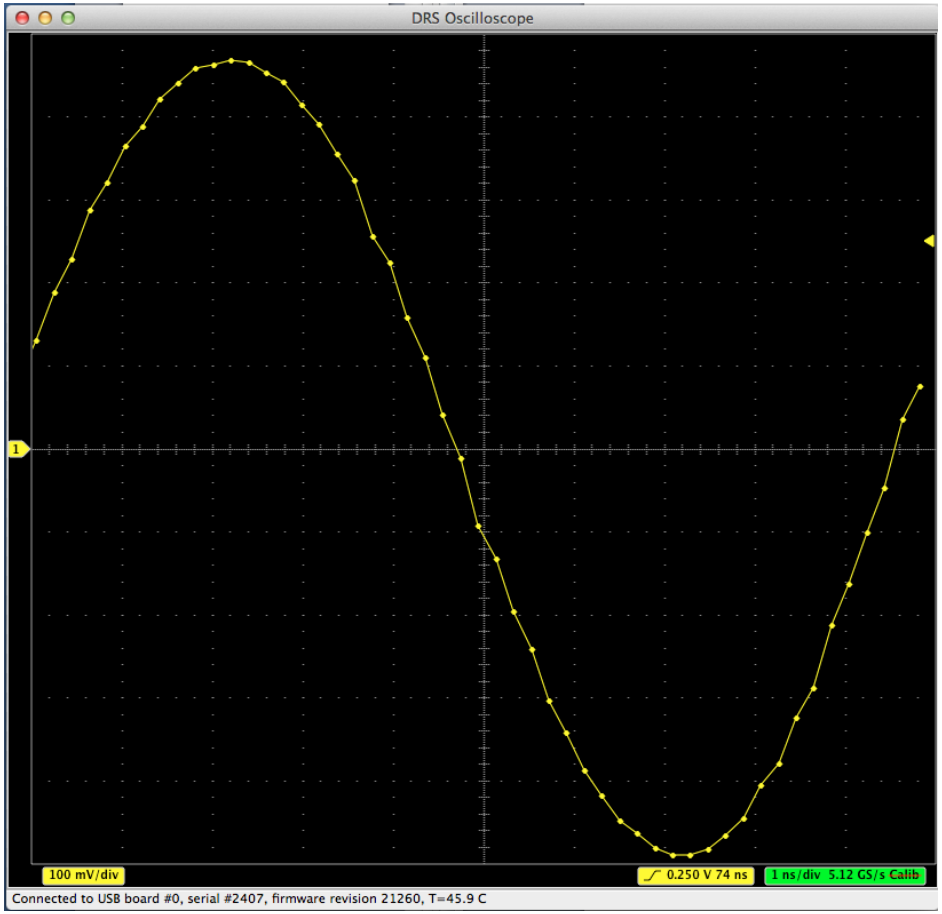


to all channels

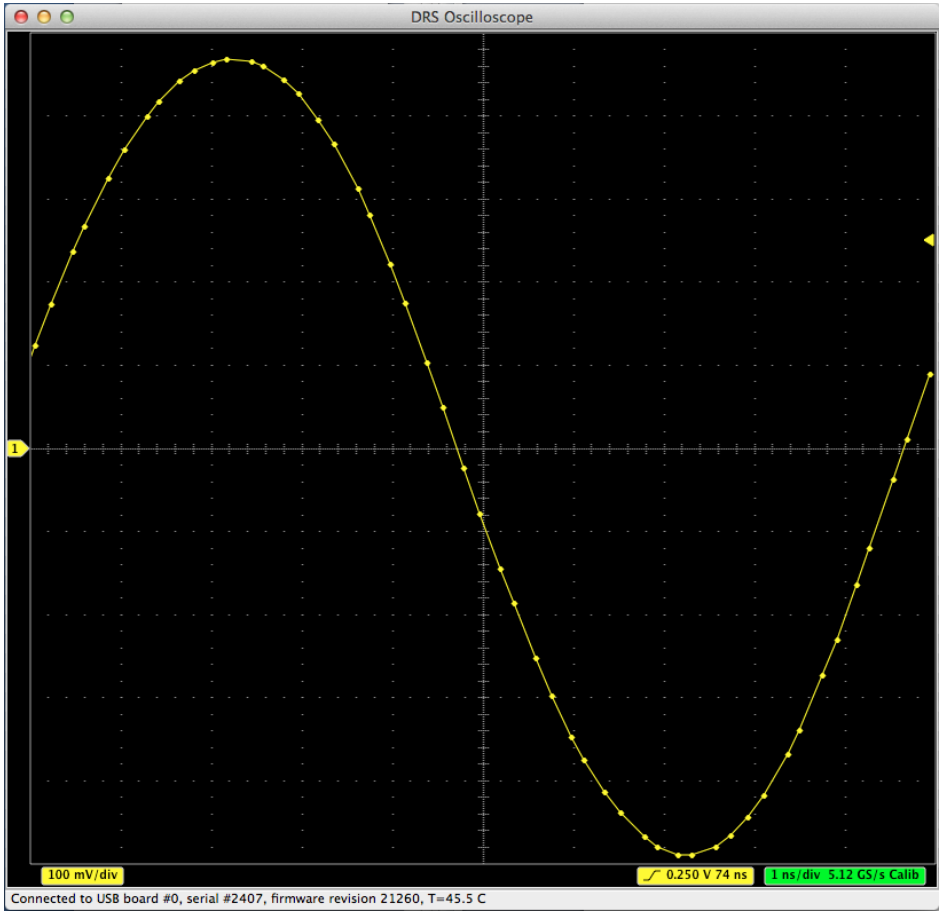


Effect of local calibration

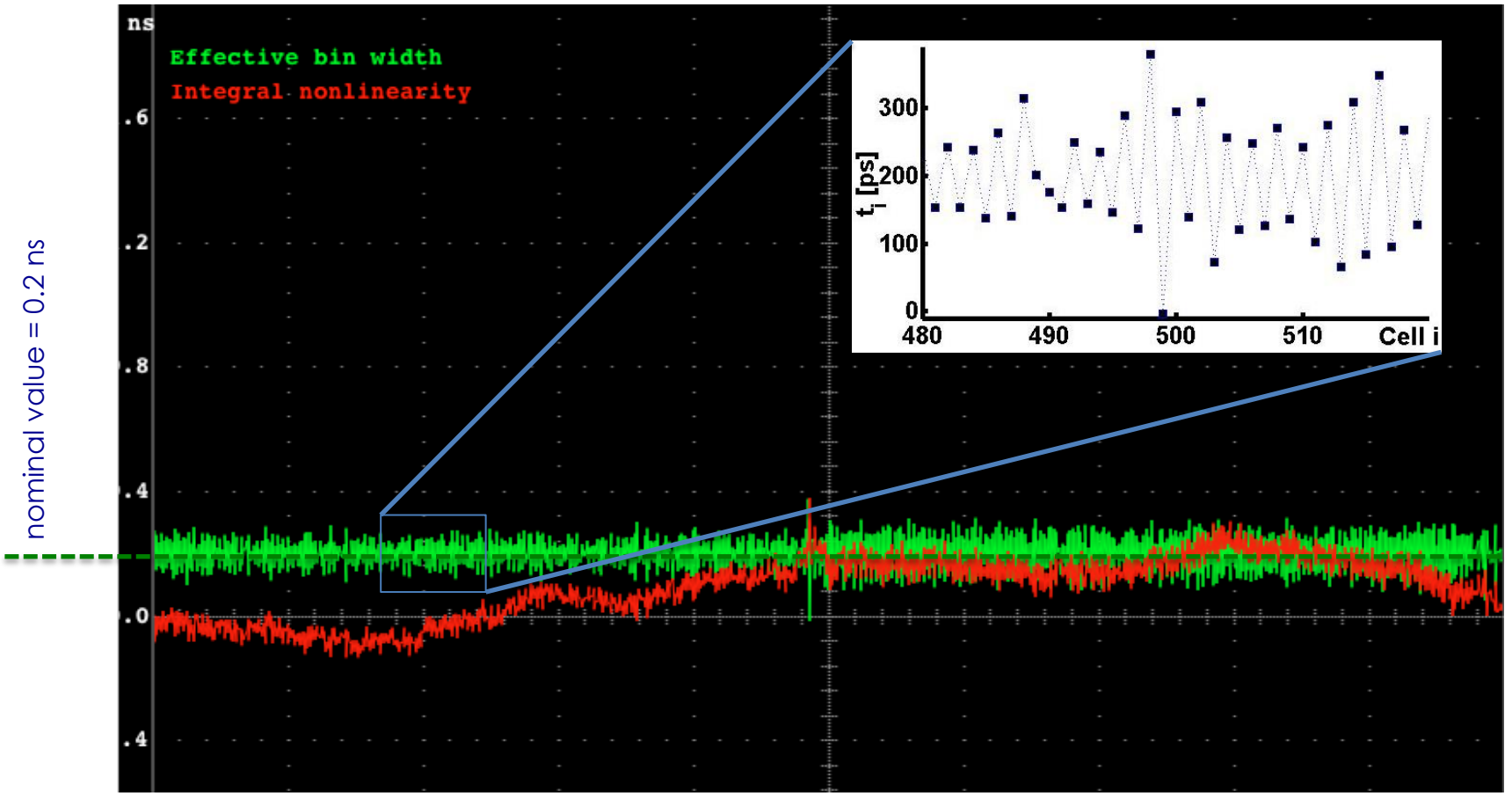
before



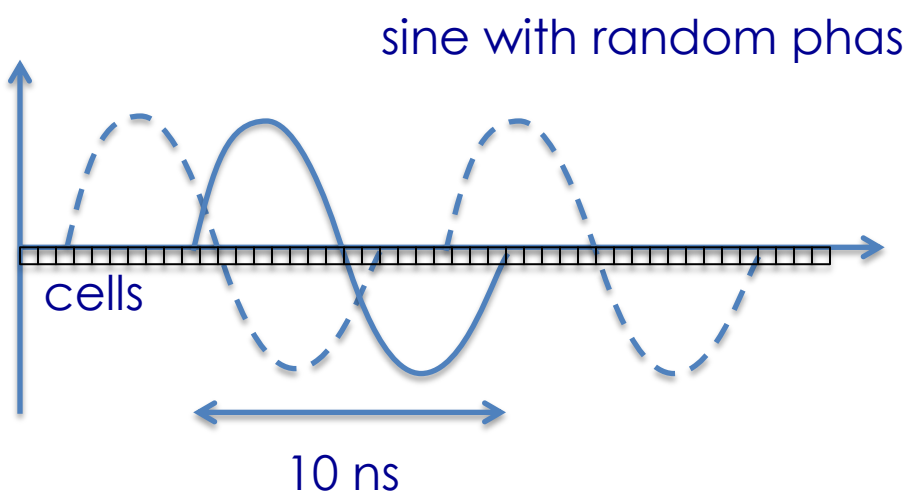
after

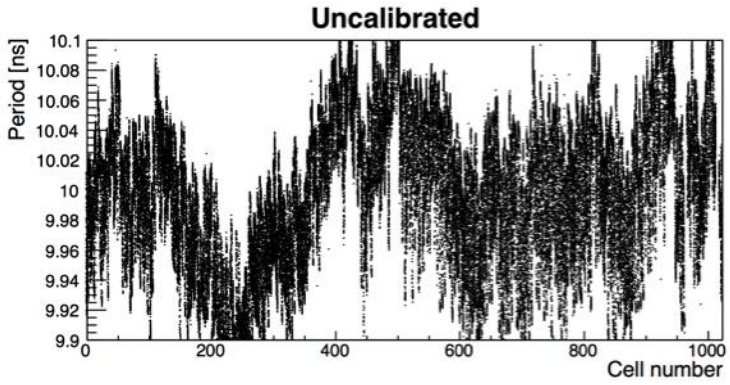


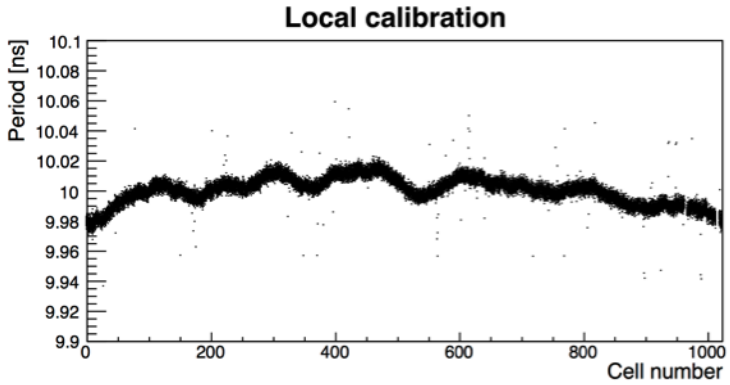
Distribution of Δt_i



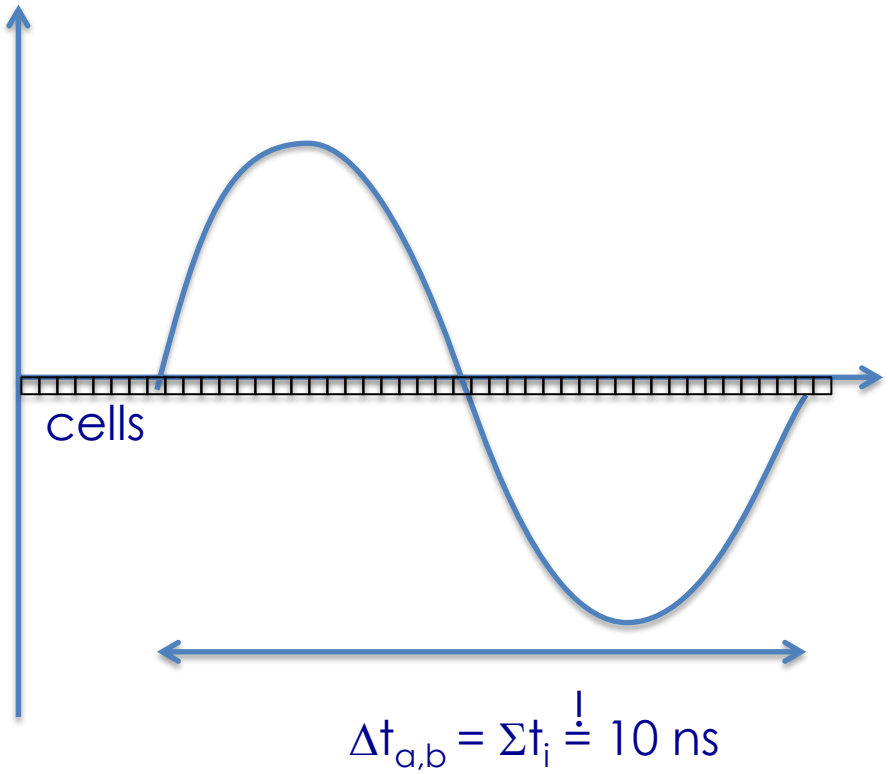
How to quantify accuracy of calibration





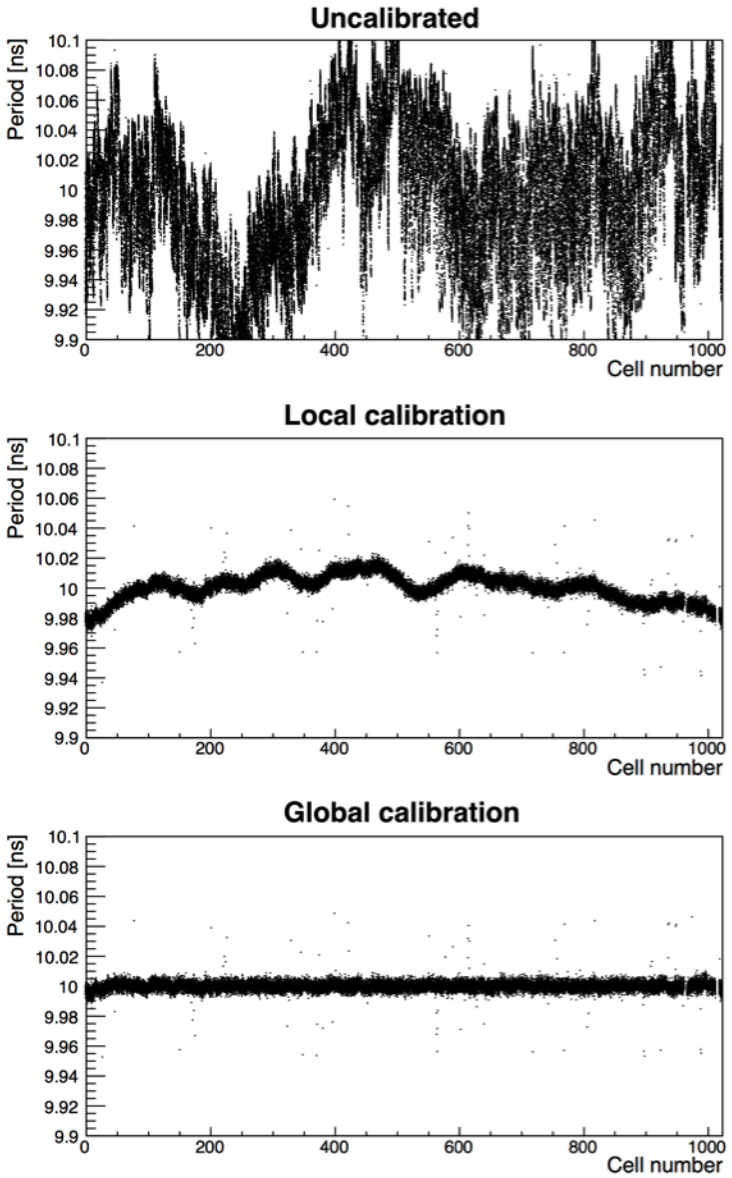


Global Calibration

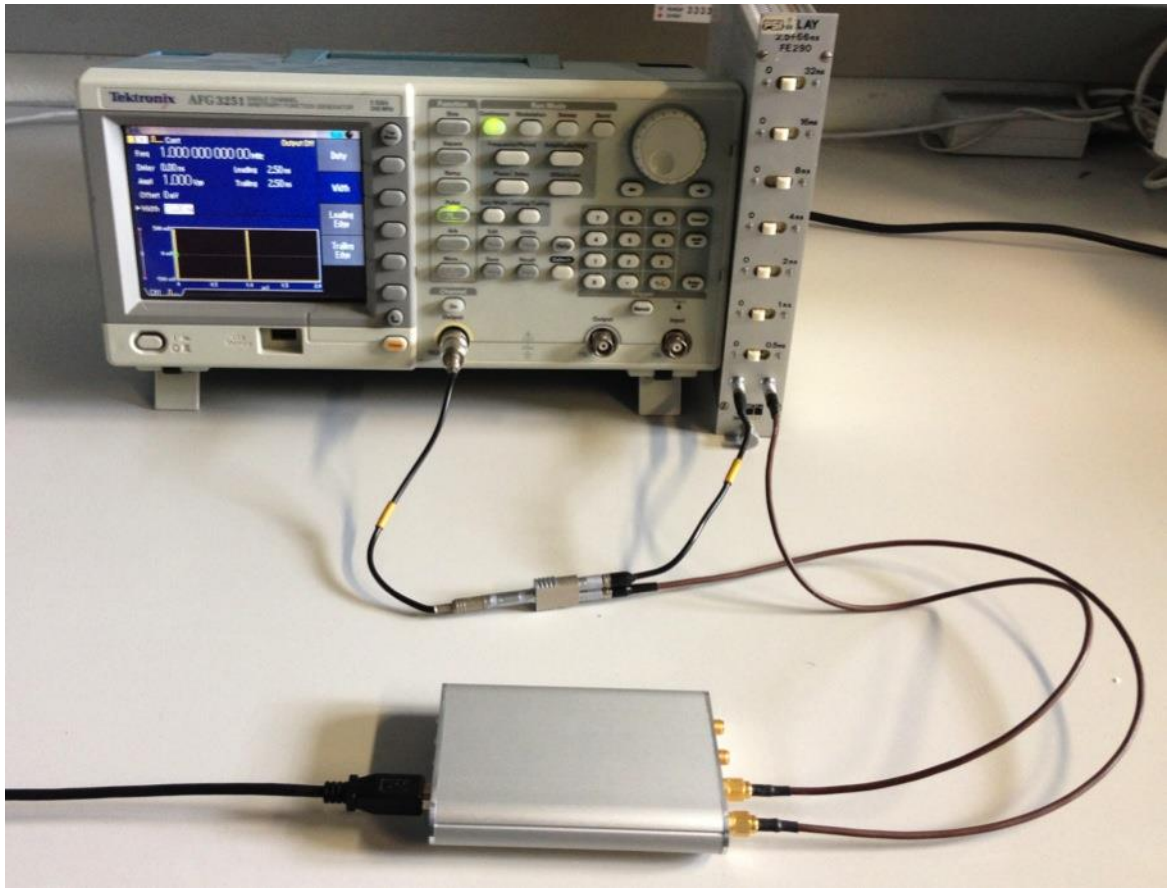


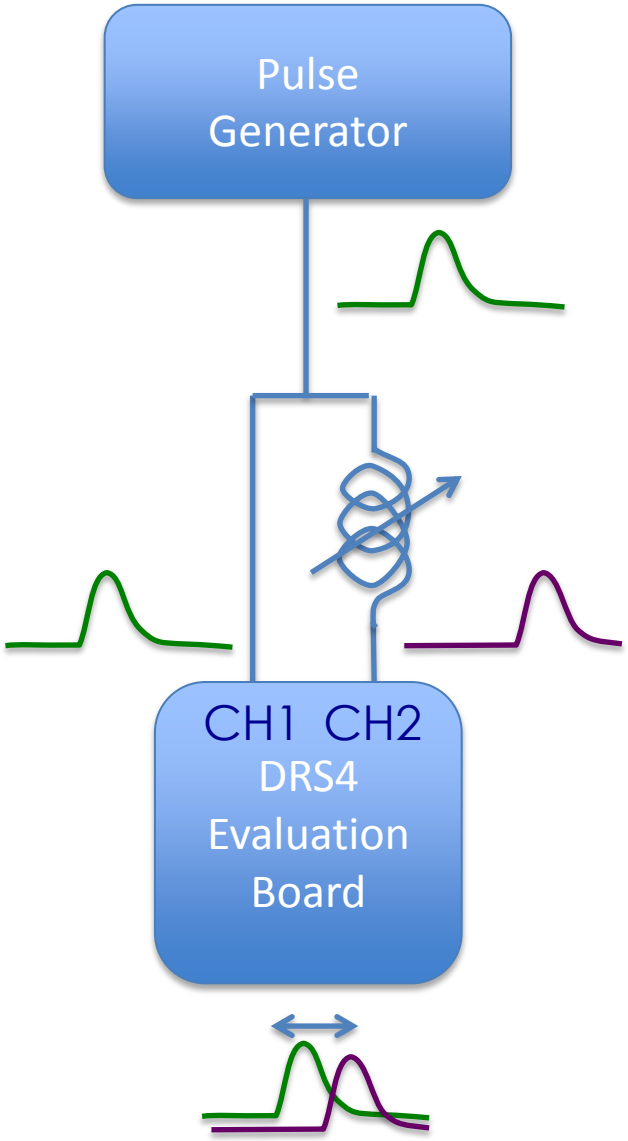
- Measure period of sine wave (linearly interpolate zero crossings)
- Calculate correct factor
- Distribute correction equally to cells between zero crossings
- Iterate with random phase

Effect of global calibration

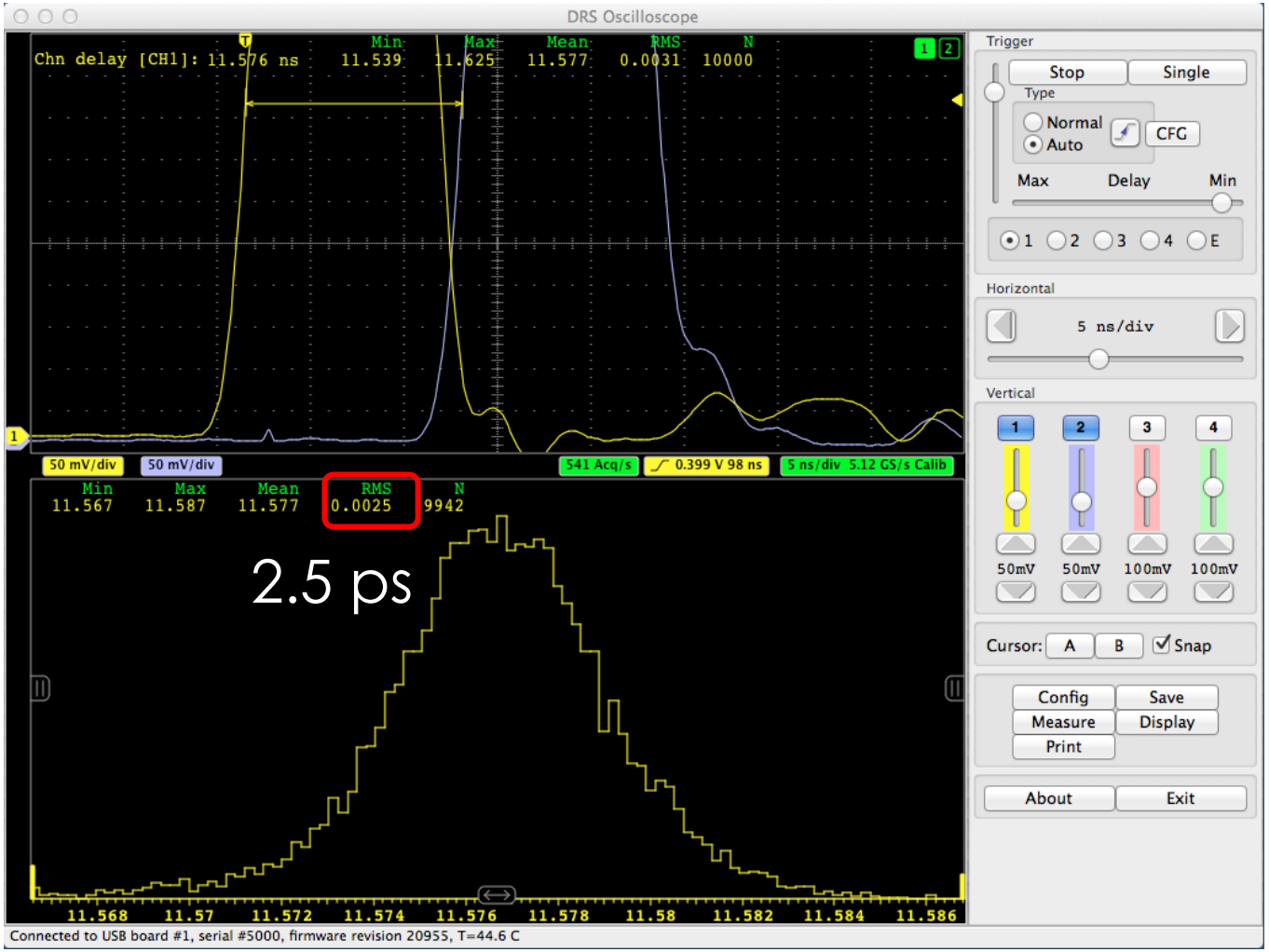


Measure resolution with real pulses





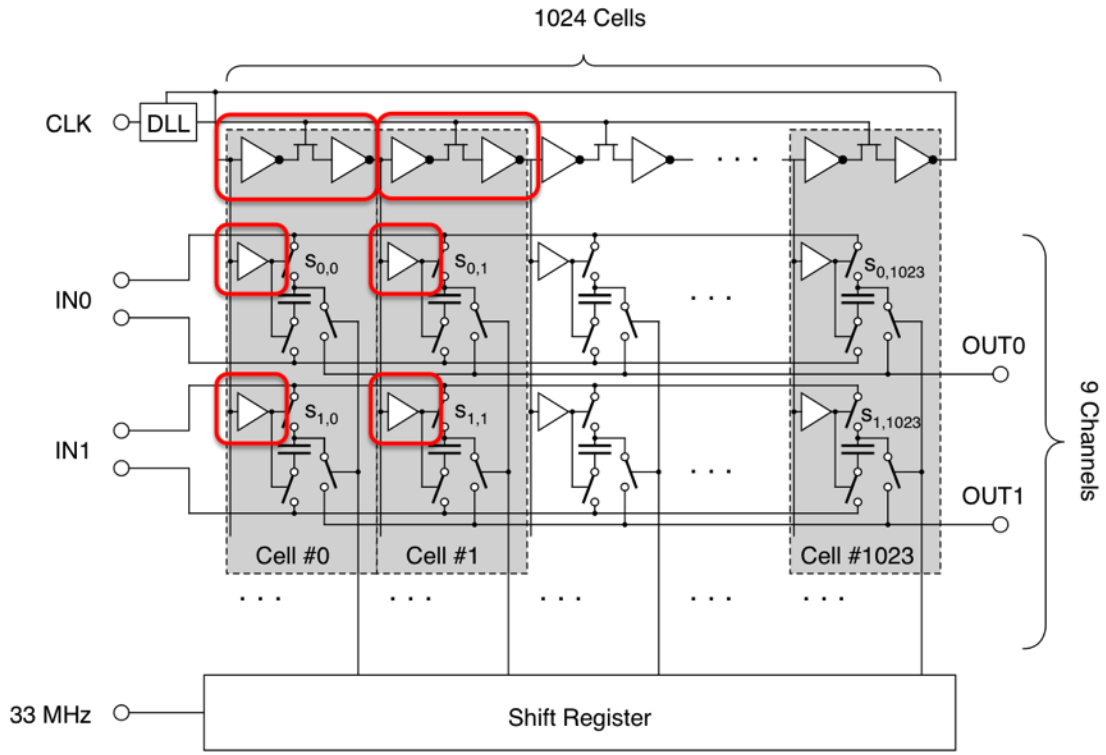
Result of time difference @ 5 GSPS



- Rise time:
  500 mV / 2 ns
  =
  100 mV / 0.36 ns
- Delay = 11.6 ns
- Value in RMS
- Linear interpolation
- Single measurement
  2.5ps/√2 = 1.8 ps

Calibration of all channels

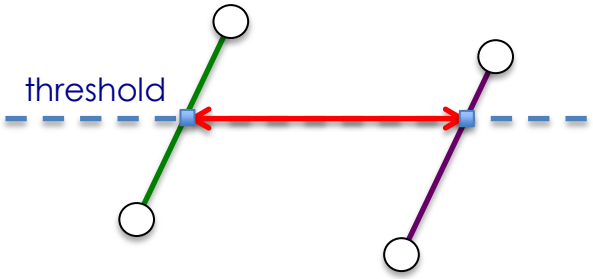
- Calibrating one channel of DRS4 chip → 12 ps
- Calibrating each channel individually → 2.5 ps
- Large system needs clock distribution with ~ps accuracy



Advanced Analysis

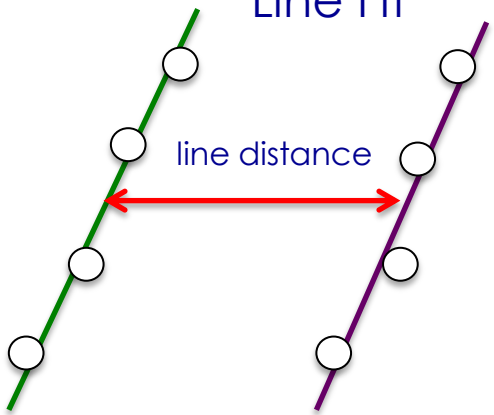
- Accuracy can be increased by taking more points into account (unlike TDC)

Simple Threshold

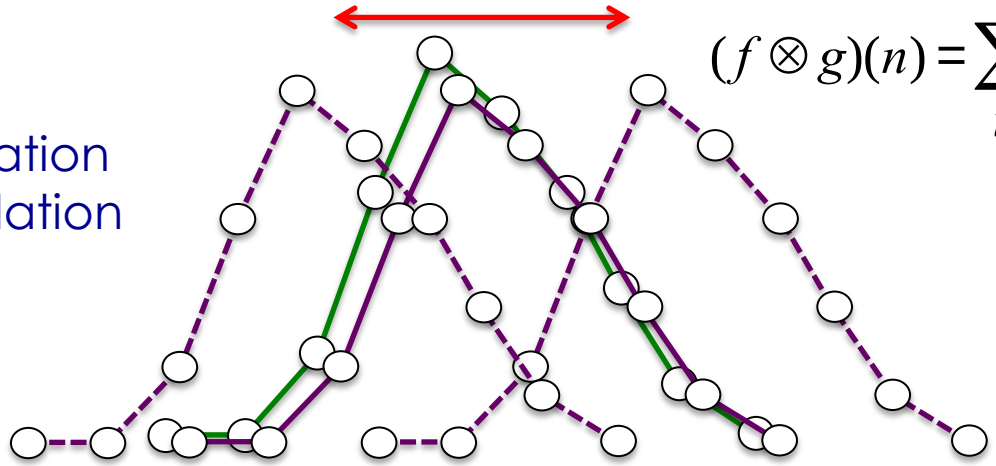


Win √n !

Line Fit

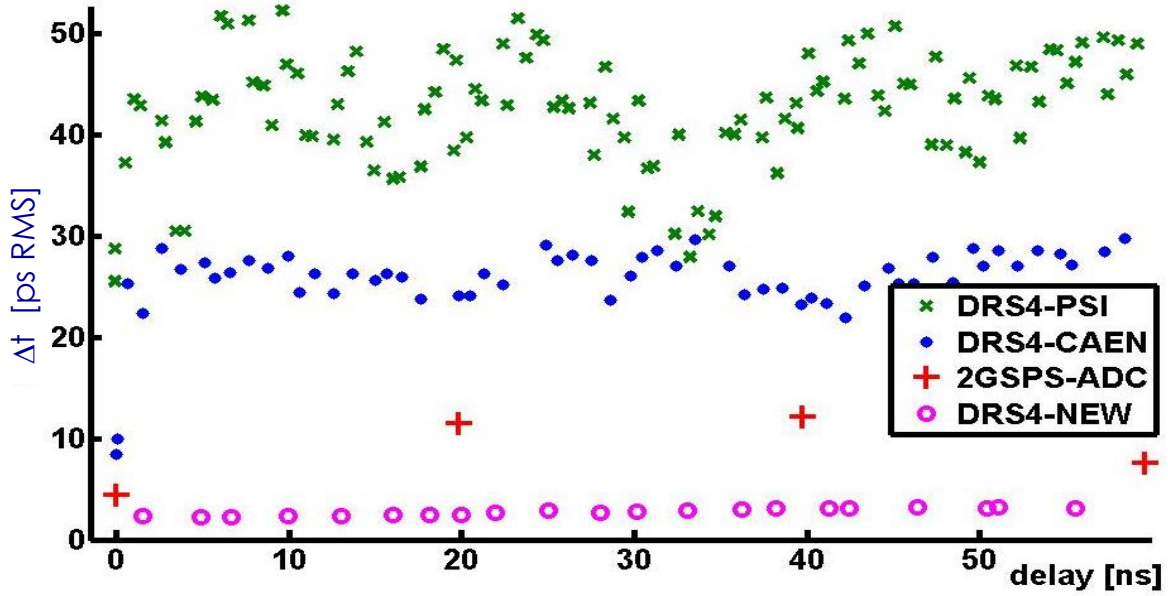


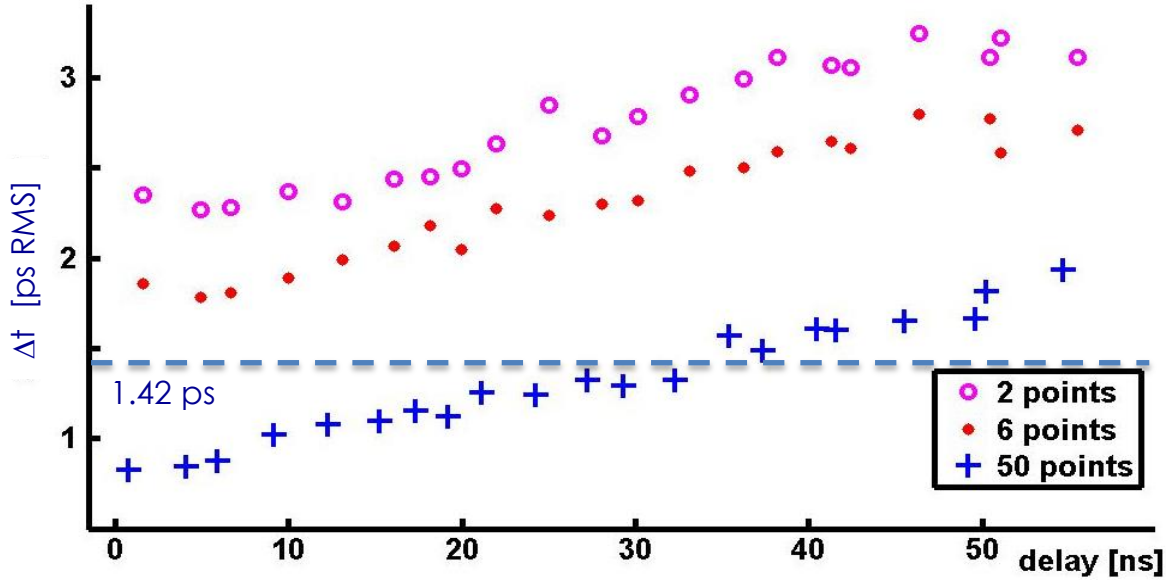
Cross-correlation with interpolation



$$(f \otimes g)(n) = \sum_i f(i) \cdot g(i - n) \rightarrow \max$$

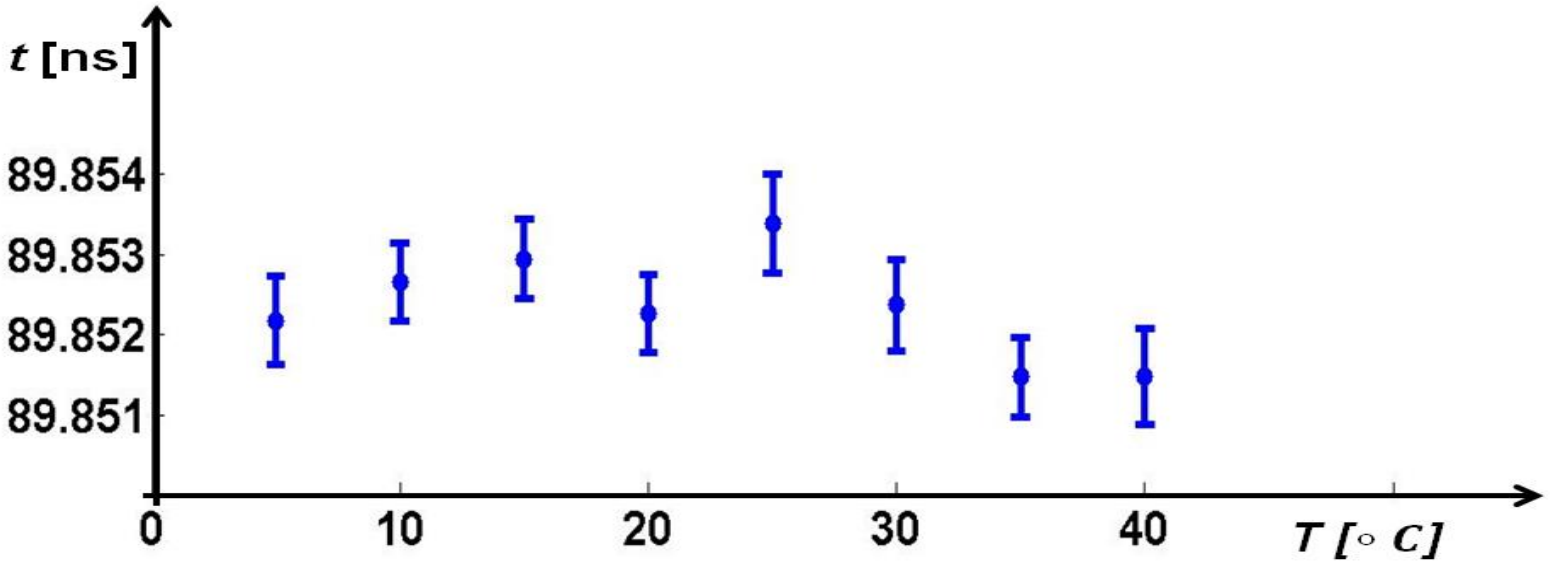
Results in dependence of delay





- Improvement of ~40 x to old calibration
- No degradation for delay > 0
- 10x better than Acquiris ADC 2 GSPS/10 bit
- Cross correlation gives best result
- Result < 1ps (single measurement) for delay < 30 ns

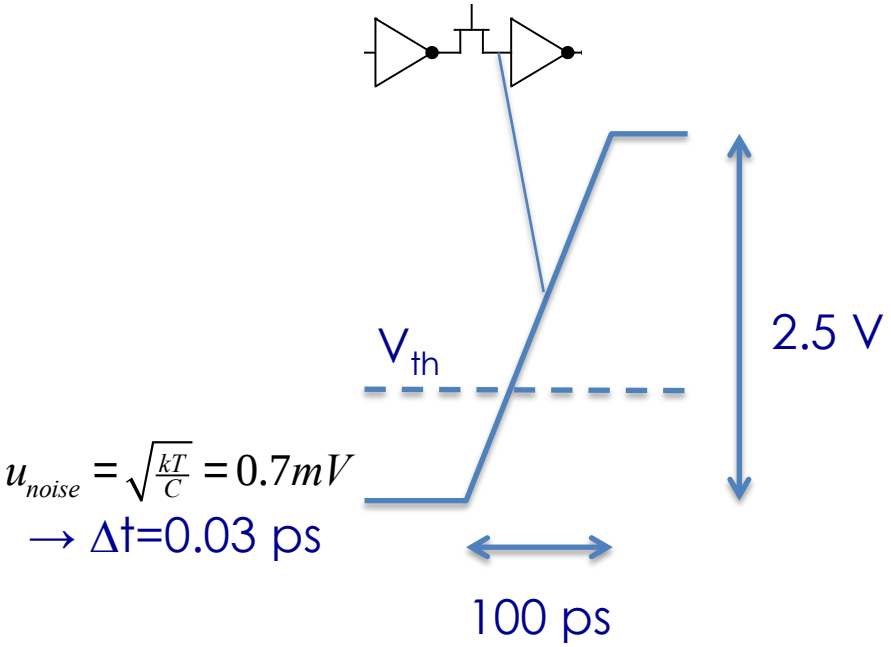
Temperature Dependence



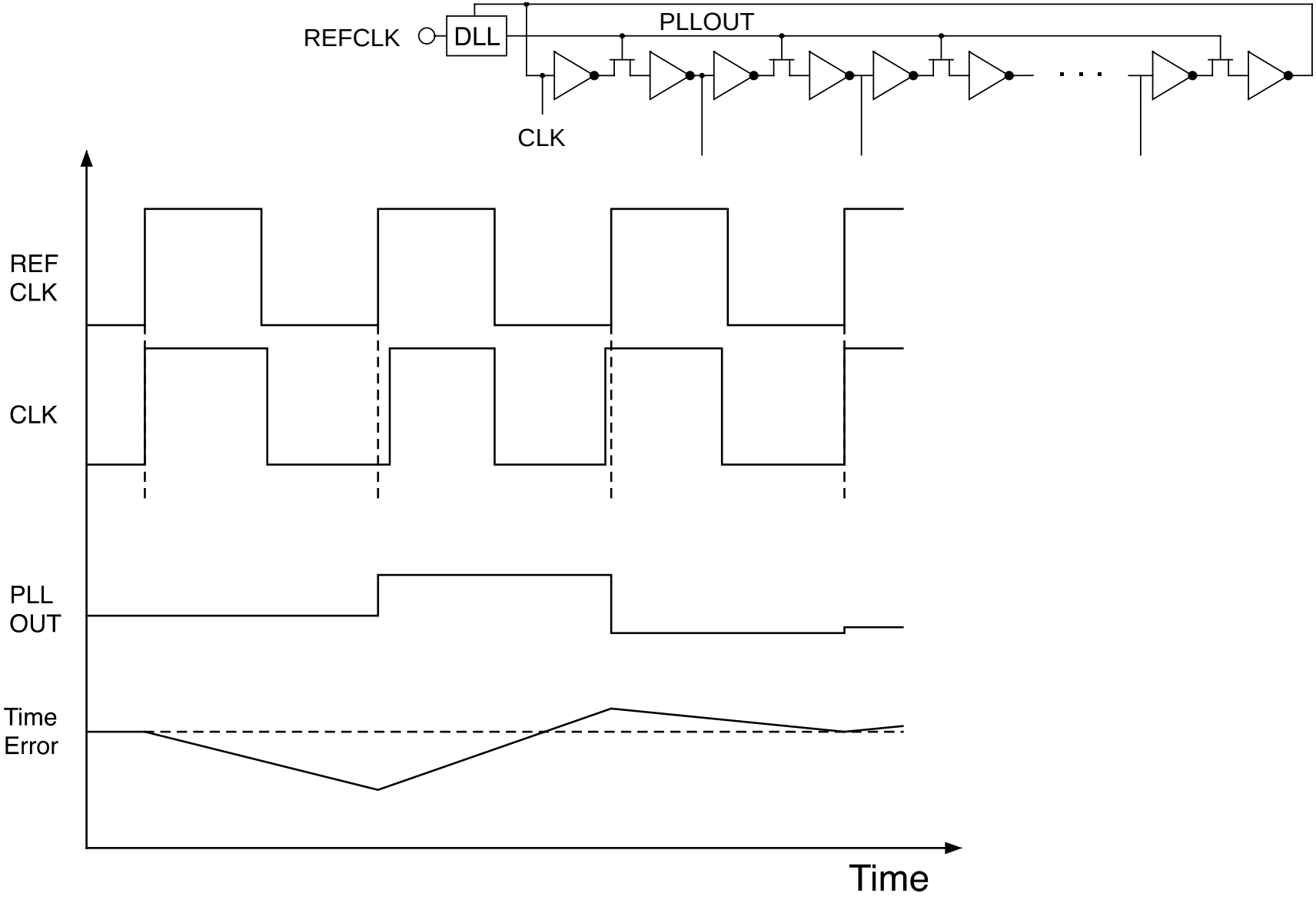
Calibration seems stable on the 1-2 ps level over wide temperature range

Limitation of time measurement

- SNR of detector signal
- Variation of V_{th} → calibration
- Noise inside inverter chain
- DLL phase noise

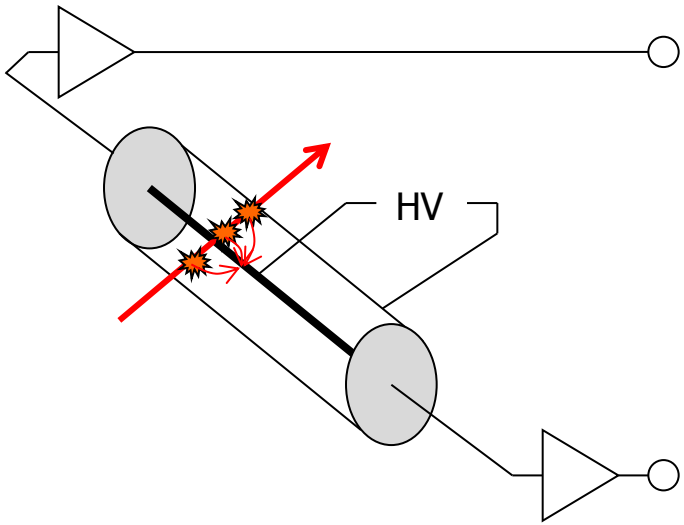


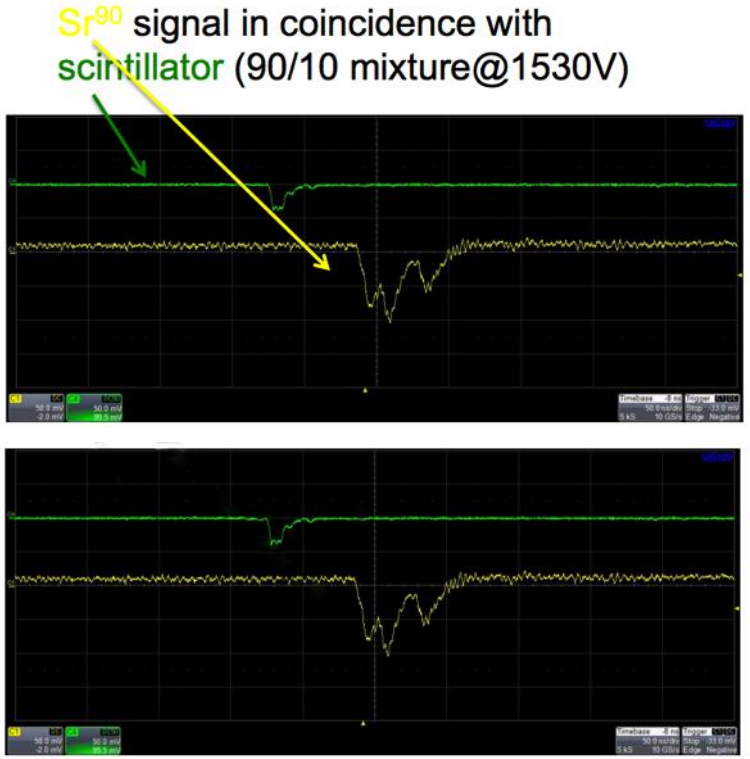
DLL Phase Noise



Application of precise timing

- Readout of straw tubes / drift chambers
- Position along the wire with charge division
- Time measurement with cluster technique should give 3 ps → 0.5 mm





Conclusions

- New calibration for DRS4 chip give sub-ps resolution for delay < 30 ns
- Patent PCT/EP2013/070892 <Bernd.Pichler@med.uni-tuebingen.de>
- SNR of detector signal limits timing
- To improve timing even further:
  - work hard on SNR
  - carefully calibrate voltage response of EACH cell
  - reduce DLL phase noise

FEMTO
WORKSHOP ON PICOSECOND PHOTON SENSORS

FOR PHYSICS AND MEDICAL APPLICATIONS, MARCH 12-13-14 2014 2017

Place and Purpose

A workshop on picosecond photon sensors, their electronics and their applications for particle physics and medical imaging will take place in Clermont-Ferrand, France, on March 12-13-14, 2014.
This workshop will address particularly the latest developments on Ultra Fast timing from 1-50 picoseconds levels becoming achievable with the new technological development around recent photodetectors like solid state photodetectors (SiPM) and Multichanel Plates Photodetectors devices (MCP) but also new development with gazeous detectors like RPCâand MGPDâ However, there are many challenging issues at many levels. The