

Signal Processing for Fast Photo-detectors

Jean-François Genat

With the help of:

Mircea Bogdan, Henry Frisch, Eric Oberla, Fukun Tang
U Chicago

and

Dominique Breton, Eric Delagnes
Orsay Saclay

Outline

- **Fast Imaging Devices and Timing Resolution**
- Silicon PMTs and Micro-Channel Plates (MCPs)
- Timing with Waveform Sampling
- 2D Readout with Timing
- Switched Capacitor Arrays
- Conclusion

Fast Timing and Imaging Photo-detectors

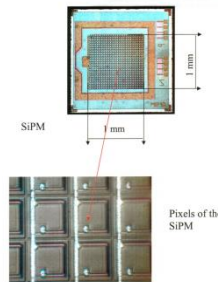
Multi-anodes PMTs

Dynodes



Silicon-PMTs

Quenched Geiger



Micro Channel Plates

Micro-Pores



QE	30%	90%	20-30%
CE	90%	70%	60%
Rise-time	0.5-1ns	250ps	50-200ps
TTS (1PE)	150ps	100ps	30-50ps
Pixel size	2x2mm ²	50x50μm ²	1.5 x1.5 mm ²
Dark counts	1-10Hz/cm ²	1-10MHz/cm ²	1-10 kHz/cm ²
Dead time	5ns	100-500ns	1μs
Magnetic field	no	yes	15kG
Radiation hardness	1kRad (PC)	noise x 10	1kRad (PC)

Outline

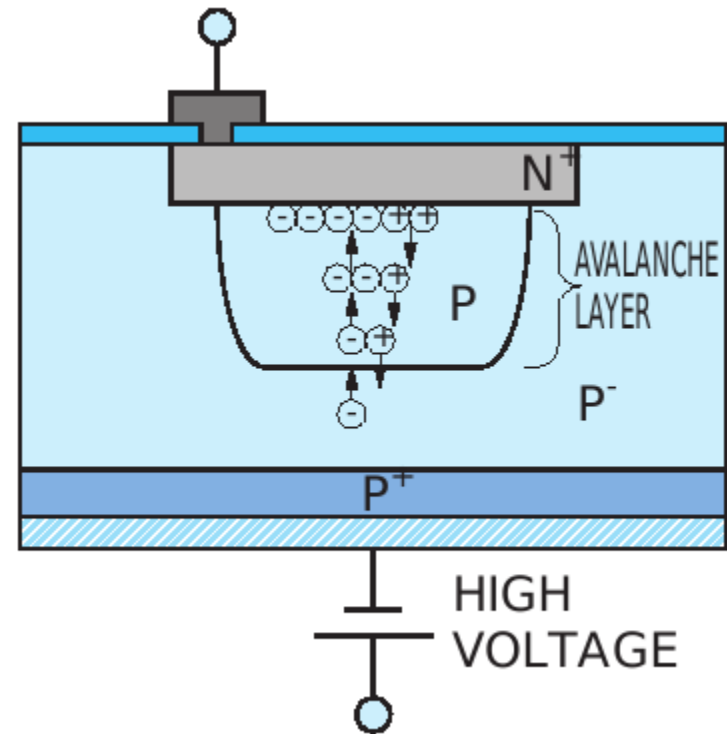
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Fast Solid State imaging Devices

Silicon Photo-Multipliers

PN junction reverse biased beyond the breakdown voltage
Avalanche “quenched” with a series resistor

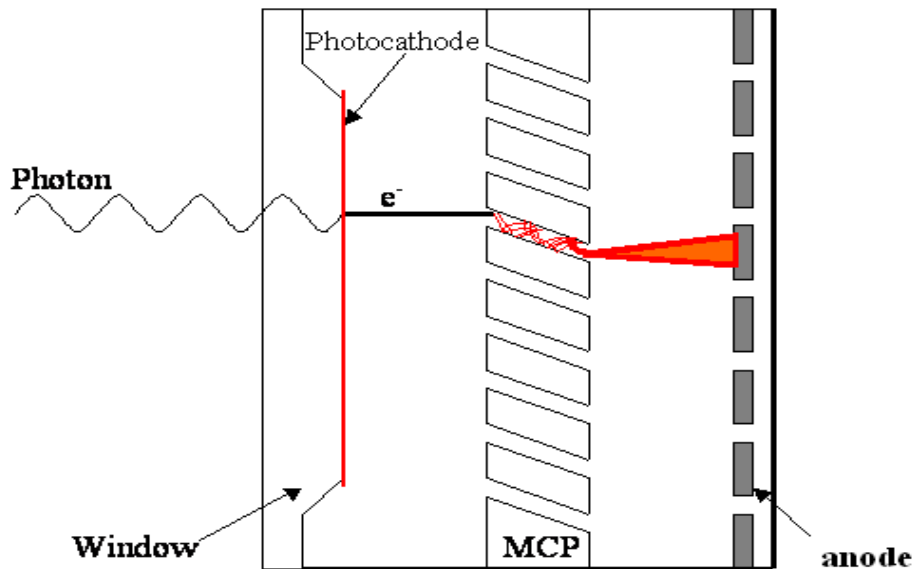
- Good Quantum Efficiency,
but small sensitive area
- High Gain 10^{5-6}
- Noise: Avalanches from reverse currents:
MHz/cm²
- Trapped carriers: after-pulses
- Optical Crosstalk
- “Cheap”



M. Haigh, Univ Oxford

Fast Solid State Imaging Devices

Micro-Channel Plates

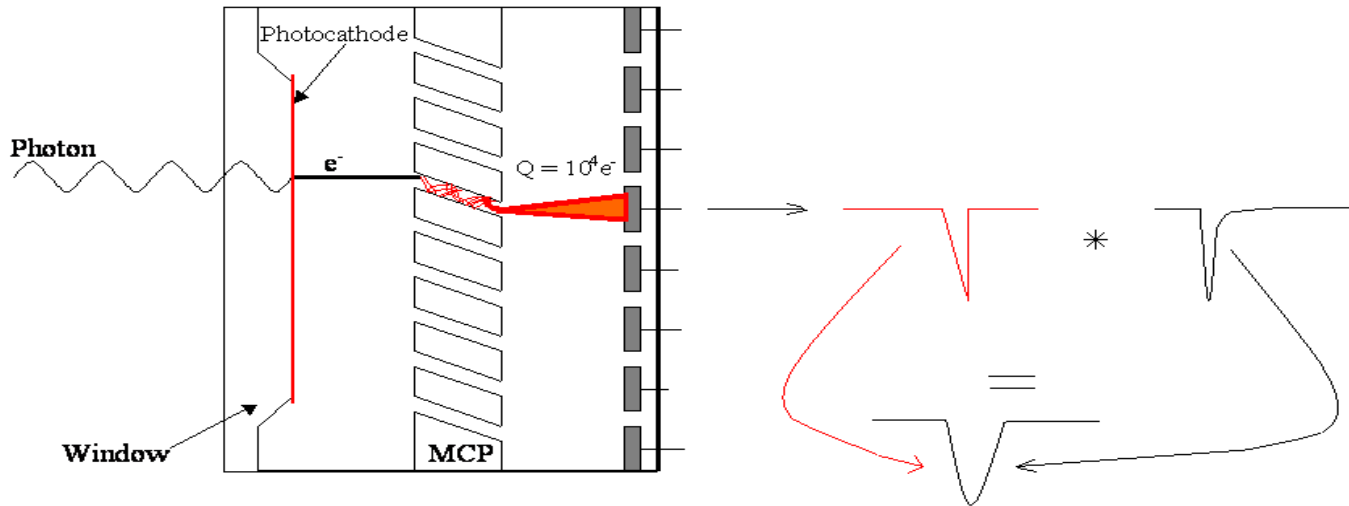


Photonis Glass MCP: area: 2" x 2"

Photocathode + amplifying MCP: a few microns diameter pores, secondary emitter
Space resolution: 0.1-1mm, timing 30-50ps

Tentative: large area (20 x 20 cm) : 2D delay line readout See Eric Oberla talk

MCPs signal development



MCP signal rising edge: $qE = ma$ $tr = l \sqrt{2m/qV}$
 $l = 1\text{mm}$, $E=100\text{V/mm}$, $tr=250\text{ps}$

Short Transit Time:

- Thin photo-cathode gap,
- High electric field
- Thin MCP: small pore size ($L/d = 40$) $< 5\mu\text{m}$, $l < 200\mu\text{m}$

Fast pulse:

- Thin anode gap,
- High electric field

10^{-5} mm Hg vacuum rigidity is $1\text{kV}/100\mu\text{m}$

Single Photo-electrons signals

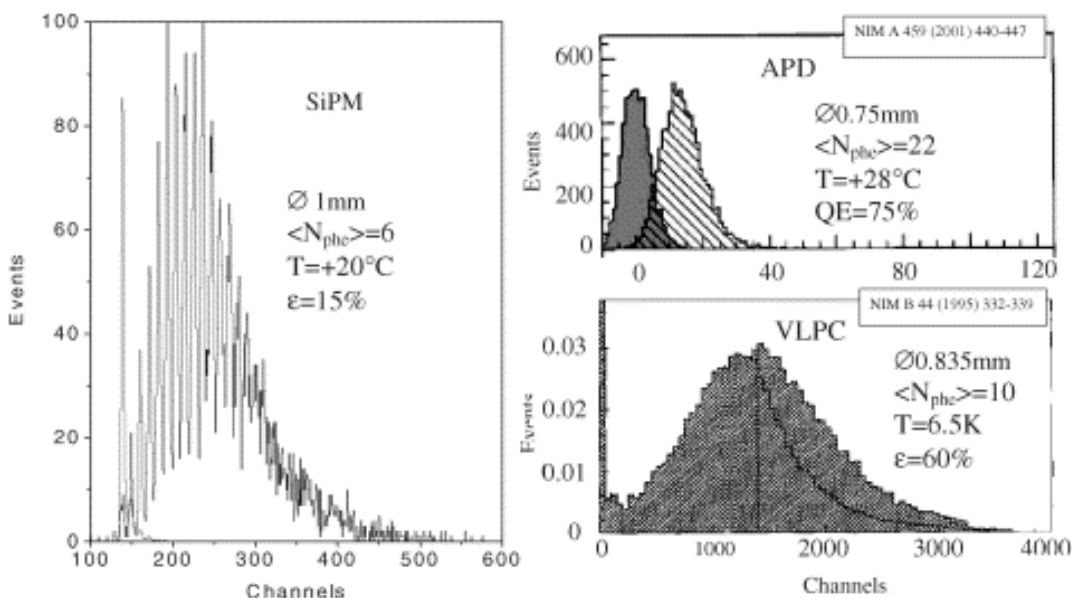
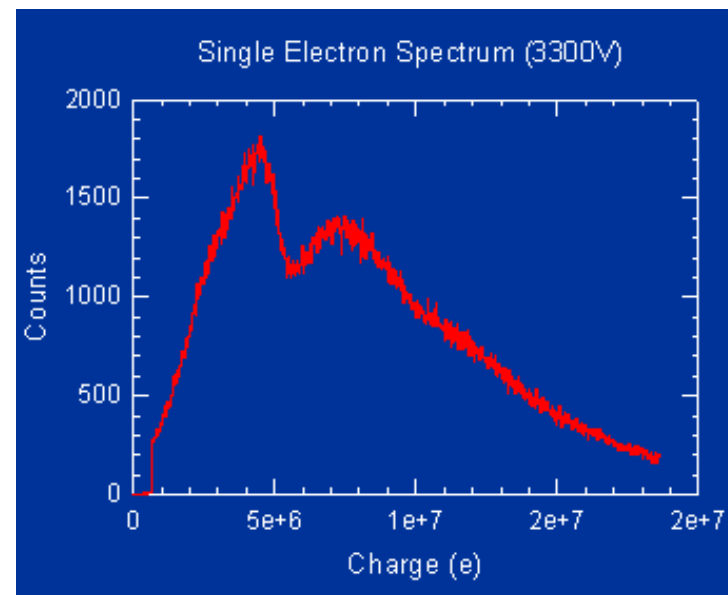


Fig. 3. SiPM application for sci fiber MIP detection (at room temperature): comparison with APD [6] (room temperature) and VLPC [7] (6.5°K).



25 microns, MCP from Burle-Photonis

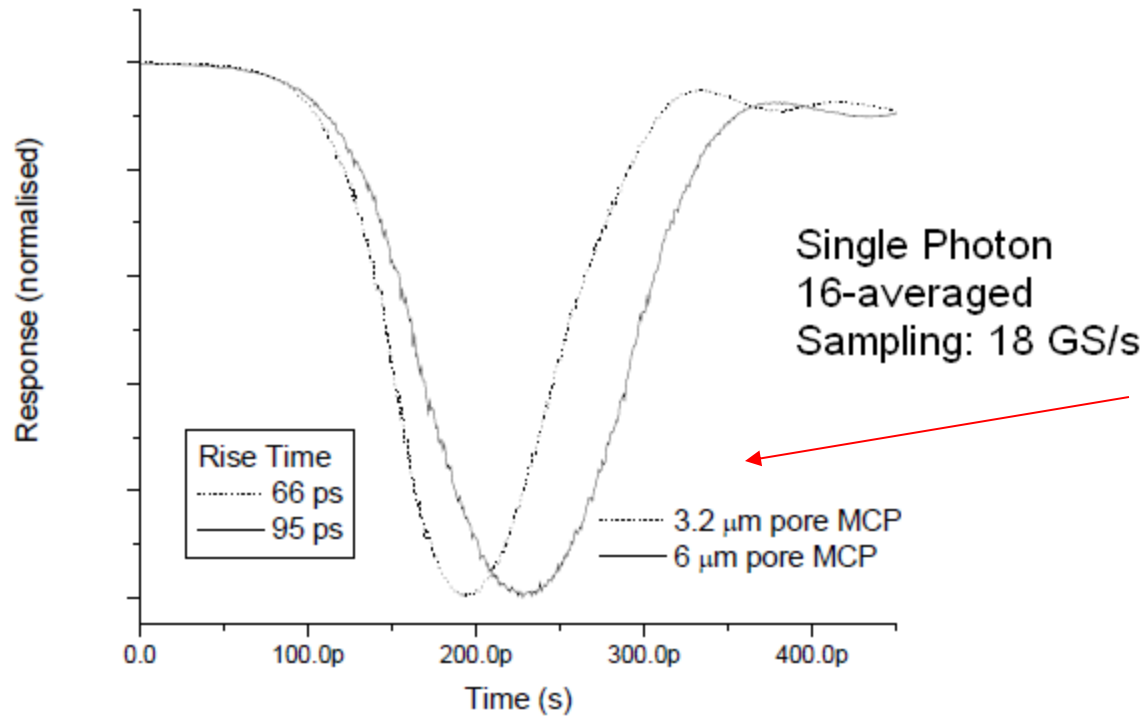
From B. Dolgoshein et al.

From P. Hink (Burle-Photonis)

MCP: Gain fluctuations in the pores: “noise” as loss of energy information

Statistical nature of the amplification process: SEE, number of bounces

Micro-Channel Plate Signals



Time response curves for two models of PMT110 with different MCP pore diameters.

Courtesy P. Hink, Photek

The fastest solid-state photo-detector to date

Micro-Channel Plates

Timing resolutions (Transit Time Spread) in the 10-100 ps range

- ***MCP parameters impacting transit time:***

 - Rise-time

 - First strike, Tilt angle, Pore size (diameter, length)

 - Bias voltage (gaps transit times)

- ***MCP parameters impacting noise and rise-time***

 - Photo-cathode noise (mainly impulse noise)

 - Secondary emitter noise

 - Gain fluctuations

- ***MCP environment***

 - 2D readout elements: delay lines

 - Magnetic field

- ***MCP readout electronics parameters with waveform sampling***

 - Analog bandwidth

 - Sample rate

 - Electronics gain (if any)

 - Electronics noise

 - Signal integrity (system noise)

Large Area Micro-Channel Plates Devices

Present MCPs Photek, HPK, Burle-Photonis **2'' x 2''**

LAPPD project : Chicago-Hawaii Large Area MCP **8'' x 8''**

See Ossy Siegmund's and Eric Oberla's talks

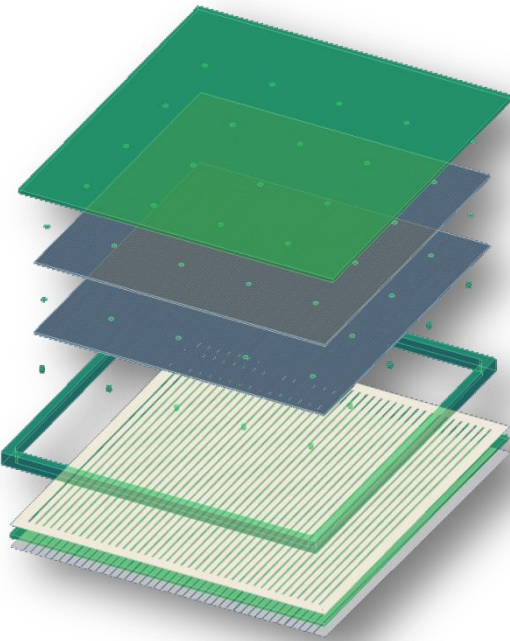
Transmission lines 2D readout:

limits the number of electronic channels compared to pixels

Goal: Both position $O(\text{mm}^2)$ and timing $O(10\text{-}100\text{ps})$

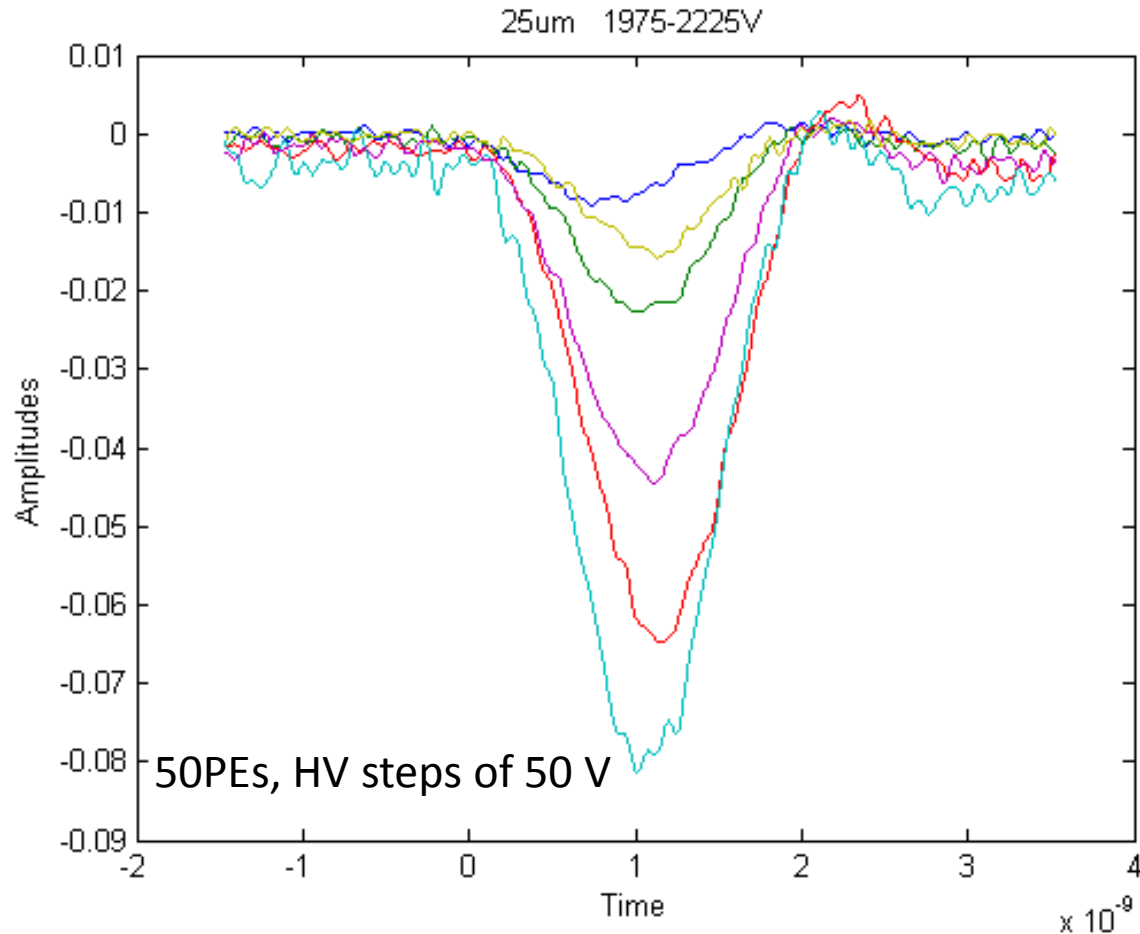
Electronics Hawaii, PSI, Orsay, Chicago-Hawaii

- GigaSample/s Waveform Sampling and Digital Processing



Micro-Channel Plates Signals

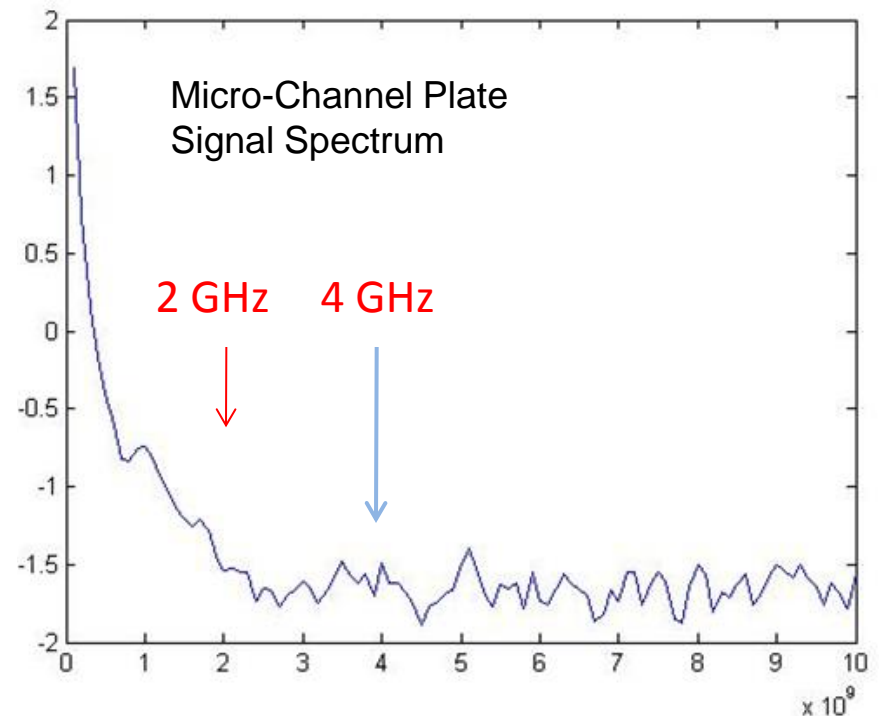
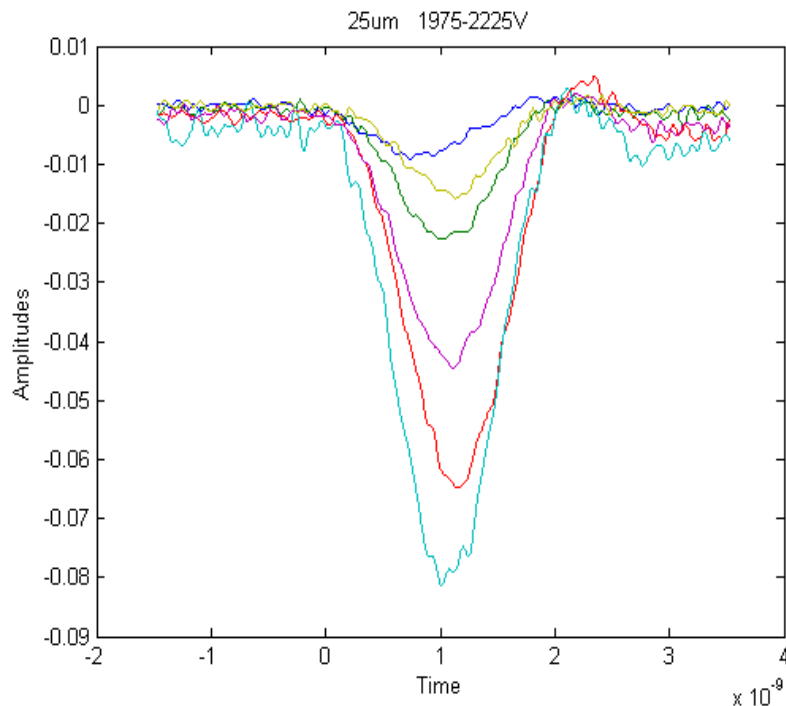
Burle-Photonis
25 μm pores



Micro-Channel Plates signals: bandwidth = 1- 2 GHz
Good candidates for fast timing

GHz Bandwidth Micro-Channel Plate Signals

Digitization: Sampling frequency $> 2 \times \text{Shannon-Nyquist} = 4\text{GHz}$
Dynamic range ~ 150 : 700 μV noise, 100 mV max



MCP Timing resolution estimate/measured

- First gap: 10ps
- Assume 2-stage pores TTS of 20ps
- Anode gap: 10ps
- Noise: 20ps

Total is 32ps

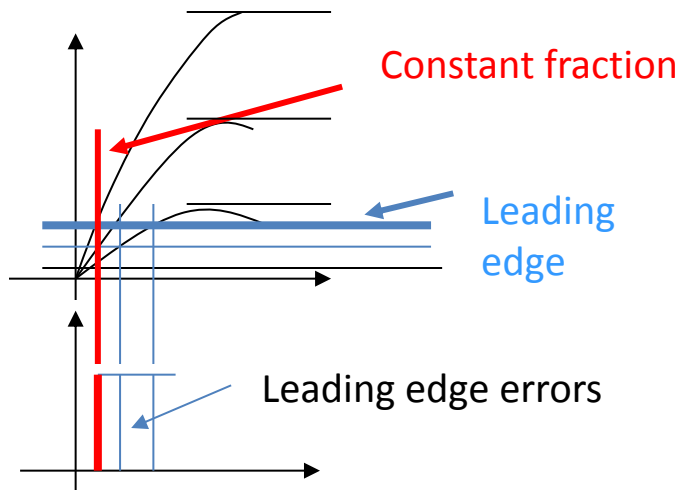
Measured Burle-Photonis 2" x 2" is 30ps

Outline

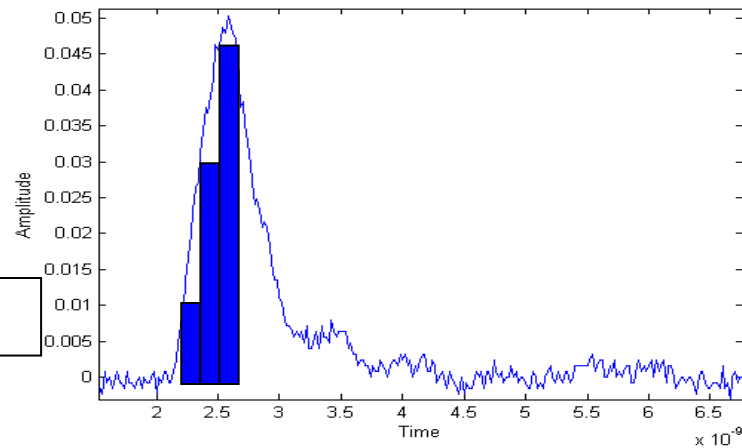
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Timing techniques

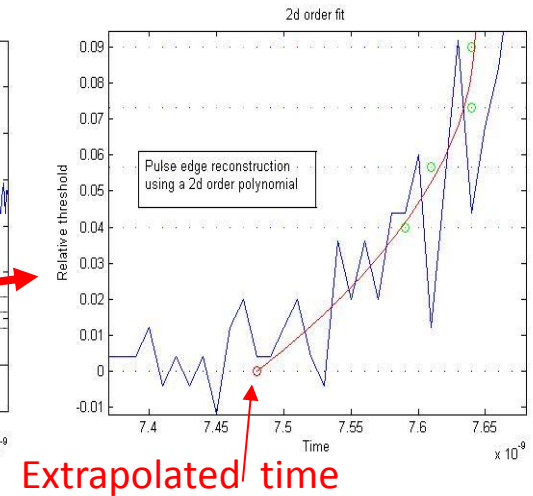
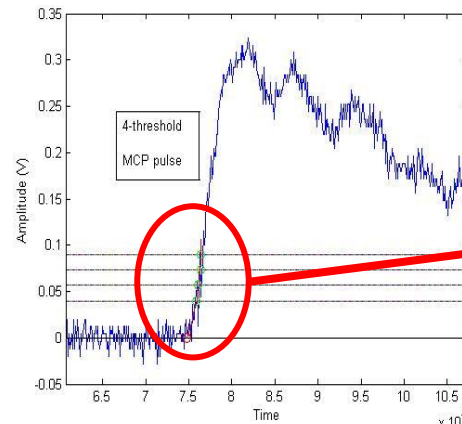
Constant-fraction



Waveform sampling



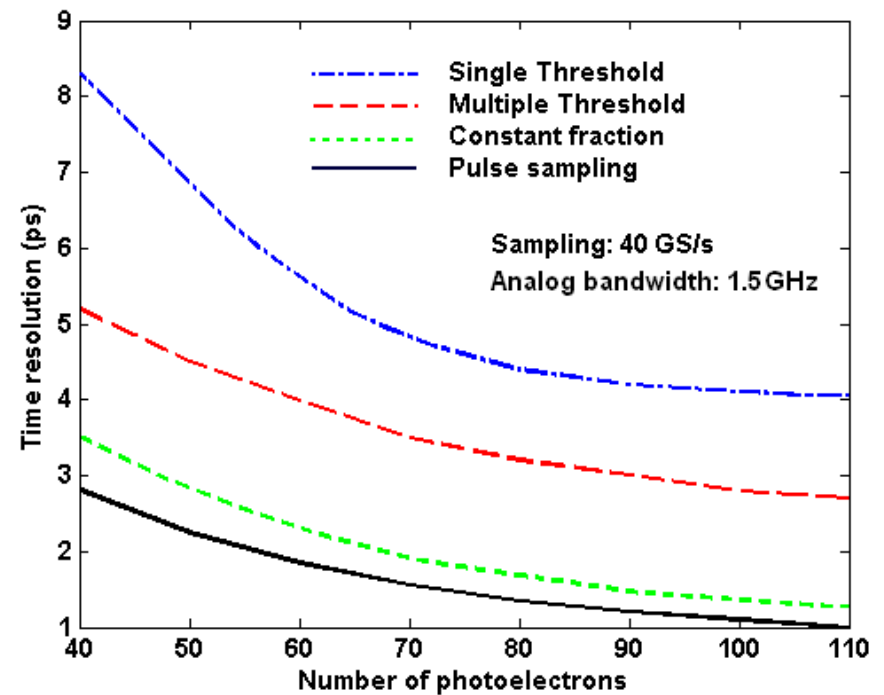
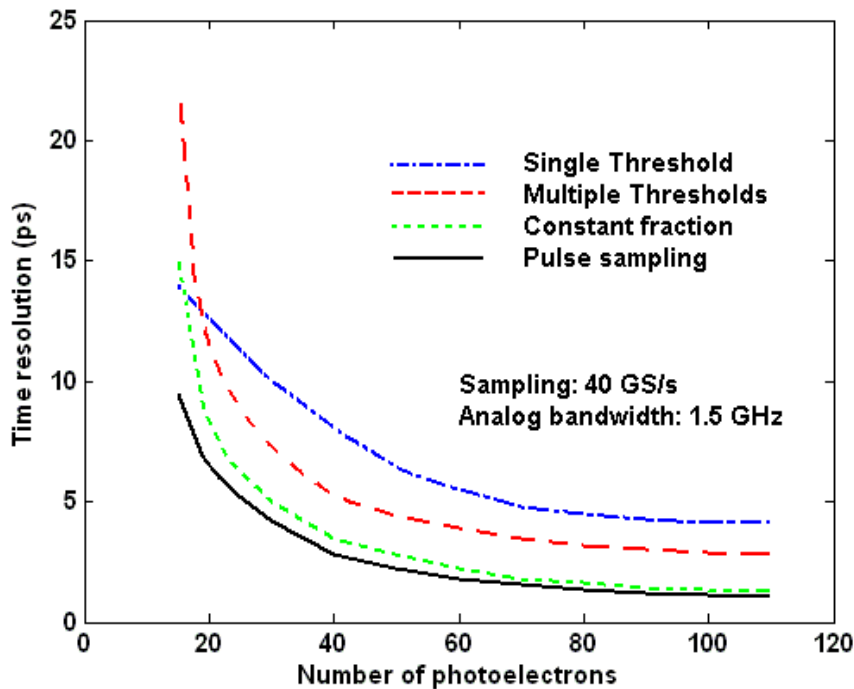
Multi-threshold



Extrapolated time

Timing Methods (simulation)

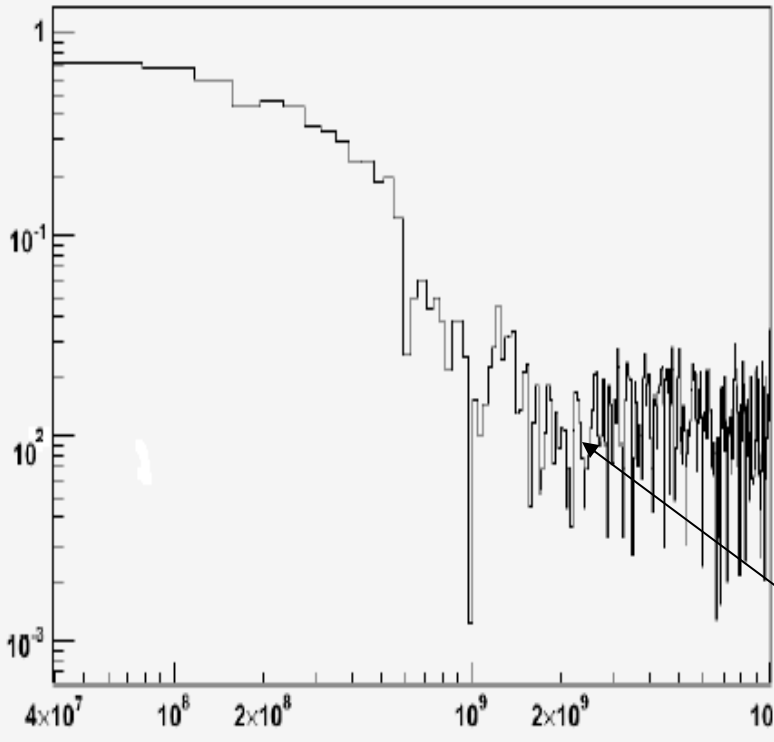
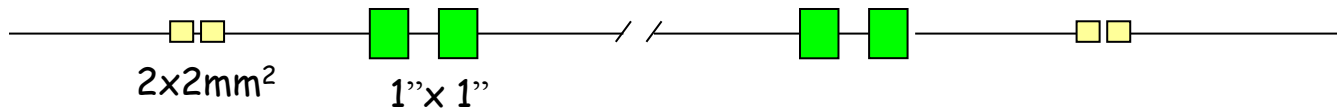
Methods: *Single threshold*
 Multiple thresholds
 Constant fraction
 Waveform sampling



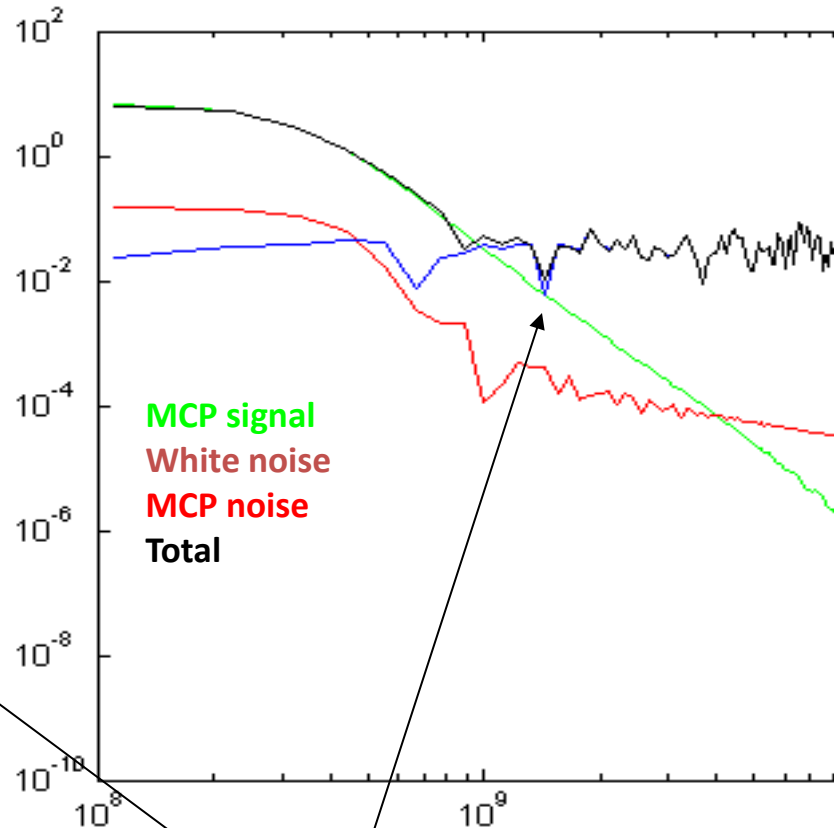
Time resolution vs Number of photo-electrons

zoom

MCP Signals spectra



Measured (FNAL T979 Beam-Tests)



Simulated

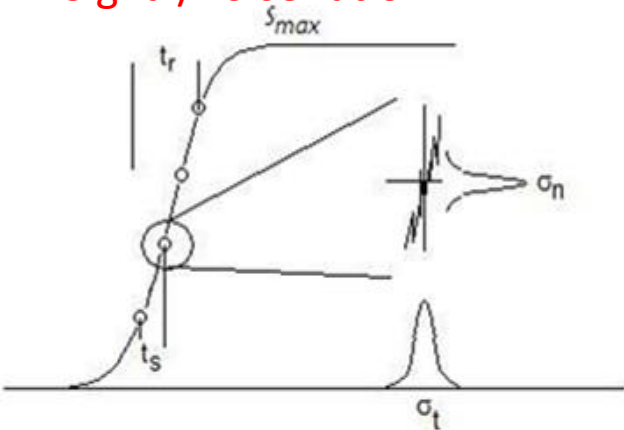
Same noise corner at 1.2 GHz

Timing Spreads

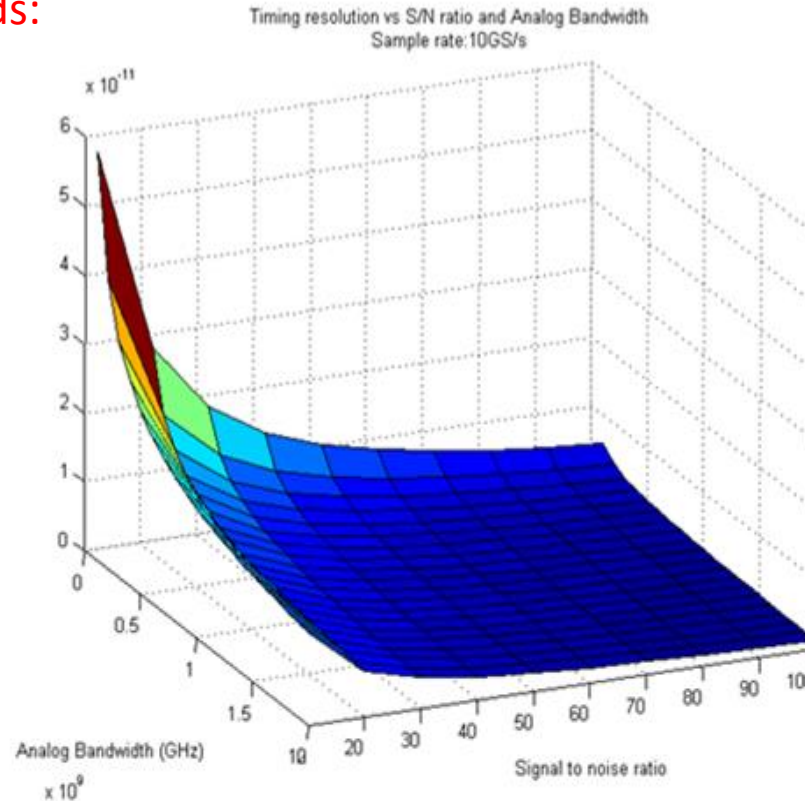
Main contributors to timing spreads:

Detector:

Noise_{detector}
Transit time fluctuations
Rise time
Signal/noise ratio



Noise_{elec}
Analog bandwidth abw



With Sampling Electronics:

$$SN = S_{max} / \sigma_n$$

$$\sigma_n = \sigma_{n\ det} + \sigma_{n\ elec}$$

$$S = G N p e$$

Sampling period t_s

Stefan Ritt:

$$\sigma_{t,n} = \frac{\sqrt{t_r t_s}}{SN} = \frac{1}{SN} \sqrt{\frac{0.35 t_s}{abw}}$$

With SN=50, fs=5GS/s, ABW=1GHz
 $\sigma = 5.3\text{ps}$

Fast Sampling Electronics Timing Resolution

Method	Institute	Device	Sample rate	Timing resolution 50PEs
Constant fraction	SLAC	- NIM		3.4ps
Waveform Sampling	Hawaii	- ASICs:		
		- BLAB line	6GS/s	10ps
	Orsay/Saclay	- SAM line	2GS/s	
	Chicago	- PSEC4	10GS/s	6ps
		- PSEC5 (dev)	15GS/s	
	PSI	- DRS line	5GS/s	3ps

PSEC5 under development Chicago + Hawaii + Orsay/Saclay

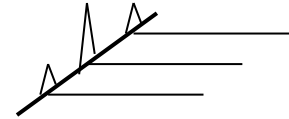
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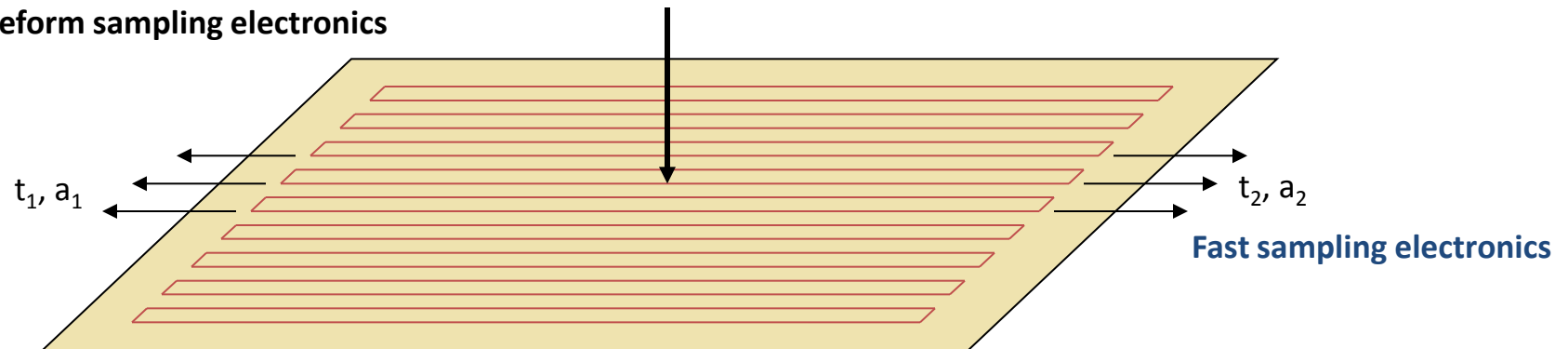
2D+ time with T-lines

- Transmission lines (T-lines) readout and pulse sampling provides

- Fast timing (2-10ps)
- One dimension with T-lines readout 100 μ m- 1mm
Transverse dimension from centroids

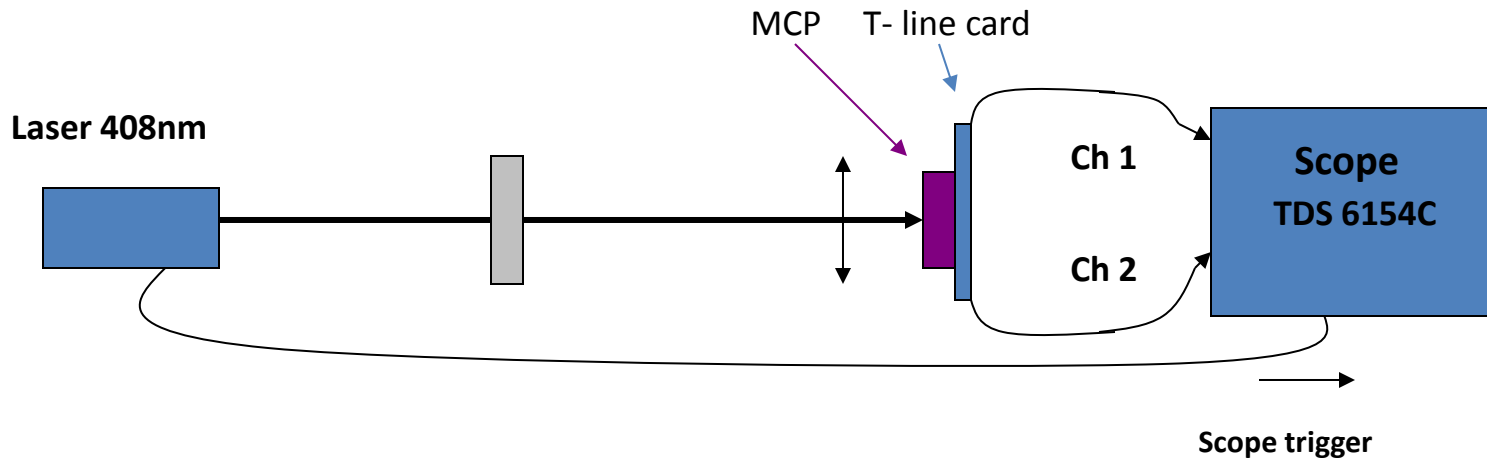


Less electronics channels for large area sensors



$$\begin{aligned}\frac{1}{2} (t_1 + t_2) &= \text{time} \\ v(t_1 - t_2) &= \text{longitudinal position} \\ \frac{\sum \alpha_i a_i}{\sum \alpha_i} &= \text{transverse position}\end{aligned}$$

Position sensing using fast timing



- Edward May, JFG, Argonne (2011-2012)

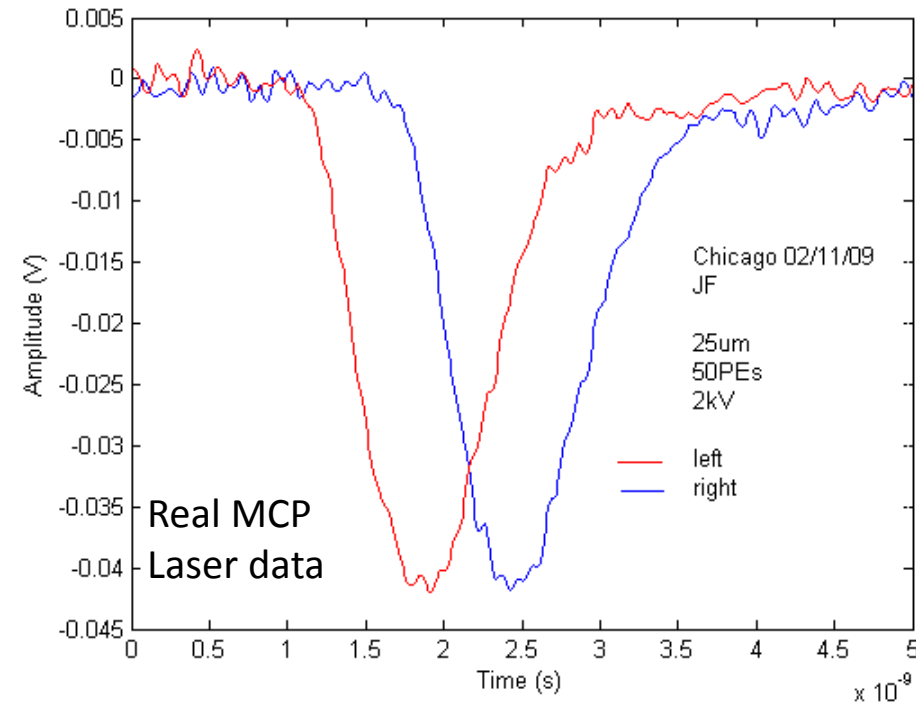
Laser test bench calibrated with the single PE known response of an MCP

- 25/10um pores MCP on transmission lines card
- Scope triggered by the laser signal
- Record two delay lines ends from the same trigger
- Tek 6154C scope at 20 Gs/s

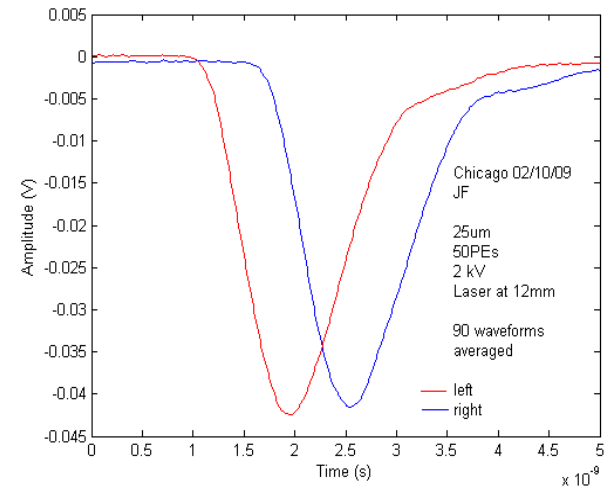
sub-mm position resolution

Sampled waveforms signal processing

Many techniques



Signal Template



B. Cleland and E. Stern, BNL

- Extract precise time and amplitude from minimization of χ^2 evaluated wrt a template deduced iteratively from the measurements, at the two ends of the T-line.
- With T-lines, the two ends responses are highly correlated, the MCP noise is removed.

Other technique (Henry Frisch) : sample the rising edge, fit to a straight line, intersect with the time axis

Pico-second timing with 2D T-lines readout

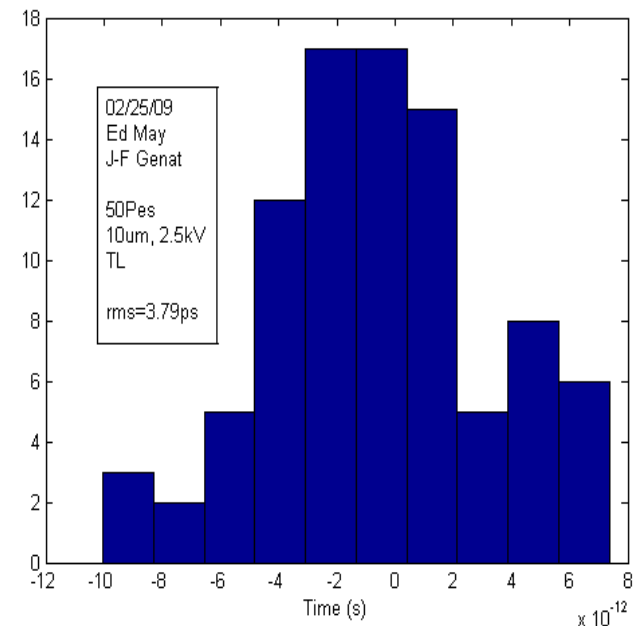
Waveform sampling provides fast timing (MCPs: 30-50ps with 1 PE).
Delay lines responses provide position information along the lines using fast timing

Less electronics channels for large area sensors wrt pixels devices

Laser tests:

**3.8 ps (measured) spread in the difference translates
in 190 μm position resolution with 50 photo-electrons**

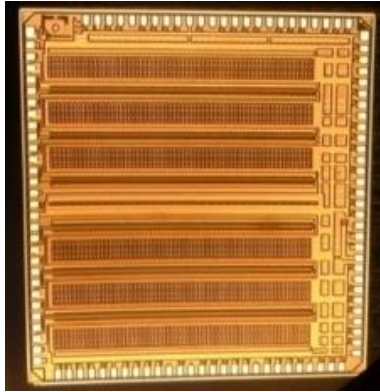
$\frac{1}{2} (t_1 + t_2)$ = time
 $v(t_1 - t_2)$ = longitudinal position
 $\Sigma \alpha_i a_i / \Sigma \alpha_i$ = transverse position



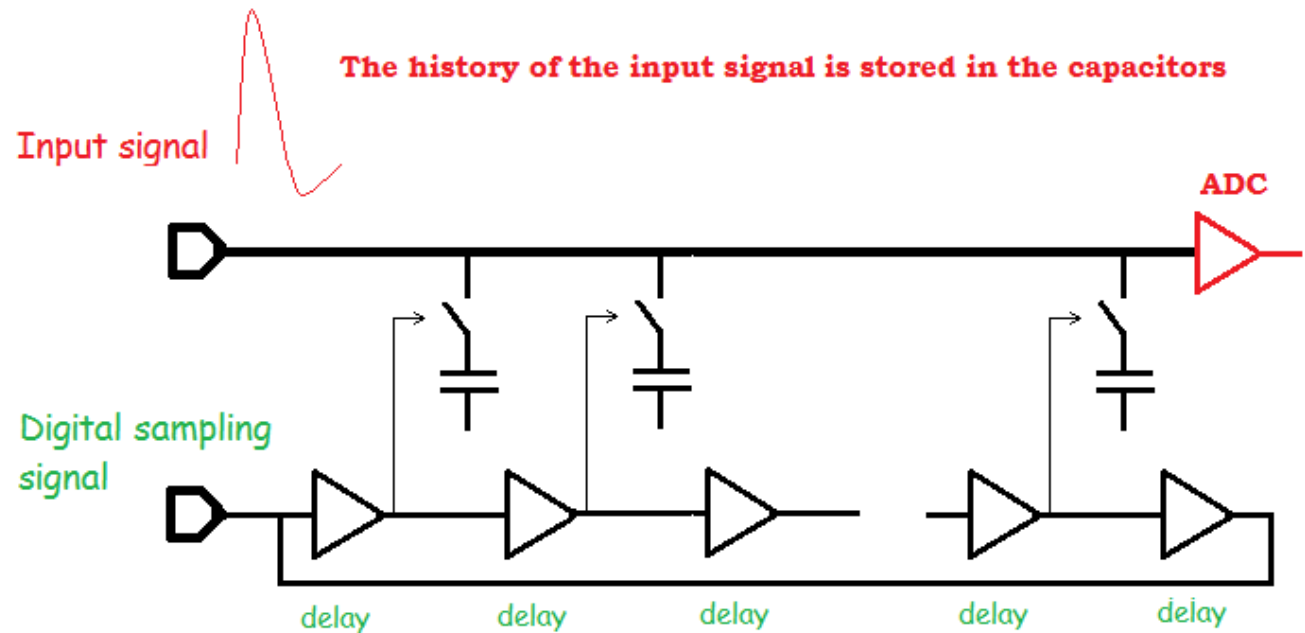
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Switched Capacitors Arrays (SCA)



Chicago PSEC4 ASIC

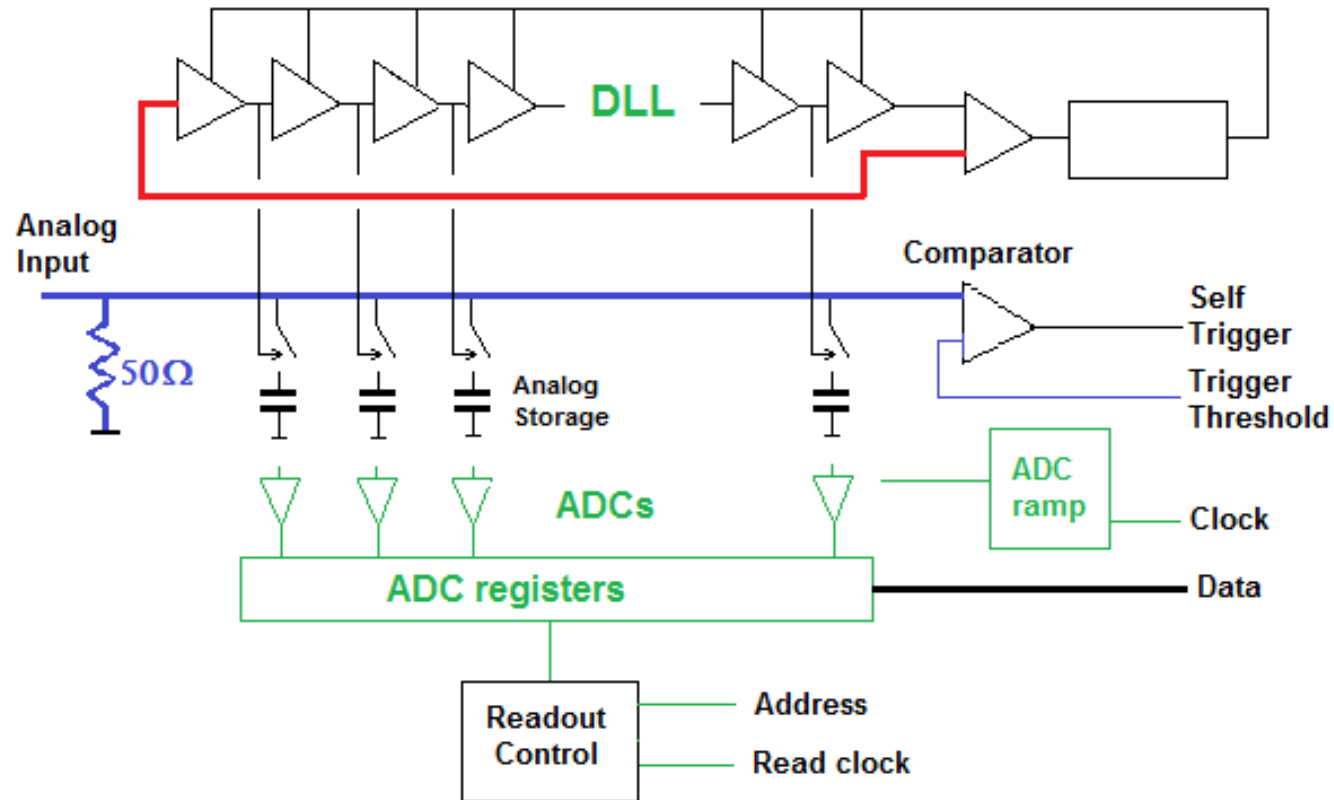


The input signal is sampled at the **delay** period (ps-ns)

Readout slow: the ADC may need to be very accurate, at the expense of conversion delay

PSEC4 digitization: one ramp generator + (one comparator + one 12-bit register) / channel

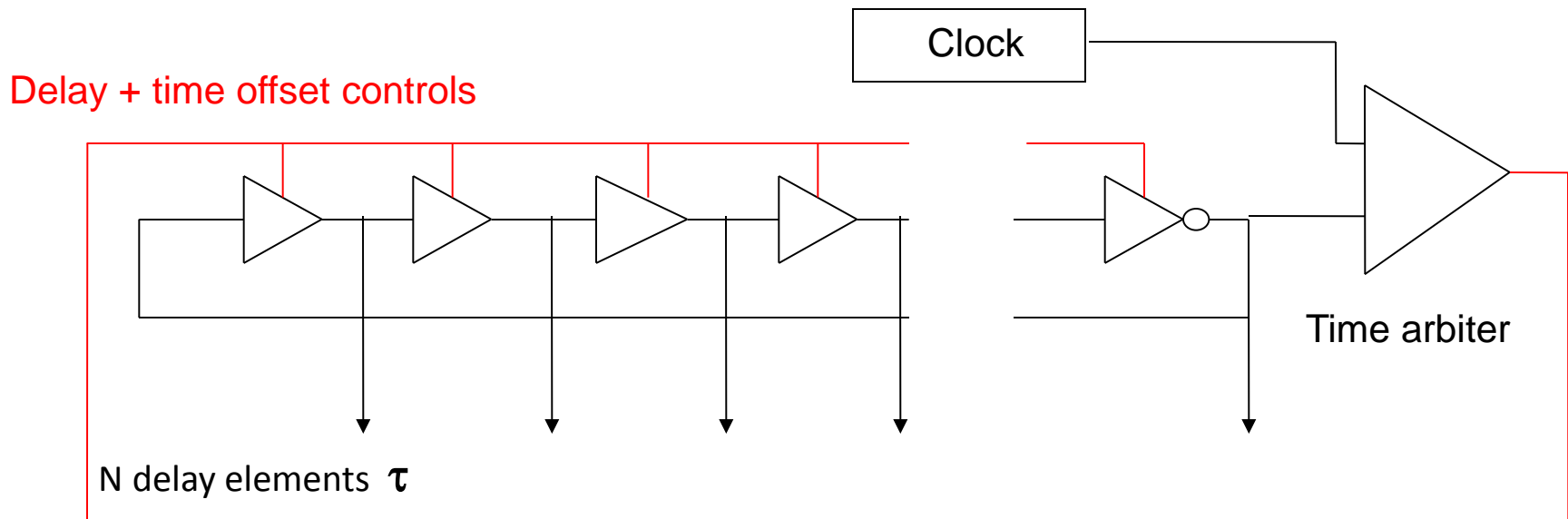
Fast Sampling Switched Capacitor Array



Analog Sampling Memory

Fine timing: Digital Delay Lines

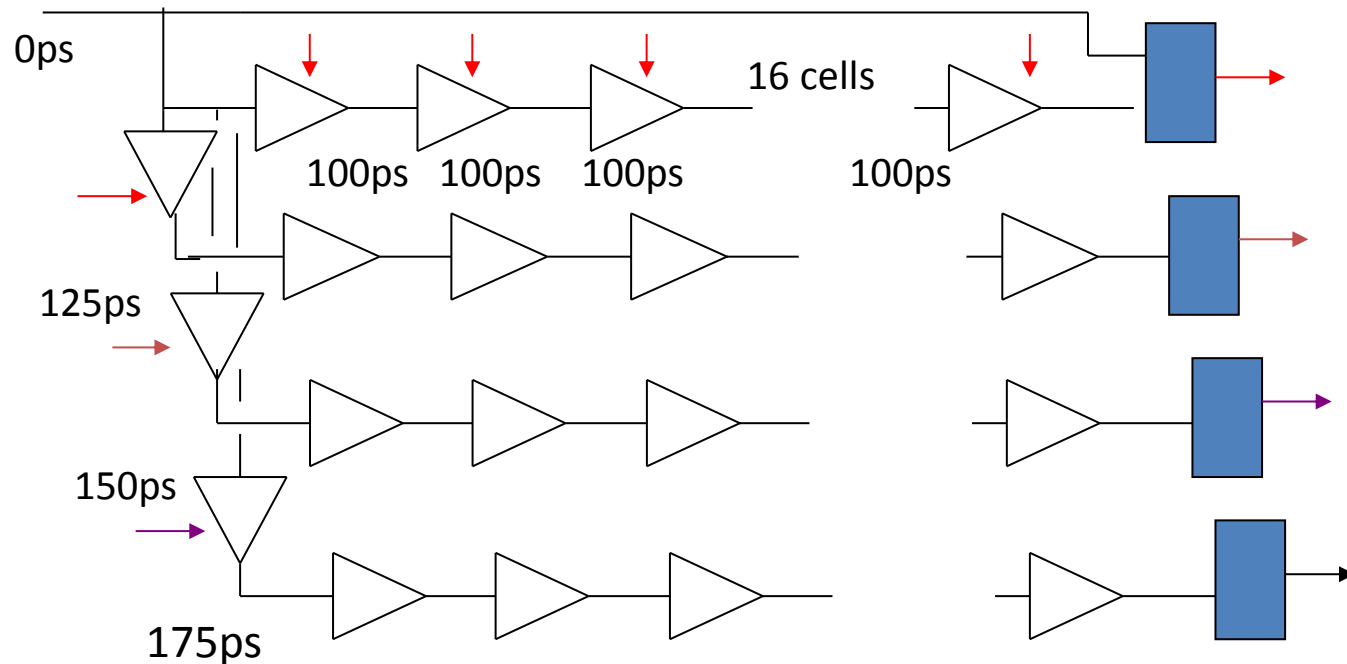
- **Locked delay line (DLL) or ring oscillator (PLL) if looped**
Loop of voltage controlled delay elements locked on a clock.
- **Generation of subsequent logic transitions distant by τ that can be as small as 10-100 ps**



Total delay is half a clock period when locked, the two edges can be locked

40 GS/s Timing generator

640 MHz clock in



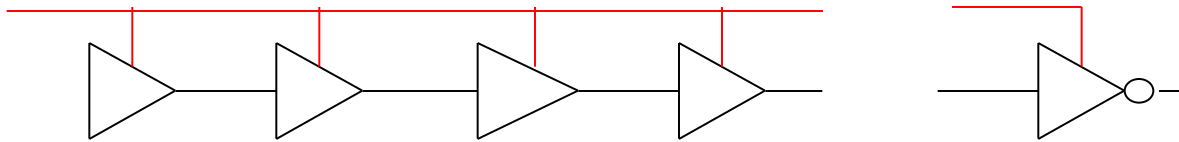
16 x 4 = 64 cells, 25ps step delays

Jorgen Christiansen, CERN

Delay Elements

Active RC element: R resistance of a switched on transistor
C total capacitance at the connecting node

Typically RC = 20ps-1ns using current IC technologies
an inverter propagation delay is 10ps in 32nm CMOS technology



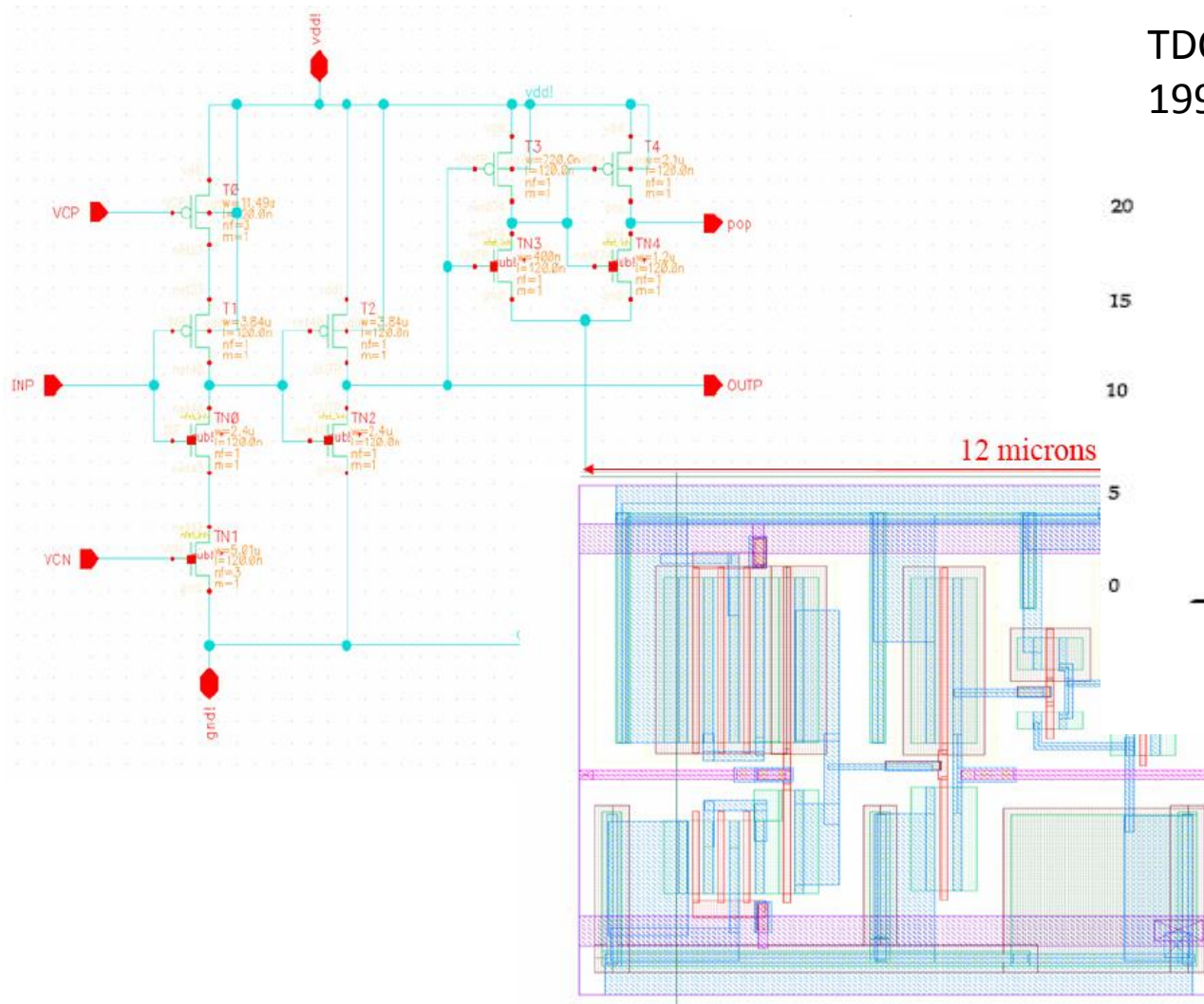
n delay elements with propagation delay $\tau = RC$

The propagation delay of RC's spread σ_{pd} limits the accuracy $\sigma_n = \sigma_{pd} \sqrt{n}$
 σ_{pd} is technology dependent: the fastest, the best.

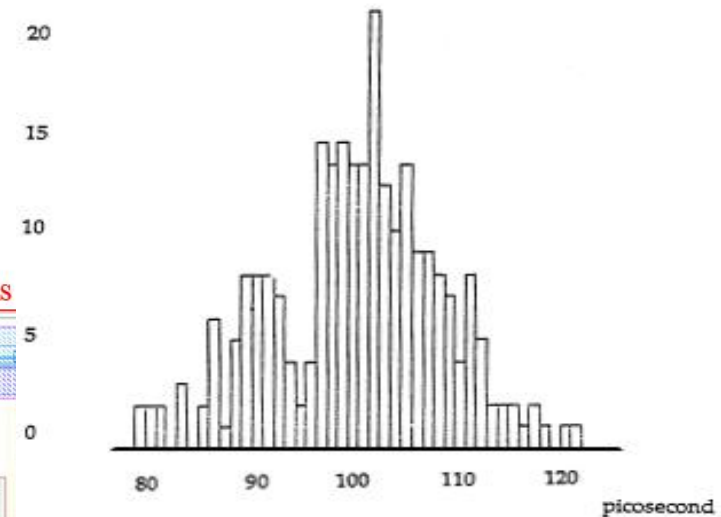
Within a chip $\sigma_{pd} \sim 1\%$
a wafer $\sigma_{pd} \sim 5-10\%$
a lot $\sigma_{pd} \sim 10-20\%$

In practice, lines of 16-32 delay elements can be safely used

Starved CMOS inverter cell (CMOS 130nm)



TDC bins histogram
1990 2 micron CMOS



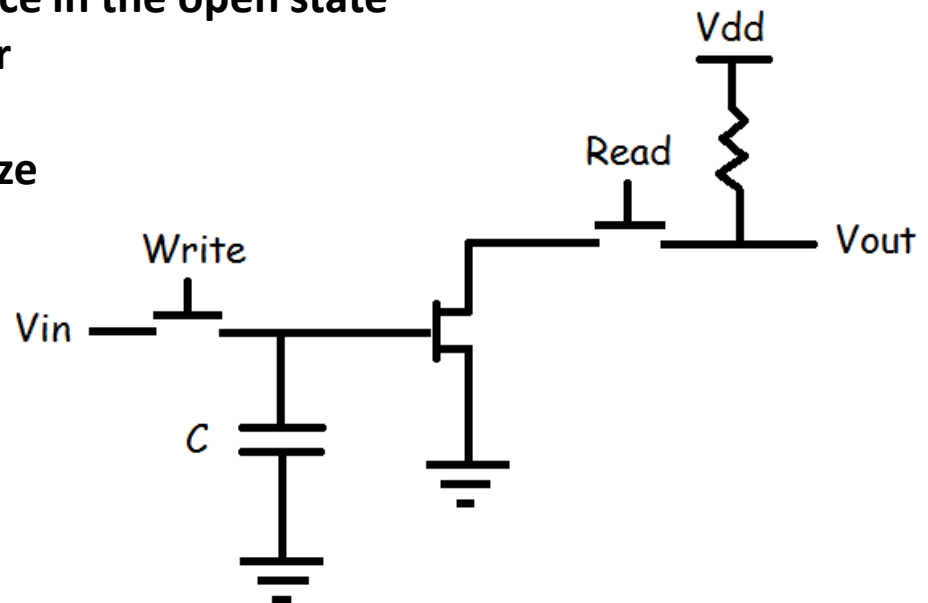
Bin size histogram for 256 bins from 4 chips.

Sampling Cell

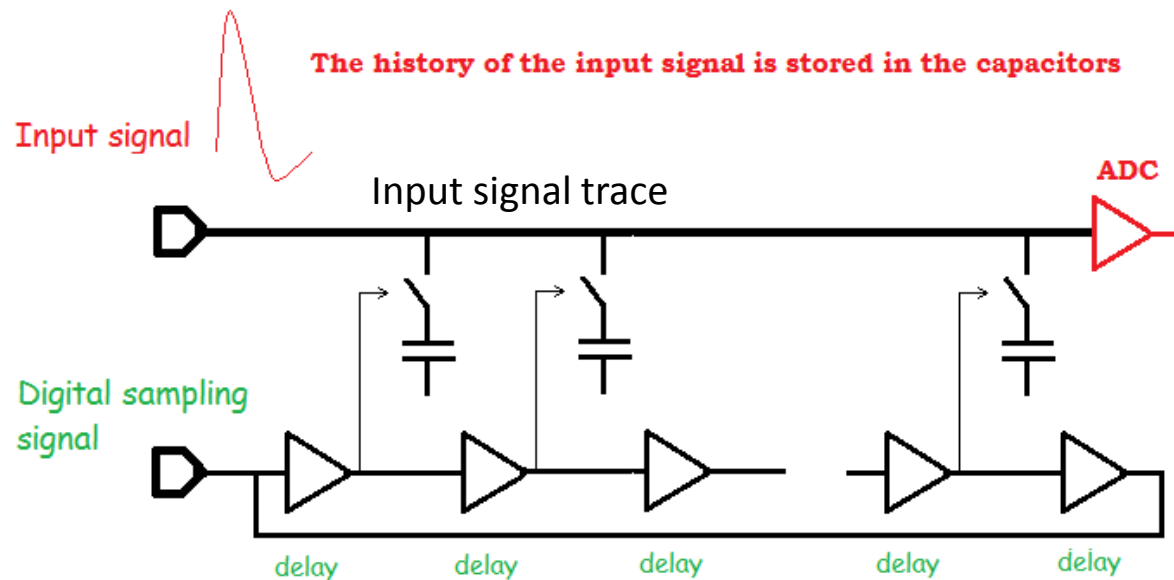
Bandwidth:

- The sampling capacitor C should be as small as **leaks, parasitics and kT/C switching noise** allow. $C = 30$ fF typical in 130nm CMOS technology
- Take care of the Write switches capacitance in the open state
- An input buffer may be a bandwidth killer
- Speed depends on the IC process feature size

GHz bandwidth



Issues for High Frequency SCA Design



- The analog bandwidth is limited by the input distribution line since all the open switches capacitors add up. The input signal distribution trace **resistance** is critical. The sampling capacitors should be as small as gate transistor leaks and parasitics allow, typ 20-100fF. ($50\text{fF} \times 1\text{k}\Omega = 50\text{ps}$)
-
- The input distribution line has to be designed as a **high frequency transmission line**
- Trade-off between recording length and analog bandwidth
- In practice, analog bandwidths $> 1\text{GHz}$, $> 10\text{GHz}$ sampling rates , 12-bit dynamic range

Fast Sampling ASICS

Several ASICS reported in this workshop

See e.g.

Eric Oberla's, D. Breton, E. Delagnes, S.Ritt, G. Varner ...

Conclusion

Sampling electronics and waveform analysis for 2" x 2" Micro-Channel Plate achieve

- **O(30ps) timing electronics (1 PE signals)**
- **2-dimension position sensing with millimeter precision**

Expect to be on the same order on Chicago-Hawaii
8" x 8" large dimensions devices

See talks by Henry Frisch, Ossy Siegmund, Eric Oberla

Thanks...