Development of fast frontend electronics for single-photon timing in RICH counters

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Overview

- Fast Timing in DIRC detectors
- TRBv3 FPGA TDC Development
- Frontend Electronics Developments for PANDA Barrel DIRC
- Characterisation of Frontend Cards
  - Laser pulser
  - Test experiment with DIRC prototype
- Conclusions

Fast Timing in Cherenkov Detectors

Fast single photon detection aids in

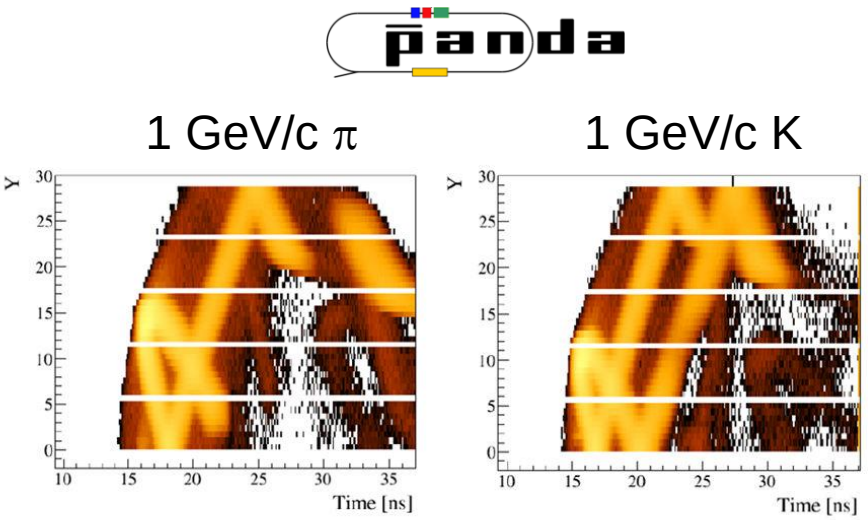
- Pattern recognition
- Improving angular resolution

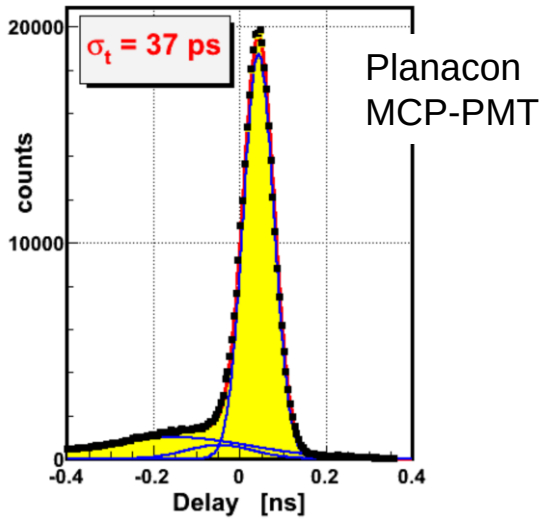
$$\sigma_{\theta_i} = \sqrt{\sigma^2_{\theta_{Pr}} + \sigma^2_{\theta_{Tr}} + \sigma^2_{\theta_{Im}} + \sigma^2_{\theta_{De}}}$$

Production
- Chrom. smearing
- Mult. scattering
- Track bending

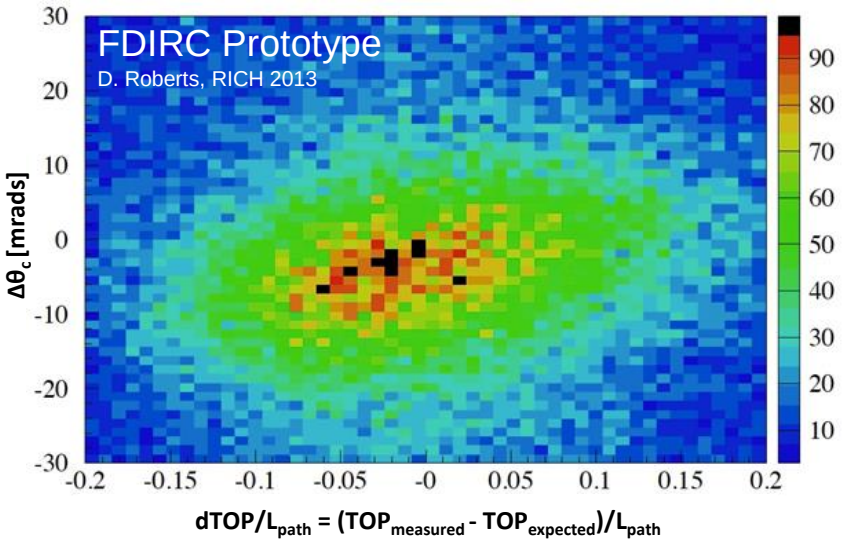
Transport
- Scattering
- Surfaces (DIRC)

Imaging & Detection
- Optics
- Pixel size
- Stand-off distance





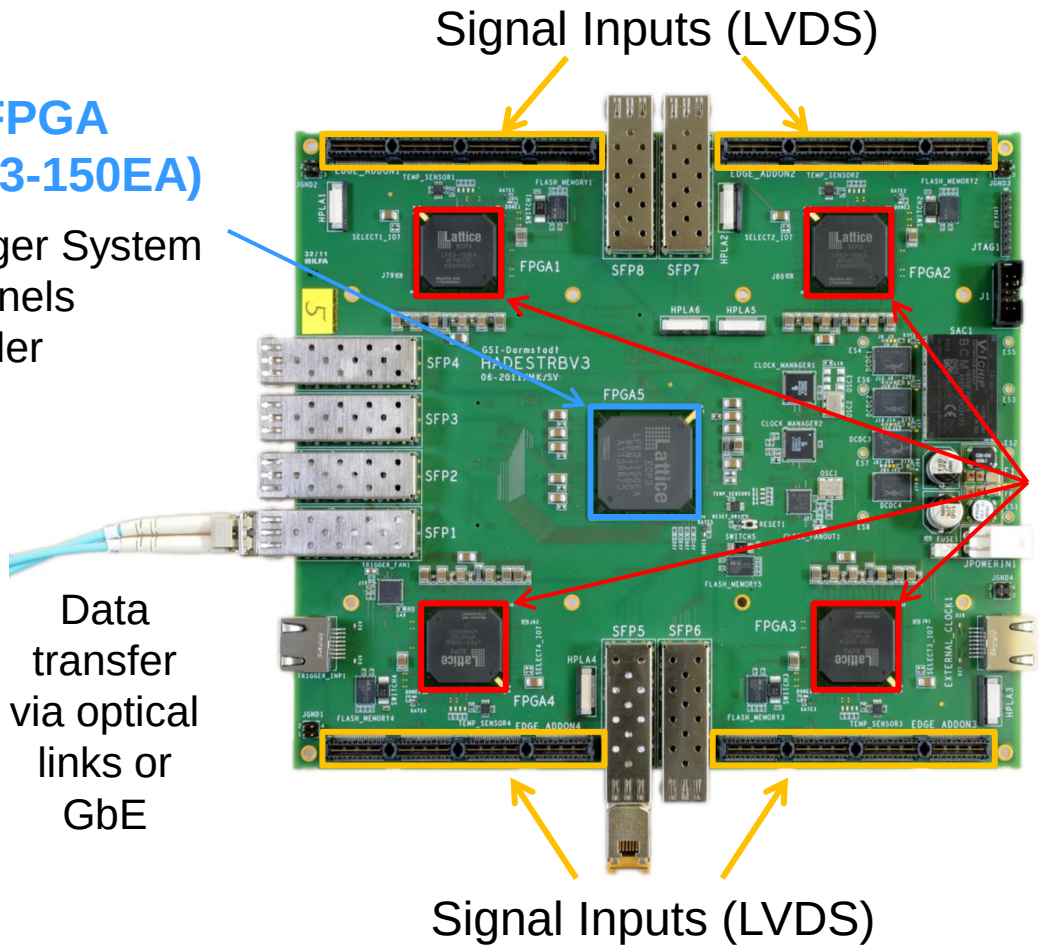
Planacon
MCP-PMT

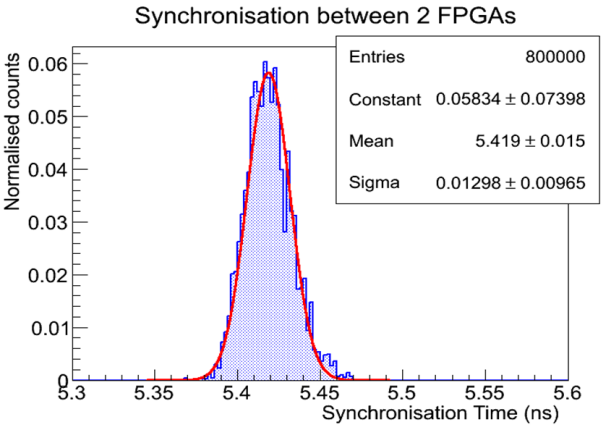


TRBv3 Platform

Central FPGA (Lattice ECP3-150EA)

- Central Trigger System
- 4 TDC channels
- GbE controller





Peripheral FPGAs (Lattice ECP3-150EA)

- Each with 64 TDC channels + Synchronisation
- 10ps RMS time precision (<20ps RMS on all channels)
- Minimum pulse width <500ps
- 50 MHz max hit rate (burst, up to 63 events)
- 700 kHz max data readout trigger rate (empty frames)

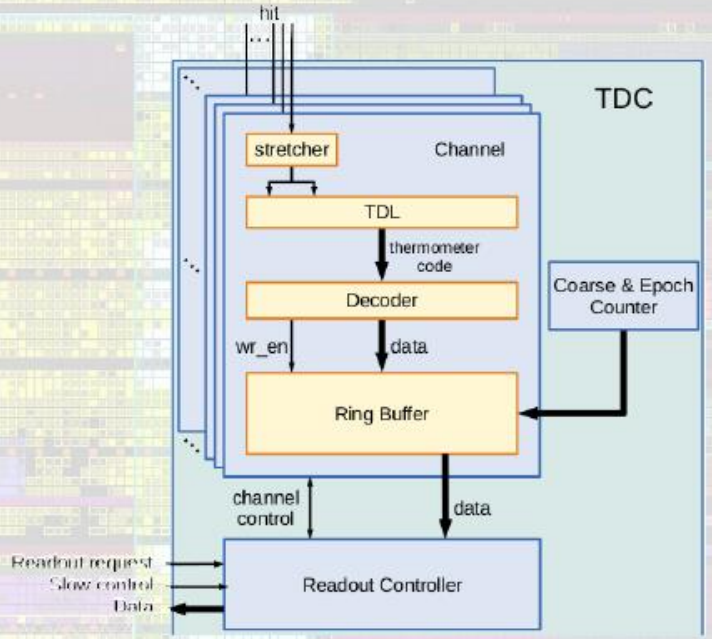
Developed at GSI (see http://trb.gsi.de/)

Readout for PANDA Barrel DIRC prototypes

TRBv3 TDC Implementation

TDC Architecture

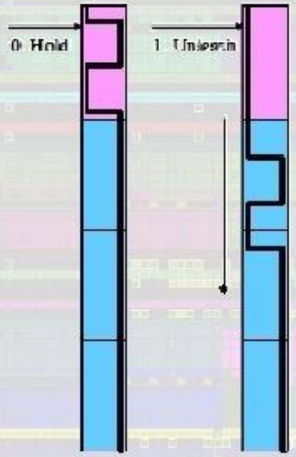
- Tapped Delay Line for fine time interpolator
- Coarse & Epoch counters for long measurement range
- Stretcher for short pulses
- Decoder: thermocode → binary
- Ring buffer for the latest hit signals



Simplified architecture of the TDC

TRBv3 TDC Implementation

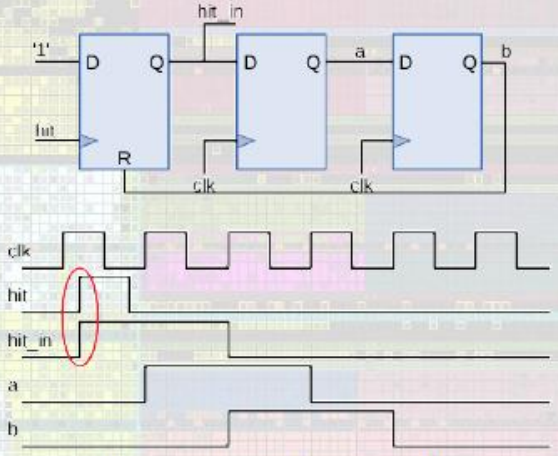
Improvements to Conventional TDC



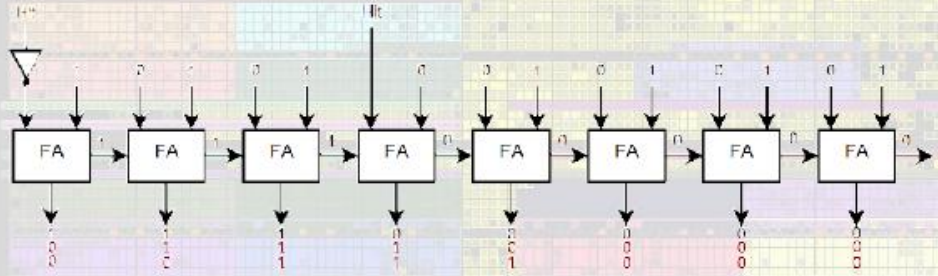
Wave Union Launcher

- Non-uniform intrinsic delays → Ultra wide bins
- The sensitivity of the TDC is reduced
- Wave Union Launcher [Jinyuan Wu]:

  send many transitions to the delay line, when a hit signal arrives, thereby increase the number of measurements on the delay line



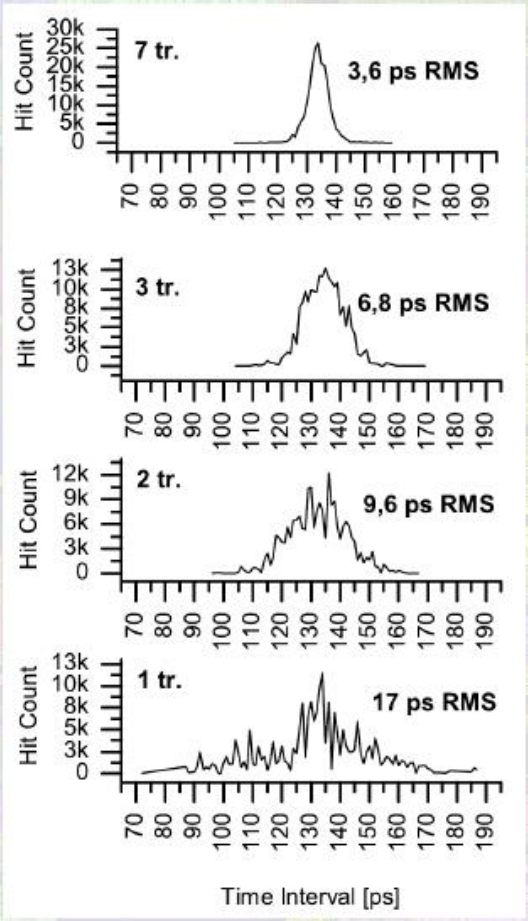
Semi-Asynchronous pulse stretcher



Implementation of WUL with Full Adders

- Traditional TDCs require hits wider than a clock period
- The width of the hit can be stretched semi-asynchronously
- The leading edge time information is still preserved

Precise TDCs in FPGAs



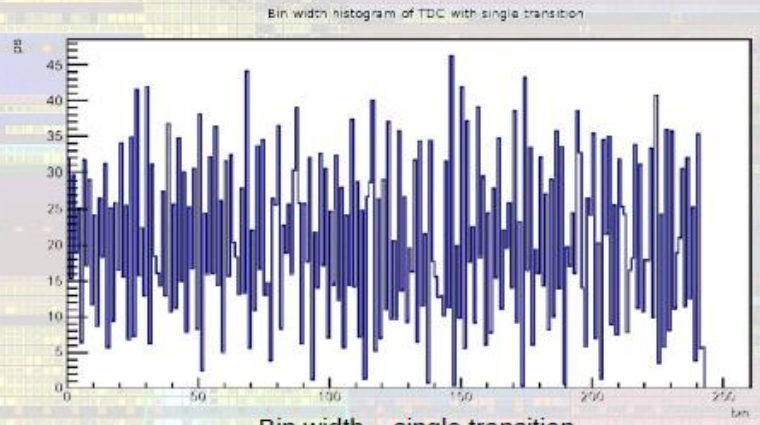
Published IEEE 2011, E.Bayer et al.

- TDC time precision down to 3.6 ps [RMS] (between two channels) using the wave union method [Jinyuan Wu] are possible
  - No cut on tails!
- Trade-off for number of channels, time precision and dead time can be adjusted to the needs of the application
  - 65 channels in an FPGA
  - <20 ps RMS time precision on each channel [RMS]

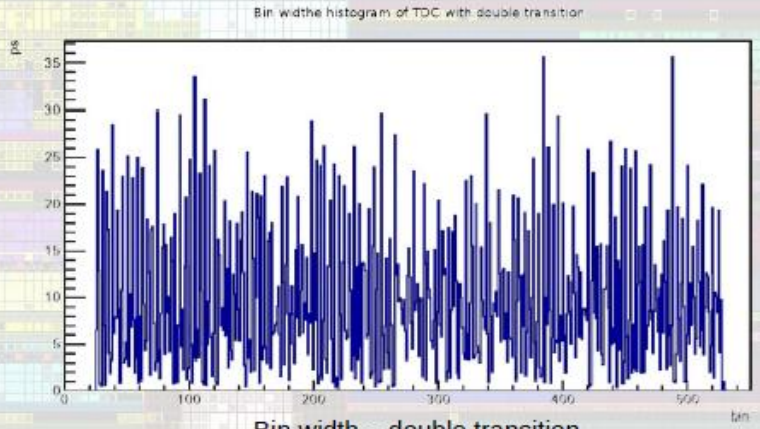
TRBv3 TDC Implementation

Non-Linearity Correction

- Non-linearities caused by non-uniform intrinsic delays
- UWBs increase non-linearities
- WUL averages the locations of the transition on the delay line, thus dividing the UWBs
- Max bin width: 45ps → 35ps
- Avg. bin width: ~20ps → ~10ps
- Calibration of the TDC further decreases the non-linearity
- Each bin width is calculated and a look-up table is generated
- $BW_n = P * H_n / H_T$

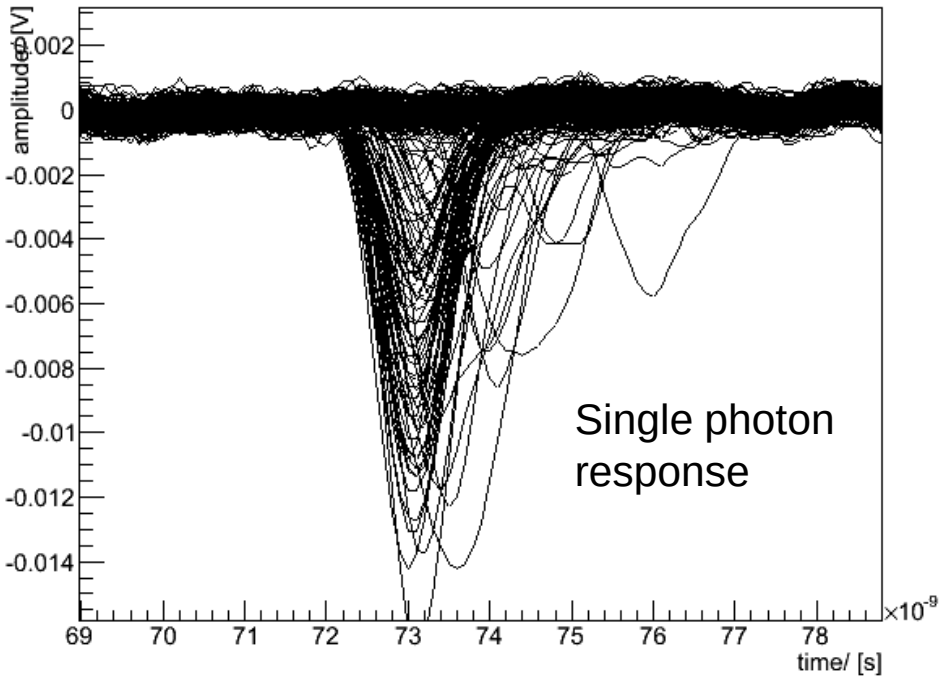


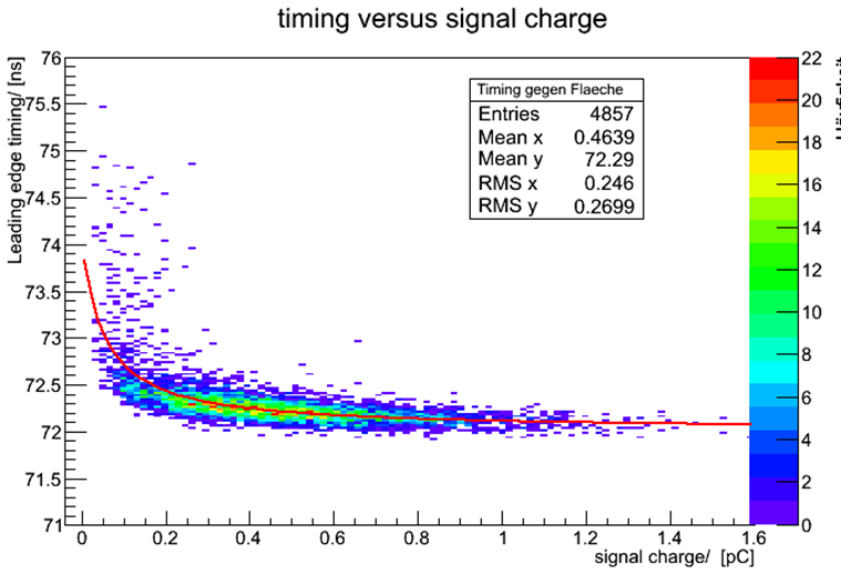
Bin width – single transition

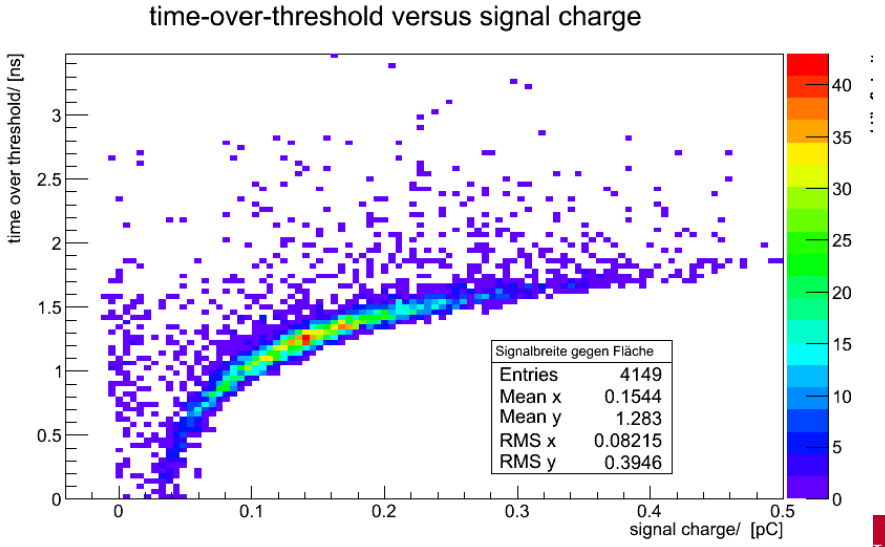


Bin width – double transition

Analogue Signals (MCP-PMTs)







Walk correction needed for best timing resolution

- Measure charge

PANDA environment demands fast readout

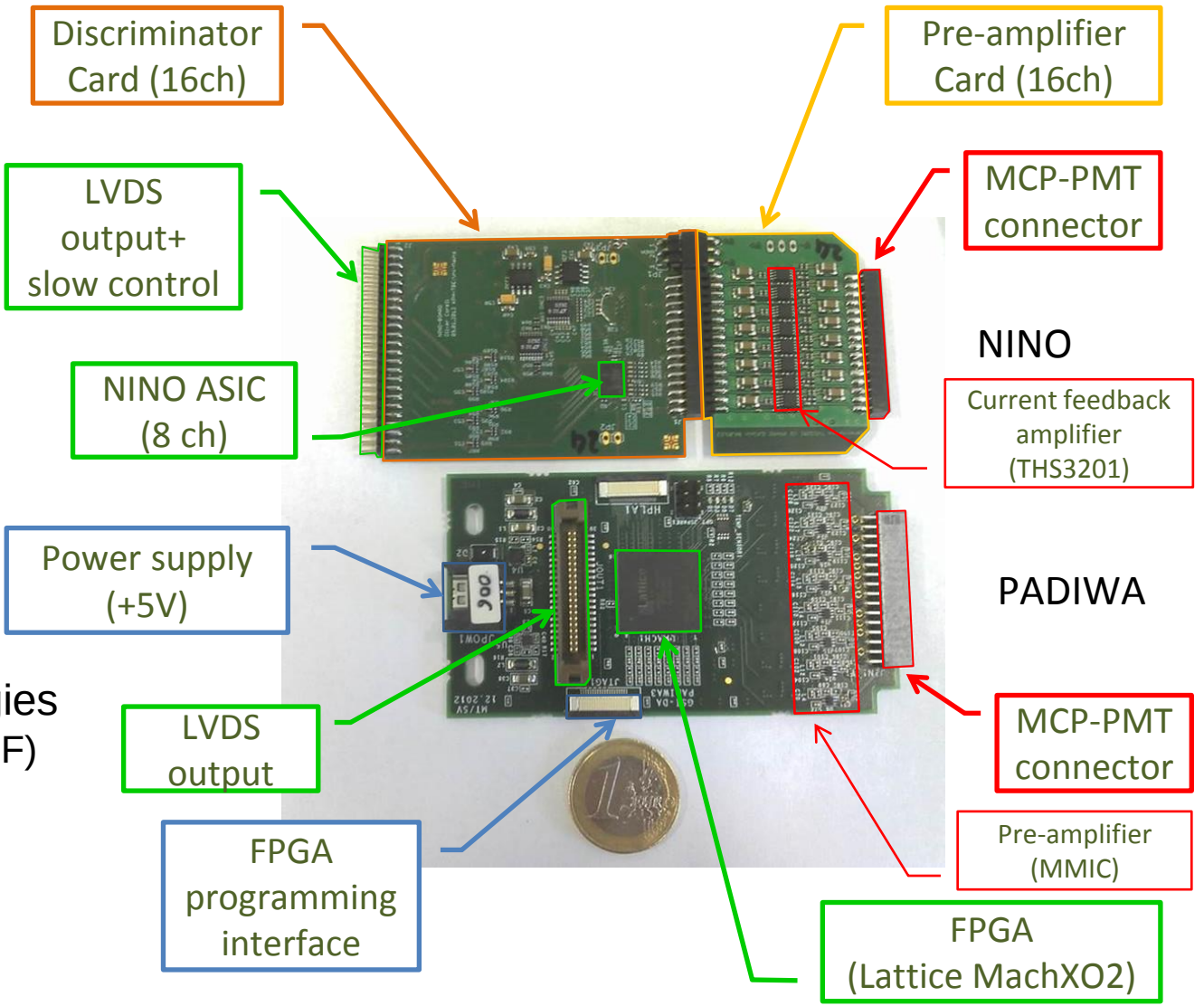
- Use Time-over-Threshold (ToT)
- Non-linear correlation!

Frontend Electronics Development

FEE Brief

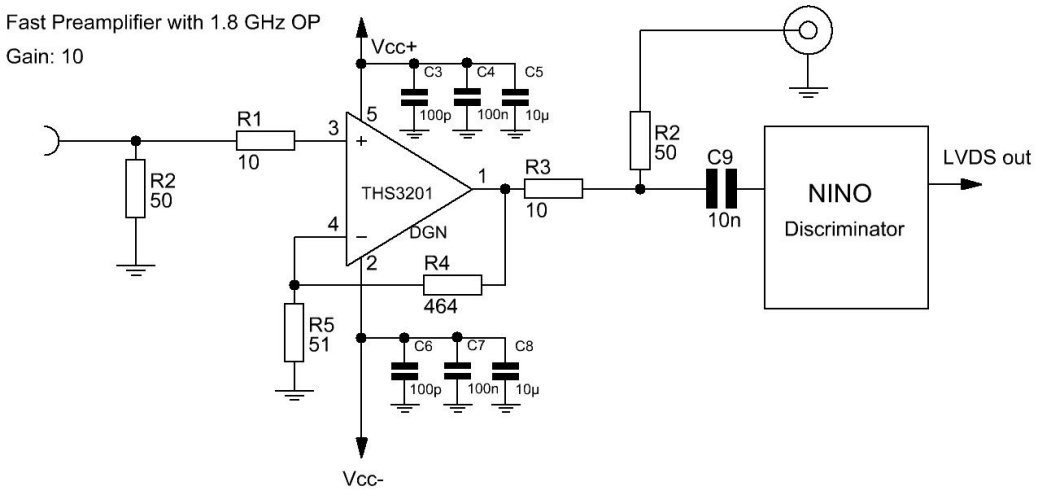
- Form factor set by MCP-PMT (5cm height)
- 16 channels per card (one connector row on Planacon MCP-PMT)
- LVDS output to interface TRBv3
- Low power consumption

- Compare different technologies
  - ASIC: NINO chip (ALICE TOF)
  - FPGA: PADIWA (GSI)

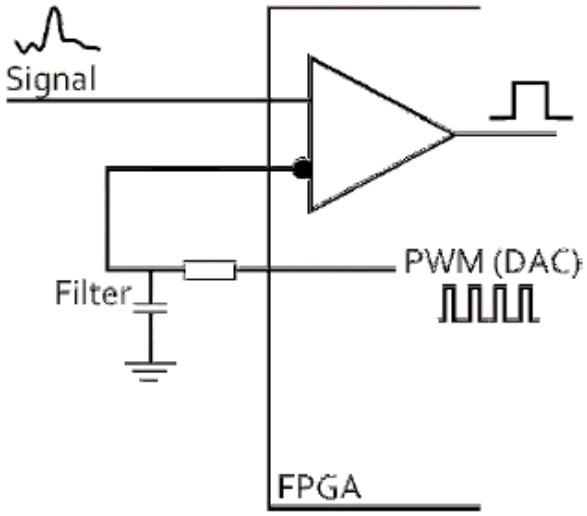


Frontend Electronics Development

- **NINO Card**
  - Adapt to single-ended signals
  - Pre-amplifier (1.8 GHz) to avoid low-charge behaviour of NINO chip

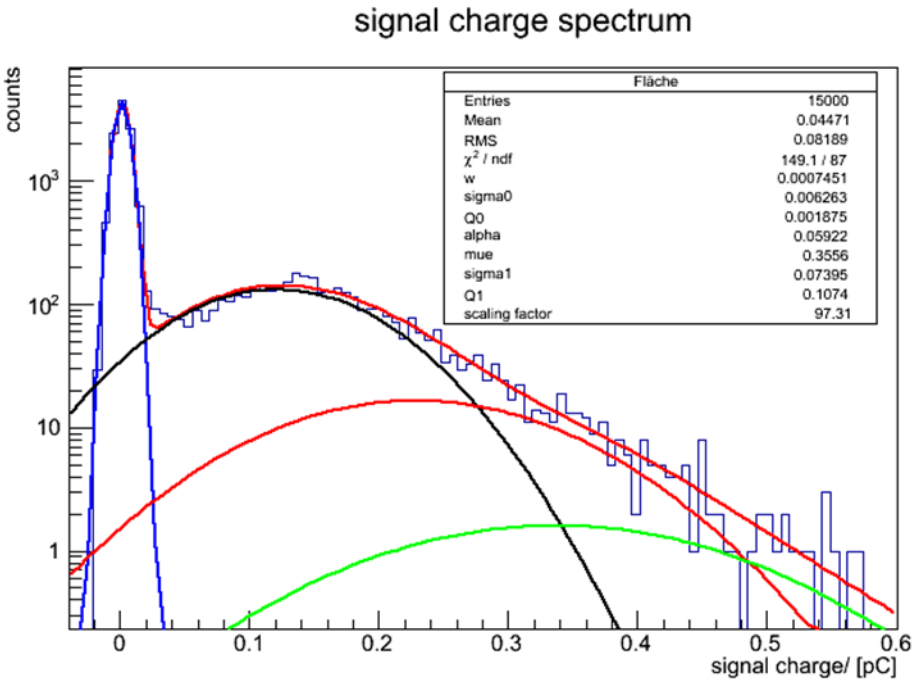


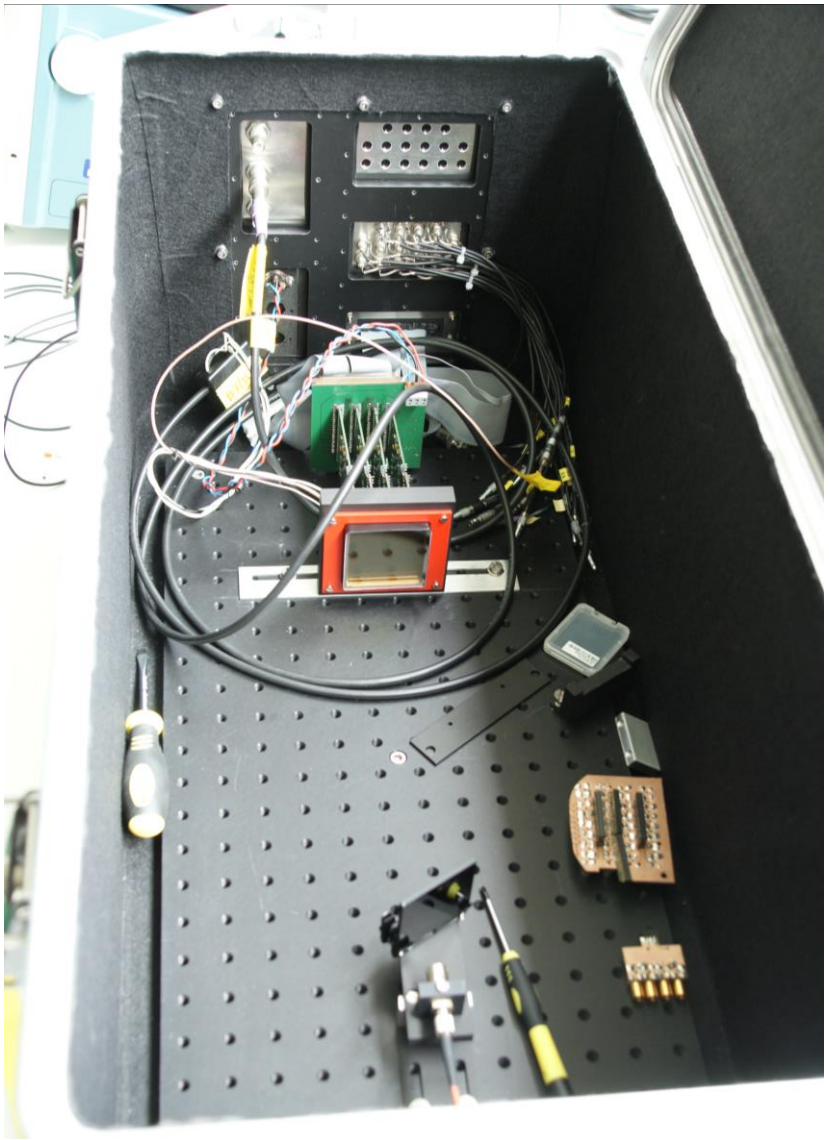
- **PADIWA**
  - Input LVDS buffers in FPGAs (Lattice MachXO2) are used as discriminators
  - Leading edge time and ToT are encoded in the output
  - The thresholds are set by using the FPGA as DAC via PWM and low pass filter



FEE Characterisation – Fast Laser

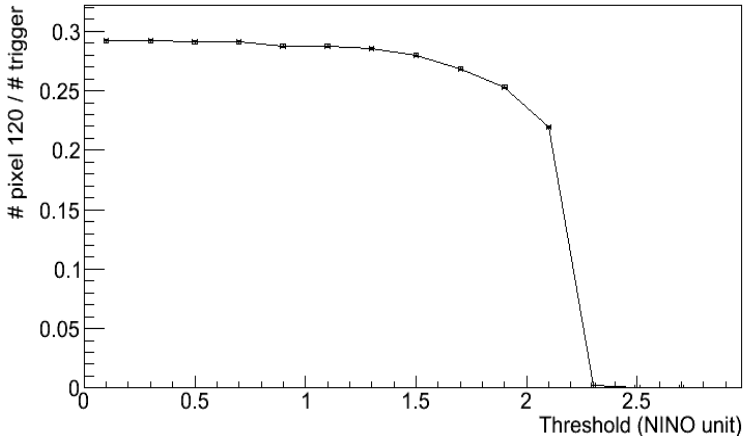
- PiLas system with 633nm diode
- Use ND filters to attenuate laser light
- Avg photon yield ~0.3
  (<4% multi photon events)
- Illuminate one pixel only
  (laser spot ~1mm)

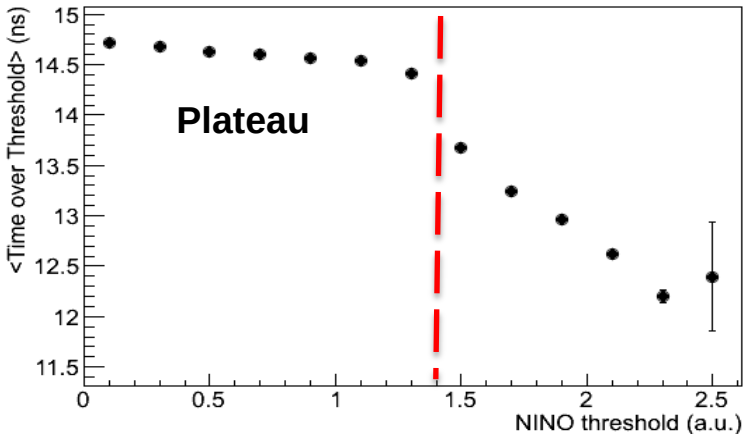


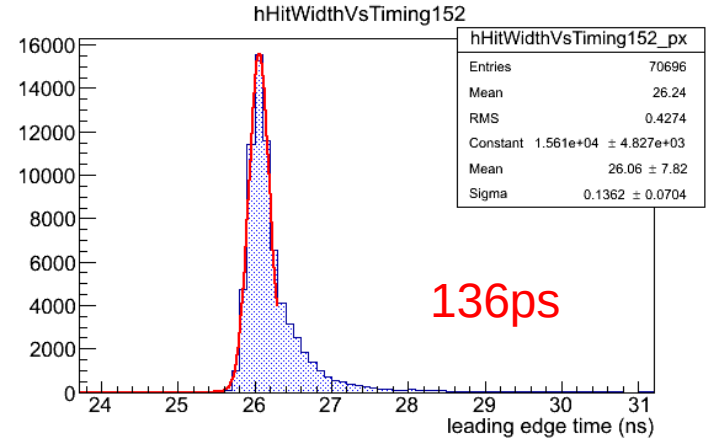


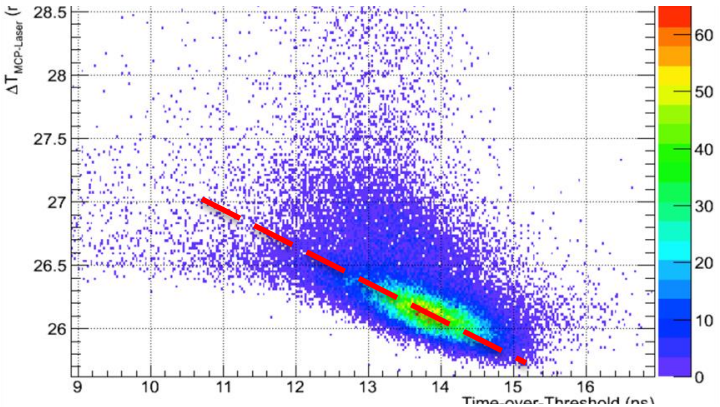
FEE Characterisation – NINO Cards

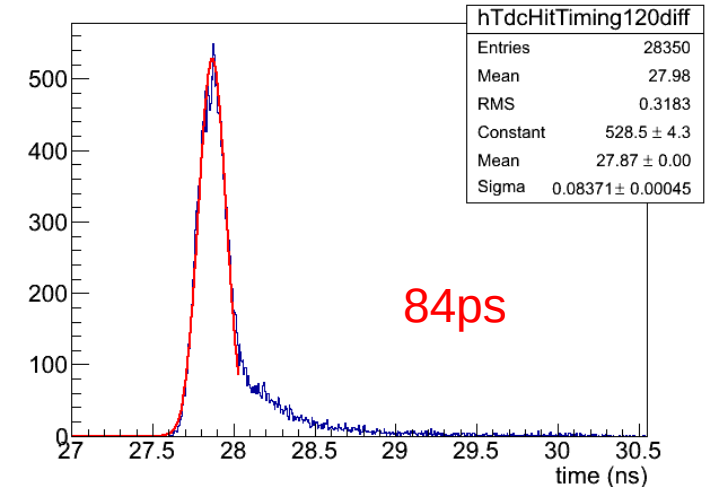
- Stable threshold achieved
- Observed plateau for thresholds
- Walk corrections effective





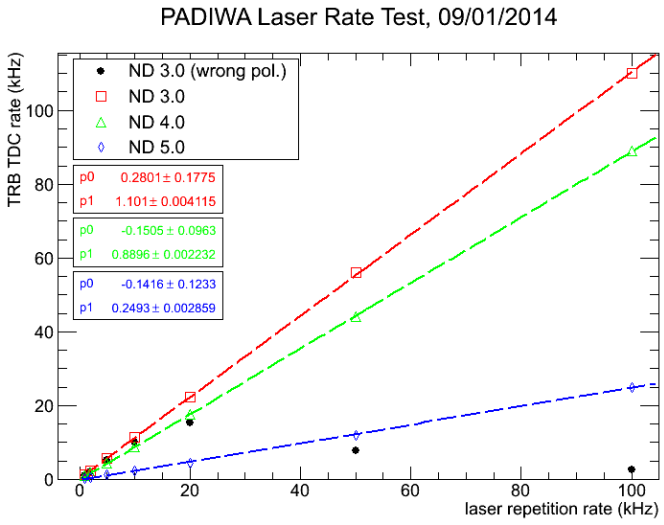


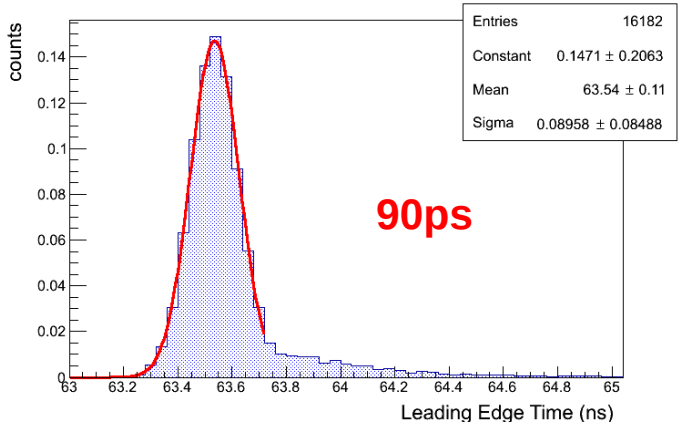


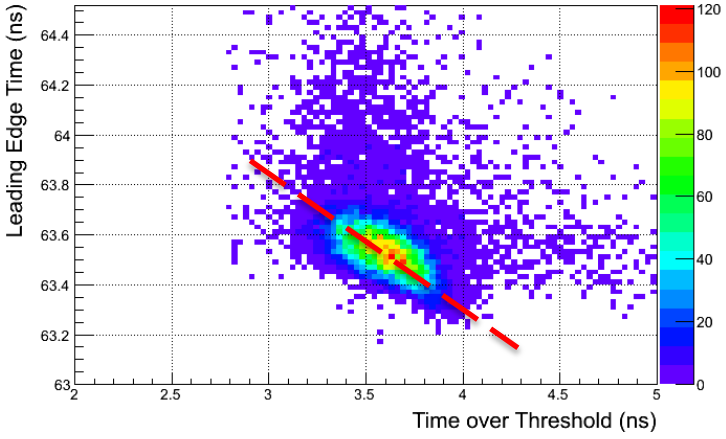


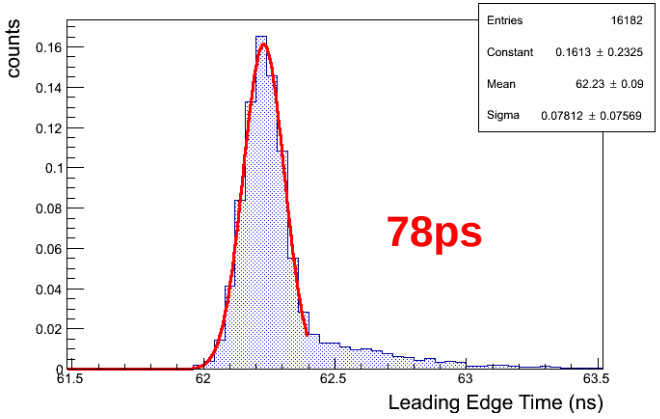
FEE Characterisation – PADIWA

- Raw single photon timing resolution ~ 90ps
- Walk correction implemented as 1st order polynomial based on ToT
- Corrected timing resolution ~ 78ps
- Rate capability tested up to 100kHz
- Threshold setting very sensitive to noise

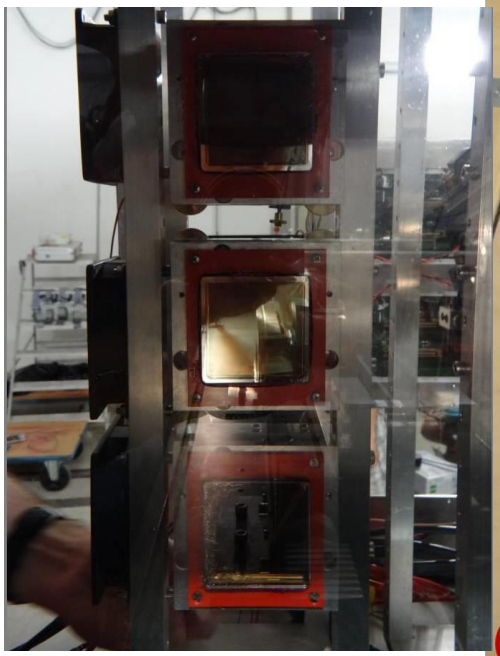




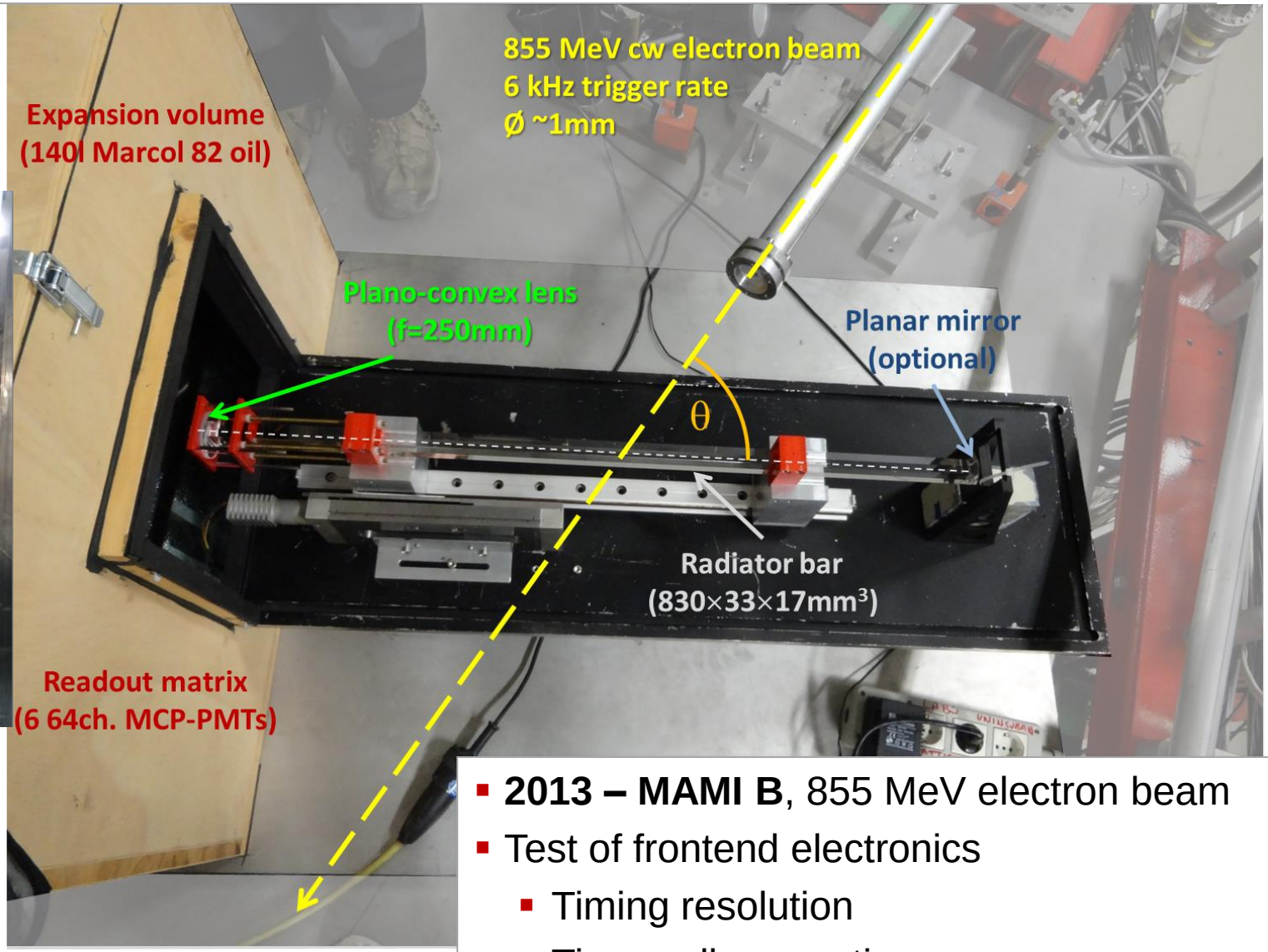




Test Experiment at MAMI (Mainz)



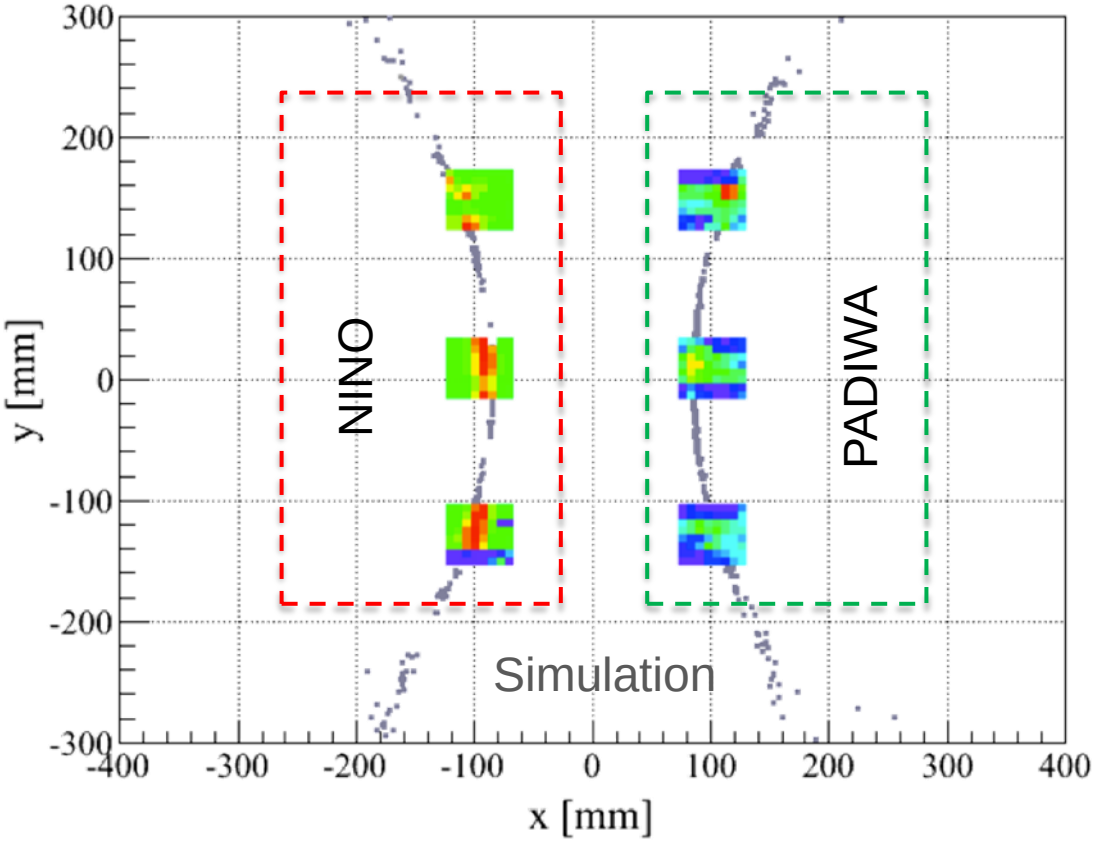
MCP Tower

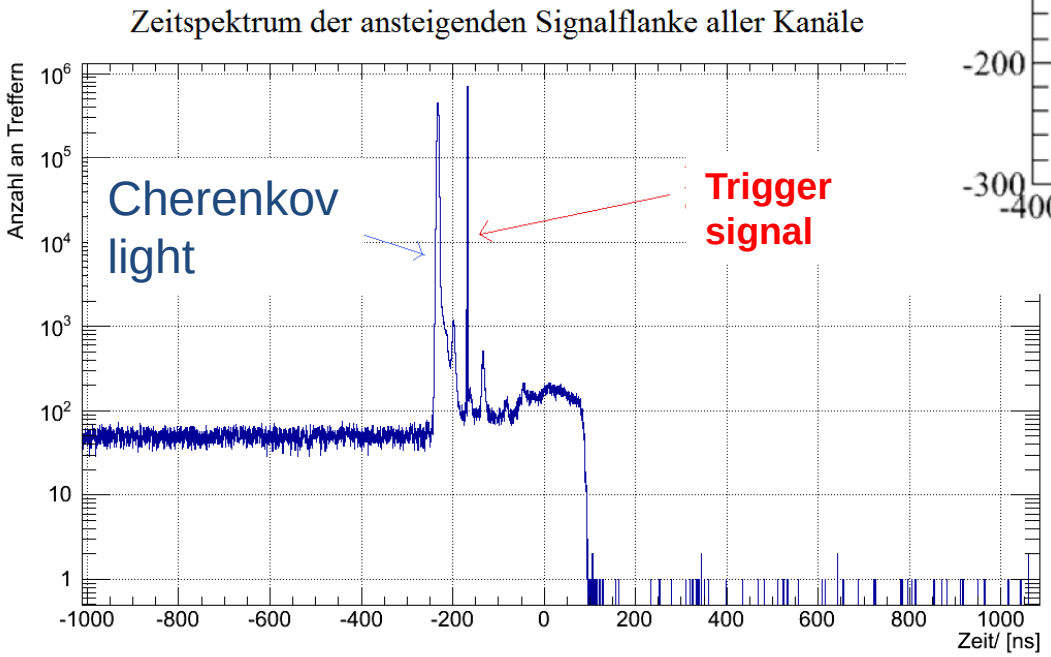


- **2013 – MAMI B**, 855 MeV electron beam
- Test of frontend electronics
  - Timing resolution
  - Time walk correction
  - Thresholds

Test Experiment – Cherenkov Patterns

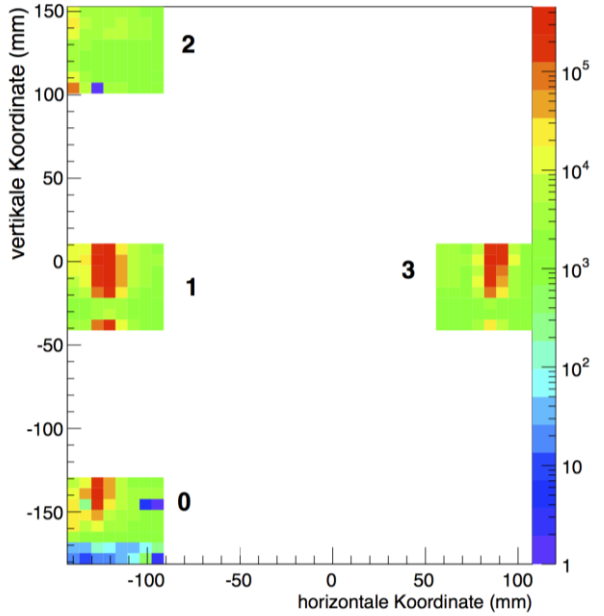
- Up to 384 channels readout with TRBv3
- Different angles to check pattern shift
- Different configuration of NINO & PADIWA cards
- MCP-PMT gain ~1×10^6

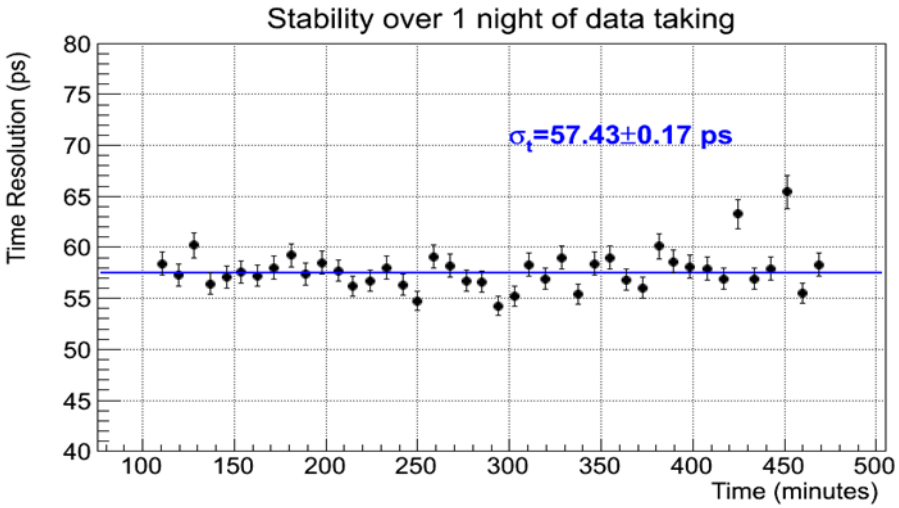


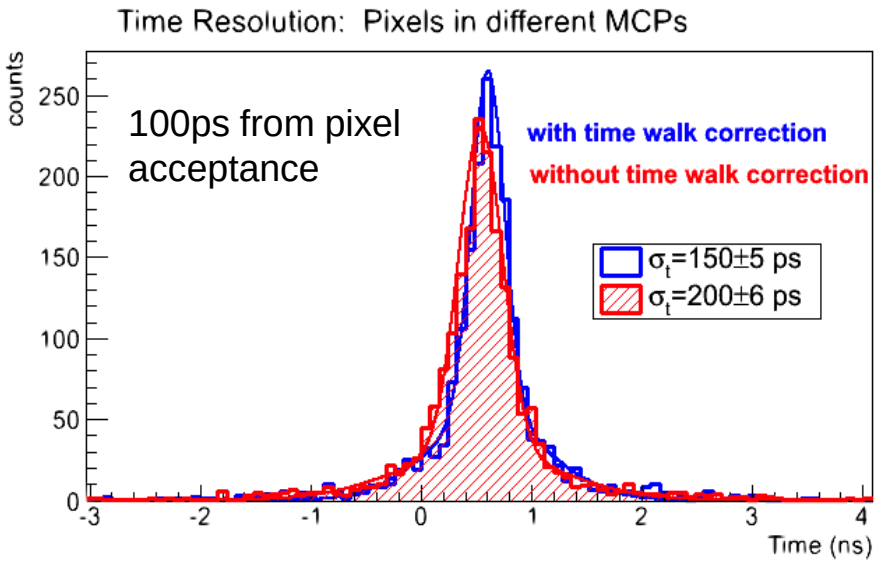


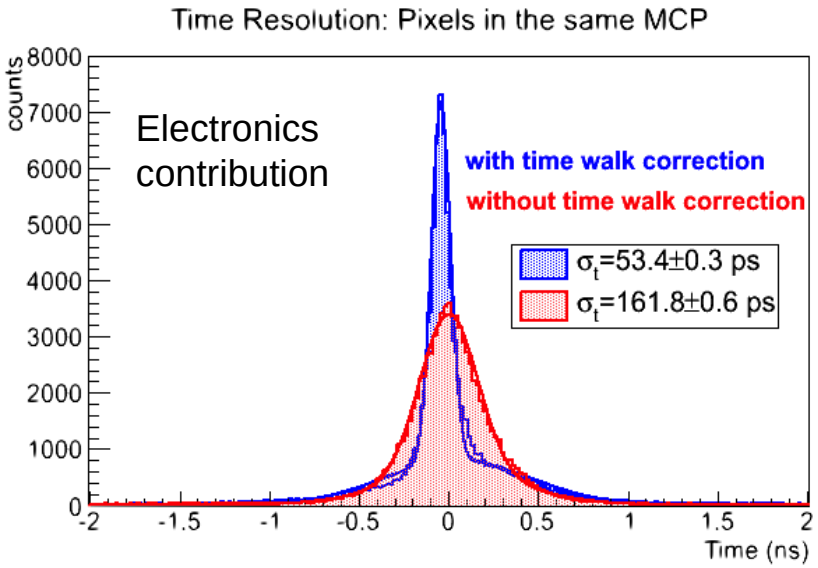
Problems with threshold setting for PADIWA cards
No useful data from test experiment

Test Experiment – Timing Results



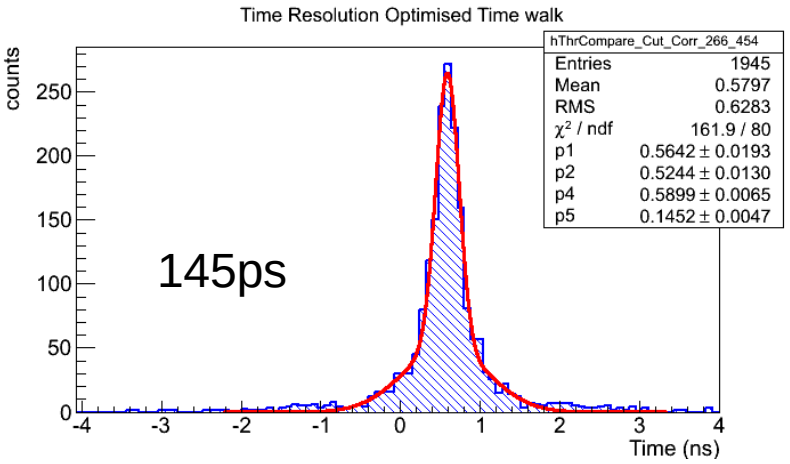


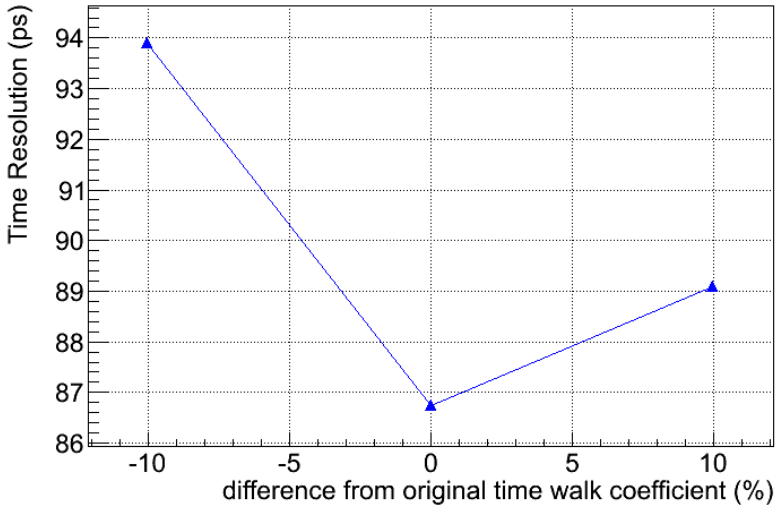


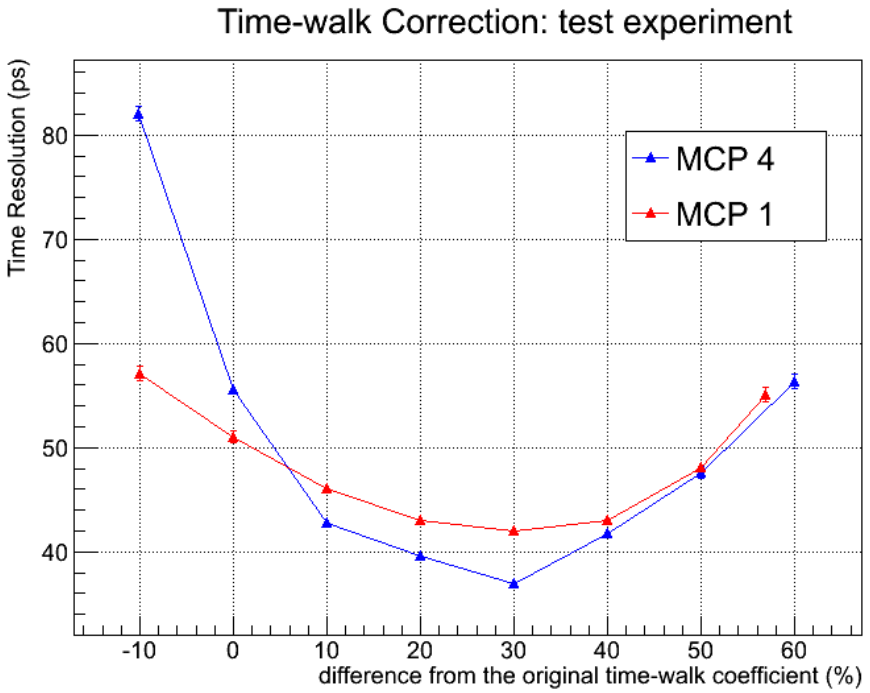


Optimisation of Timing

- Initially using walk parameters from laser characterisation
- Different parameters during test experiment
  - Optimise walk parameters using charge sharing
- Improving resolution to ~40ps
  - Works on different MCP-PMTs
- Little impact on system timing (~5ps)
  - Governed by path length variation







Conclusions

- Fast single photon timing (<100ps) in DIRC counters aids
  - Pattern recognition
  - Chromatic correction
- TRBv3 FPGA TDC provides
  - High-precision low cost TDC
  - Up to 256 channels with <10ps RMS
- Two types of Frontend Electronics developed
  - NINO ASIC
  - PADIWA based on FPGA
- Successful characterisation with laser & test experiment
  - Similar performance (<100ps SPE timing)
  - Electronics contribution to timing resolution ~40ps