Edge-TCT studies of non-irradiated HVCMOS sensors

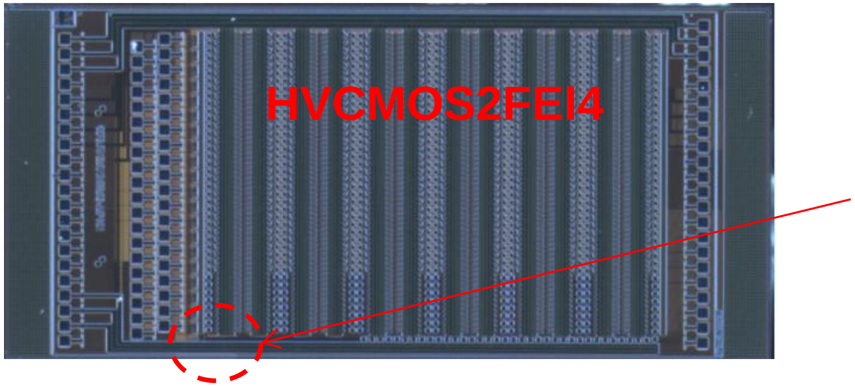
G. Kramberger

Jožef Stefan Institute, Ljubljana

on behalf of HVCMOS collaboration

Motivation/Introduction

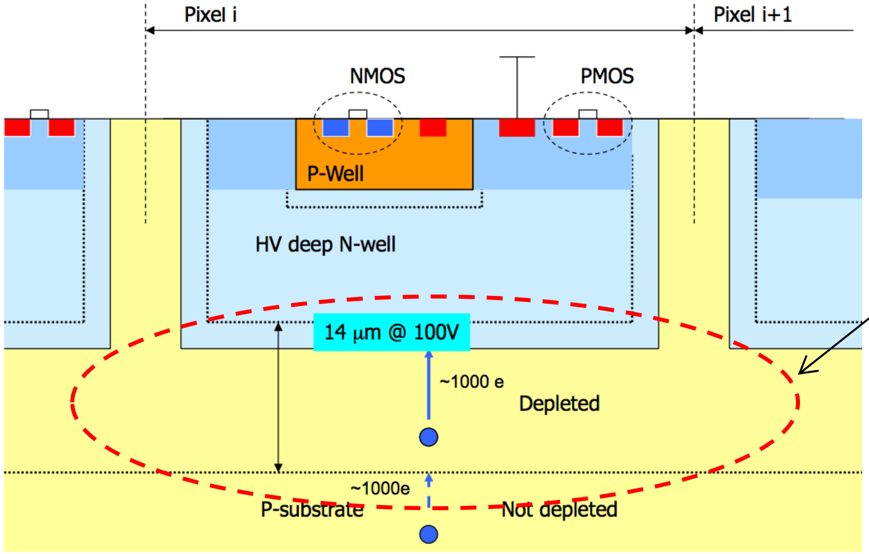
- Detectors based on HV/HR CMOS technology can offer significant cost reduction and open new ways of operation of silicon detectors
- Prototypes HVCMOS2FEI4 have been tested in strip and pixel readout mode
- It is essential to understand the charge collection from low-res silicon
  - particularly after large fluences of hadrons
  - at readout speeds required for HL-LHC
- Edge-TCT is an ideal tool to study charge collection properties



A single cell of 125 x 33 μm^2 was investigated – output to readout after the charge sensitive amplifier.

Not ideal (not observing induced current) , but good enough!

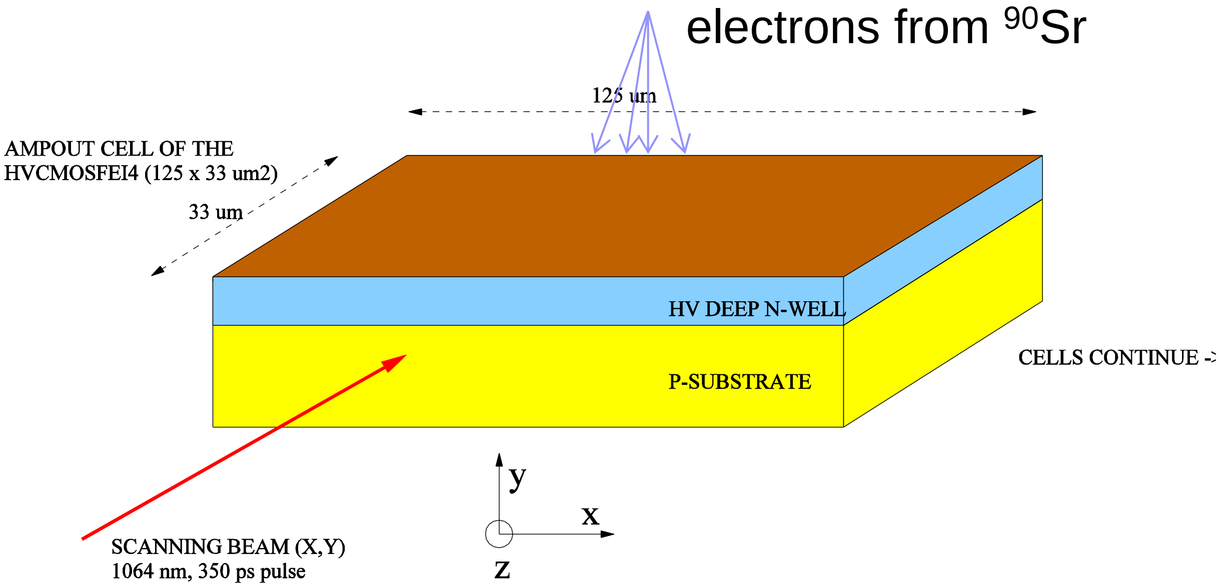
Basics of measurments



We are interested in charge collection studies at the **N-well – p substrate** junction.

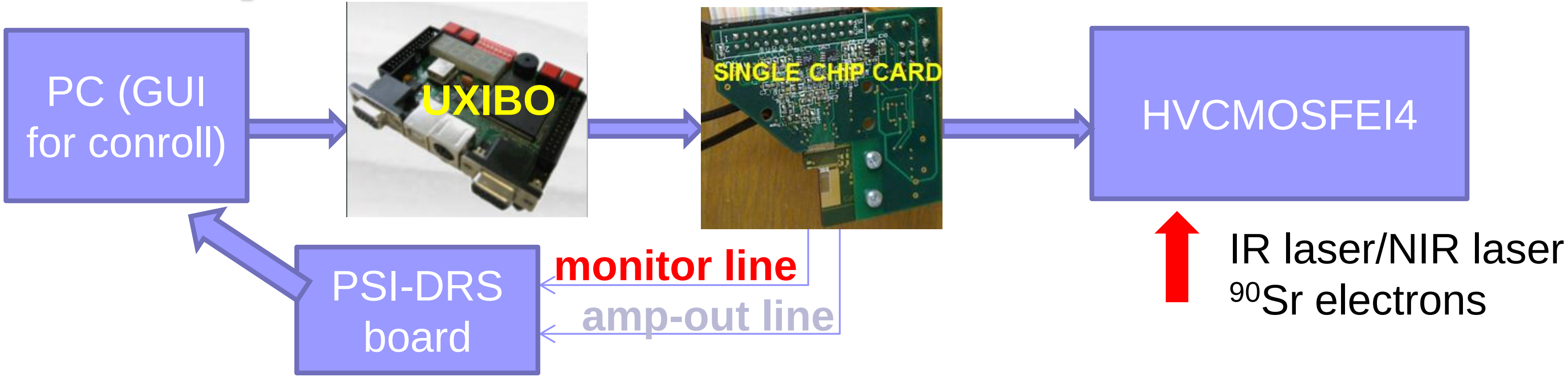
Two modes of charge generation:

- **IR beam**
- **Electrons from ^{90}Sr**



The simplified structure under test with axis orientation.

Setup



PC (GUI for conroll)

HVCMOSFEI4

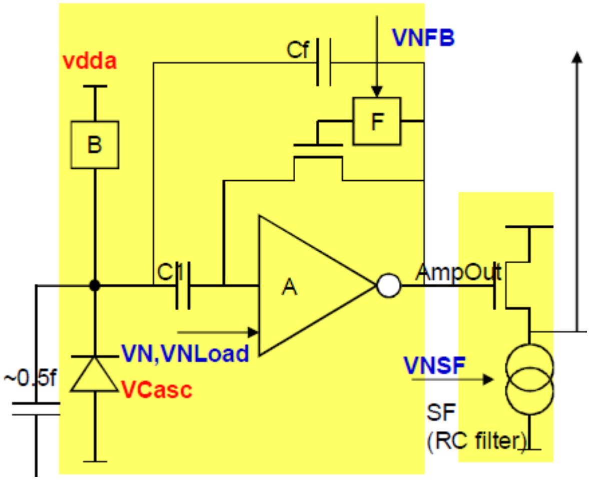
PSI-DRS board

monitor line

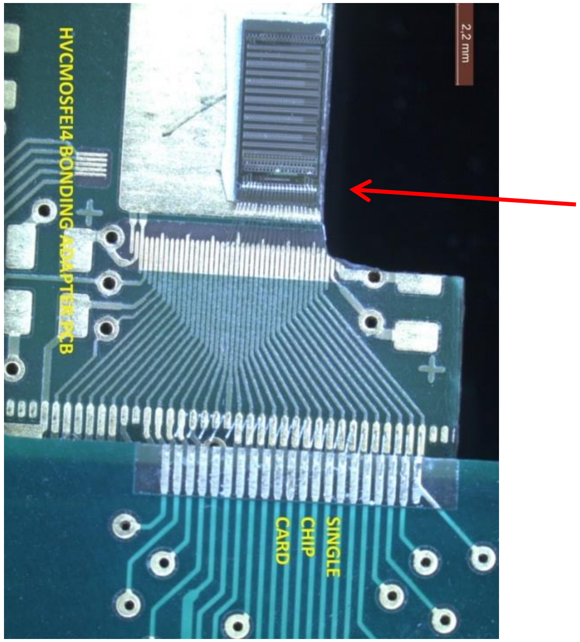
amp-out line

IR laser/NIR laser
^{90}Sr electrons

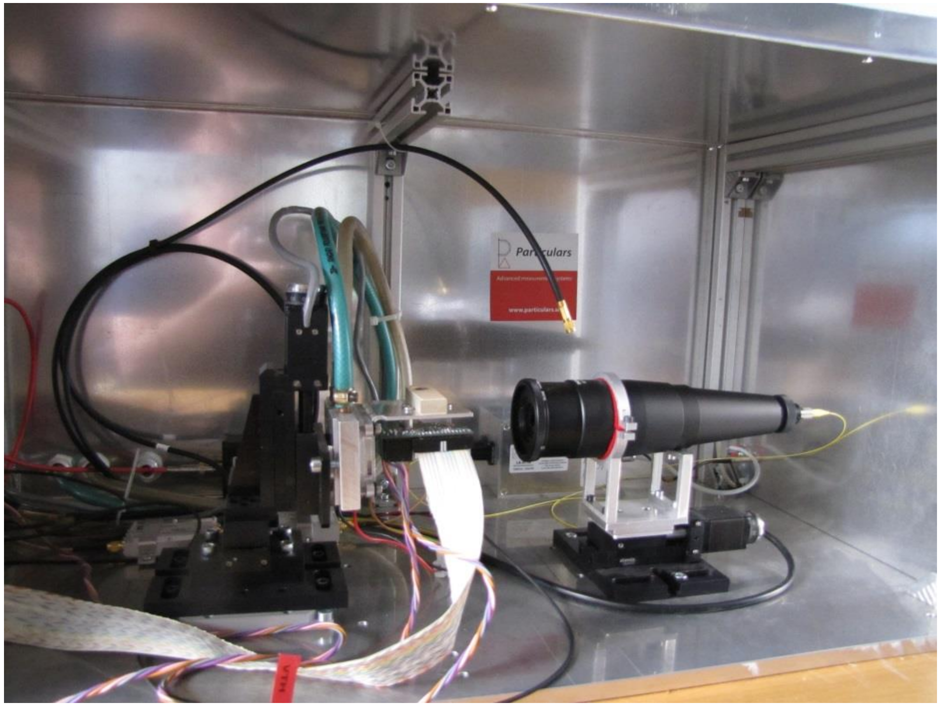
Single cell readout

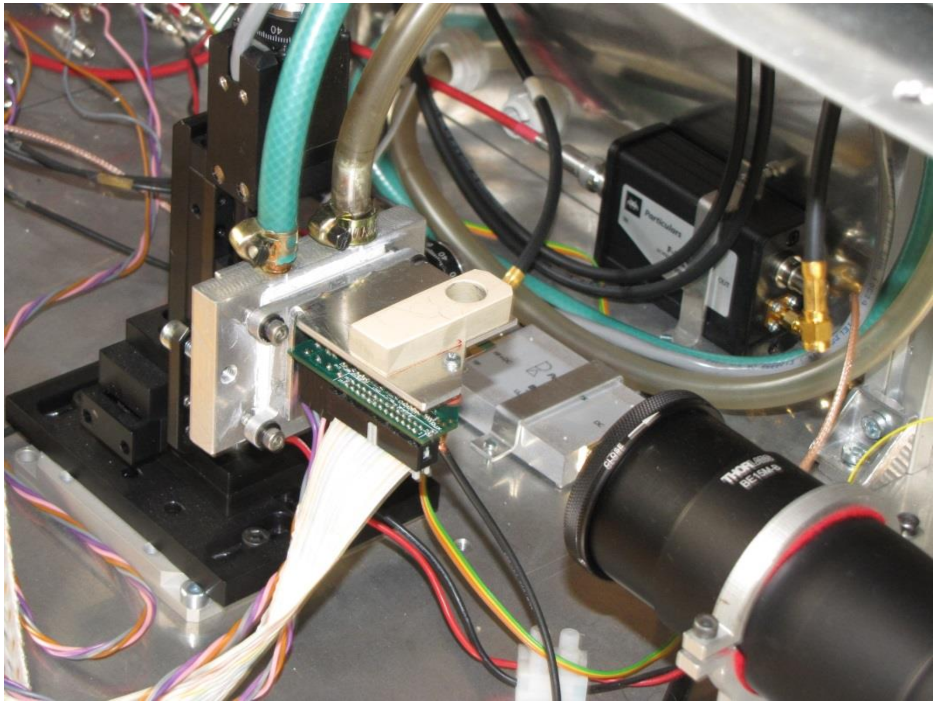


The line monitored in the oscilloscope



Scanning TCT sytem

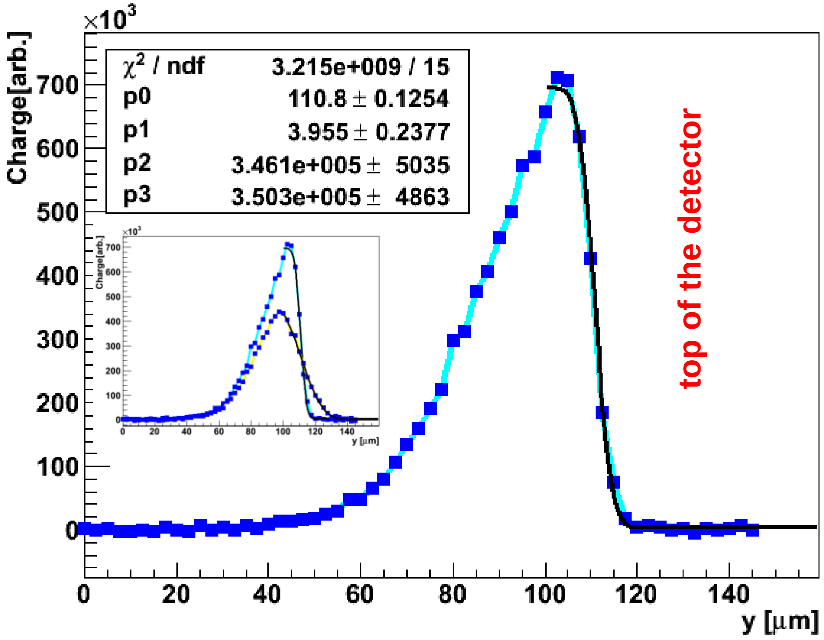


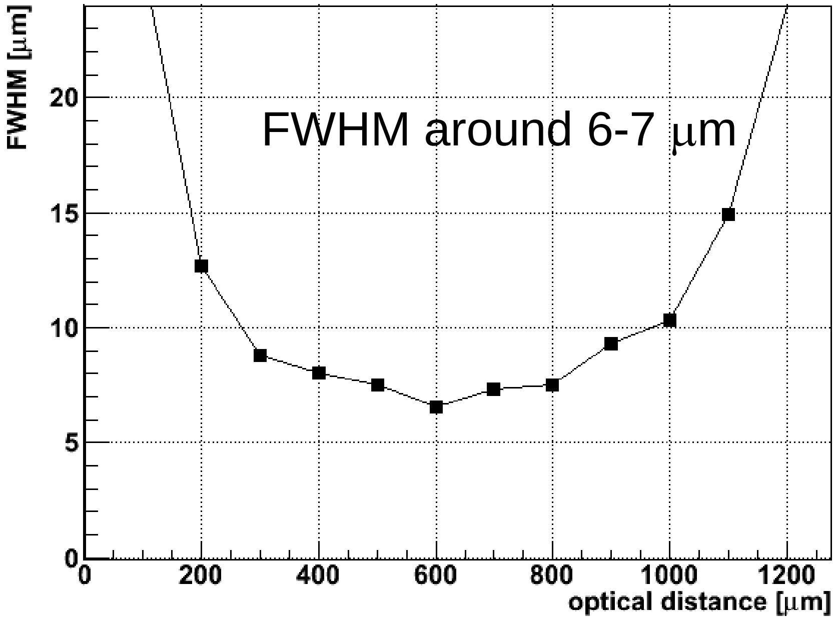


- Particulars Scanning-TCT system used:1060 nm pulse laser, 350 ps, 500 Hz
- The mount has a opening for ^{90}Sr source on top.
- At the moment the chip can not be actively cooled.

Finding the focus

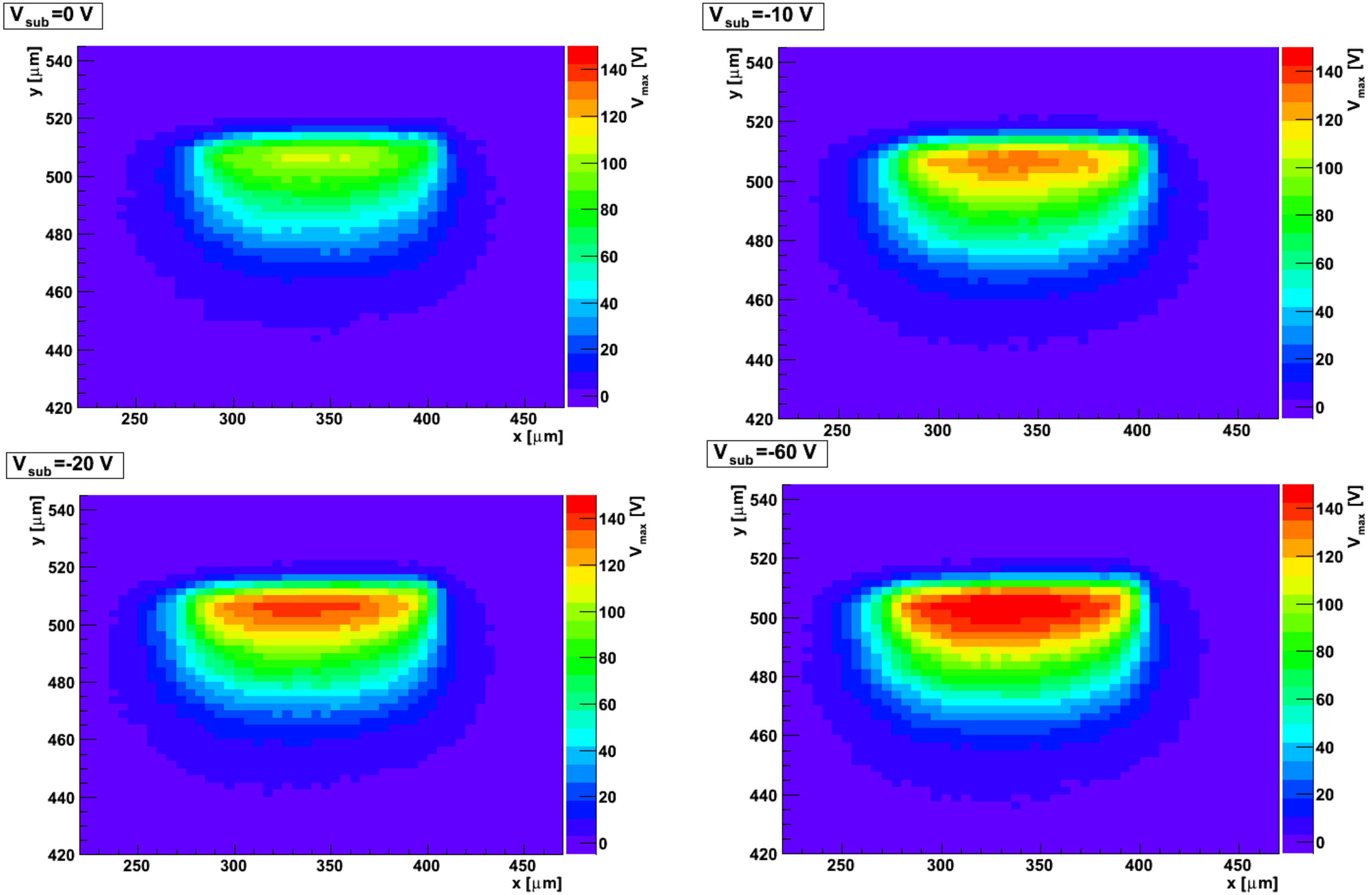
- Scanning takes place in z (optical axis) and y (depth of the sensor) direction with x being fixed in the middle of the sensor
- Error-function fit to the signal at the edge of the detector
- The beam has FWHM of 6-7 μm when it enters the detector from the side
  - probably surface is relatively flat (polishing is not necessary ?)
  - Close proximity of the cell reduces the importance of polishing



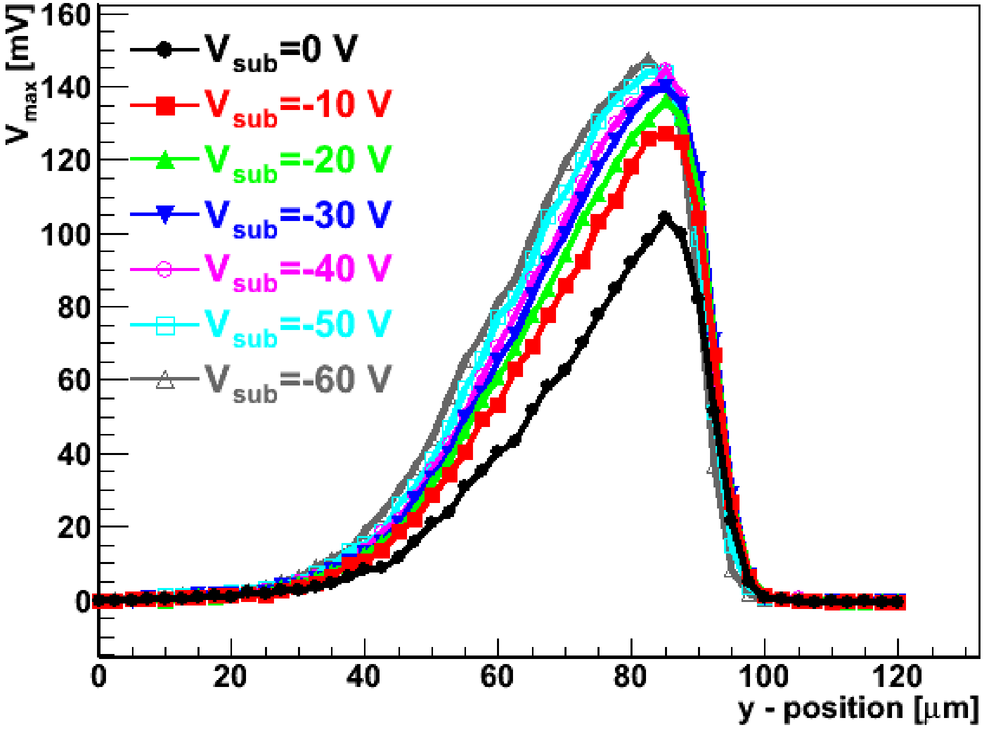


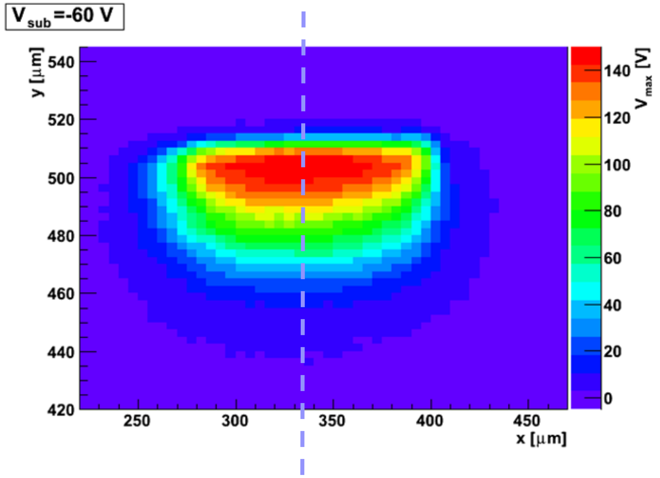
In inset a case of "good" and "bad" focus

XY scan at different bias voltages



Charge collection profile along y-axis



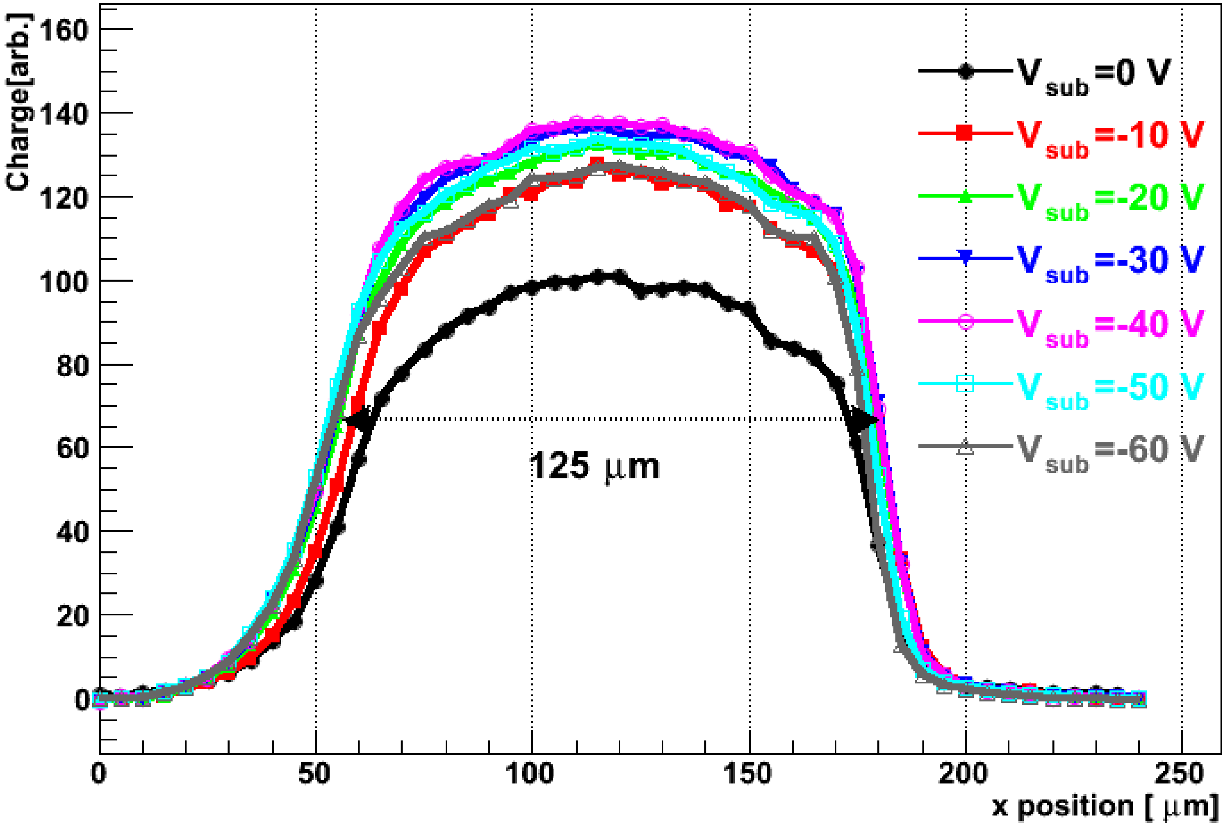


profile taken along that line

- clear dependence of the signal on voltage
- small dependence of charge profile width (collection region) on voltage. Indication that most of the signal comes from diffusion – only a smaller portion of the charge collection region (~30 μm) is depleted.

Charge collection profile along x-axis

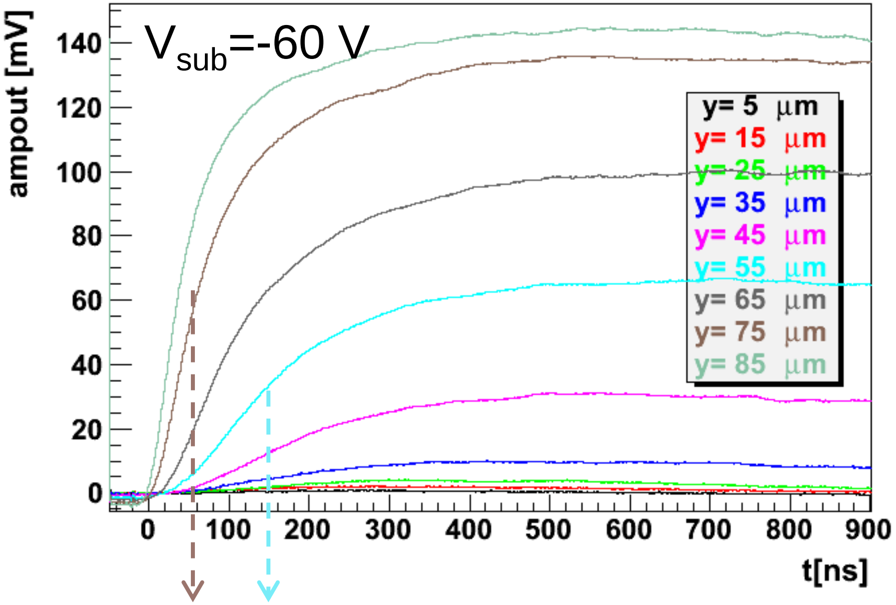
y= *85* µm
(just underneath the surface of the chip)



- The transition at the pixel edge/border is not so sharp. Probably due to the diffusion of charge to the neighboring pixel.
- Very good agreement of the measured pixel width with the designed one.

Depletion depth from amplifier curve

x in the middle of the pixel

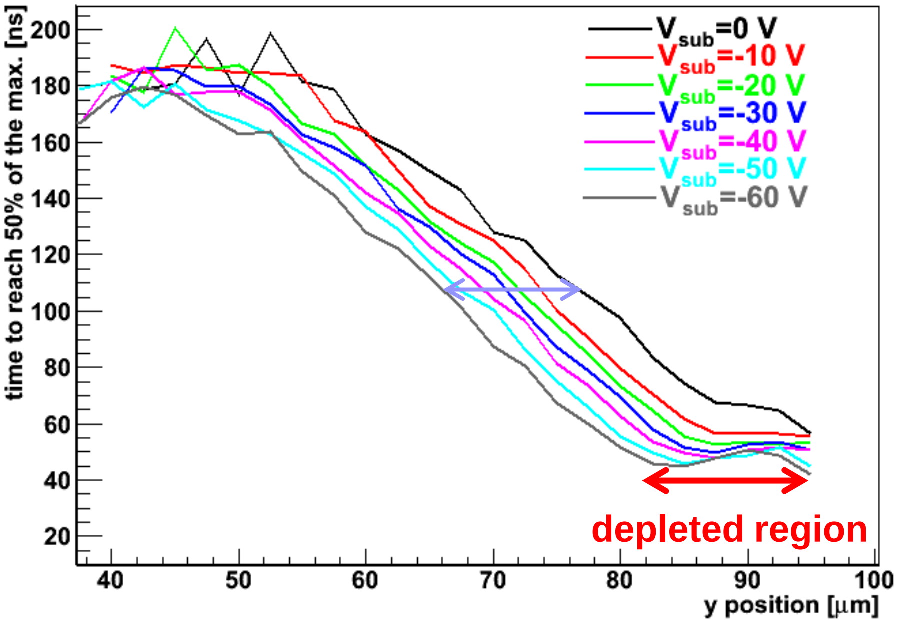


Different times needed to cross 50% of the max charge

Delay needed to cross the "threshold" is mainly due to carriers arriving by diffusion (any contribution from the drift is on this time scale prompt)

Shift in "threshold time" t_{th} with voltage at given y can be used as an indication of the depletion depth.

t_{th} as a function of y position at different voltages

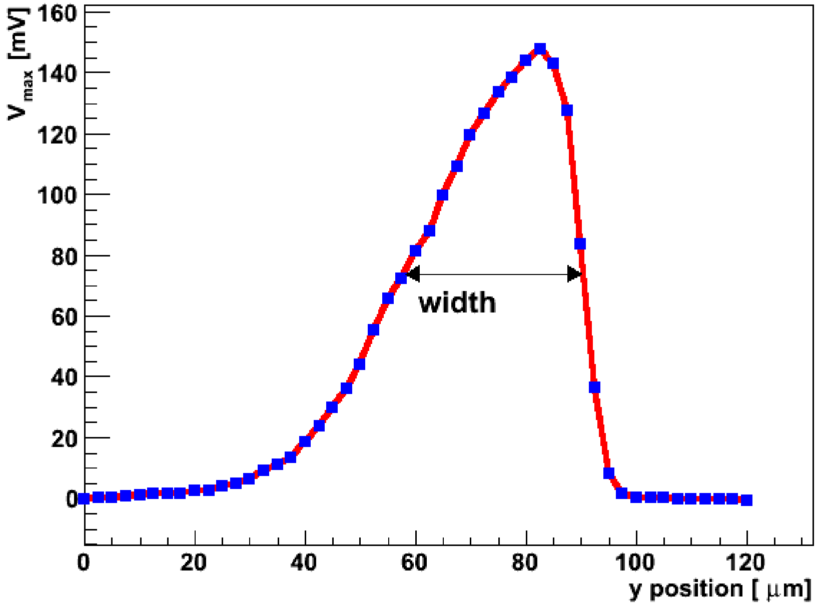


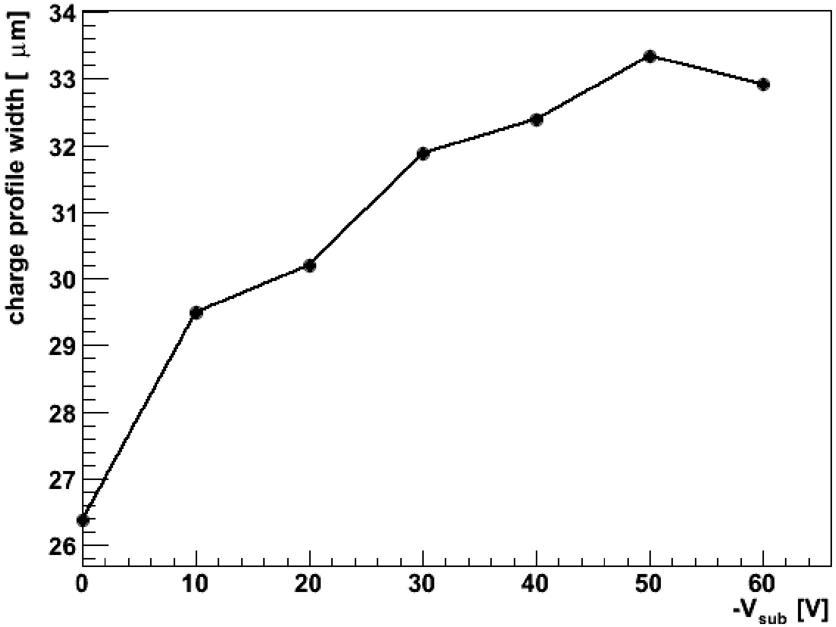
Flat part close to the surface (hockey stick like shape) indicates depleted region:

- at 0 V – hard to estimate – if, only few µm at most
- at 60 V some 10-15 µm

Shift in y-position for the required t_{th} is related to change in the depleted region – less distance for carriers to cross by diffusion. 60 V amounts to around 10 µm of depleted region (blue arrow)

Depletion depth from charge profile





The width of the charge profile increases moderately with voltage. It can be attributed to the growth of depleted region. The increase of the width is around *d*~7 μm. Roughly agrees with depletion region estimated from the amplifier curve.
Estimation of the effective doping concentration (just to get an estimate):

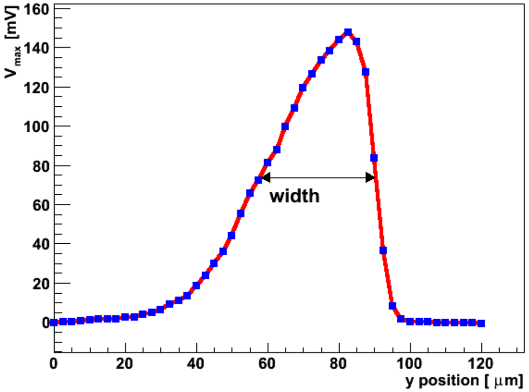
$$N_{eff} = \frac{2\varepsilon\varepsilon_0 V_{sub}}{e_0 d^2} \sim 10^{15}\ \mathrm{cm}^3$$

Estimated substrate resistivity from the measured values with both methods is around 20 Ωcm and agrees with resistivity of the substrate used.

Expected charge for fast readout

- Assuming that charge collection time is limited to 25 ns, the main contribution must come from the drift. How much of the measured charge can we expect?
- Integration of the charge collection y-profile gives the charge proportional to the charge collected by a m.i.p. like particle

$$Q_{mip} \propto \langle Q \rangle = \int_0^W Q(y)\,dy$$



- around 1/3 of the signal comes from drift region (drift region only from y=80 µm to 95 µm only) at 60V.
- Roughly in agreement measurement at 0 V,

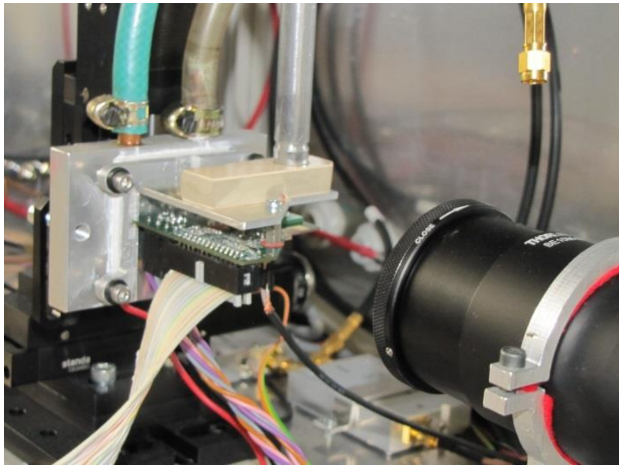
where the drift region is negligible

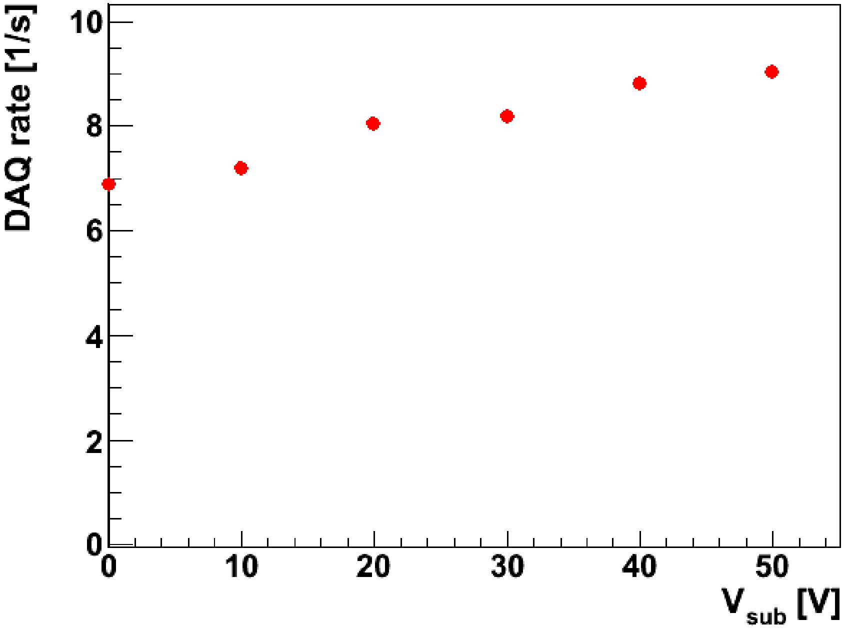
$$\frac{\int_{y=80\,\mu m}^{y=95\,\mu m} Q(y)\,dy}{\int_{y=0\,\mu m}^{y=95\,\mu m} Q(y)\,dy} = 0.35$$

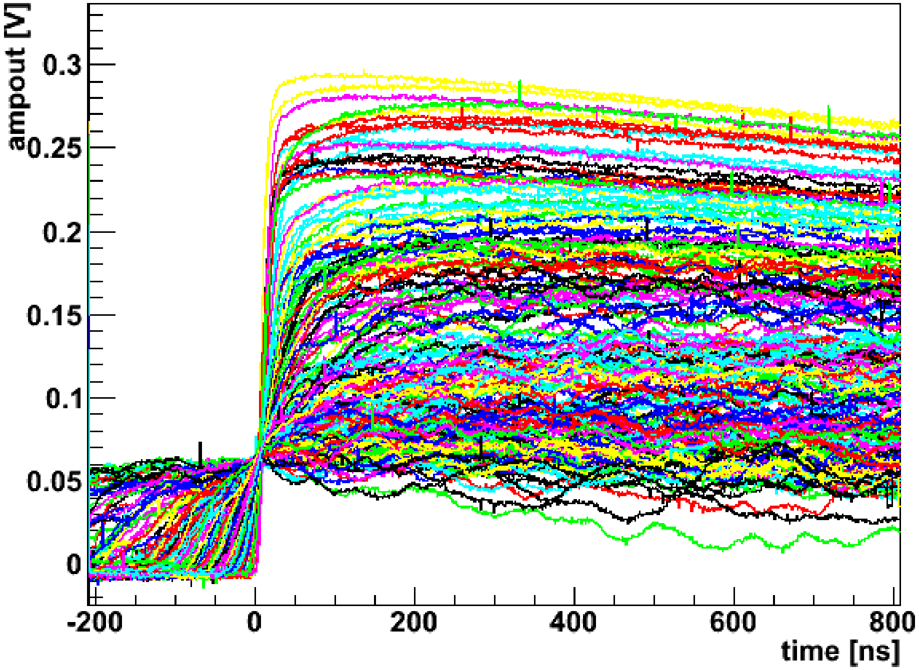
$$1 - \frac{\int_{y=0\,\mu m}^{y=95\,\mu m} Q(y,0V)\,dy}{\int_{y=0\,\mu m}^{y=95\,\mu m} Q(y,60V)\,dy} = 0.38$$

^{90}Sr Measurements (I)

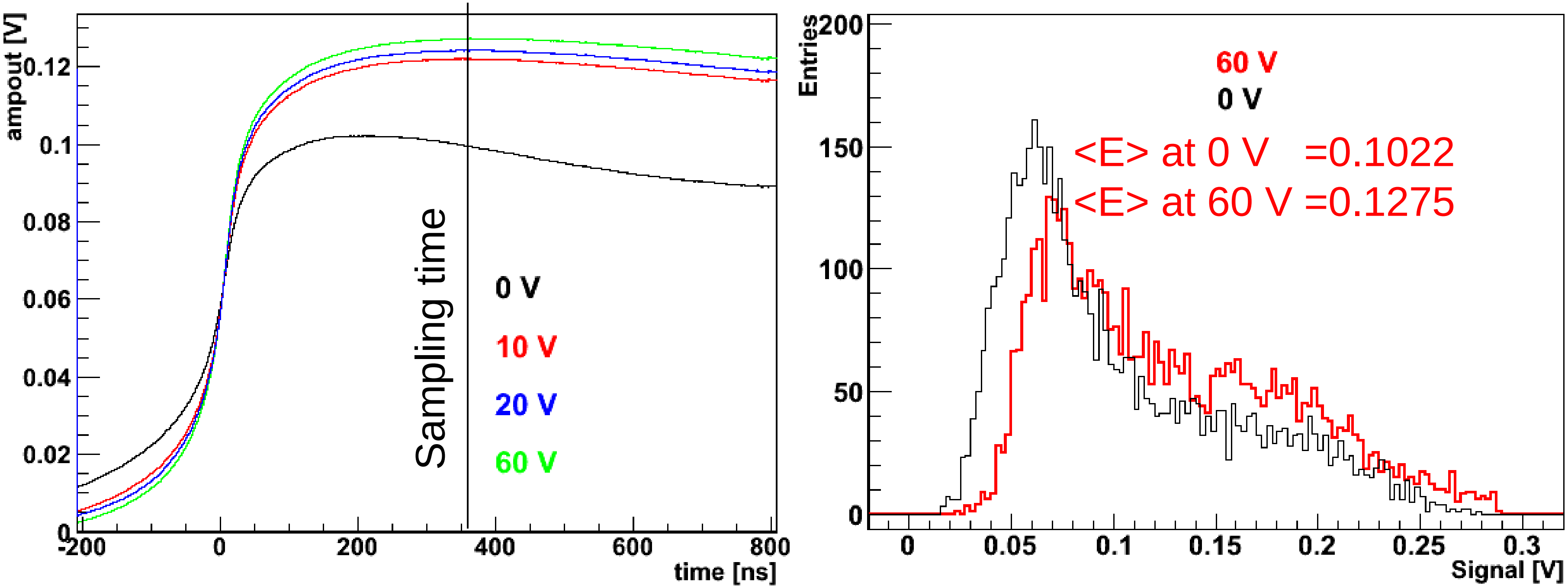
- 5000 triggers taken at each voltge
- Self-triggering (not mip!) with 50 mV trigger
- DAQ rate depends on bias – it rises for above 30% from 0 to 60 V
- Triggered pulses differ a lot – complex spectrum of ^{90}Sr electrons







^{90}Sr Measurements (II)



- Average response from the amplifier shows weak dependence on voltage
- Acquired spectrum differ at 0 and 60 V in average depostited energy for around 20% - in accordance with expectations
- No significant difference in amplifier speed response – unlike E-TCT the cahrges are generated all along the depth and not at given depth

Conclusions

- Edge-TCT was performed on HVCMOS2FEI4 structure using a cell amplifier output after initial amplifying stage
  - ☐ Most of the signal comes from diffusing carriers – the depth of the region is around 20-30 μm
  - ☐ Depleted region was investigated by two methods with roughly consistent results (~30% of the signal comes from the depleted region only at 60 V)
    - Growth of charge profile width (y-depth direction) with bias votlage
    - time response speed of the amplifier at different generation depths as a function of bias voltage
    - The calculated N_{eff}~2e15 cm^{-2} agrees very well with the nominal one – confirming the validity of the methods.
  - ☐ Only around 35% would be collected in 25 ns
- ^{90}Sr signals show compatible results
  - ☐ Weak dependence of collected charge on substrate voltage (20% between 0 and 60 V)
  - ☐ Increase of rate as a function of voltage