Evaluation of the Low Resistance Strip Sensors (Low-R) Fabricated at CNM

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Outline

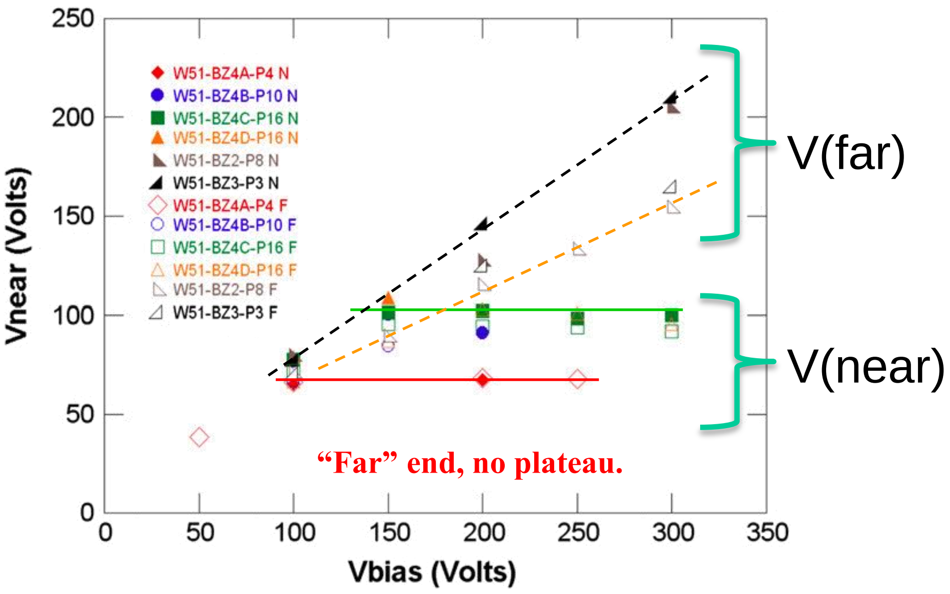
- Motivation
- Proposed solution
- Design
- First batch
- Second batch tests
- Alternative technological solutions
- Conclusions

Motivation

- ➢ In the scenario of a **beam loss** there is a **large charge deposition** in the sensor bulk and **coupling capacitors can get damaged**
- ➢ Punch-Through Protection (PTP) structures used at strip end to develop low impedance to the bias line and evacuate the charge

But…

- ➢ Measurements with a large charge injected by a laser pulse showed that the strips can still be damaged
  - The **implant resistance** effectively **isolates** the “far” end of the strip from the PTP structure leading to the large voltages

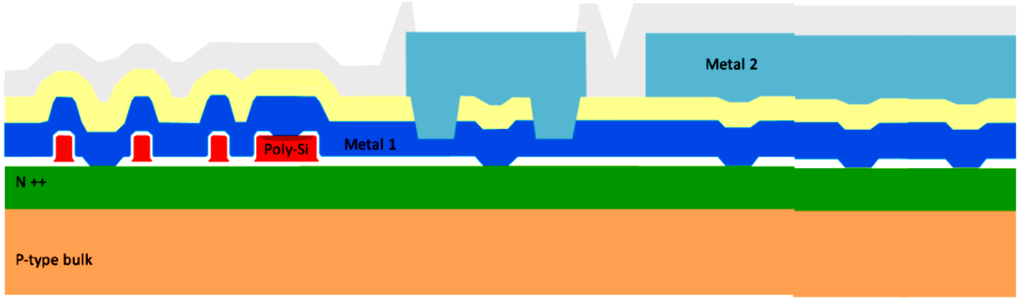


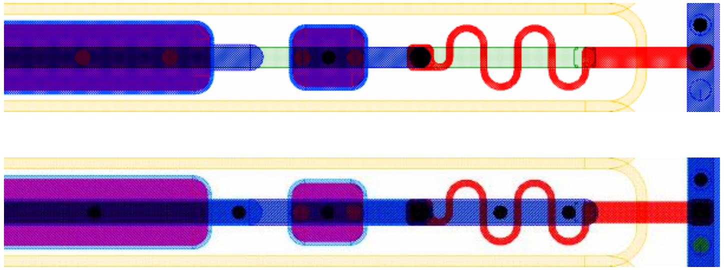
“Far” end, no plateau.

H. F.-W. Sadrozinski, et al. “Punch-through protection of SSDs in beam accidents” NIMA 658, Issue 1, pp. 46-50, 2011.

Proposed solution

- To reduce the resistance of the strips: “**Low-R strip sensors**”
- Deposition of Aluminum on top of the implant:
  $R_{\square}(Al) \sim 0.04\ \Omega/\square \Rightarrow 20\ \Omega/cm$ (Drastic reduction of strip resistance!)
- Metal layer deposition on top of the implant (first metal) before the coupling capacitance is defined (second metal).
  - Double-metal processing to form the coupling capacitor
  - A layer of high-quality dielectric is needed between metals for the coupling cap.
    - ☞ **Deposited** on top of the first Aluminum (not grown)
    - ☞ **Low temperature processing** needed not to degrade Al: T < 400 ºC
      - – **Plasma Enhanced CVD (PECVD)** process at 300-400 ºC
    - ☞ **Triple-layer** (oxide (1000 Å) + Si_3N_4 (1000 Å) + oxide (1000 Å)): to avoid pinholes → Yield

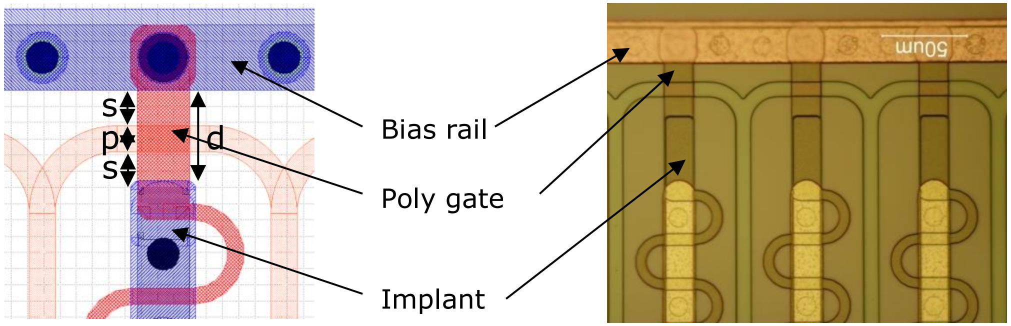




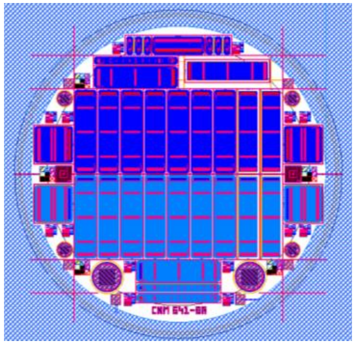
Design

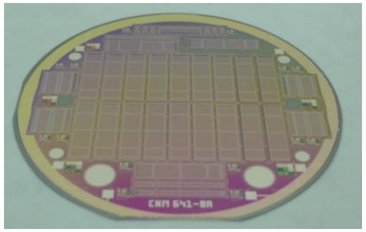
- PTP design:
  - Design of experiments (DOE): varying p, s $\Rightarrow$ d

DOE		N–P separation ‘s’ [um]		
		12	8	6
P-stop width ‘p’ [um]	8	32	24	20
	6	30	22	18
	4	28	20	16
		Total PTP distance ‘d’		



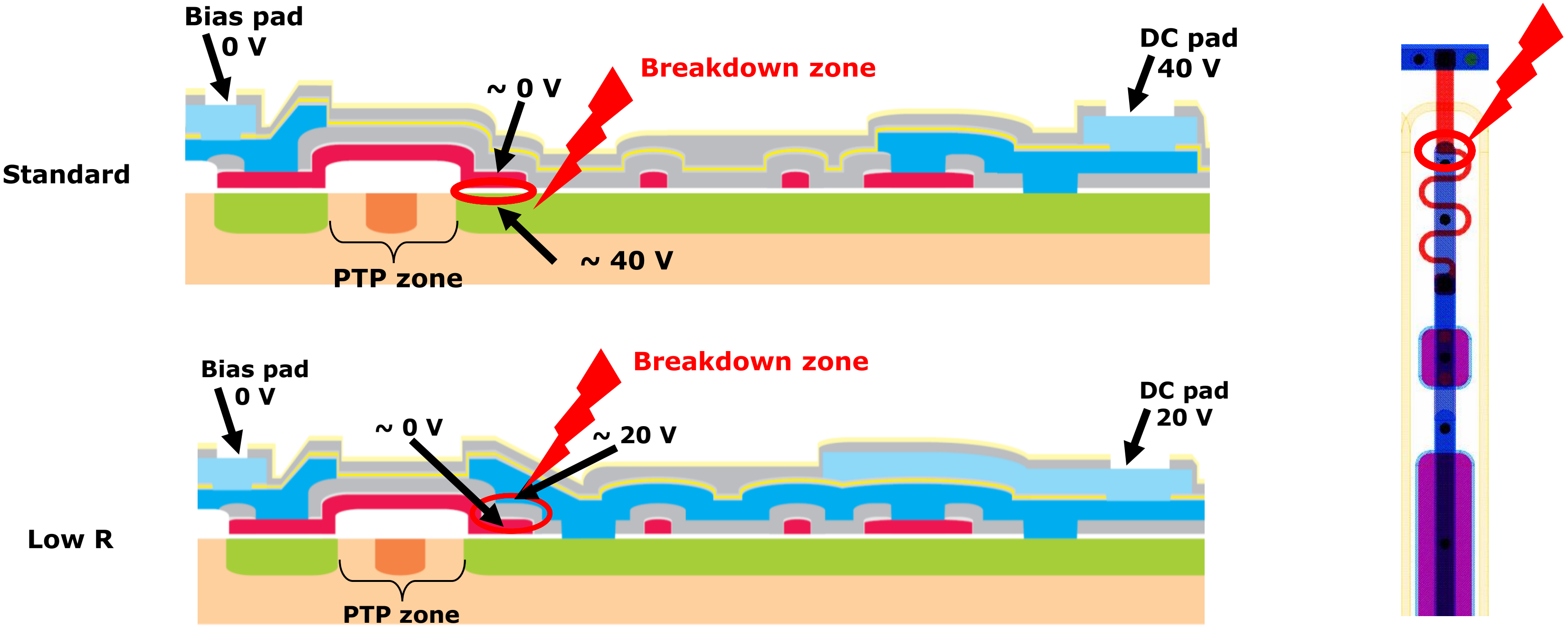
- Wafer design:
  - 10 ATLAS-barrel-like sensors: “LowR sensors”
    - 64 channels, ~2.3 mm long strips
    - First metal connected to the strip implant to reduce R_{strip}
    - Each sensor with a different PTP geometry (with polysilicon bridge)
  - 10 extra standard sensors for reference (no metal in implant). Identical design to the LowR but without metal strip on top of the implant





First batch

- PTP tests showed unexpected behavior:
  - Irreversible breakdown
  - Breakdown voltage independent of PTP structure geometry
  - at ~40 V in standard sensors and at ~20 V in LowR sensors
  - Oxide breakdown at a different place in the strip occurs before PTP is activated.
    - Thin oxides overlooked during fabrication
    - Only critical when PTP structures are present and tested



Second batch

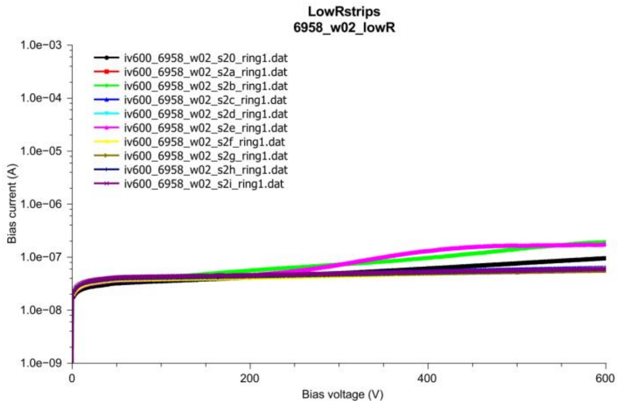
- New batch processed correcting these problems:
  1) Thicker thermal oxide between implant and polysilicon Rbias to avoid breakdown in standard sensors ➔ Thicker coupling capacitor in standard sensors (~1000 A)
  2) Thicker oxide deposited between polysilicon Rbias and Metal1 in LowR sensors to avoid breakdown in LowR sensors
  3) In some extra sensors new metal mask (METAL-B) with no metal on top of polysilicon Rbias area to avoid the possibility of breakdown in that area
  4) Some wafers have a reduced p-stop doping to make sure we have PTP

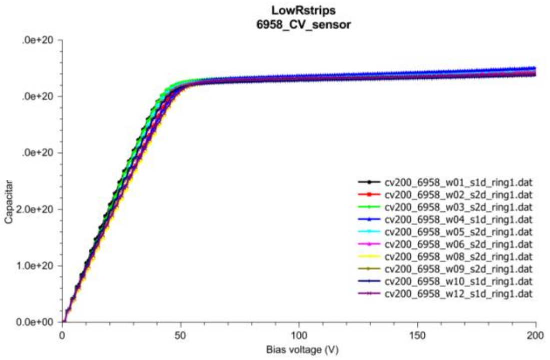
- Design of Experiments:

	P-stop implant dose	
WAFERS	4.00E+13	1.00E+13
• Metal1 over poly-R_{bias} • Extra isolation layer (1500 A) between poly and metal • Coupling capacitance triple-layer: 1000/1000/1000 A	**1-6**	7,8
• No Metal1 over poly-R_{bias} • No extra isolation layer between poly and metal • Coupling capacitance triple-layer: 700/700/700 A	9,10	11-12

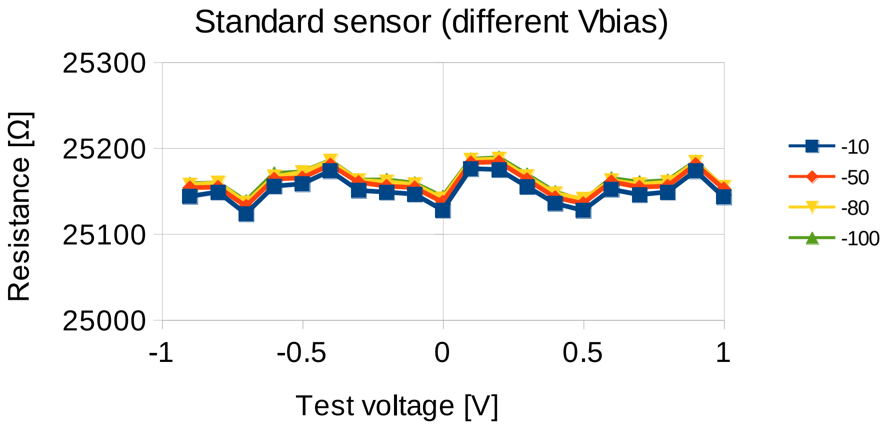
General performance

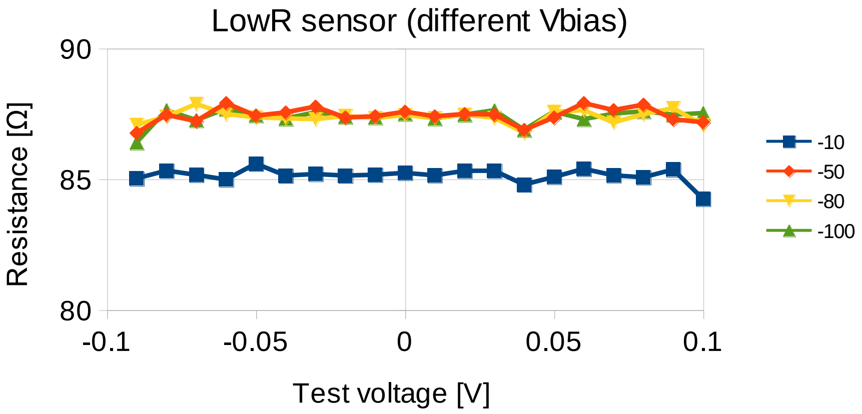
- IV, CV
  - ➢ Normal behaviour
  - ➢ V_{FD} ~ 70 V
  - ➢ Higher leakage currents after cut (under study)





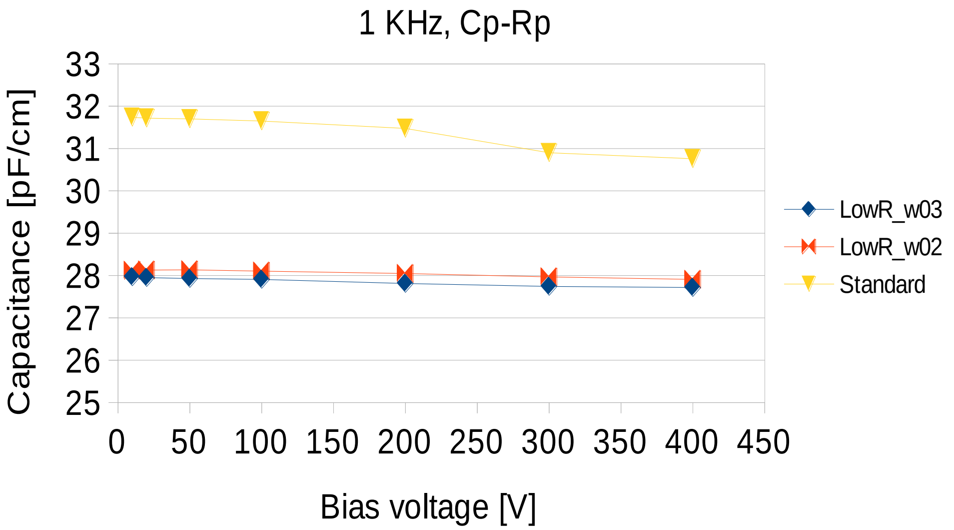
- Strip resistance
  - ➢ ~3 orders of magnitude reduction



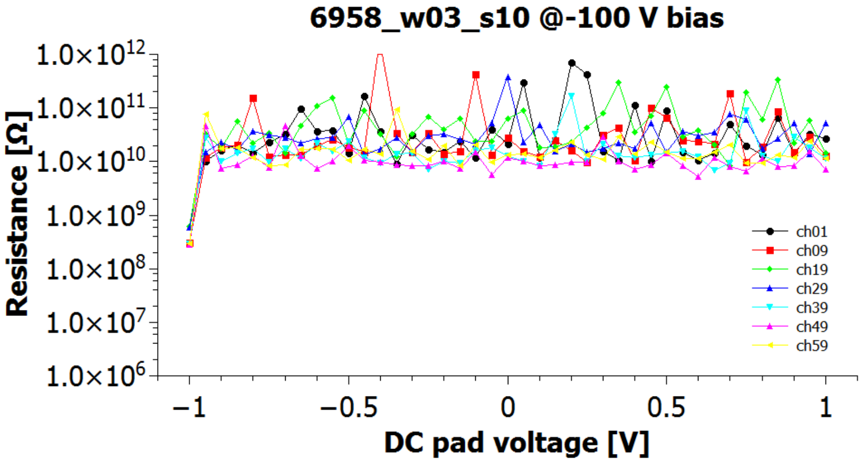


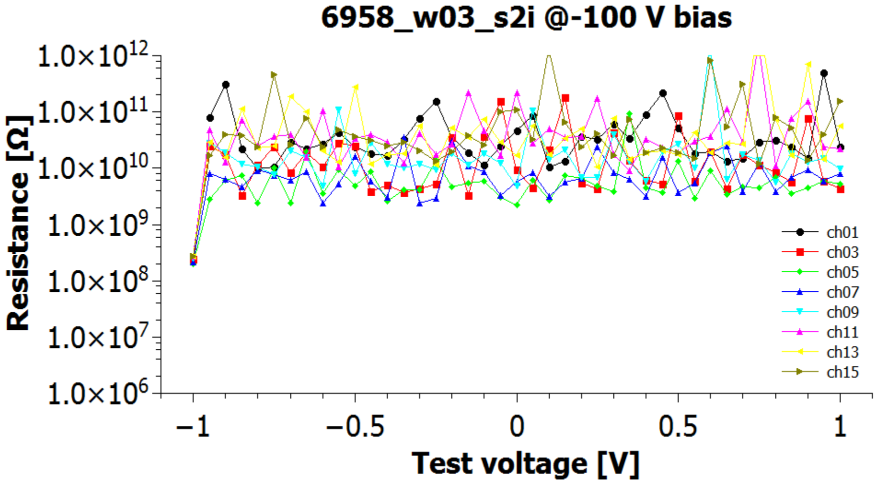
General performance

- Coupling capacitance
  - Standard sensors: 31 ± 2 pF/cm
  - LowR sensors: 28 ± 1 pF/cm
  - ATLAS12 specs: > 20 pF/cm.



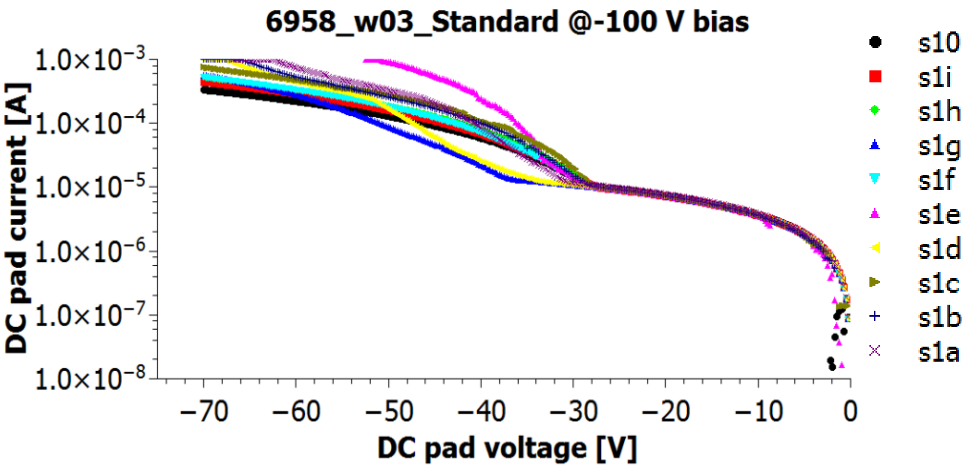
- Interstrip Resistance
  - Interstrip resistance > 1 GΩ



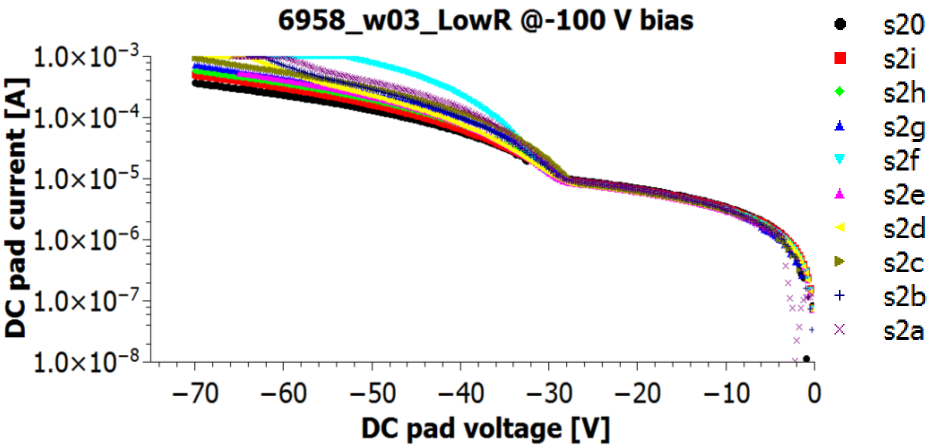


PTP structure tests

- IV sweeps
  - Reversible breakdown (=> PT)
  - PTP voltage ~ 30 V
  - No evident correlation between PTP distance and PTP voltage

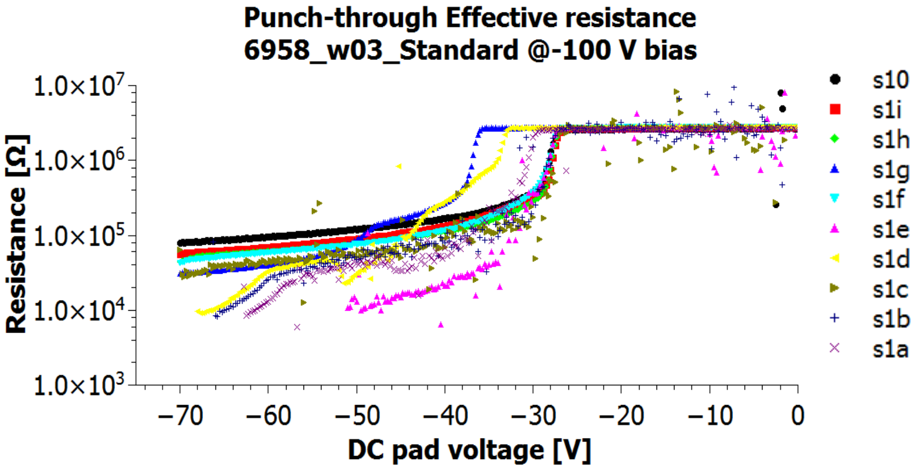


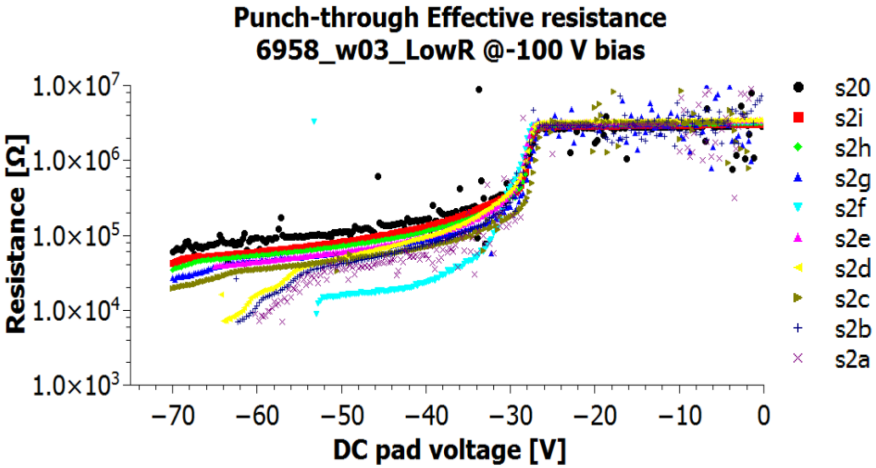
1m_d16_p04_s06 (s1a)	2m_d16_p04_s06 (s2a)
1m_d18_p06_s06 (s1b)	2m_d18_p06_s06 (s2b)
1m_d20_p04_s08 (s1c)	2m_d20_p04_s08 (s2c)
1m_d20_p08_s06 (s1d)	2m_d20_p08_s06 (s2d)
1m_d22_p06_s08 (s1e)	2m_d22_p06_s08 (s2e)
1m_d24_p08_s08 (s1f)	2m_d24_p08_s08 (s2f)
1m_d28_p04_s12 (s1g)	2m_d28_p04_s12 (s2g)
1m_d30_p06_s12 (s1h)	2m_d30_p06_s12 (s2h)
1m_d32_p08_s12 (s1i)	2m_d32_p08_s12 (s2i)
1m_d70_p08_s31 (s10)	2m_d70_p08_s31 (s20)



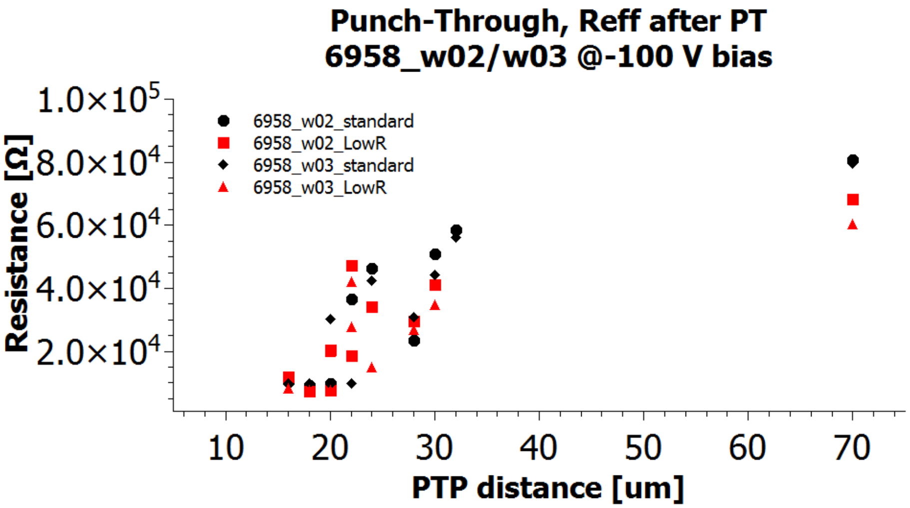
PTP structure tests

- PT effective resistance


Punch-through Effective resistance
6958_w03_Standard @-100 V bias

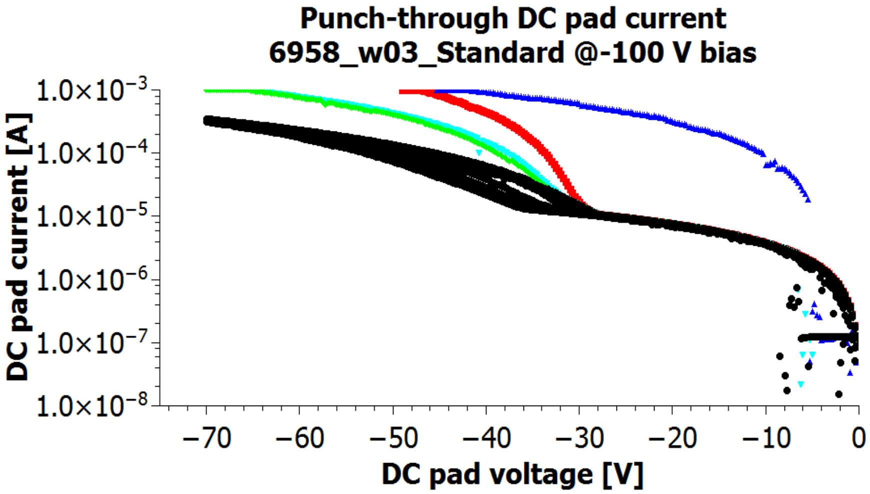

Punch-through Effective resistance
6958_w03_LowR @-100 V bias

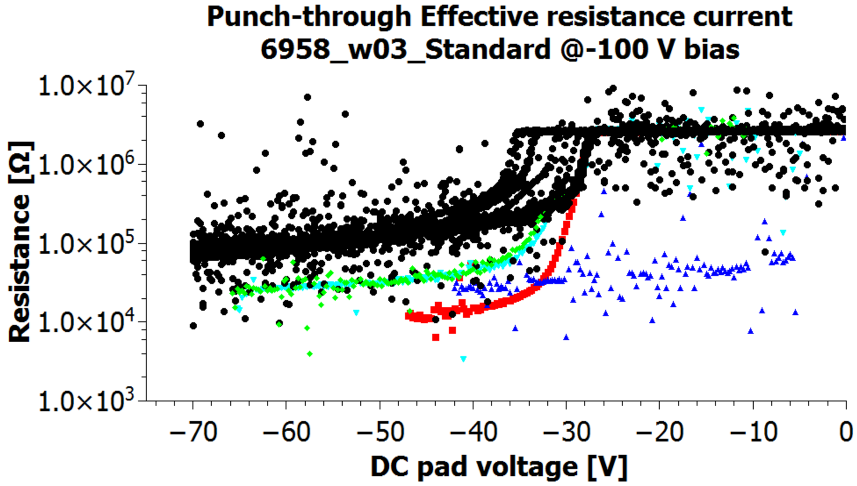
- There seems to be a correlation between final effective resistance and PTP distance, although not evident within the same wafer


Punch-Through, Reff after PT
6958_w02/w03 @-100 V bias

PTP structure tests

- Channel-to-channel
  - Punch-Through activation voltage (Vpt) is not stable among channels, geometry dependence seems to be low.
  - Final effective resistance value is stable among channels.

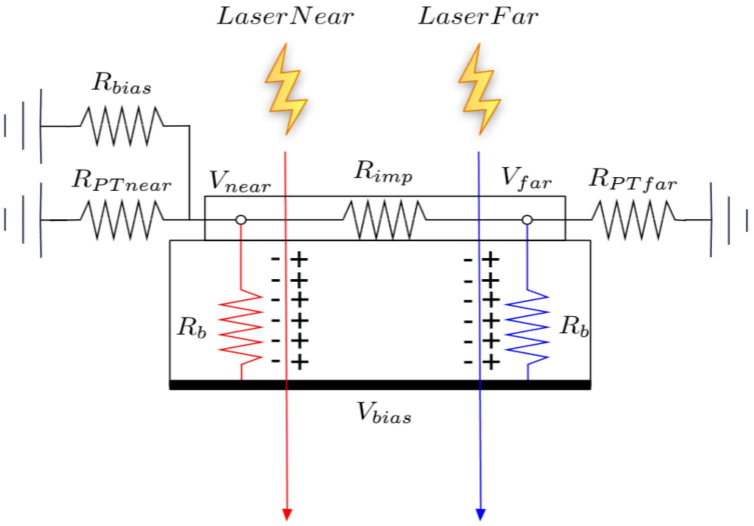

Punch-through DC pad current
6958_w03_Standard @-100 V bias


Punch-through Effective resistance current
6958_w03_Standard @-100 V bias

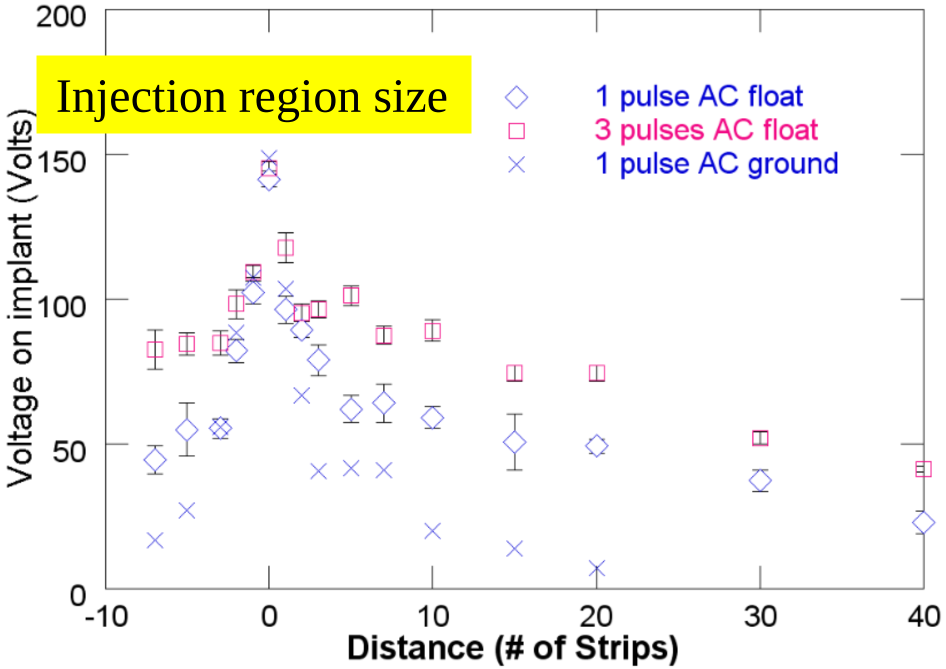
Laser tests

- We use Alessi LY-1 “cutting” IR laser (1064 nm) to inject a large amount of charge locally in the sensor.
- The total amount of charge is about 3x10^7 MIPS, spread over few mm.
- We inject the laser at either near and far locations to assess the sensor vulnerability to large charges, since PTP(near) is superior to PTP(far).

Injection scheme

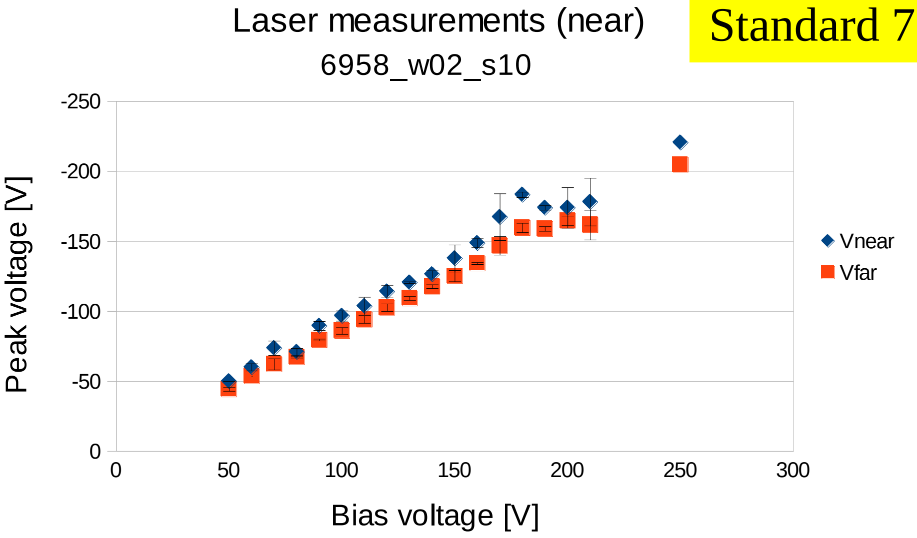


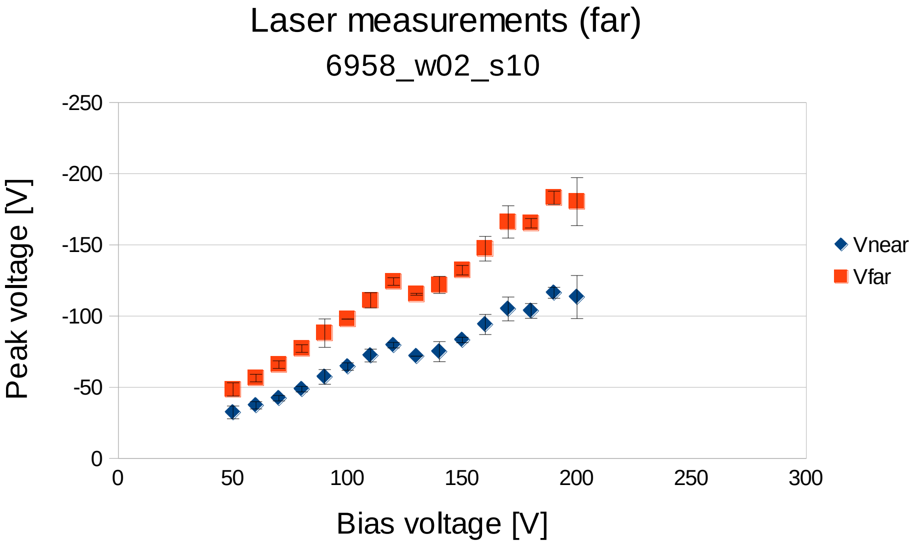
Injection region size



Laser scan results

Standard 70 um PTP

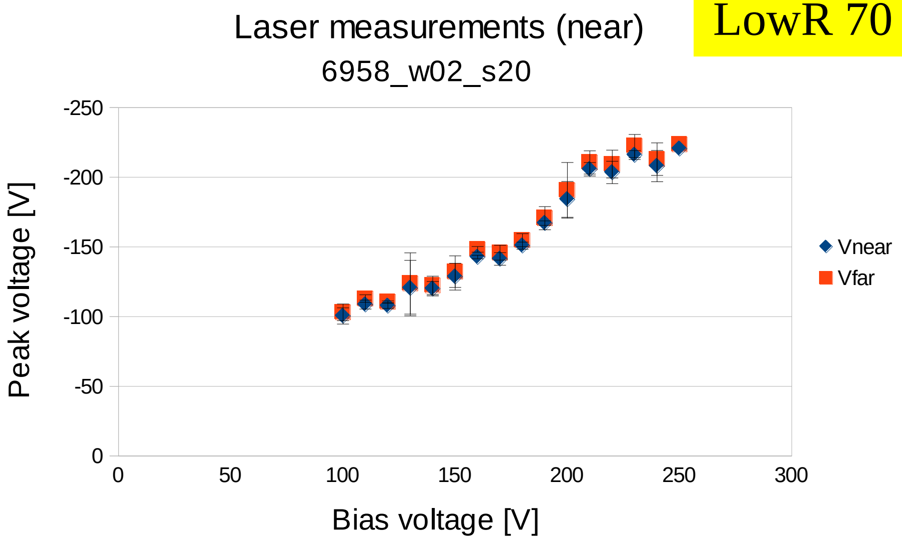


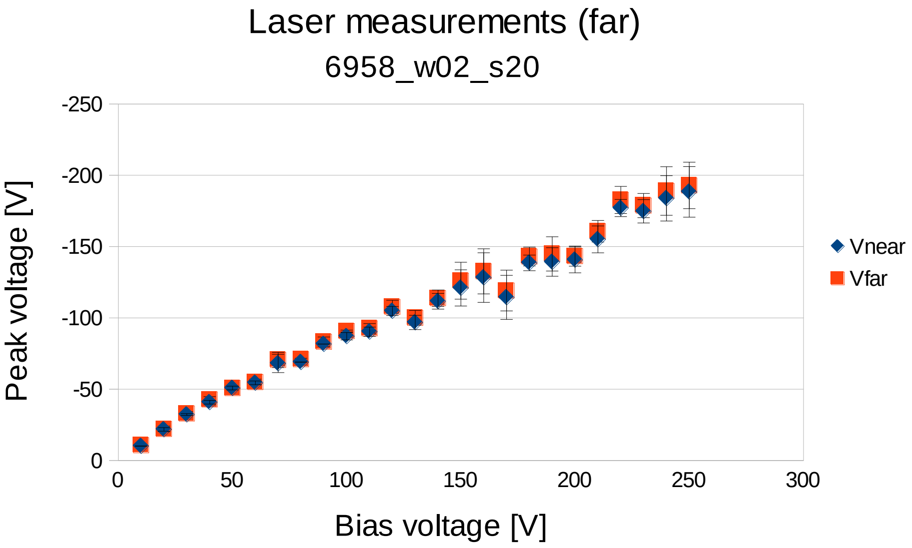


- When laser is injected next to the near DC pad, peak values on Vfar are similar to the ones on Vnear.
- As seen before, **when laser is injected next to the far DC pad, peak values on Vfar are higher than on Vnear**.
- **No plateau** up to ~180 V.
- Strange “bump” at 140 V bias.
- At 250 V, sensor current value jumps.

Laser scan results

LowR 70 um PTP


Laser measurements (near)
6958_w02_s20

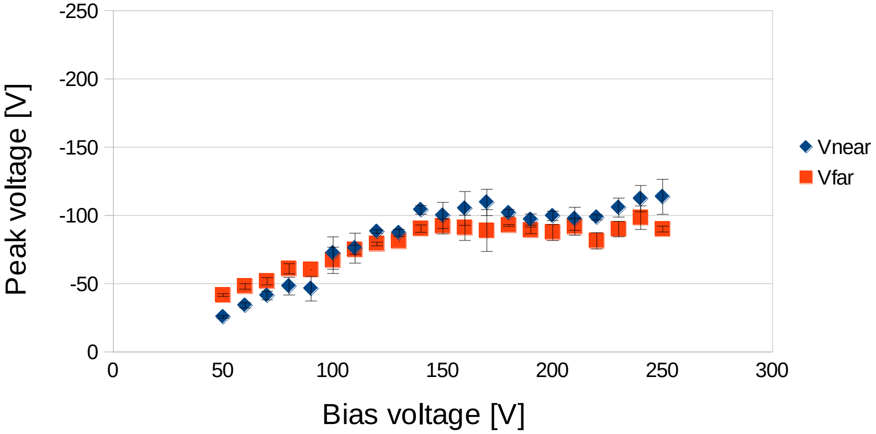

Laser measurements (far)
6958_w02_s20

- **For LowR sensors, Vfar and Vnear peak values are similar**.
- Peak voltages on both near and far ends tend to stabilize at ~180 V bias. **But no evident plateau is observed**.
- Sensor leakage current jumped at 250 V

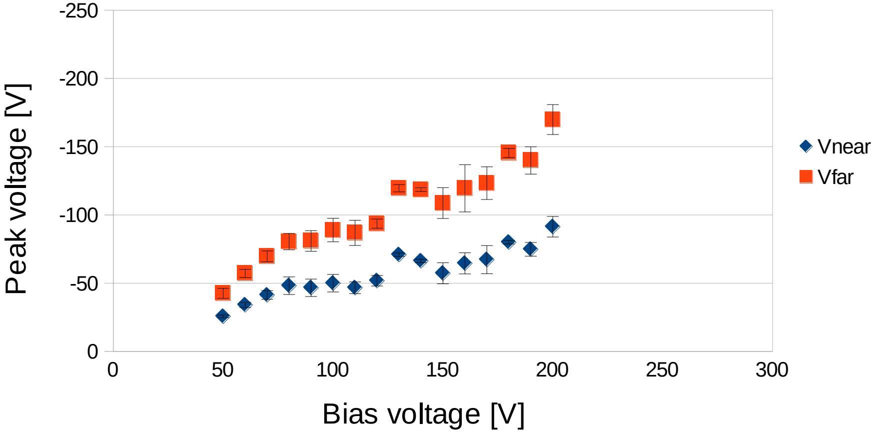
Laser scan results

Standard 20 um PTP

Laser measurements (near)
6958_w02_s1d



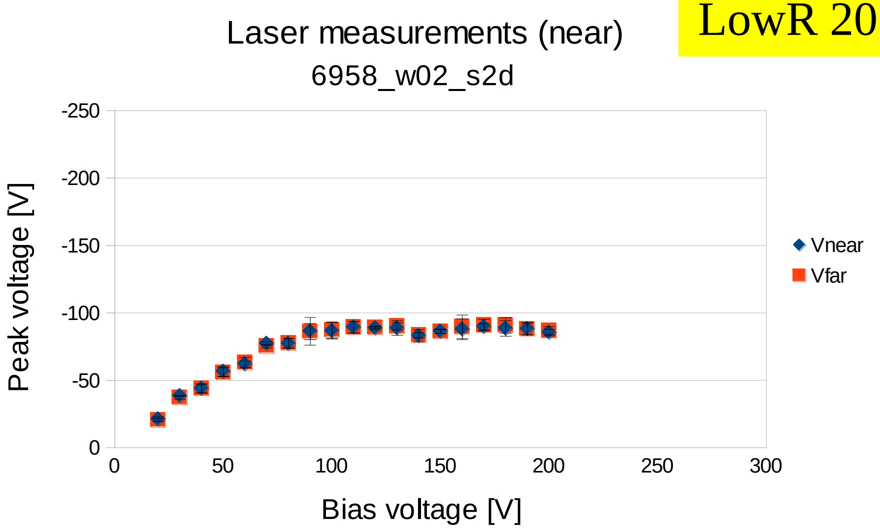
Laser measurements (far)
6958_w02_s1d

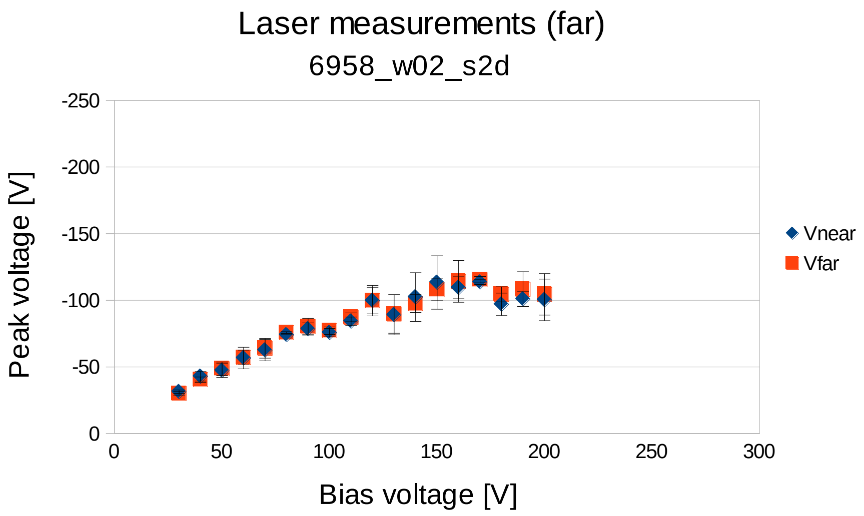


- **When laser is injected on near side, plateu is observed after 150 V bias.**
- No difference is observed between Vnear and Vfar when laser is injected in the near side.
- **No plateau observed in Vfar after charge injection on far side**
- Peak voltages are similar to previous results on HPK sensors with p-stop isolation.
- Sensor bias current jumped one order of magnitude when sensor bias reached 200 V.

Laser scan results

LowR 20 um PTP





- ✓ **Vfar = Vnear**
- ✓ **A plateau is observed for both near and far laser injections on Vfar and on Vnear**.
- ✓ When laser is fired on the near side, plateu is seen after 100 V bias. For the far side case, plateau is observed after 120 V.

Alternative technological solutions

- Other methods to obtain LowR sensors being studied:
  - $TiSi_2$: allows the use of high temperature steps after the oxide deposition

    → oxide densification → higher yield
  - Highly doped polysilicon: allows the growth of thermal oxide after it

    → high quality oxide

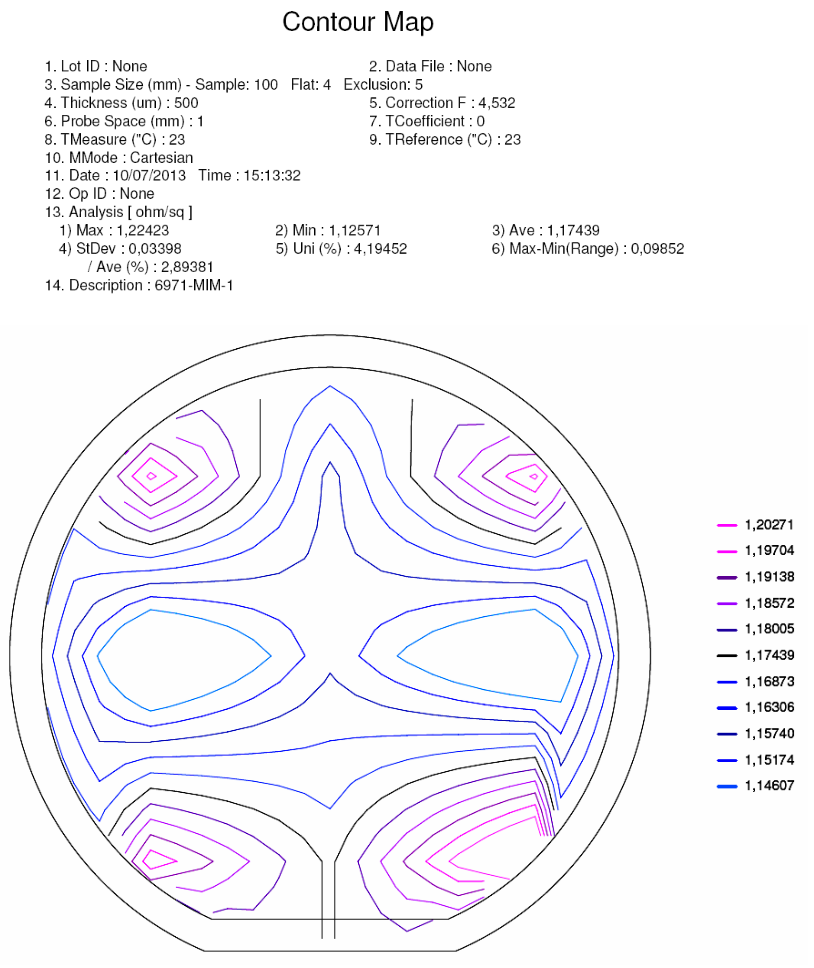
    → back to “standard” process

	sheet R (Ohm/#)	kOhm/cm	strip R (kOhm)
Implant	22	11	25.3
Metal	0.04	0.02	0.05
Metal-B			0.946
TiSi2	1.2	0.6	1.38
Poly	3	1.5	3.45

- A small batch of sensors currently being fabricated at CNM

Titanium Silicide ($TiSi_2$)

- $TiSi_2$ processing technology at CNM
  - Good formation of $TiSi_2$ layer
  - Low sheet resistance: ~1.2 Ω/□
  - Densification at 900 ºC , 30 min
  - Self aligned process (→ No mask)
- $TiSi_2$ MiM capacitors fabricated
  - 98-100 % yield up to 100 V
    (not enough statistics: 1-2 cap failing out of 62 measured)

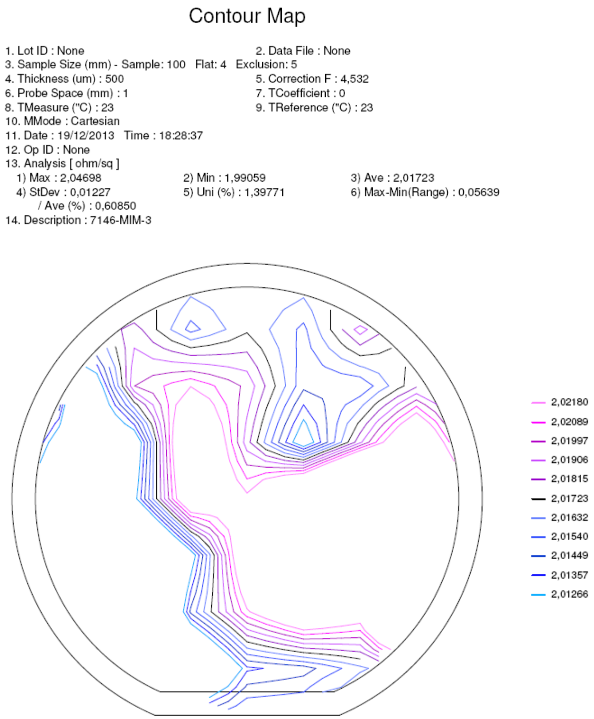


Contour Map

1. Lot ID : None 2. Data File : None
3. Sample Size (mm) - Sample: 100 Flat: 4 Exclusion: 5
4. Thickness (um) : 500 5. Correction F : 4,532
6. Probe Space (mm) : 1 7. TCoefficient : 0
8. TMeasure ("C) : 23 9. TReference ("C) : 23
10. MMode : Cartesian
11. Date : 10/07/2013 Time : 15:13:32
12. Op ID : None
13. Analysis [ohm/sq]
1) Max : 1,22423 2) Min : 1,12571 3) Ave : 1,17439
4) StDev : 0,03398 5) Uni (%) : 4,19452 6) Max-Min(Range) : 0,09852
/ Ave (%) : 2,89381
14. Description : 6971-MIM-1

Highly doped Poly-Si

- Polysilicon layer doped with liquid source ($POCl_3$, “Phosphoryl chloride”) in contact with the silicon implant (substitutes the metal layer)
  - ➢ High doping levels reached at high temperatures (1050ºC) and long times
- Possibility to grow a thermal oxide on top of the polysilicon layer to form the coupling capacitor
  - ➢ Much higher quality oxide
  - ➢ Although risk of lower breakdown voltages
  - ➢ Higher thermal load of the process
  - ➢ Risk of dopant precipitates later in the process
- MIM capacitors
  - ➢ Good conductance (~2-3 Ohm/sq)
  - ▪ 98-100 % yield up to 20 V
  - ▪ Breakdown @ 40-50 V (2000 A ox. thickness)



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                         Contour Map

1. Lot ID : None                              2. Data File : None
3. Sample Size (mm) - Sample: 100   Flat: 4   Exclusion: 5
4. Thickness (um) : 500                       5. Correction F : 4,532
6. Probe Space (mm) : 1                       7. TCoefficient : 0
8. TMeasure ("C) : 23                         9. TReference ("C) : 23
10. MMode : Cartesian
11. Date : 19/12/2013   Time : 18:28:37
12. Op ID : None
13. Analysis [ ohm/sq ]
  1) Max : 2,04698            2) Min : 1,99059              3) Ave : 2,01723
  4) StDev : 0,01227          5) Uni (%) : 1,39771          6) Max-Min(Range) : 0,05639
      / Ave (%) : 0,60850
14. Description : 7146-MIM-3
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Conclusions & future work

- ✓ Low-resistance strip sensors (LowR) proposed to extend the protection afforded by PTP structure to the entire active area of the sensor
- ✓ Implementation with Aluminum layer in contact with the implant to drastically reduce strip resistance
  - ▪ LowR sensors show similar general characteristics as standard sensors
  - ▪ PTP behaviour varies for different structures (problems of first batch solved), although still some features to be fully understood.
  - ▪ Laser tests show an effective reduction of the implant voltage at both near and far sides of the strip, and for charge injection at either strip side.
- ✓ New possible implementations being tried with $TiSi_2$ and polysilicon to assure a better coupling capacitor formation, and a more standard processing
- ➢ Future work
  - ○ Irradiations
  - ○ Test new devices with $TiSi_2$ and highly doped Poly-Si

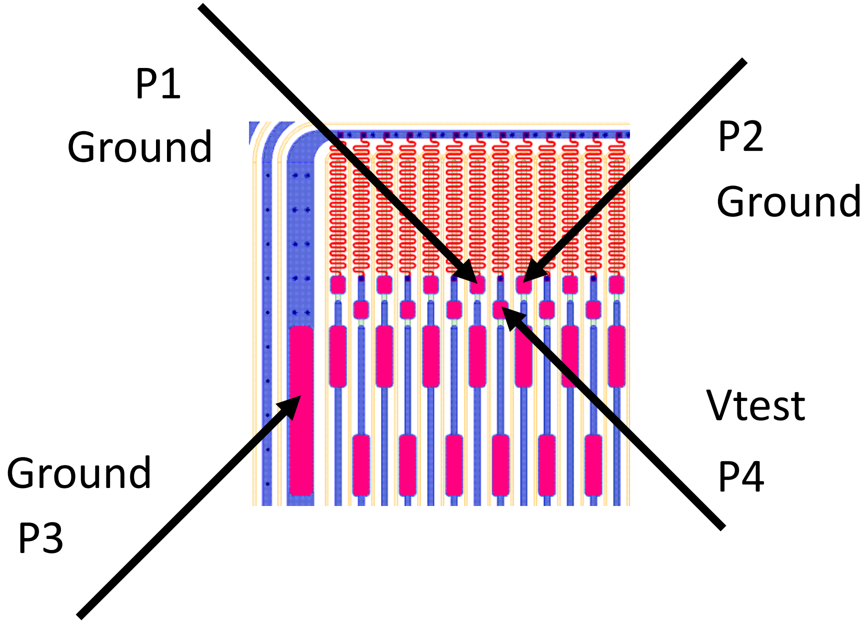
Thank you

Extra slides

Interstrip resistance measurement

HP4156

Voltage sweep: -1 V to 1 V (P4)
Voltage step: 0.05 V
Bias voltage: -100 V (chuck)

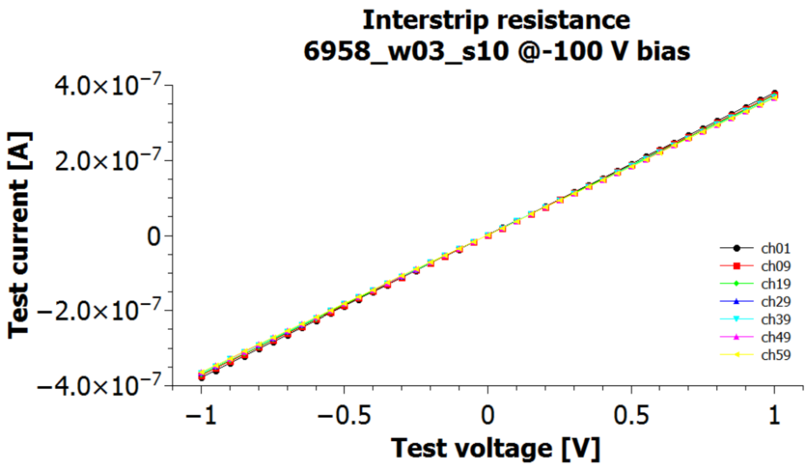


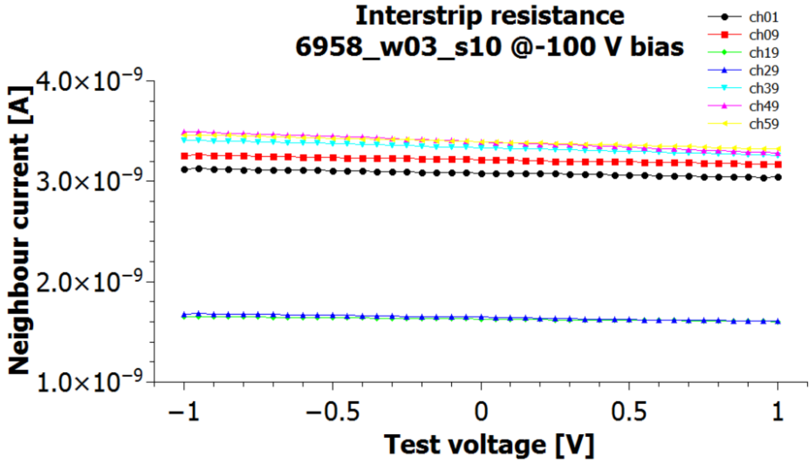
Expected value:

$R_{interstrip} > 10 \times R_{bias}$ @ Full depletion

- Rbias: <2.5 – 3.0> MΩ

$$R_{interstrip} = 2 / (\partial I_{Neighbour} / \partial V_{test})$$





Punch-Through measurement

HP4156

Voltage sweep: 0 V to 70 V (P4)

Voltage step: 0.25 V

Bias voltage: -100 V (chuck)

- For Vbias < -100 V
  - Use K2410 for -300 V, -200 V bias

Effective resistance:

$$R_{eff} = 1 / (\partial I_{test}/\partial Vtest) = Rbias // R_{PTP\ zone}$$