



AGH UNIVERSITY OF SCIENCE
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Setup of multilayer detector modules for FCAL test-beams

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Măgurele, Romania

- **Status found**
- **Present works**
 - **HV filtering**
 - **Voltage regulator**
 - **Decoupling**
 - **Multiboard integration**
- **Present status and plans**

LumiCal readout boards status Before my work...

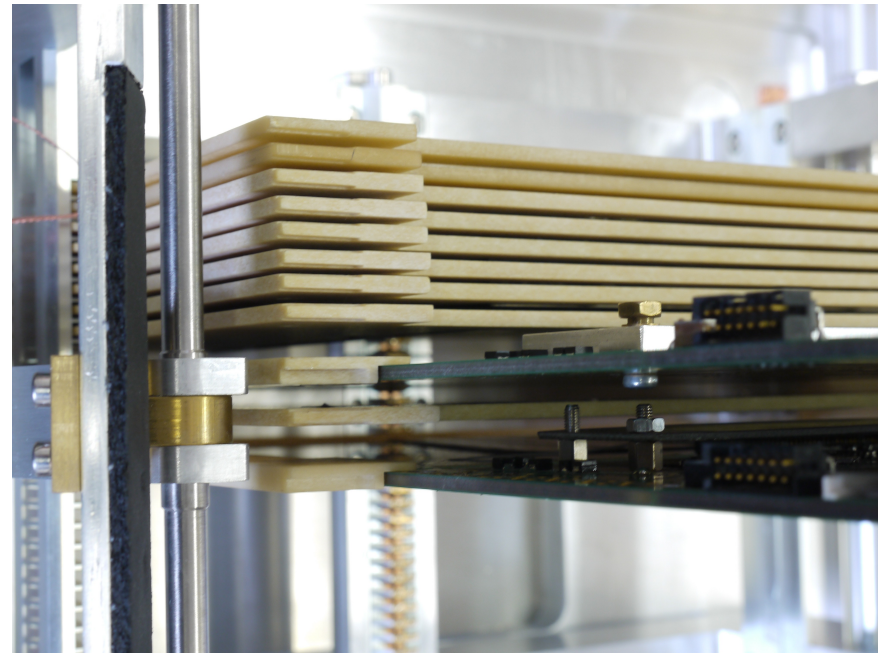
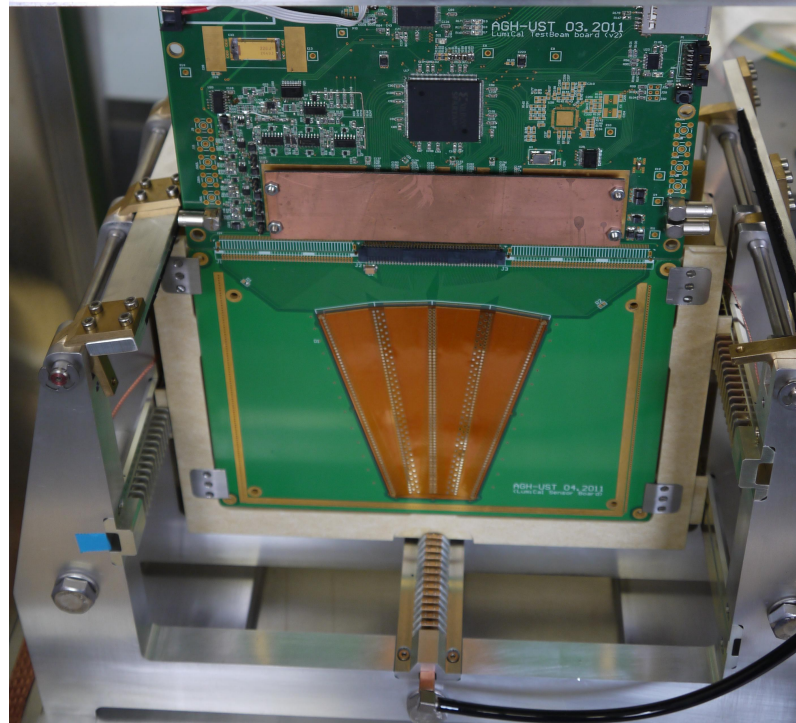
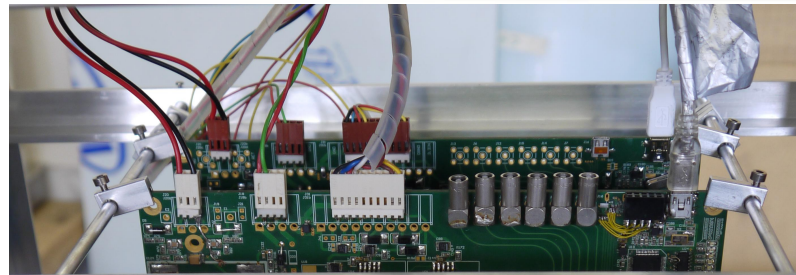
- Currently we have four readout boards and three sensors (**we are still missing one...**)
- Status of the boards:

Board ID	Owner	PCB version	Assembly version	HV filter	Noise (active feedback)	Noise (resistive feedback)	CERN tests
63	Krakow	2.0	1	OK	6	3	*
67	DESY	2.1	1	OK	6	3	
76	Tel-Aviv	2.1	2	NO	32	16	*
64	Krakow (second)	2.1	2	Wrong	32	16	*

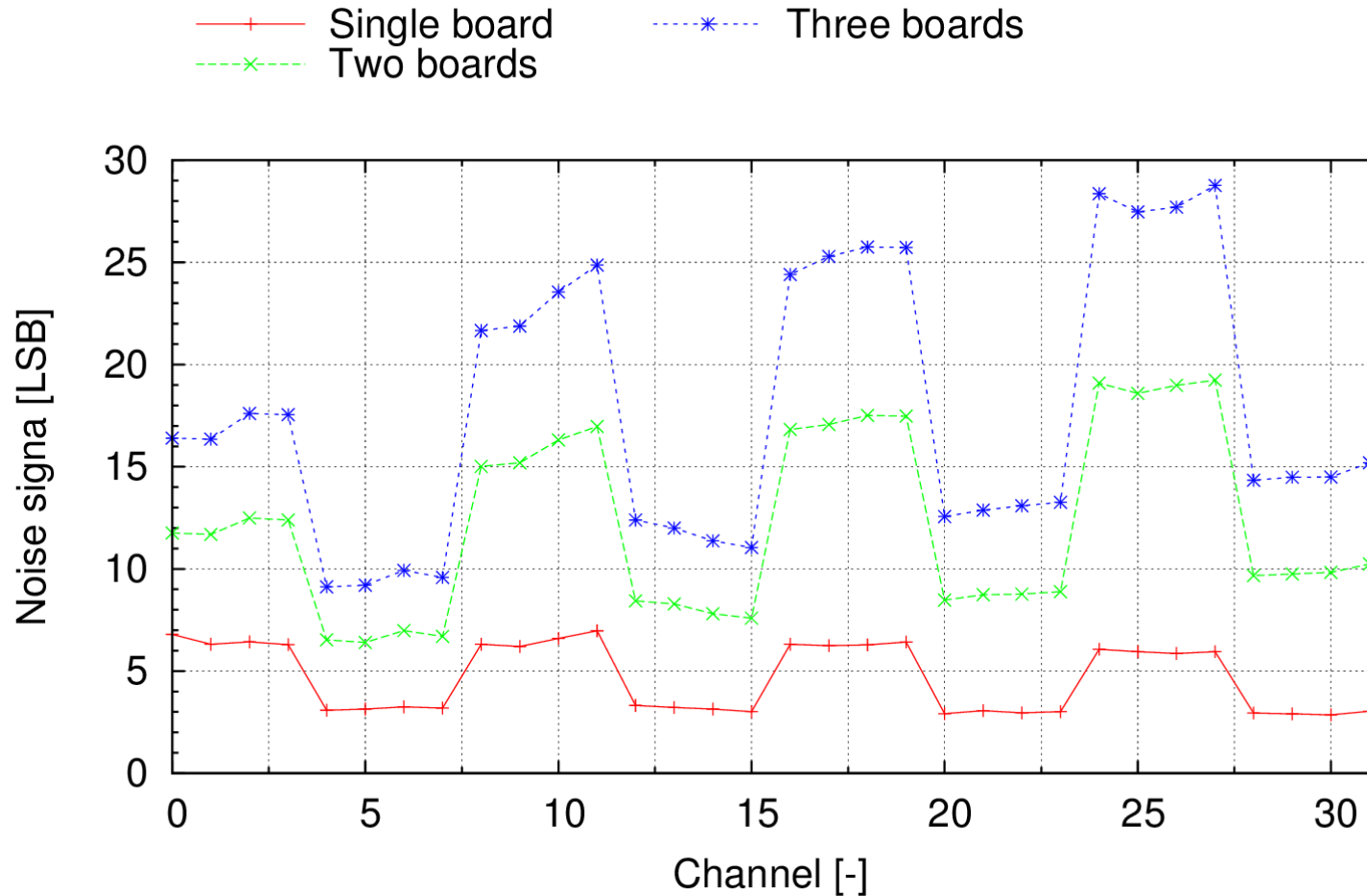
Integration of multi-plane readout at CERN

First try in November 2013...

- Tested configuration:
 - Three readout boards with three sensors
- Main problem: **a large increase in noise** with two or more boards connected together



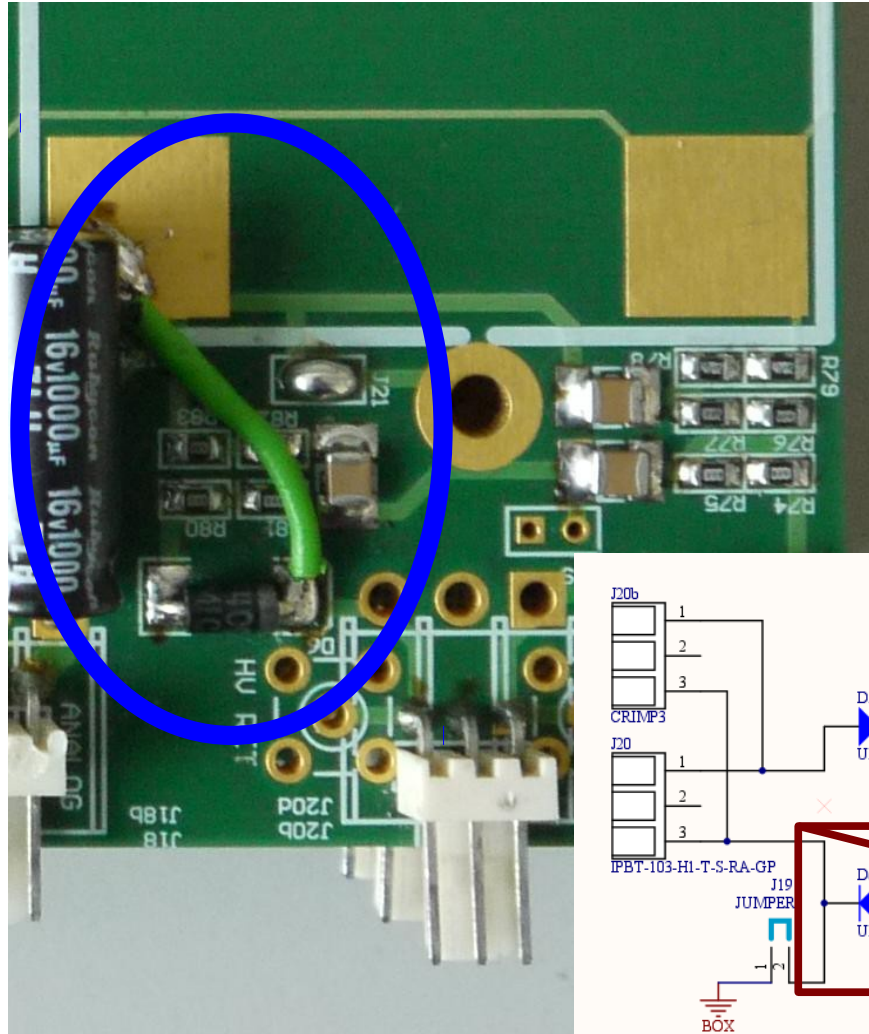
Integration of multi-plane readout at CERN First try in November 2013...



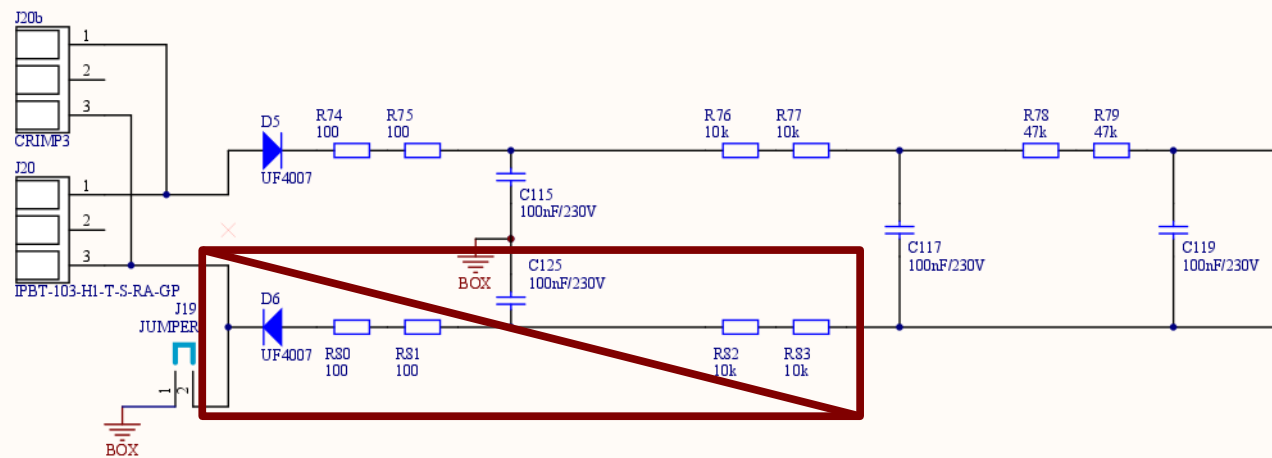
Not acceptable increase of noise for more than one board !!!

Present works in Krakow

HV filter modification on boards 64 and 76



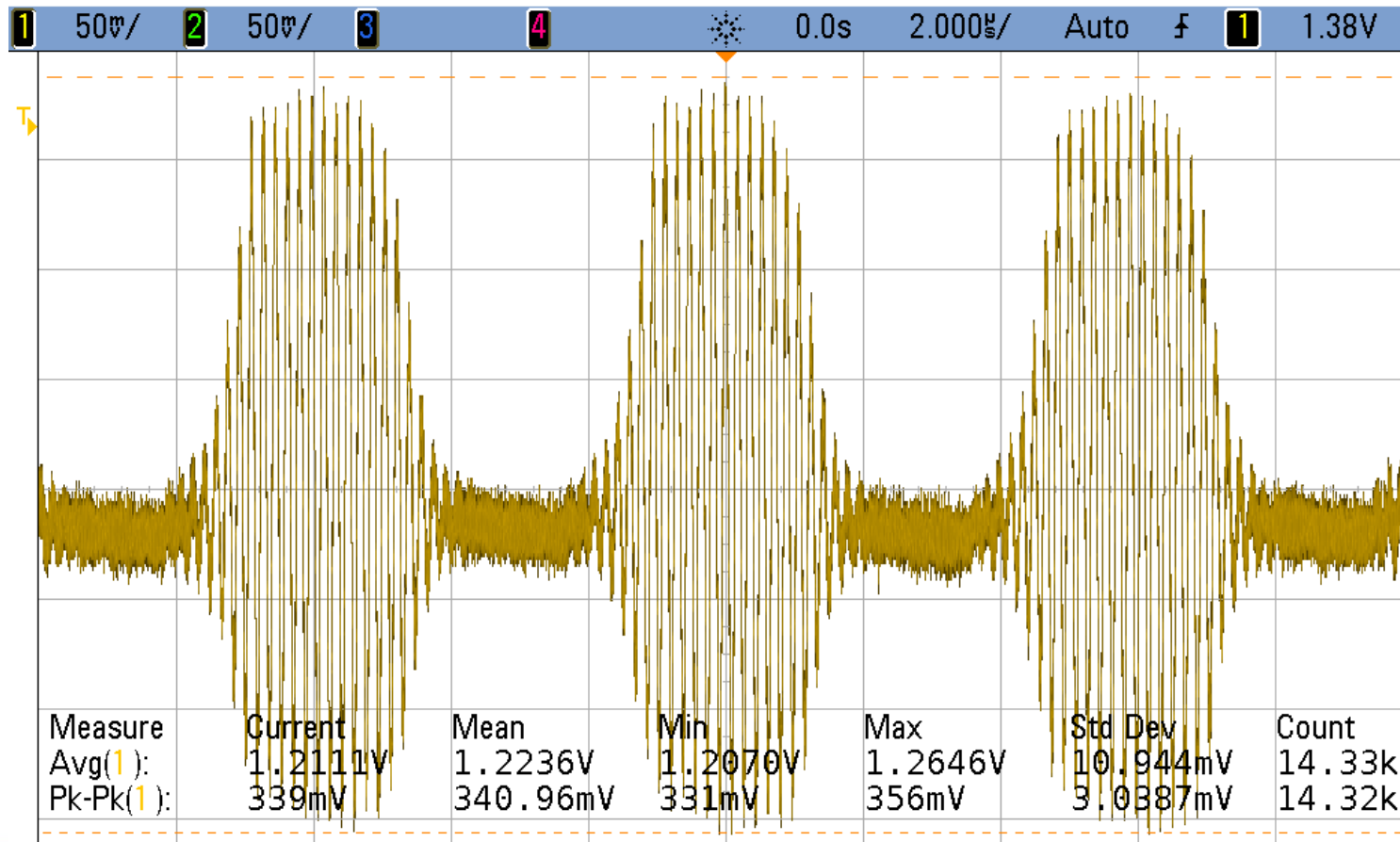
- **Noise reduction not achieved** by HV filter modification...



Present works in Krakow

FPGA core voltage regulator oscillations

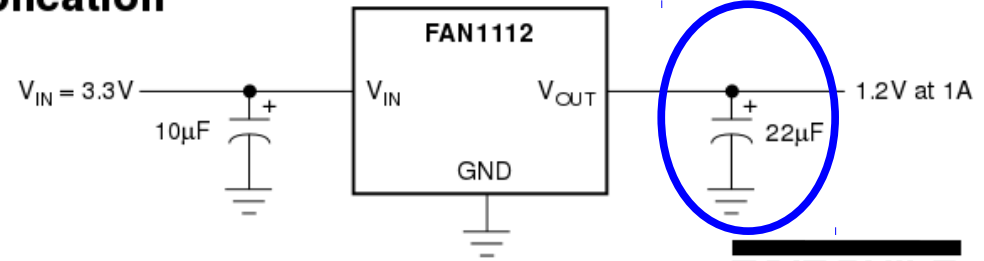
- FPGA core voltage regulator oscillations founded on boards 76 and 64 (second assembly version)



Present works in Krakow

Wrong decoupling causes FPGA voltage regulator oscillations

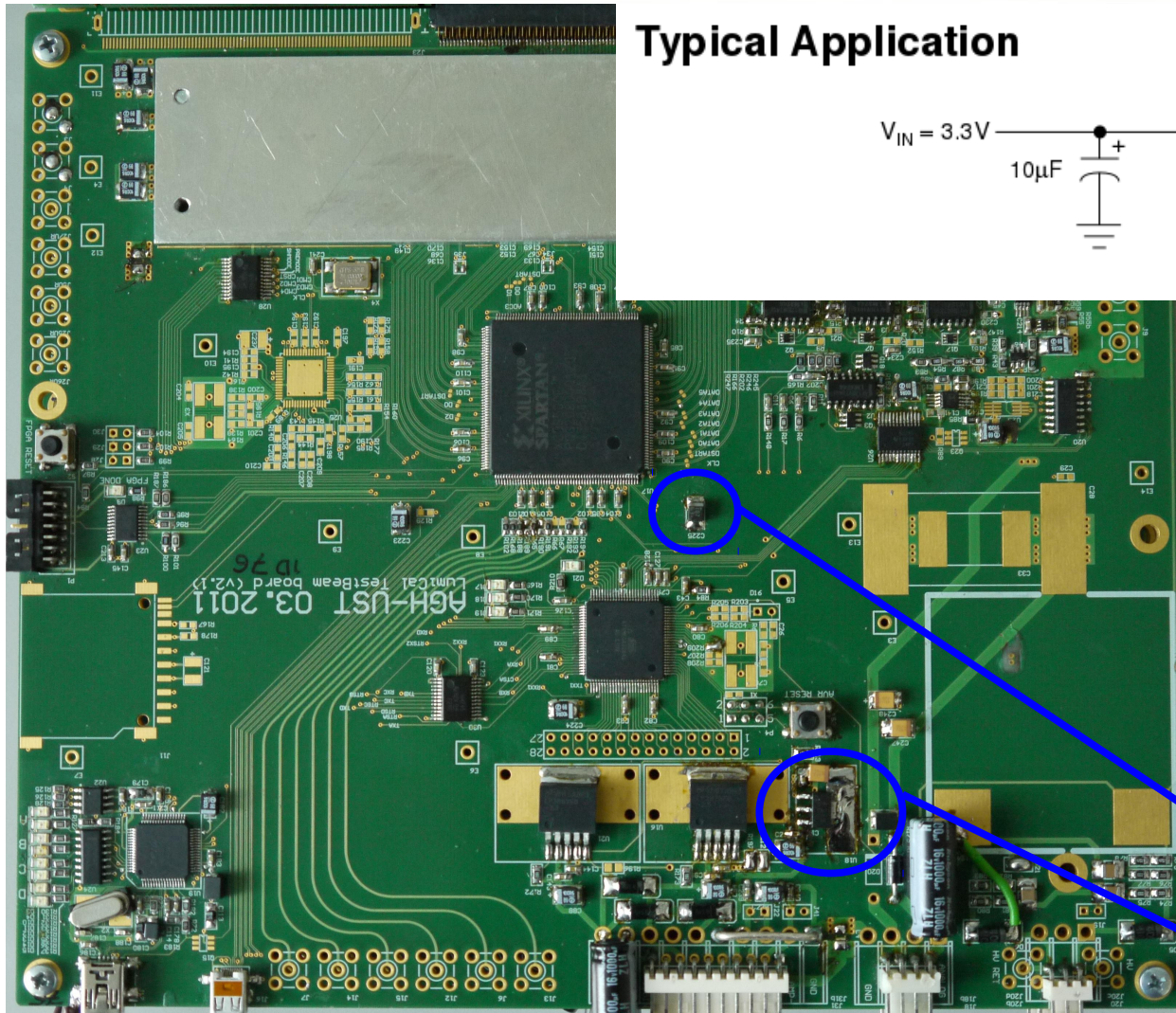
Typical Application



FAIRCHILD
SEMICONDUCTOR™
FAN1112

- Output capacitor too far from regulator
- Only 100nF directly at regulator output

Output 100µF capacitor
Regulator



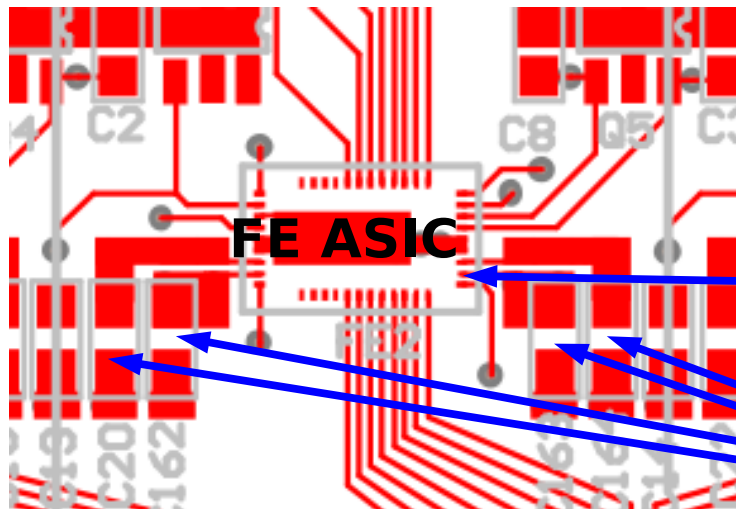
Present works in Krakow FPGA core voltage regulator oscillations

- 100uF capacitance added to regulator output
- Noise reduced to **12/6 LSB** - to times higher than reference level

Board ID	Owner	PCB version	Assembly version	Noise (active feedback)	Noise (resistive feedback)	Modifications
63	Krakow	2.0	1	6	3	-
67	DESY	2.1	1	6	3	-
76	Tel-Aviv	2.1	2	12	6	HV filter, FPGA regulator
64	Krakow (second)	2.1	2	12	6	HV filter, FPGA regulator

Present works in Krakow FrontEnd decoupling capacitances

- FrontEnd power supply 100nF decoupling capacitances used in two assembly runs differs - probably have different ESR (Equivalent Series Resistance)
- Capacitances located very close to the wirebonds (around 1mm)



Wirebonds

FrontEnd power supply
decoupling capacitors

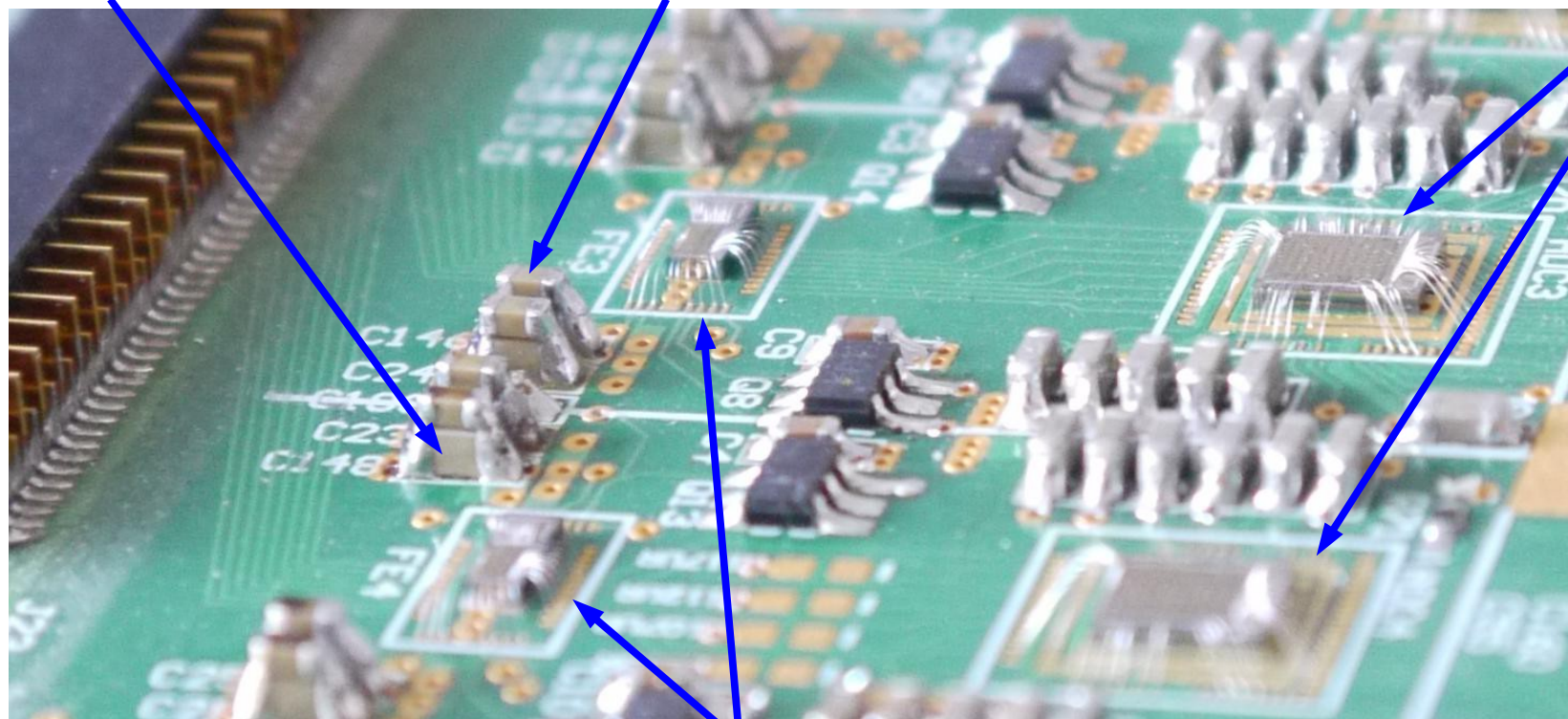
Present works in Krakow FronEnd decoupling capacitances

- Low ESR 1 μ F decoupling capacitors added paralelly to existing 100nF capacitances

Old 100nF

New 1 μ F

ADC ASICs



FE ASICs

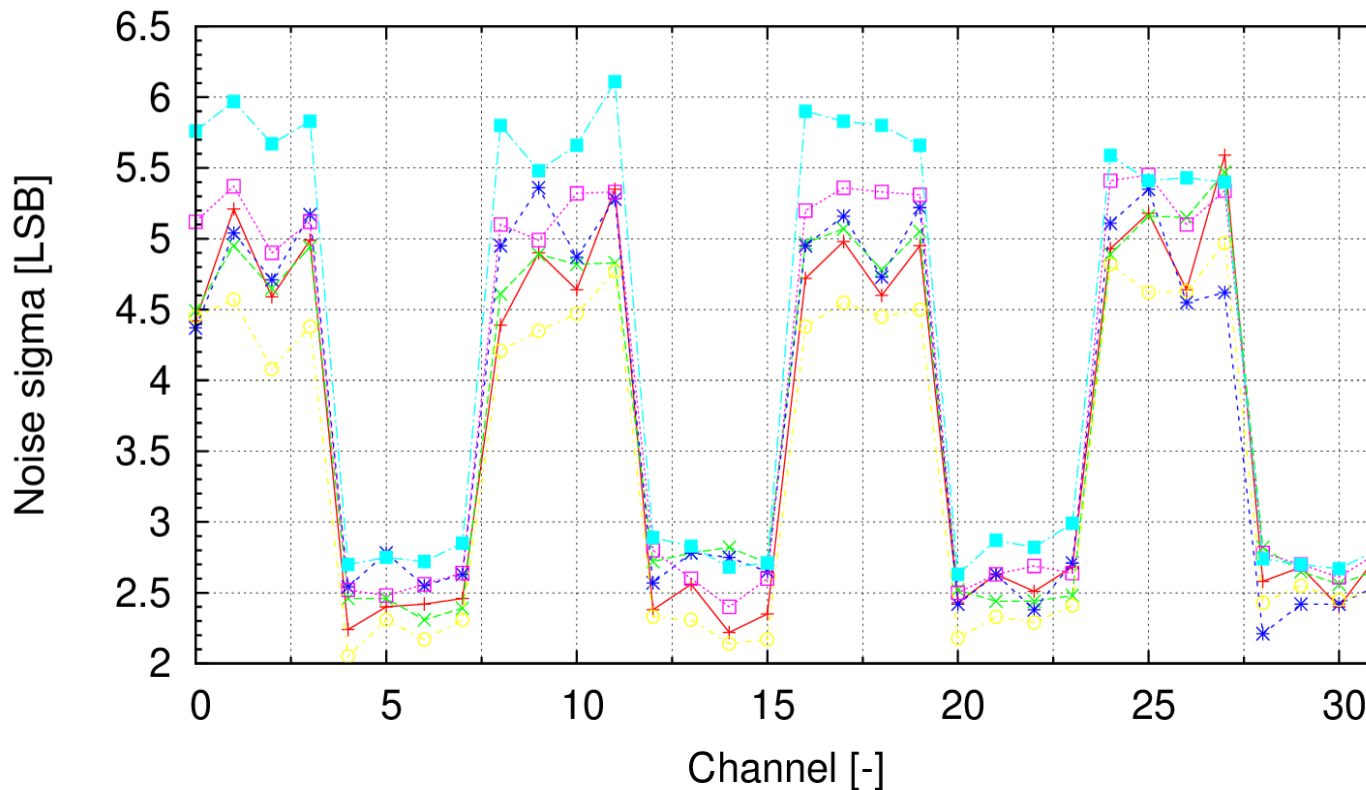
Present works in Krakow FronEnd decoupling capacitaces

- Noise reduced to 5.5/2.5 LSB – **below** reference level
- Decoupling capacitances added to all boards

Board ID	Owner	PCB version	Assembly version	Noise (active feedback)	Noise (resistive feedback)	Modifications
63	Krakow	2.0	1	6	3	-
67	DESY	2.1	1	6	3	-
76	Tel-Aviv	2.1	2	5.5	2.5	HV filter, FPGA regulator FE decoupling
64	Krakow (second)	2.1	2	5.5	2.5	HV filter, FPGA regulator FE decoupling

Present works in Krakow

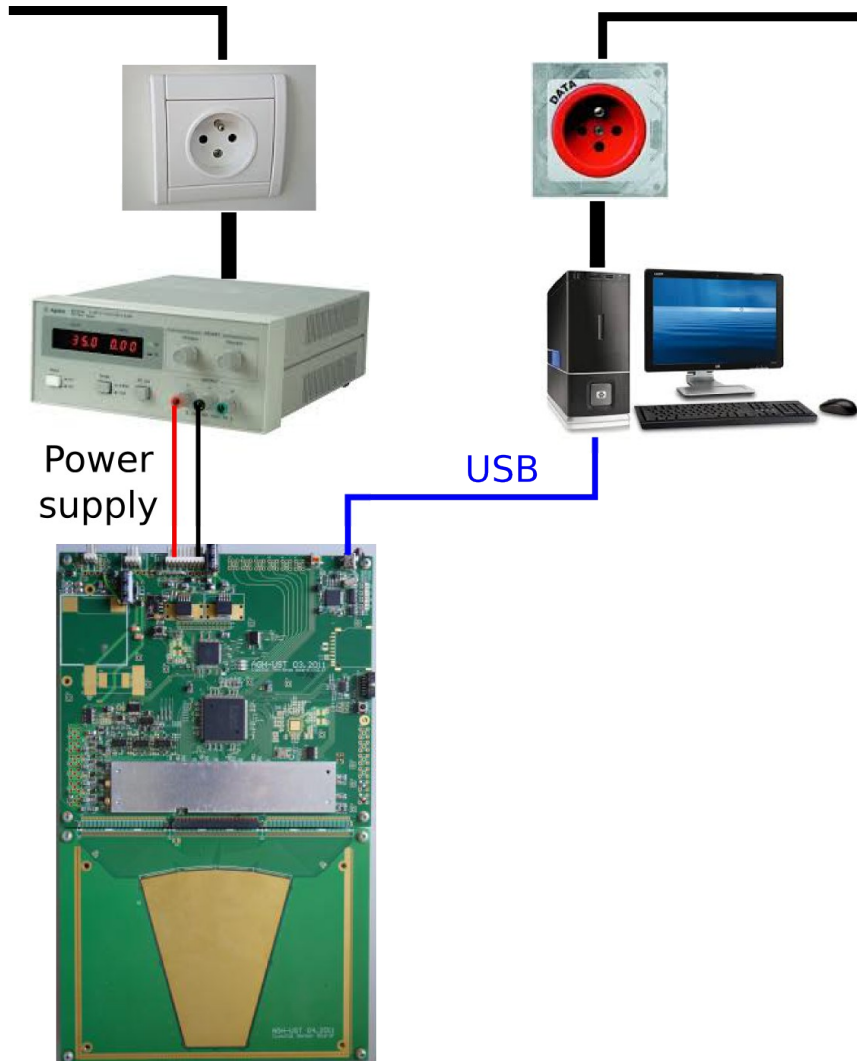
Single boards noise



After all modifications four boards have the same noise

Present works in Krakow

Single board readout - USB ground loop problem

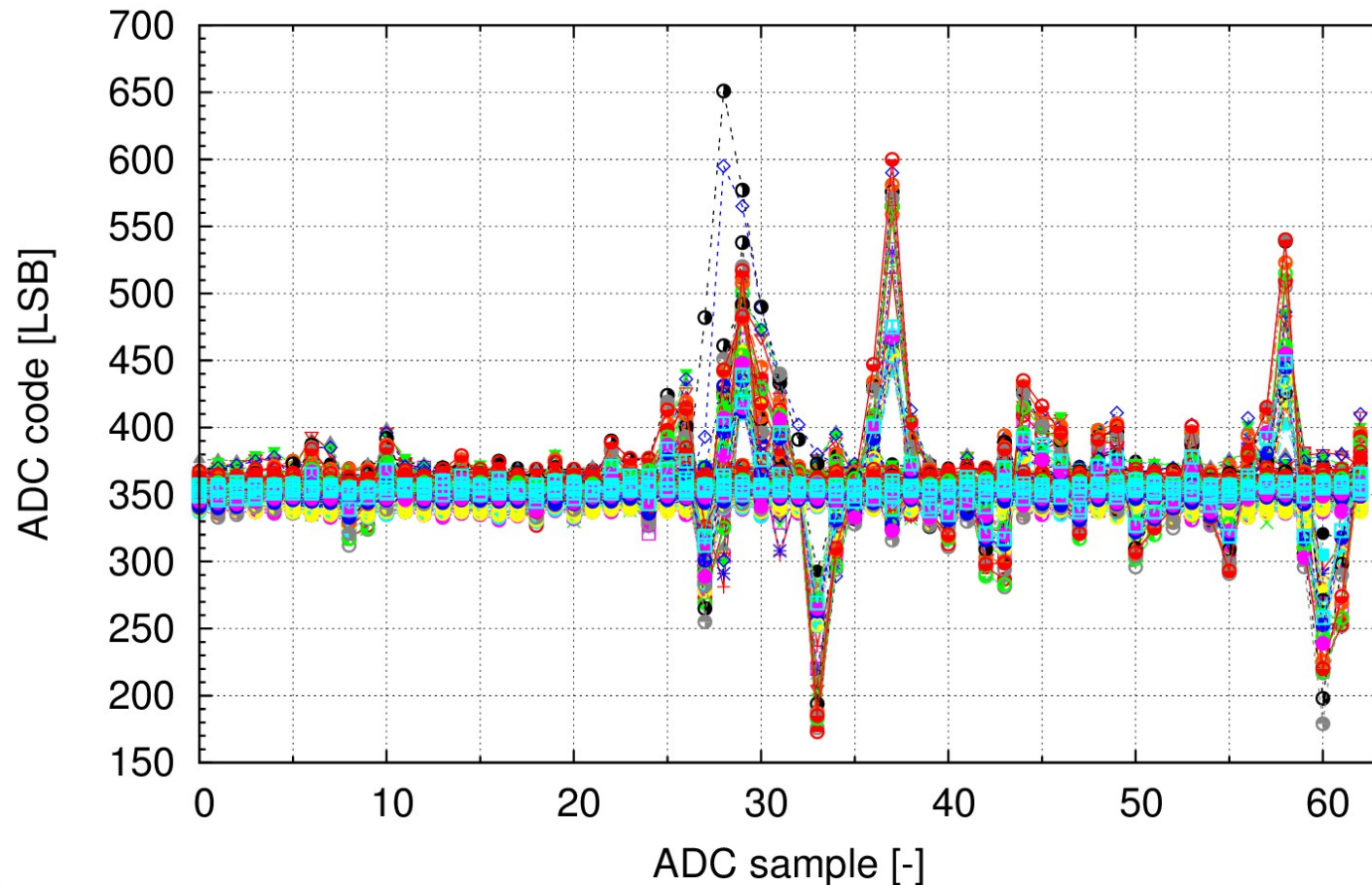


- Two separated power supply networks - one for equipment (ie. power supply) and second for computer
- Bad ground loop created by USB to PC connection

Present works in Krakow

Single board readout - USB ground loop problem

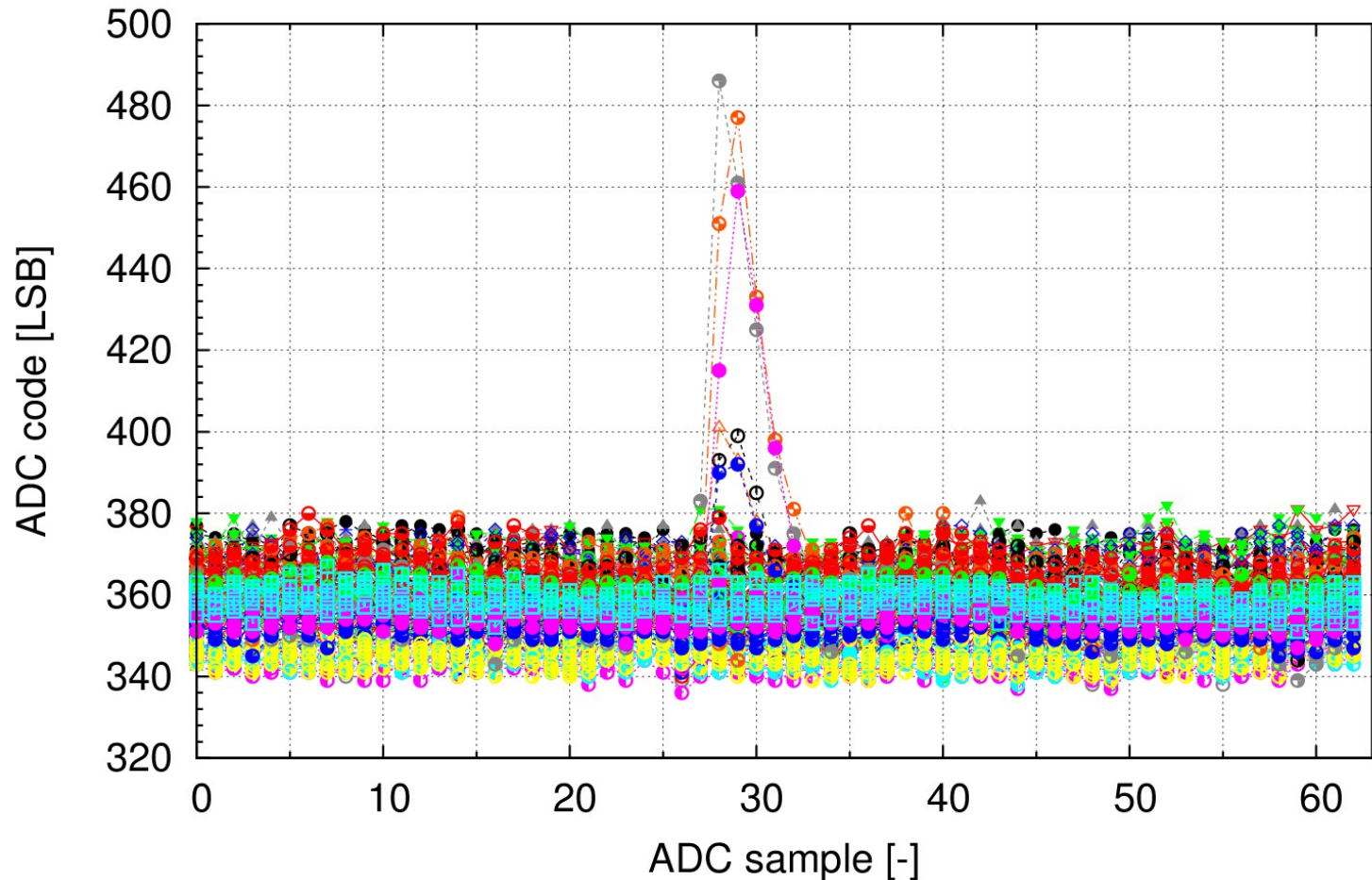
Disturbances caused by the connection of PC to separate power network



Present works in Krakow

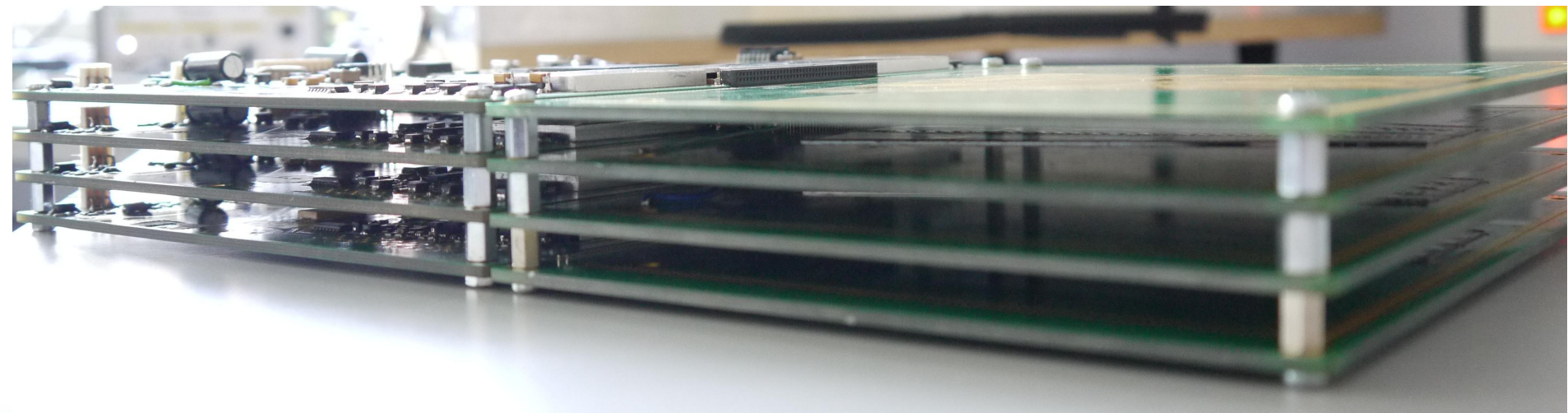
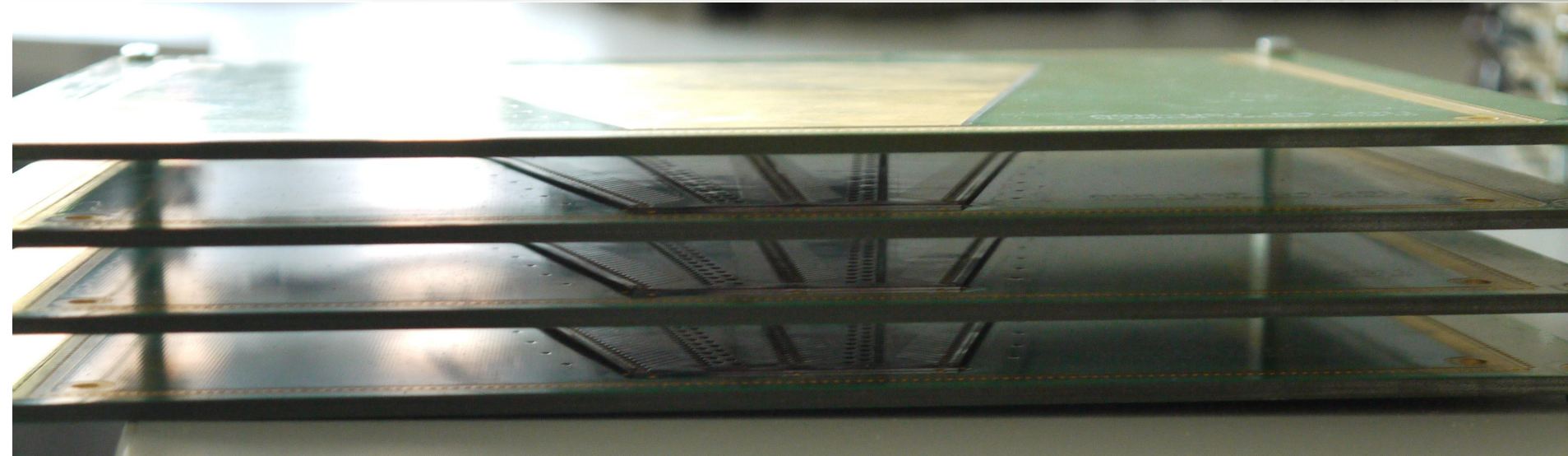
Single board readout - USB ground loop problem

PC and power supplies connected to the same power

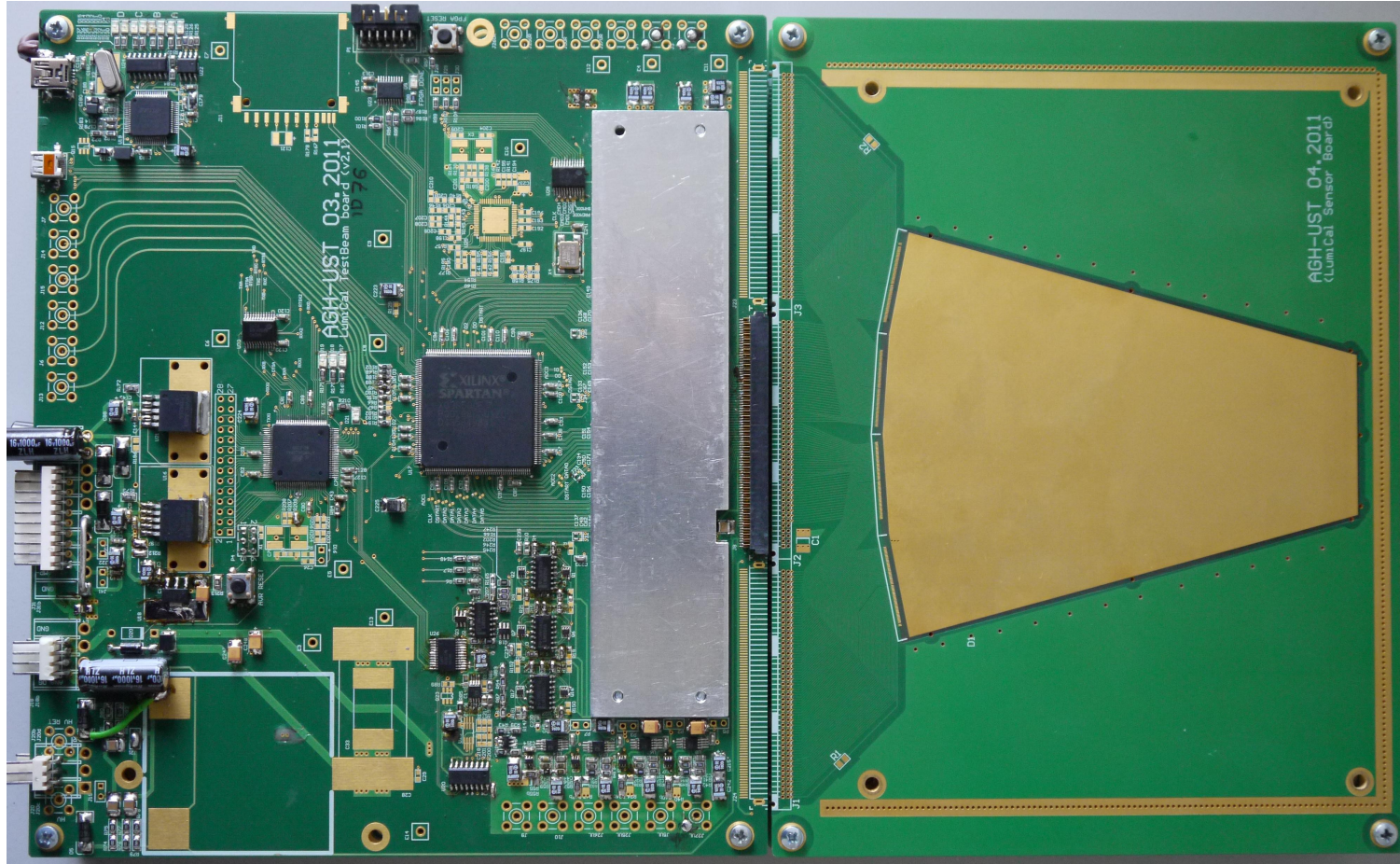


Present works in Krakow

Multiboard readout integration



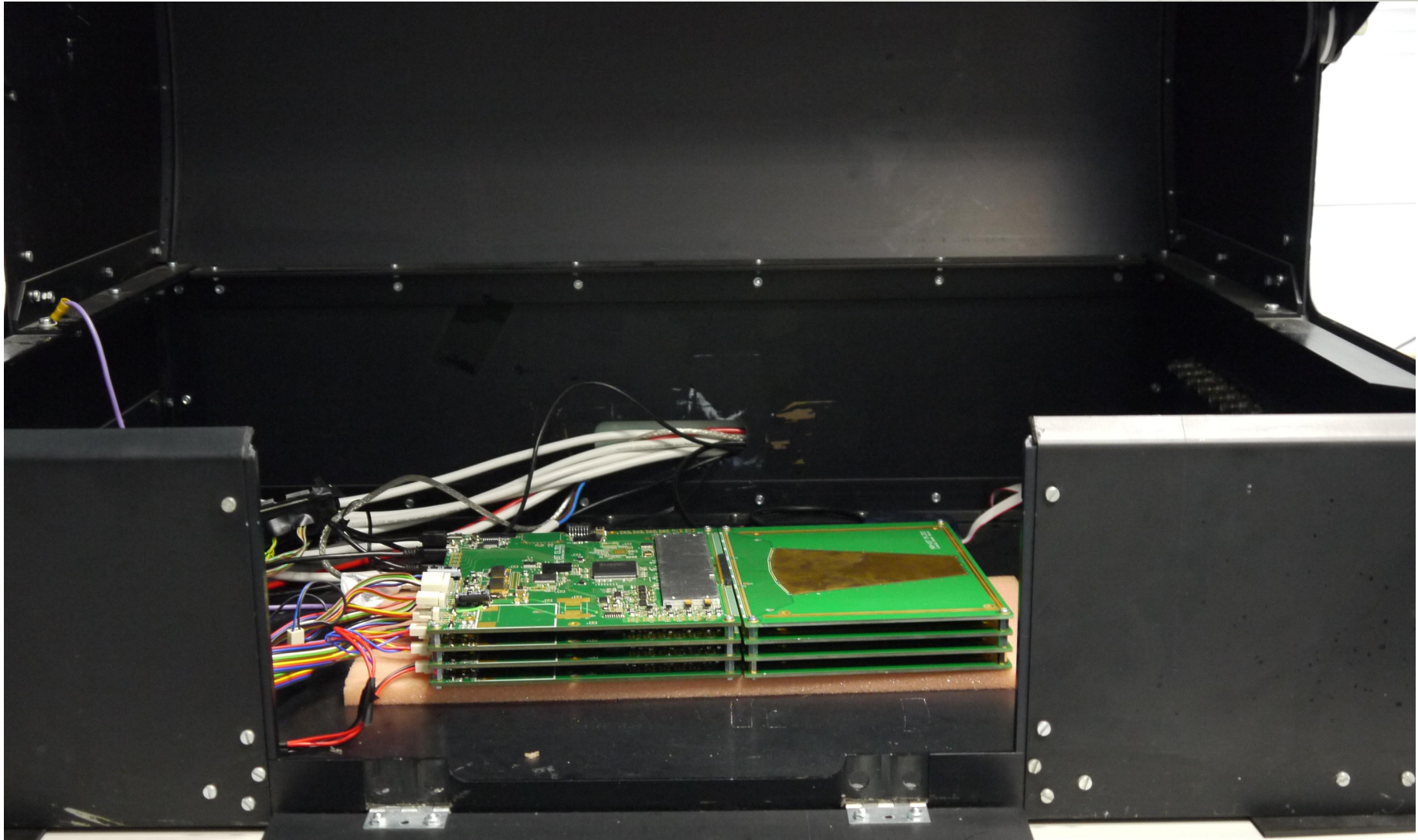
Present works in Krakow Multiboard readout integration



The fourth sensor is still missing !!!

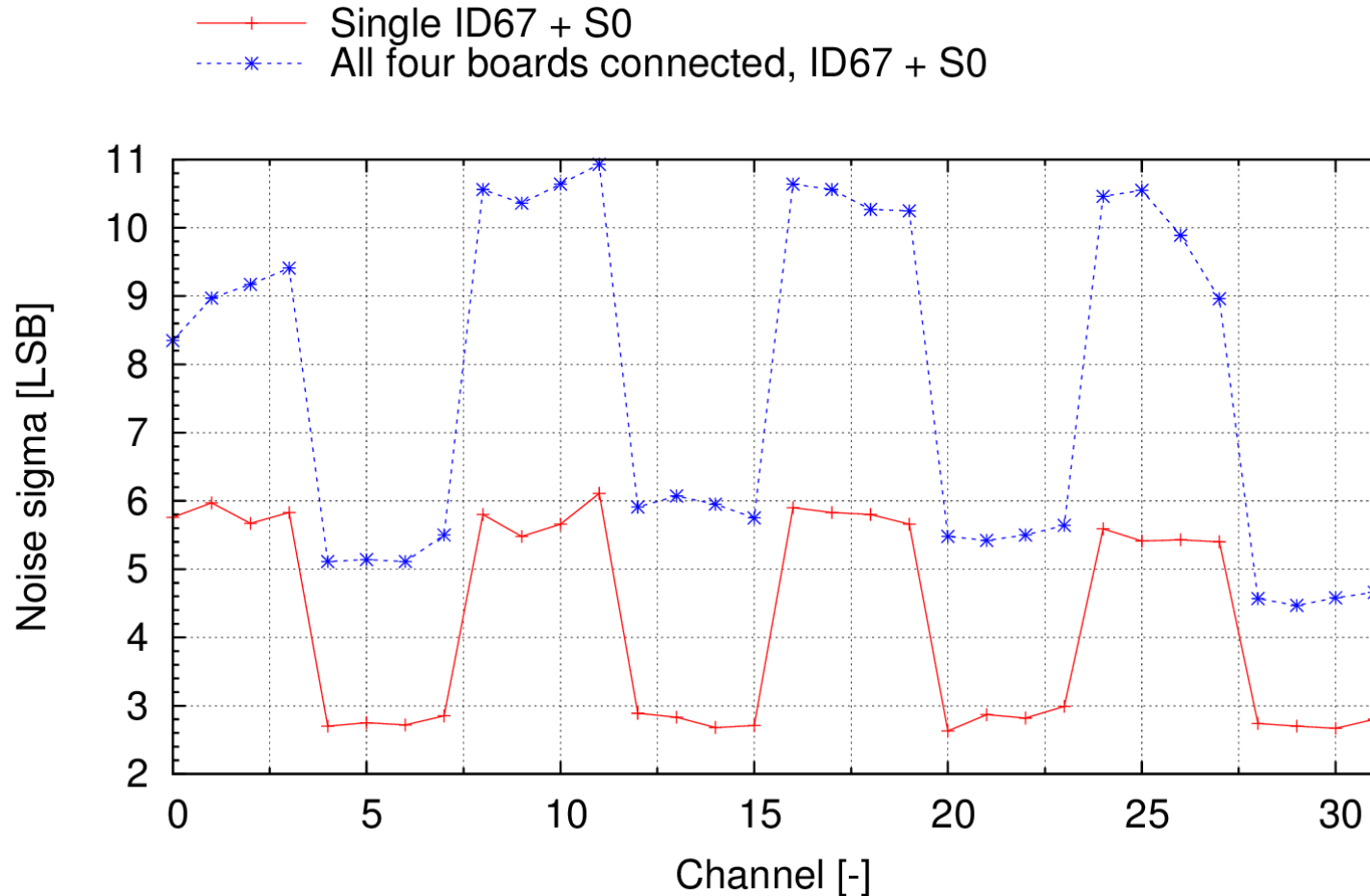
Present works in Krakow

Multiboard readout integration



Present works in Krakow

Multiboard readout integration - power supply decoupling



Again, the noise increases, but much less than at CERN

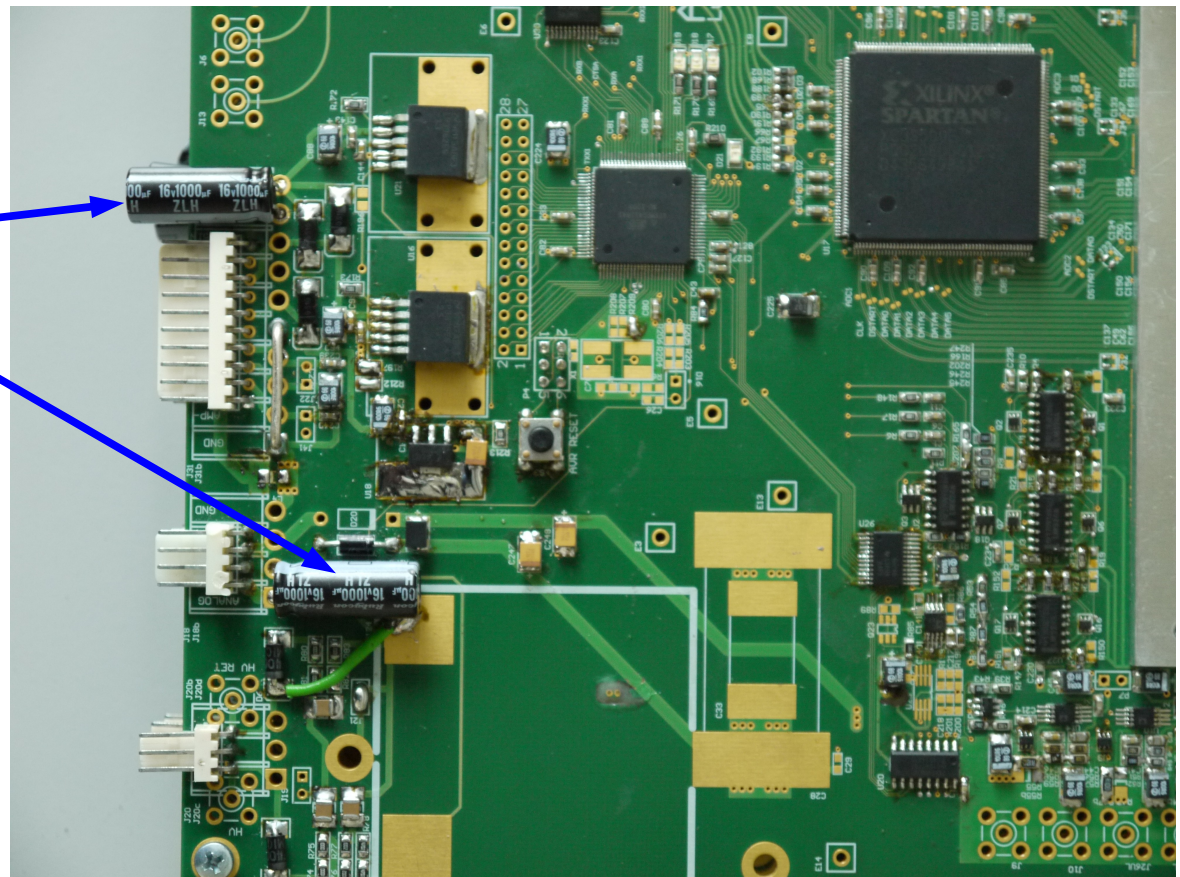
Present works in Krakow

Multiboard readout integration - power supply decoupling

- Low ESR, 1000uF decoupling capacitors added on each board at power supply inputs

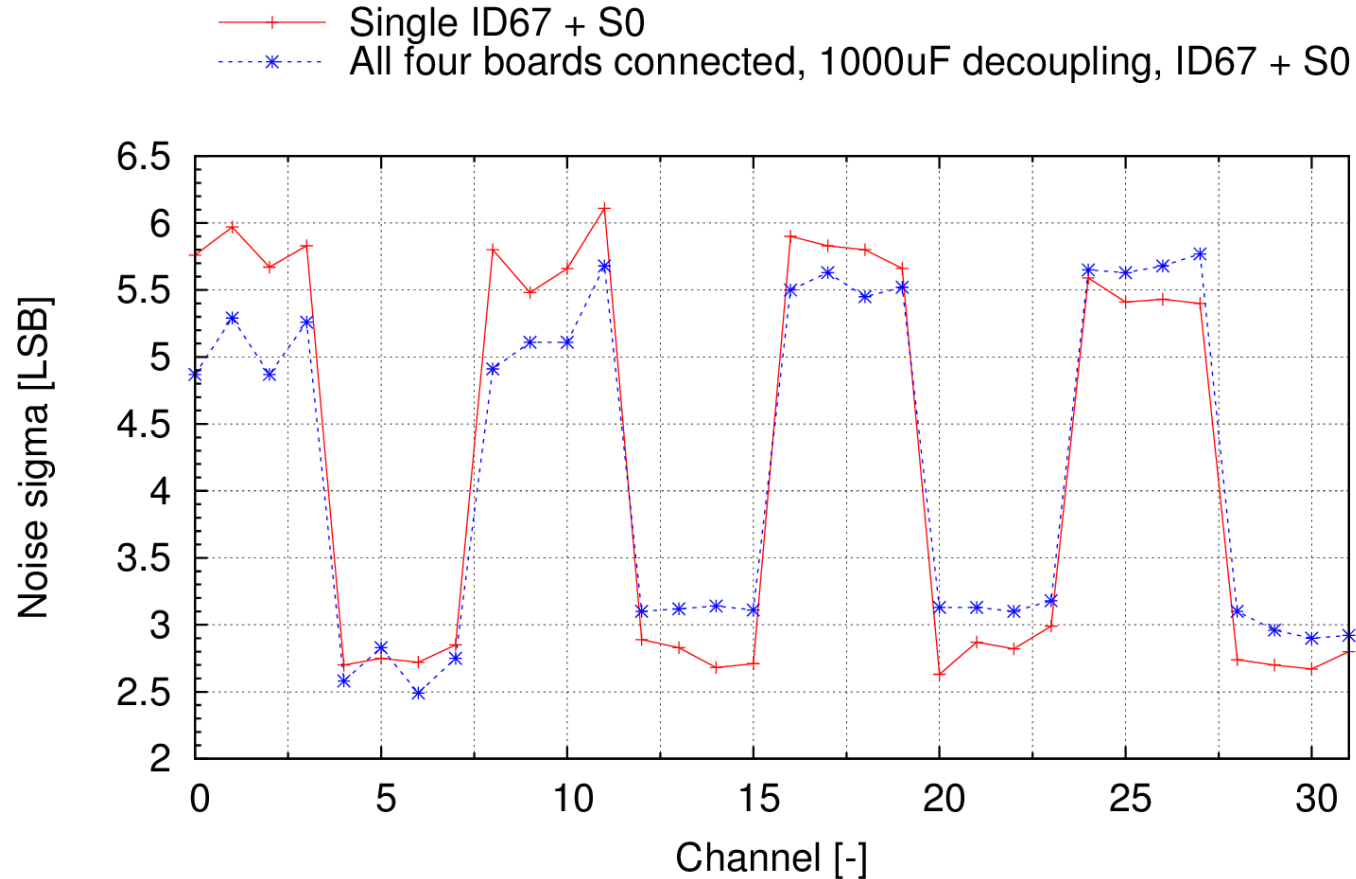
1000uF
added

- Smaller tantalum capacitors needed



Present works in Krakow

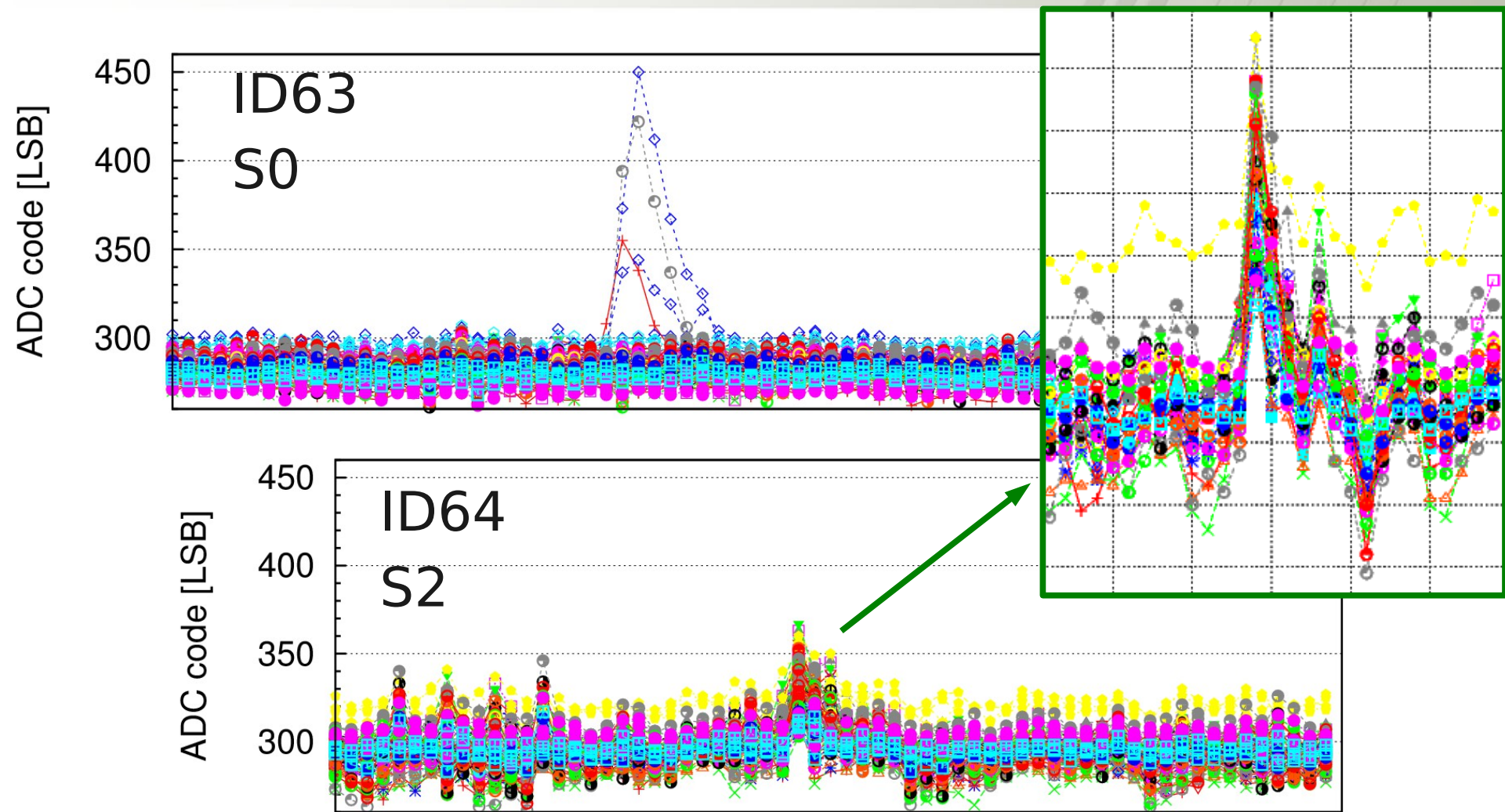
Multiboard readout integration - power supply decoupling



Four boards together have the same noise as the single board, but ... see next slide

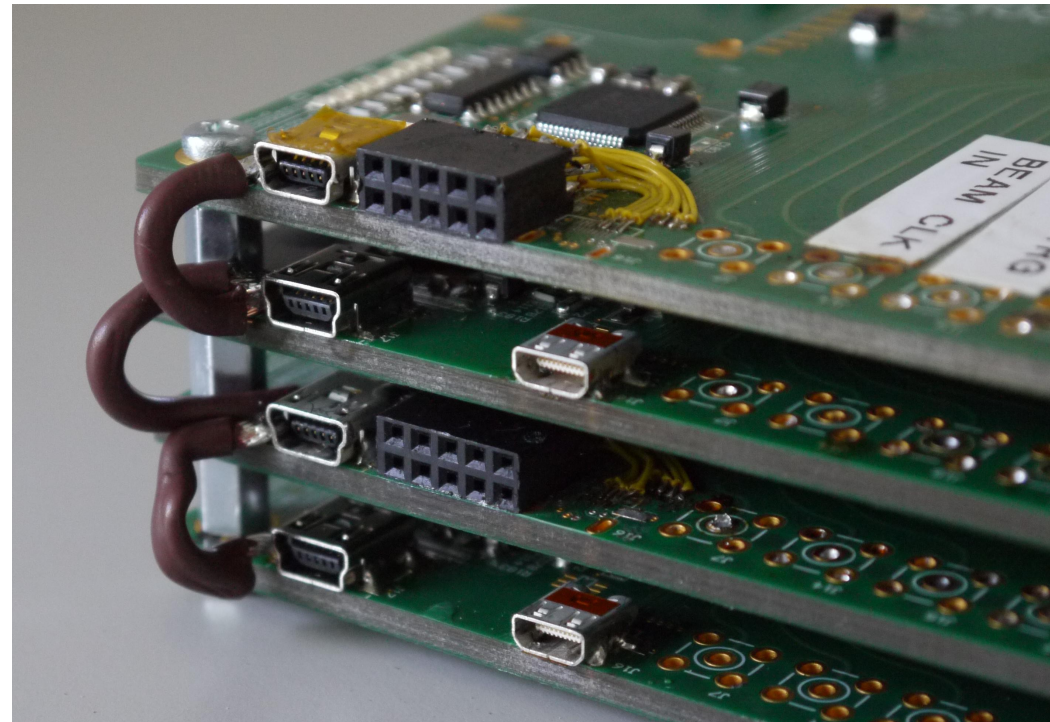
Present works in Krakow

Multiboard readout - USB ground loop problem (?)



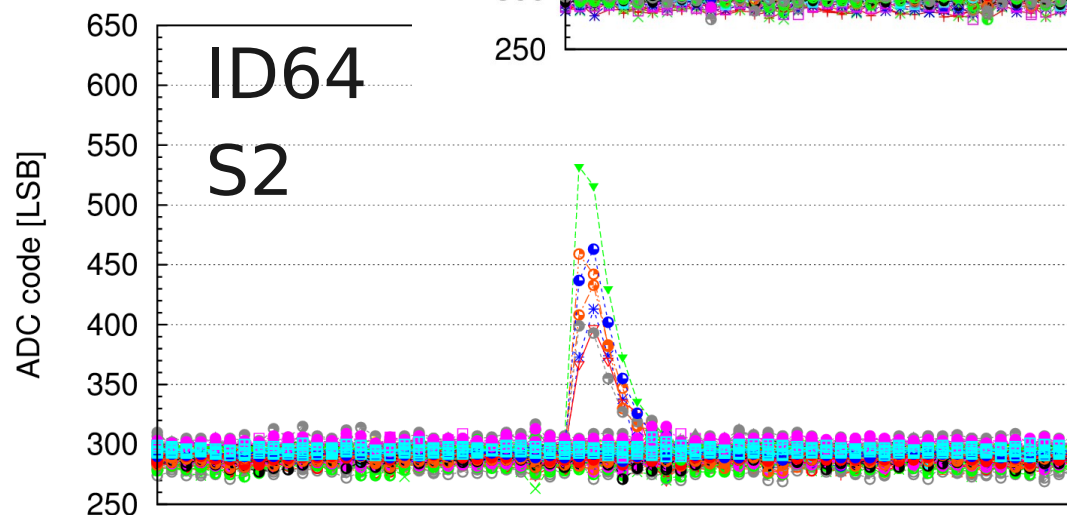
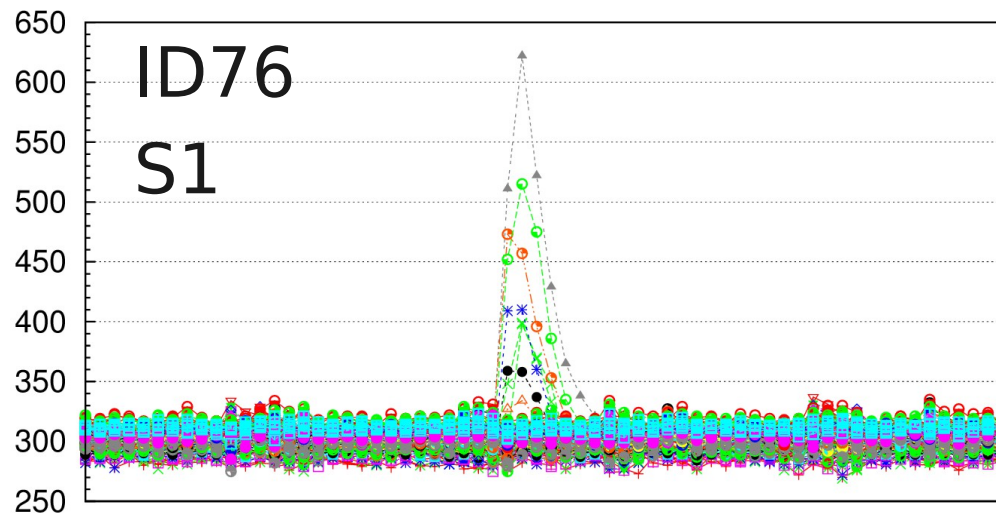
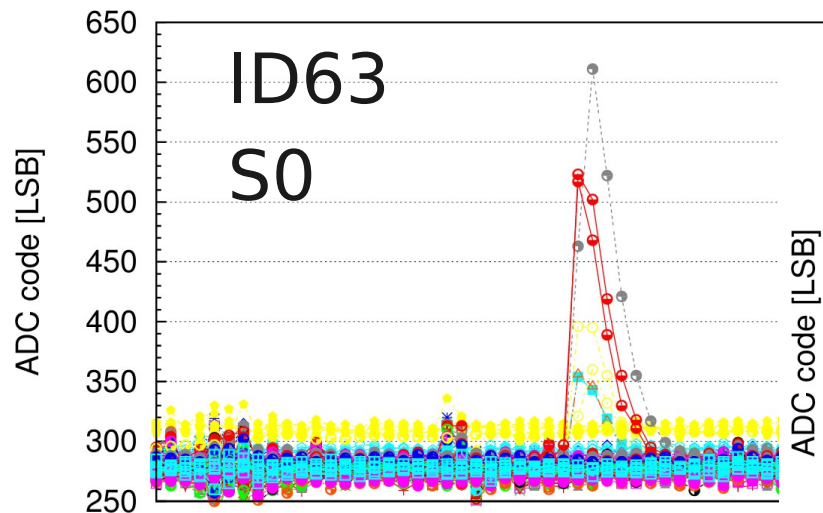
Present works in Krakow Multiboard readout - USB ground loop problem (?)

- Each board connected via USB cable to PC - ground multiloop created
- USB ground shorted between boards - baseline variations reduced but not eliminated...
- FPGA core voltage instability found on friday evening - probably better regulator needed...



Present works in Krakow

Multiboard readout - USB ground loop problem - high trigger treshhold



- All four boards uniformed and noise reduced
 - HV filter modifications
 - FPGA core voltage oscilation eliminated
 - FrontEnd decoupling improved
 - Ground loop through PC connnection reduced
- Multiboard integration still in progress...
 - Noise reduced by power supply decoupling
 - **Baseline variations still require some work...**
 - **TLU-like trigger system for cosmic measurements needs to be developed...**