AGH UNIVERSITY OF SCIENCE AND TECHNOLOGY

Development of new front-end electronics in CMOS 130 nm

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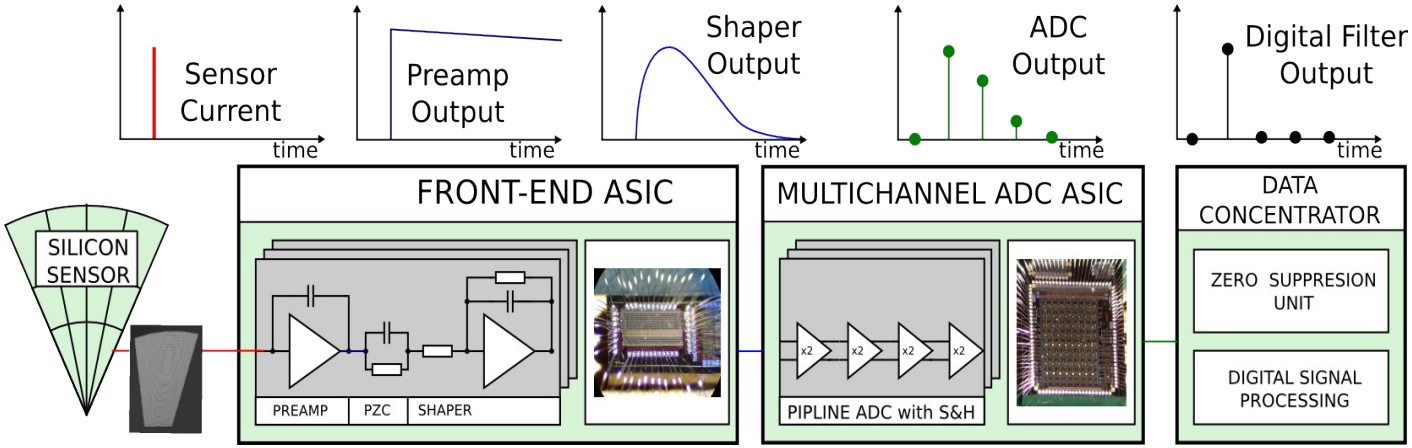
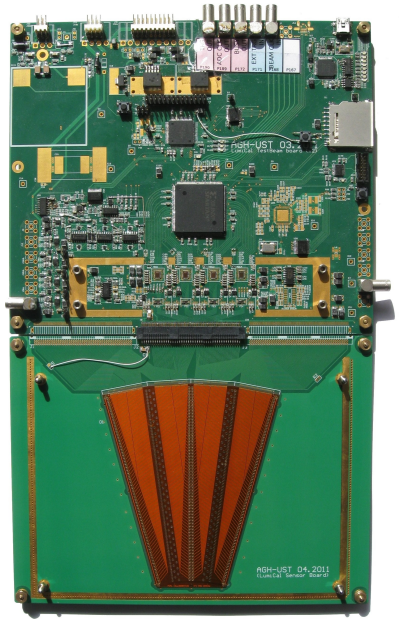
Outline

- Introduction and Where we are
- ASIC developments in CMOS 130 nm
  - Preamp-Shaper, ADC, PLL, SLVS blocks
  - IBM, TSMC technologies
- Summary and Plans

Introduction
LumiCal detector readout chain





Existing readout developed in CMOS AMS 0.35 um comprises:

- 8 channel front-end ASIC (preamp, shaper Tpeak~60ns, ~9mW)
- 8 channel pipeline ADC ASIC, Tsmp<=25MS/s, ~1.2mW/MHz
- FPGA based data concentrator and further readout

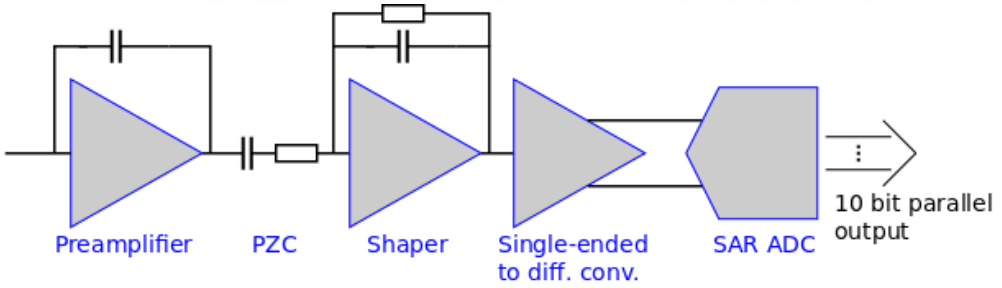
New developments in IBM CMOS 130 nm:

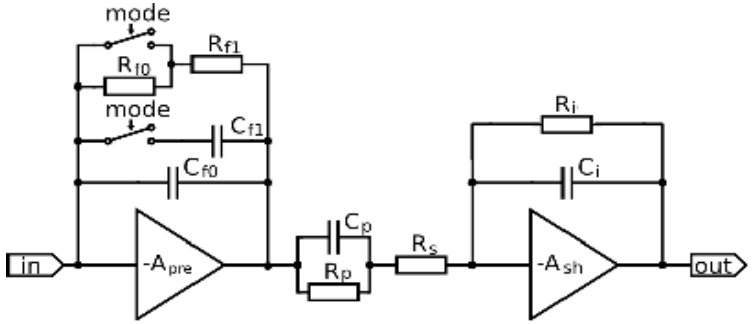
- First prototype of front-end ASIC developed and under tests
- First prototypes of SAR ADC ASIC developed and under tests

Even Newer developments in TSMC CMOS 130 nm just started...

New readout for LumiCal in IBM CMOS 130 nm
Architecture and technology comparison

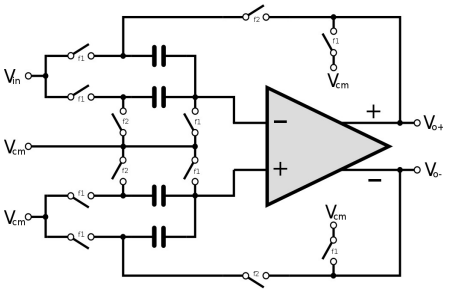
New readout in 130 nm has very similar architecture to existing one in 0.35um but should consume much less power and be radiation resistant





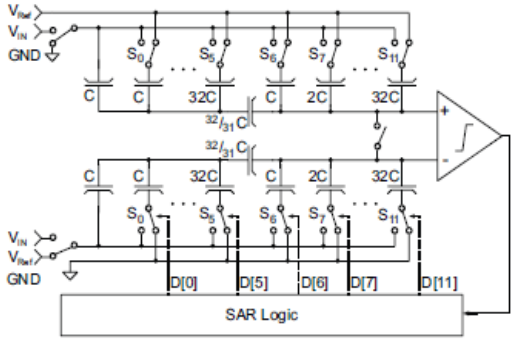
Front-end specs:

- Cdet ≈ 5 ÷ 50pF
- 1st order shaper (Tpeak ≈ 50 ns)
- Variable gain, two modes:
  - calibration: MIP sensitivity
  - physics: Q_{in} up to ~6 pC
- Power pulsing
- Peak power cons. **~1.5 mW**/channel (in AMS 0.35um it was **~9mW**)



Single-to-Diff specs:

- Max freq. > 40MHz
- Power pulsing
- Peak power ~ 0.5mW

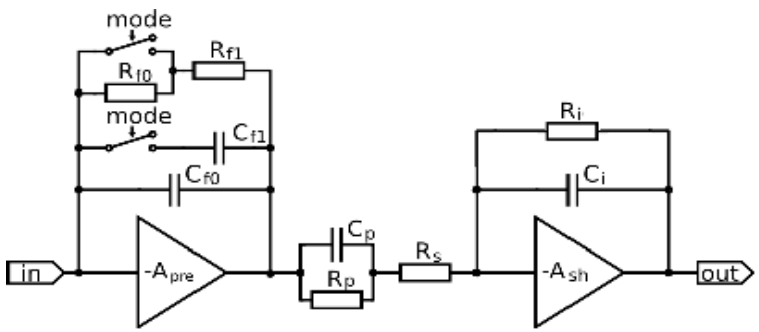


ADC specs:

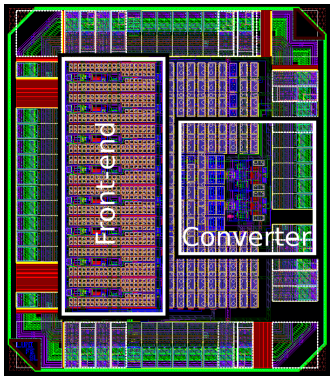
- 10-bit resolution
- Architecture: SAR ADC
- Max frequency > 40 MHz
- Power pulsing
- Peak power ~ 1 mW @40MHz (in AMS 0.35u mit would be > 40mW)

LumiCal front-end in IBM 130 nm Design, Simulations, Tests

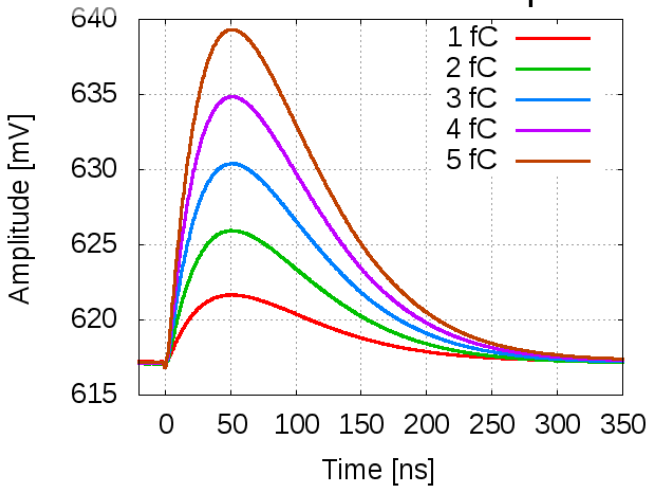
Channel schematic diagram



Layout



Measured front-end response



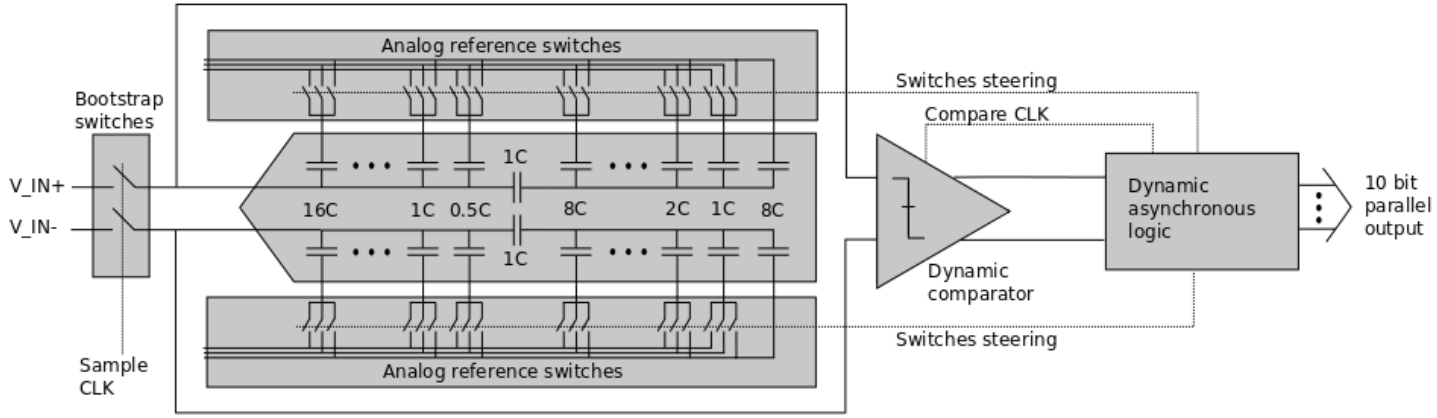
Design specs:

- 8 channels
- Cdet ≈ 5 ÷ 50pF
- 1st order shaper (Tpeak ≈ 50 ns)
- Variable gain:
  - calibration mode - MIP sensitivity
  - physics mode - input charge up to ~5 pC
- Power pulsing implemented
- Power consumption ~1.5 mW/channel

Very Preliminary Measurements:

- Fully functional
- Tpeak ≈ 51 ns
- Calibration mode @10pF:
  - gain 4.1 mV/fC
  - linear range ~60 fC
  - ENC 930 e-
- Physics mode @10pF
  - gain 105 mV/pC
  - Linear range ~2.7 pC (saturates >5pC)

10-bit SAR ADC for LumiCal in IBM 130 nm Architecture&Design considerations



Architecture of ADC:

- Differential segmented/split DAC with MCS switching scheme – ***ultra low power***
- Dynamic comparator – ***no static power consumption, power pulsing for free***
- Asynchronous logic – no clock tree – ***power saving, allows asynchronous sampling***
- Dynamic SAR logic – ***much faster than conventional static logic***

Design considerations:

- Resolution 10 bits
- Variable sampling frequency up to ~50 MS/s
- Power consumption at 40 MS/s ~1 mW
- pitch, ready for multichannel integration 146 µm

J. Moron, M. Firlej, T. Fiutowski, M. Idzik, Sz. Kulis, K. Swientek. "Development of variable sampling rate low power 10-bit SAR ADC in IBM 130 nm technology", TWEPP2013 23-27 September 2013, Perugia Italy

ADC testing
Measurement setup

DFT and data analysis – custom software

Power supply

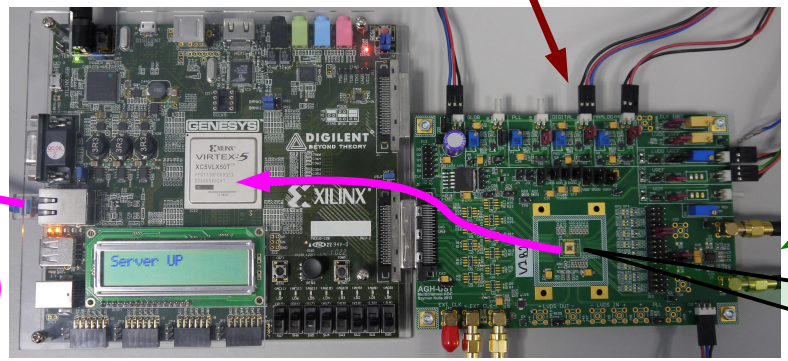
Differential function generator – Agilent 81160A

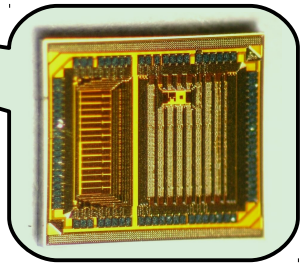
Input sine

Sample clock

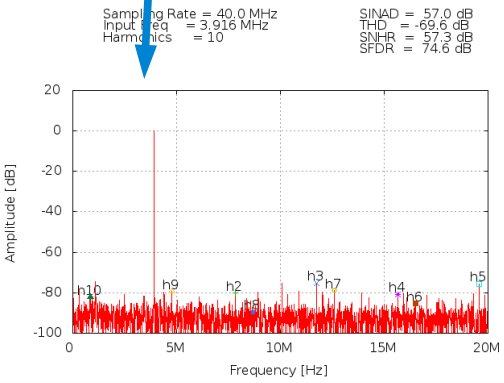
Results

Sampled data (**low bitrate**)





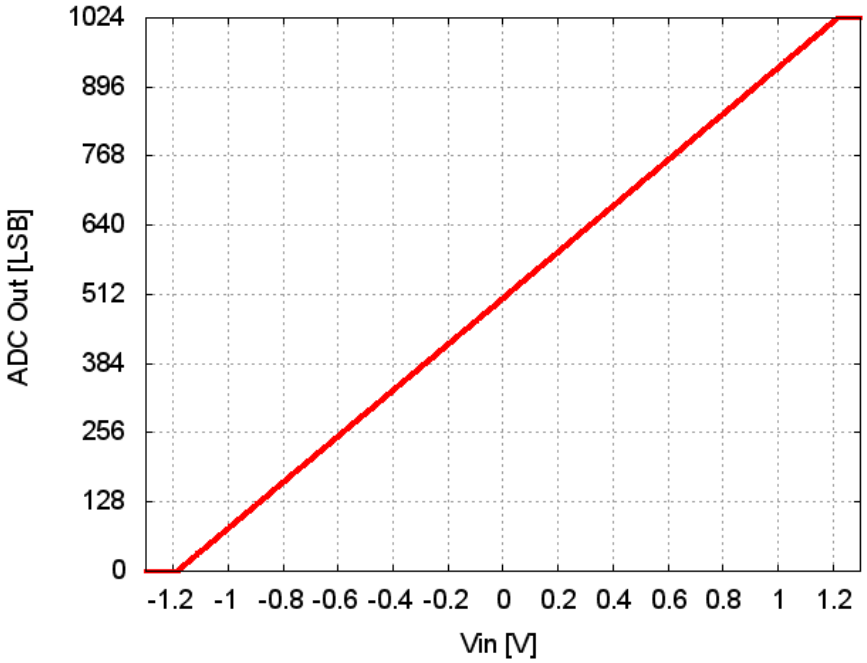
Sampled data (**high bitrate**)



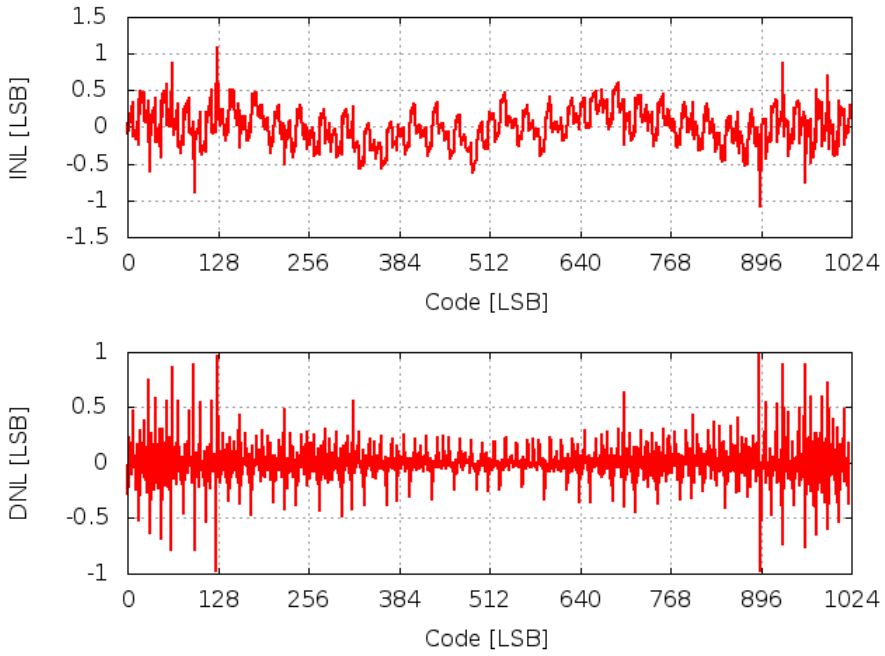
DAQ – receives fast transmission from ADC (up to 500 Mb/s), captures the data and sends to PC via Ethernet for offline analysis

10-bit SAR ADC in IBM 130 nm
Static measurement results

Transfer function



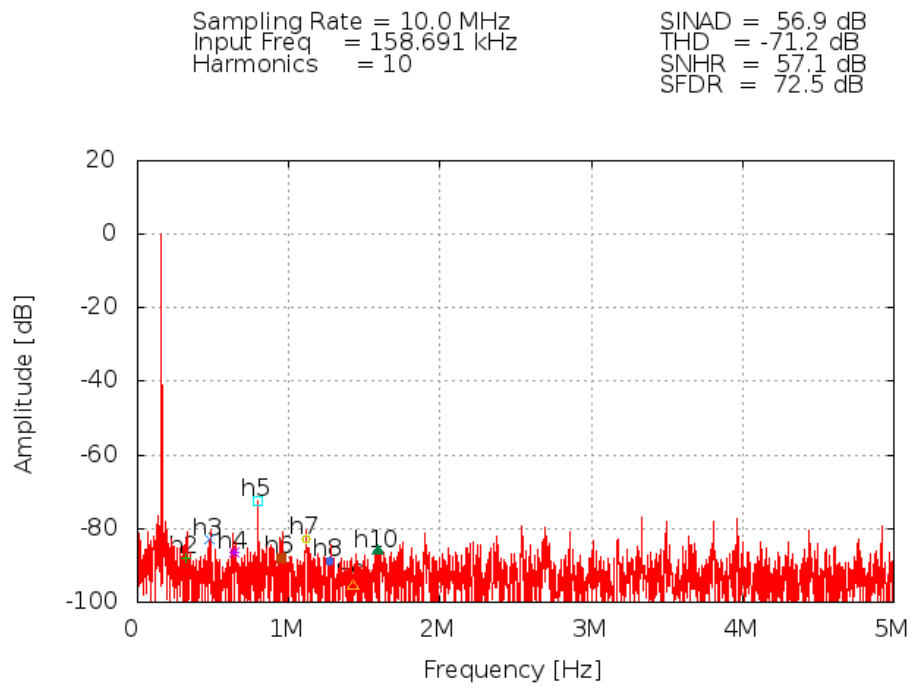
INL/DNL measurements



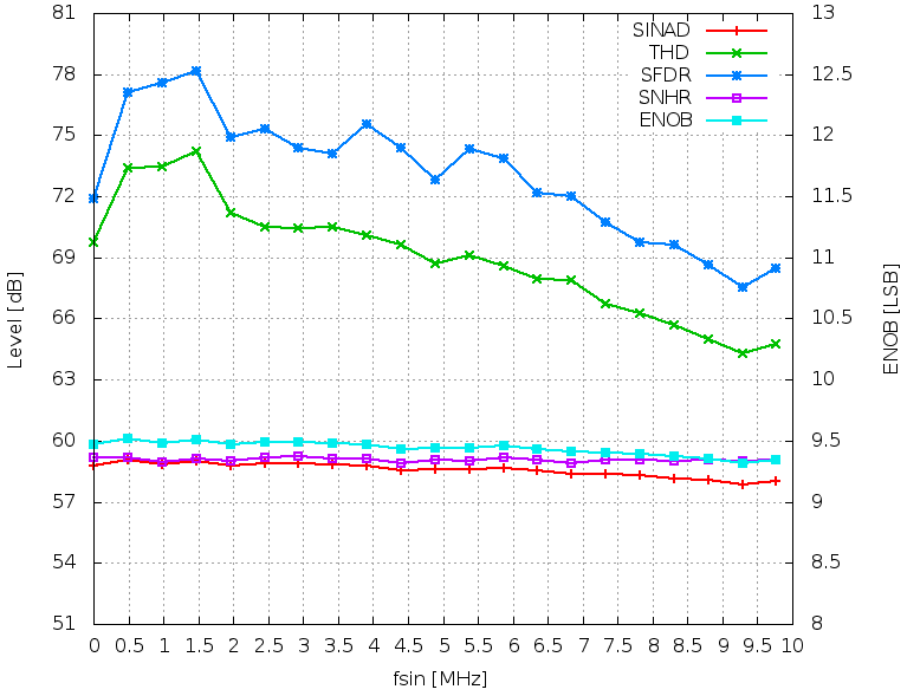
- ADC works well in the whole input signal range
- Generally, good linearity is measured, although for a few codes improvement is still needed

10-bit SAR ADC in IBM 130 nm
Dynamic measurement results (@20 MS/s)

Example DFT Spectrum



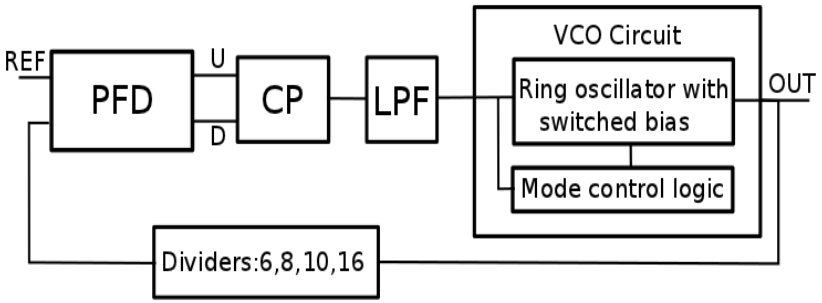
Input frequency sweep

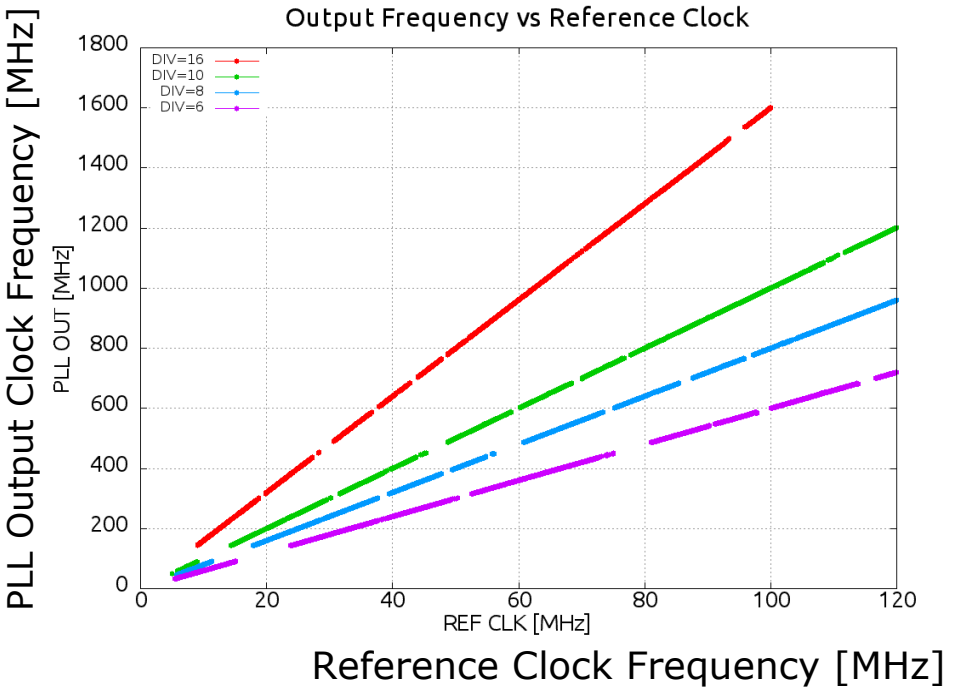


ENOB~9.3 up to Nyquist input frequency for f_{sample} ~20MHz & P~0.7mW

ADC works for f_{sample} beyondt 40 MS/s, but above 20 MS/s ENOB start to decrease.
Problem with jitter above 20 MS/s found..., will be fixed in next submission.

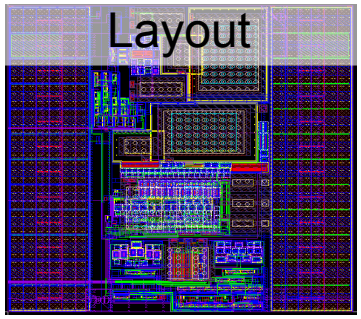
Low power PLL in IBM 130 nm Architecture, design, and measurements





Main features:

- General purpose PLL block
- Very wide output frequency range: **10MHz – 3.5GHz** (tested up to 1.6GHz)
  - Gaps in frequency are found in the prototype – to be eliminated...
- 16 VCO modes - Automatically (or manually) changed
- Jitter 15-70 ps (to be improved...)
- Power consumption **~0.6mW@1GHz**
- Different loop division factors: **6,8,10,16**
- Size 300um x 300um

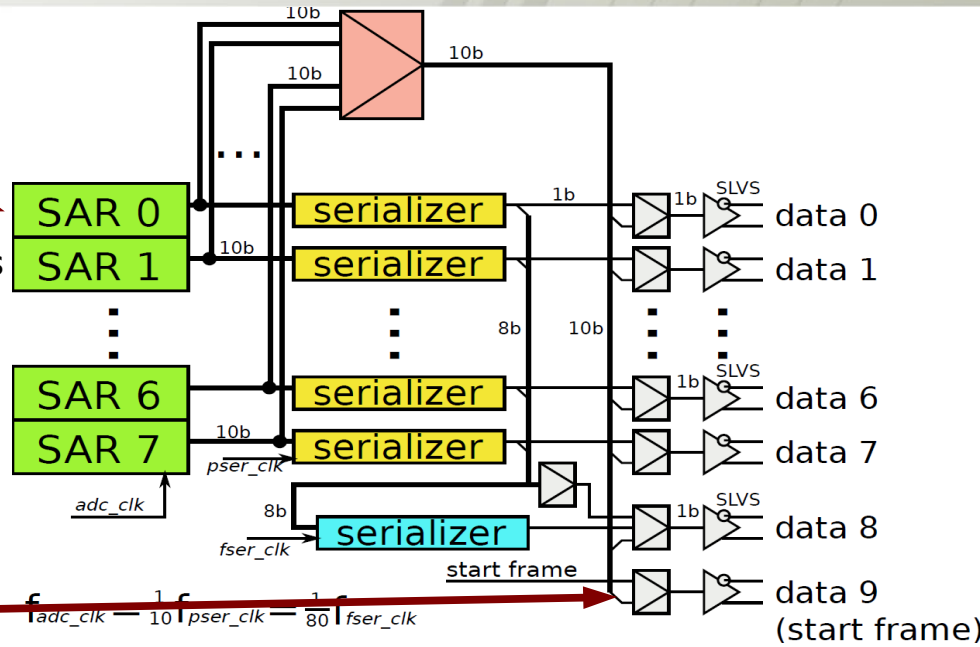


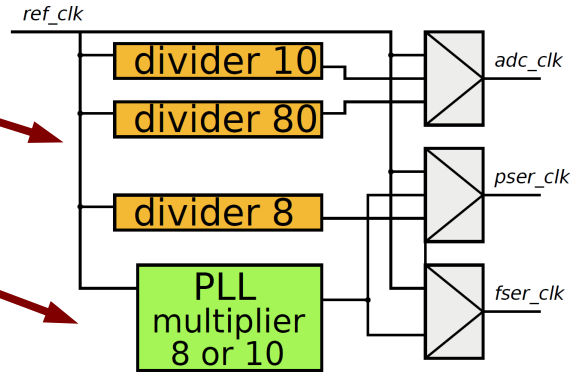
Very low power PLL has been developed and the prototype is fully functional.
Few issues (frequency gaps, jitter) need to be improved

8-channel 10-bit SAR ADC in IBM 130 nm Architecture and Design

Specifications & implementation issues:

- 8 channels of 10-bit SAR ADC
- Multimode digital multiplexer/serializer:
  - Full serialization: one data link per all channels (external clk division or PLL clk generation)
  - Partial serialization: one data link per channel (external clk division or PLL clk generation)
  - Test mode: single channel output (max fsmp ~50 Msps)
- High speed SLVS interface (~1GHz)
- Multiple clock generation schemes (with or without PLL)
- PLL for data serialization
- Power pulsing





Chips just arrived to CERN !

TSMC CMOS 130nm story…

- CERN contract wit IBM finishes in 2015
- The future with IBM is not clear...
- We need to change the technology
- CERN is moving to TSMC 130 nm (radiation hardness needs to be verified...)
- TSMC seems cheaper than IBM but one need to submit large chips (>= 50k$)
- We are following CERN
  - development in IBM 130 nm stopped
  - first designs in TSMC 130 nm just starting
  - looks like never ending story...

Summary and Plans

- **New LumiCal readout in IBM 130 nm under development (but stopped)**
  - First 8 channel prototype of front-end electronics fabricated. First test show good results
  - First prototypes of 10-bit SAR ADC, PLL, SLVS already fabricated and tested:
    - 10-bit SAR ADC: results show good functionality, low power and ENOB~9.3
    - PLL fully functional, some improvements foreseen for 2nd prototype
    - SLVS interface works well at least up to 1 GHz
  - 8 channel ADC with PLL based serialization, SLVS interface, just fabricated, will be tested soon...
- **We need to change the technology again, most probably to TSMC 130 nm, design is just starting...**

Thank you for attention