SILAB
Silizium Labor Bonn

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DMAPS Design in XFAB Technology

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Outline

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- ✓ SOI process and overview of XFAB technology
- ✓ Prototype-chip XTB01 & readout design
- ✓ Measurement results
  - Leakage current
  - TID effects on transistor characteristics
- ✓ Layout improvement of the sensor

Silicon on Insulator

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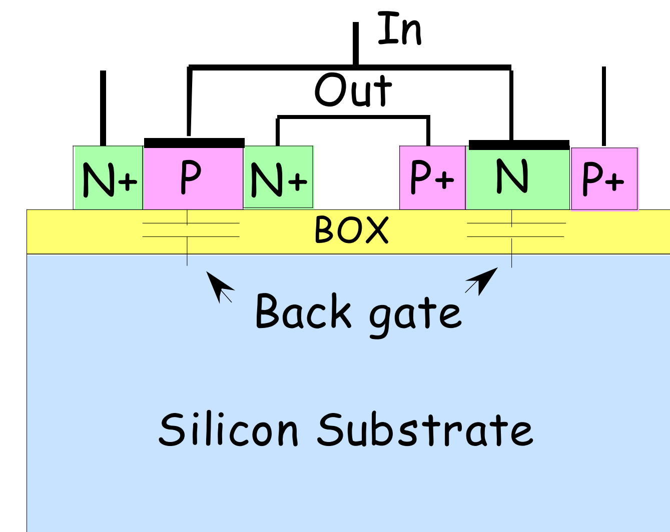
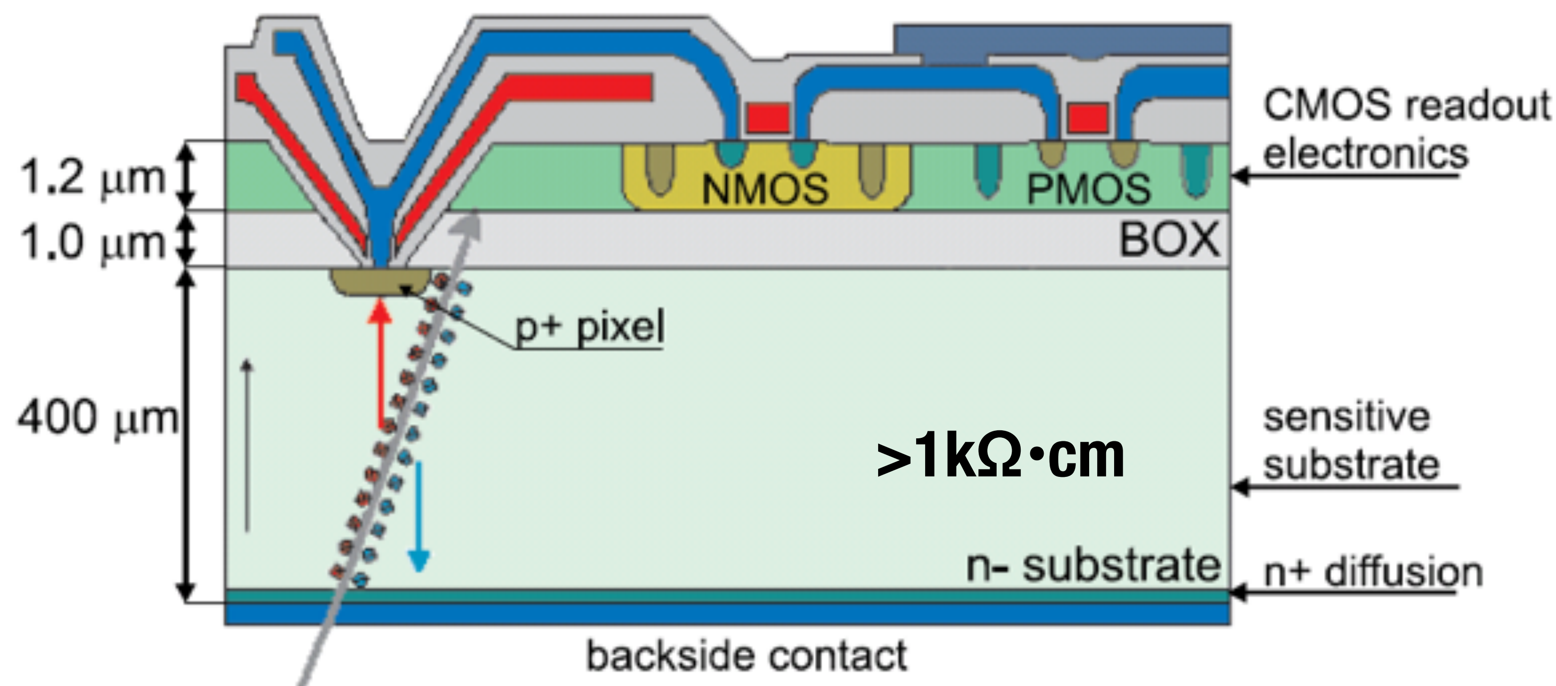
SOI utilizes the "handle wafer" as a detector, with electronics implemented in the thin device layer on top of the "buried oxide" (BOX).



Lapis (OKI) 0.15 - 0.2 um FD-SOI process

driven by KEK group



First approach toward truly monolithic device!

Performance is limited by:

- ✓ **mutual coupling between the electronics and the sensor**
- ✓ **charge injection due to swing of CMOS signals**
- ✓ **radiation effects: charge accumulation in BOX shifts transistor characteristics**

Technological overview

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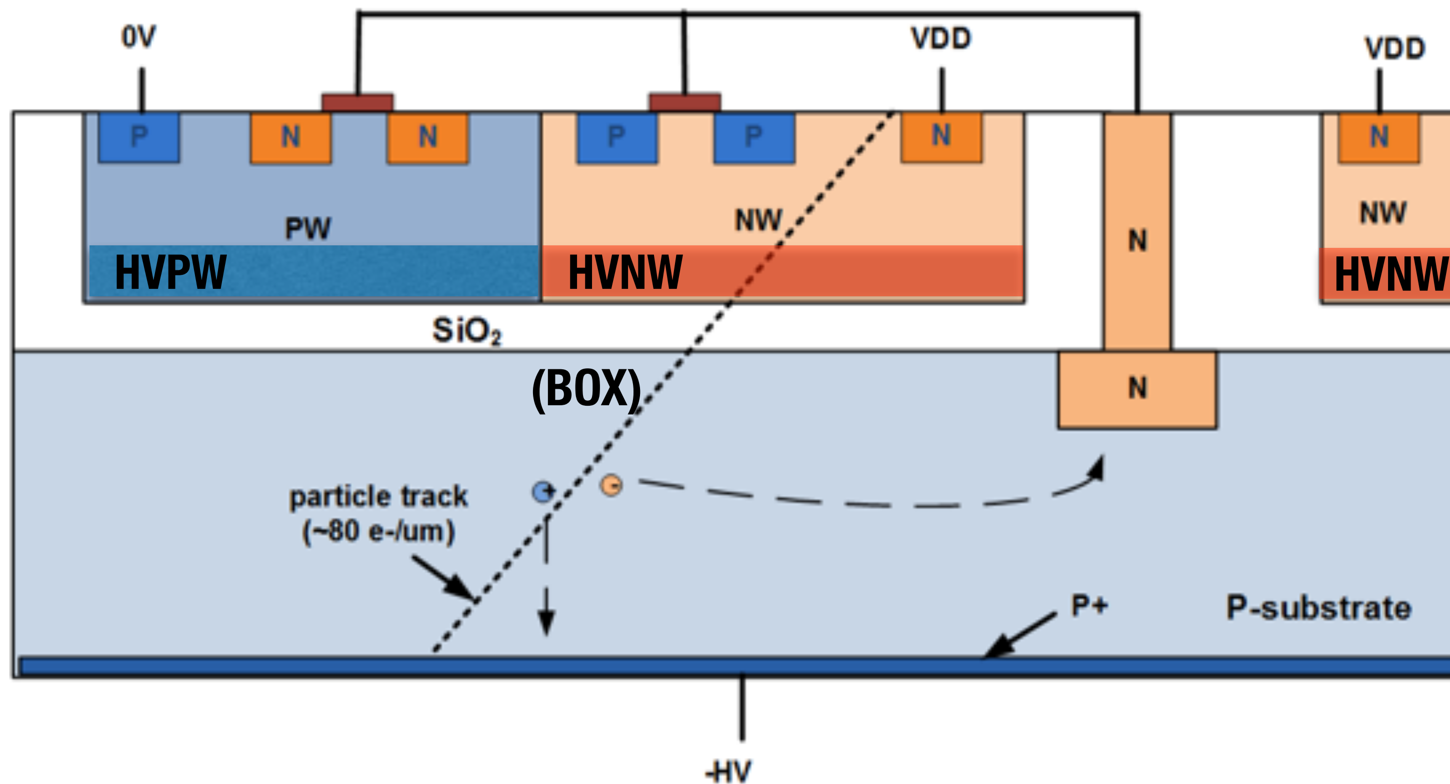
XFAB 180 nm HV SOI CMOS process



Feature size: 180 nm
Supply rail: 1.8 V
p-type bulk, 4 metal layers
Resistivity: ~100 Ω cm
High voltage: ~several 100 V

Thickness:
gate oxide: 4.1 nm
BOX: 1 um
Chip: 300 um
Distance from Gate to BOX: 3 um

- ✓ BOX isolates electronics part from the sensor part
- ✓ Depletion (full depletion possible in future)→ fast & high signals $d \sim \sqrt{\rho \cdot V}$
- ✓ Full CMOS electronics (CSA, shaper etc. if needed)
- ✓ Theoretically rad-hard (less SEU) + separated with HV-layers
  →also less coupled with sensor

more details…

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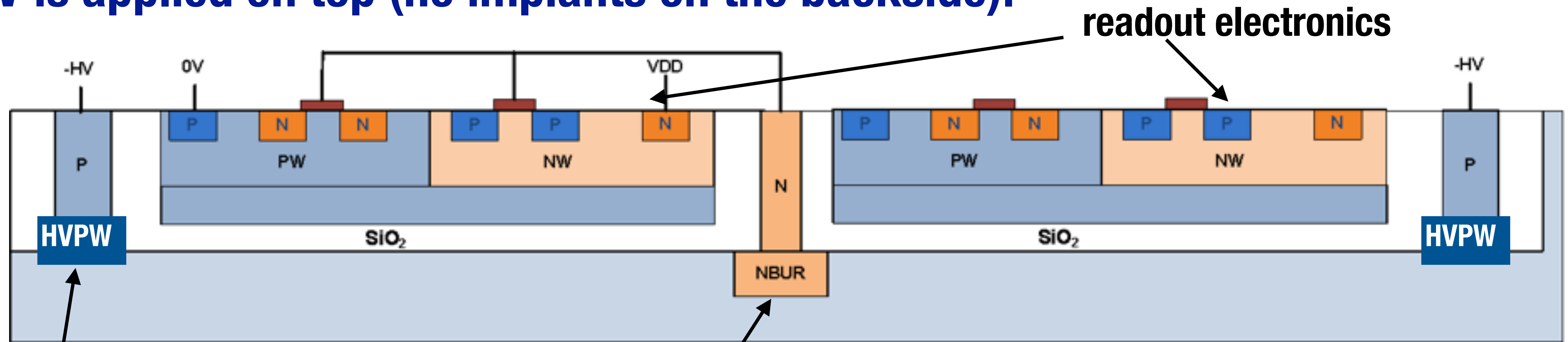
HV is applied on top (no implants on the backside).



sensor bias

charge collecting node

Resistivity: ~100 Ω cm
→Depletion thickness: ~50 um

Expected diode parameters from vendor

Type A	handle wafer diode breakdown	110 V
	handle wafer diode leakage	2 fA/um
Type B	handle wafer diode breakdown	160 V
	handle wafer diode leakage	5 fA/um
Type C	handle wafer diode breakdown	220 V
	handle wafer diode leakage	3 fA/um

Layout should be optimized…

- ✓Sensor part (breakdown, # of GR)
- ✓Radiation effects from BOX
- ✓Electronics part (area, power)

Practical layout

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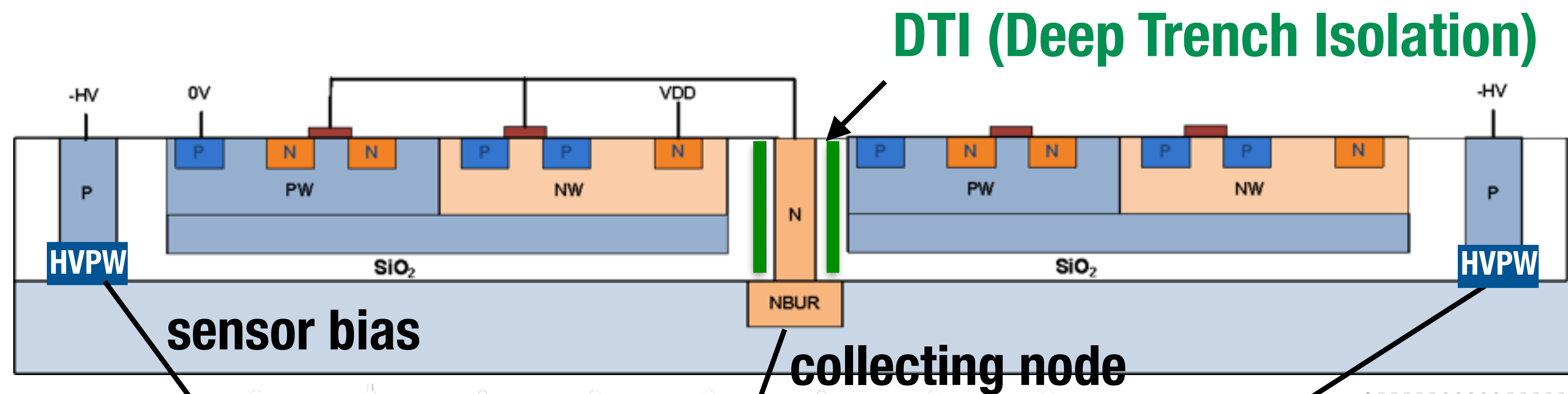
25 um pixel layout (cross-section)

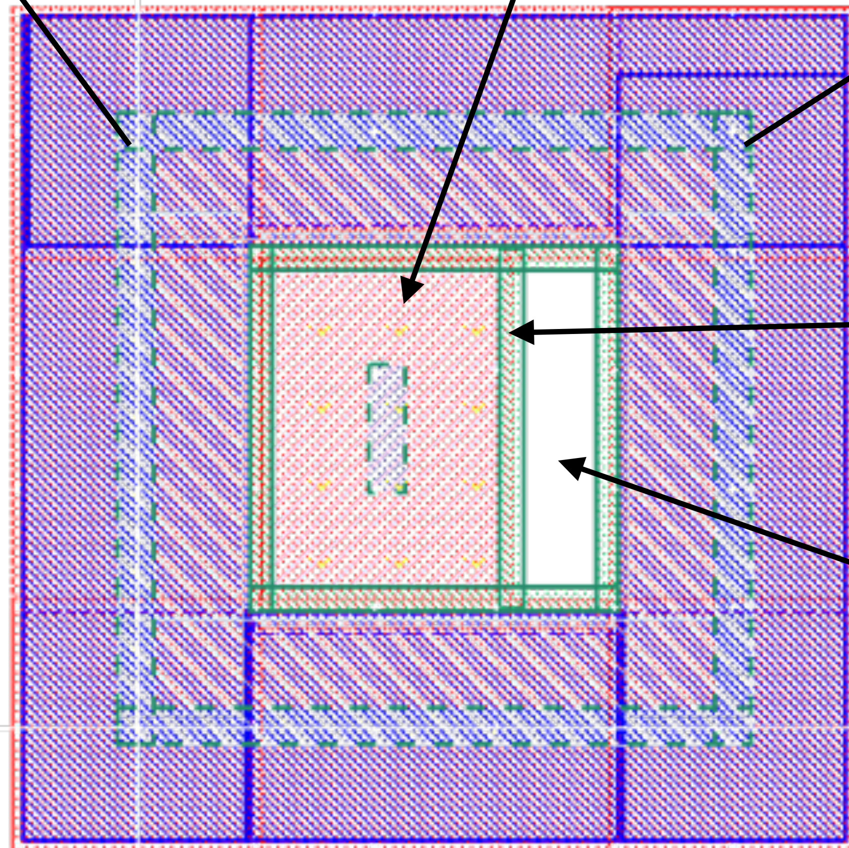
DTI (Deep Trench Isolation)



sensor bias

collecting node

TOP view



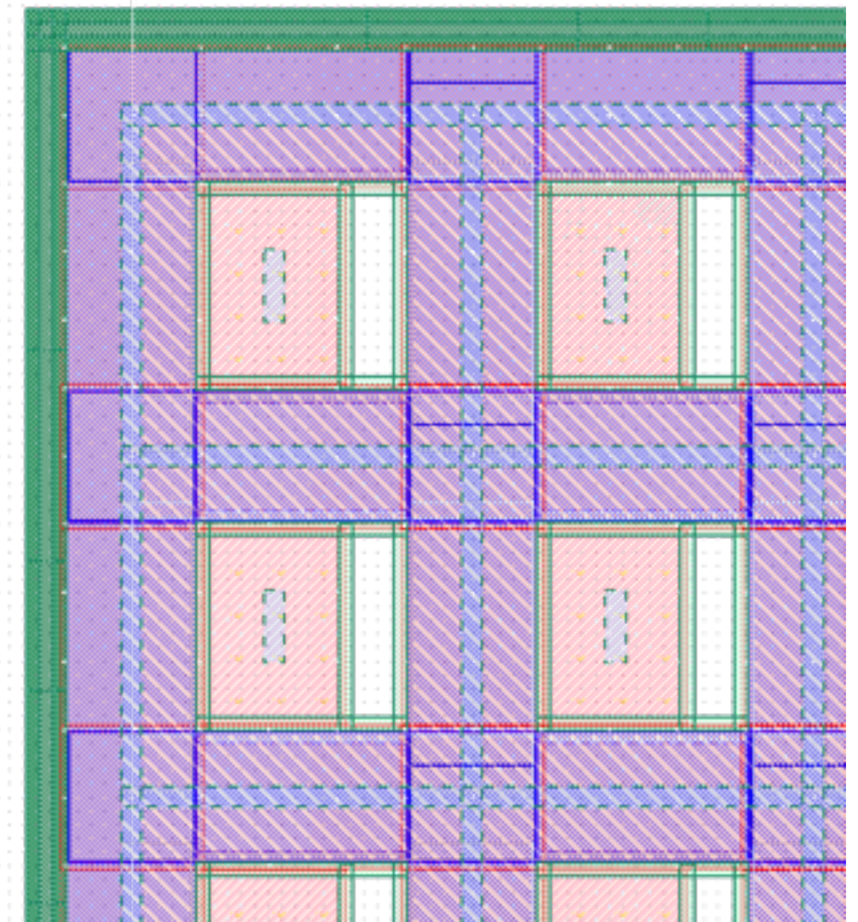
DTI

readout electronics (surrounding the collecting node)

P bias contact in every pixel through Metal 1

Array example

HV (bias) ring between pixels and around the chip



Readout electronics

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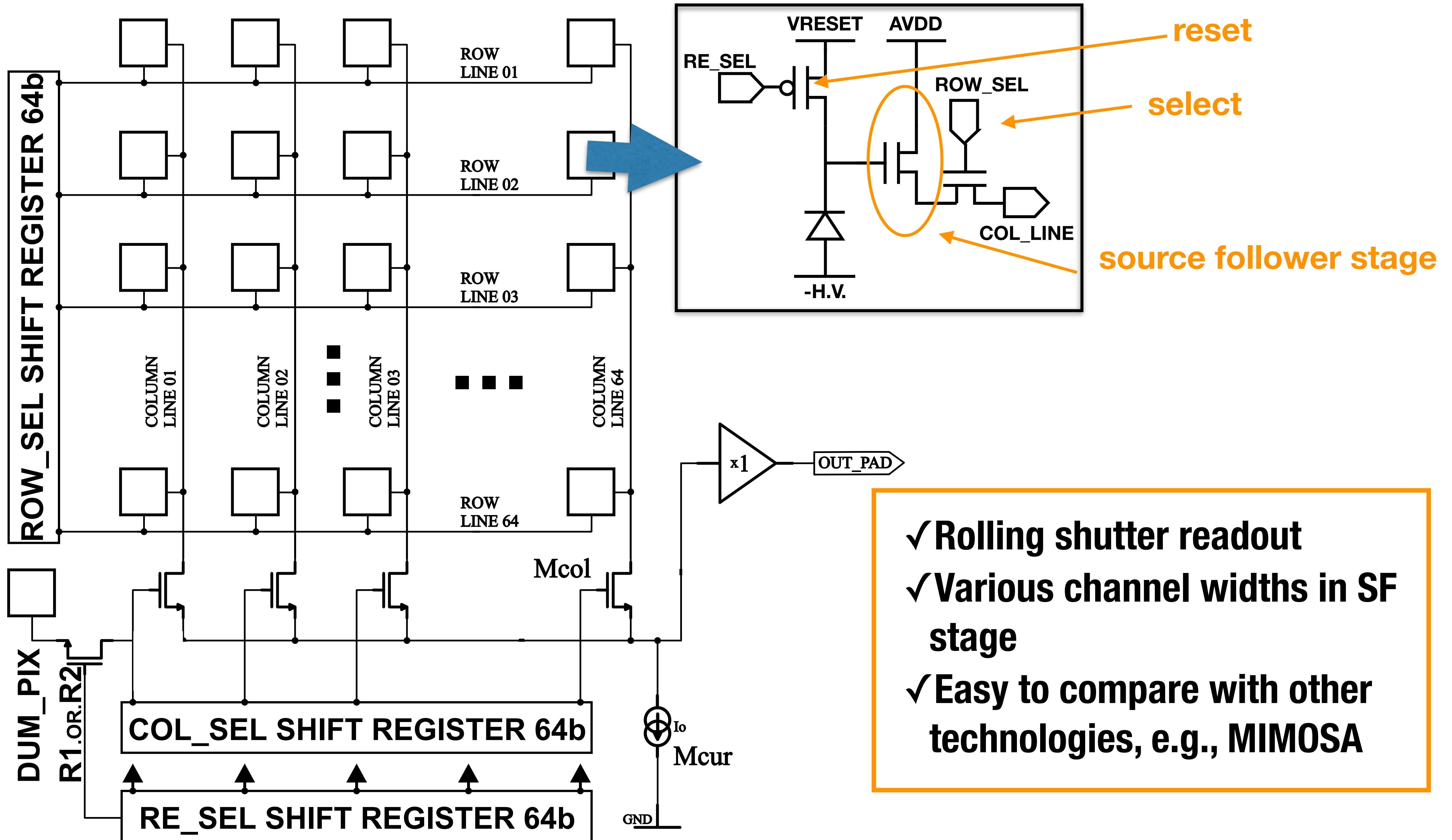
1. "standard" 3 transistor (3T) R/O scheme

R. Turchetta et al. NIM A, 458 (2001) 677



- ✓Rolling shutter readout
- ✓Various channel widths in SF stage
- ✓Easy to compare with other technologies, e.g., MIMOSA

Readout electronics (cont.)

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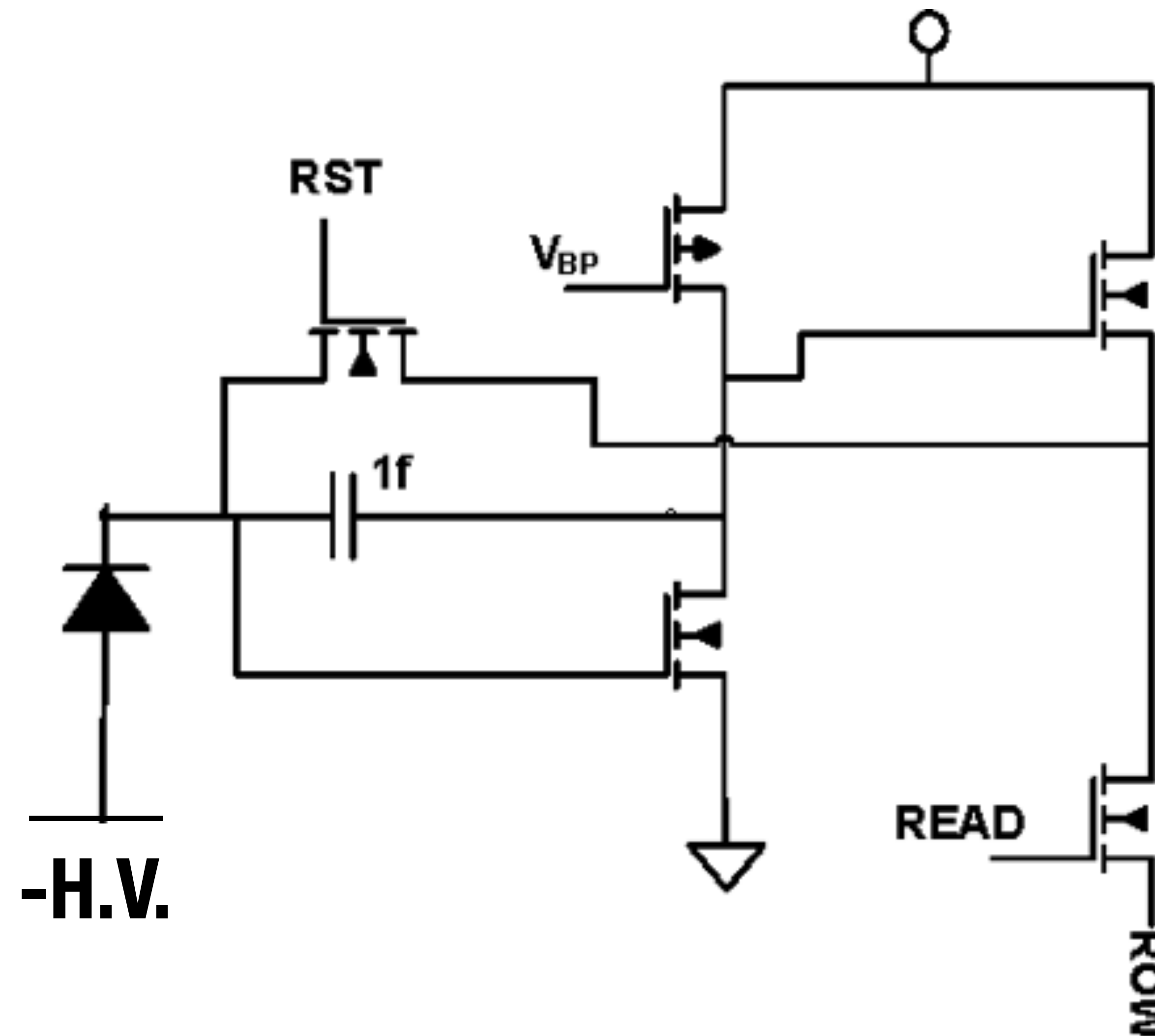
2. Common-source architecture



✓ CS amp. + Source follower
✓ Rolling shutter readout

Readout electronics (cont.)

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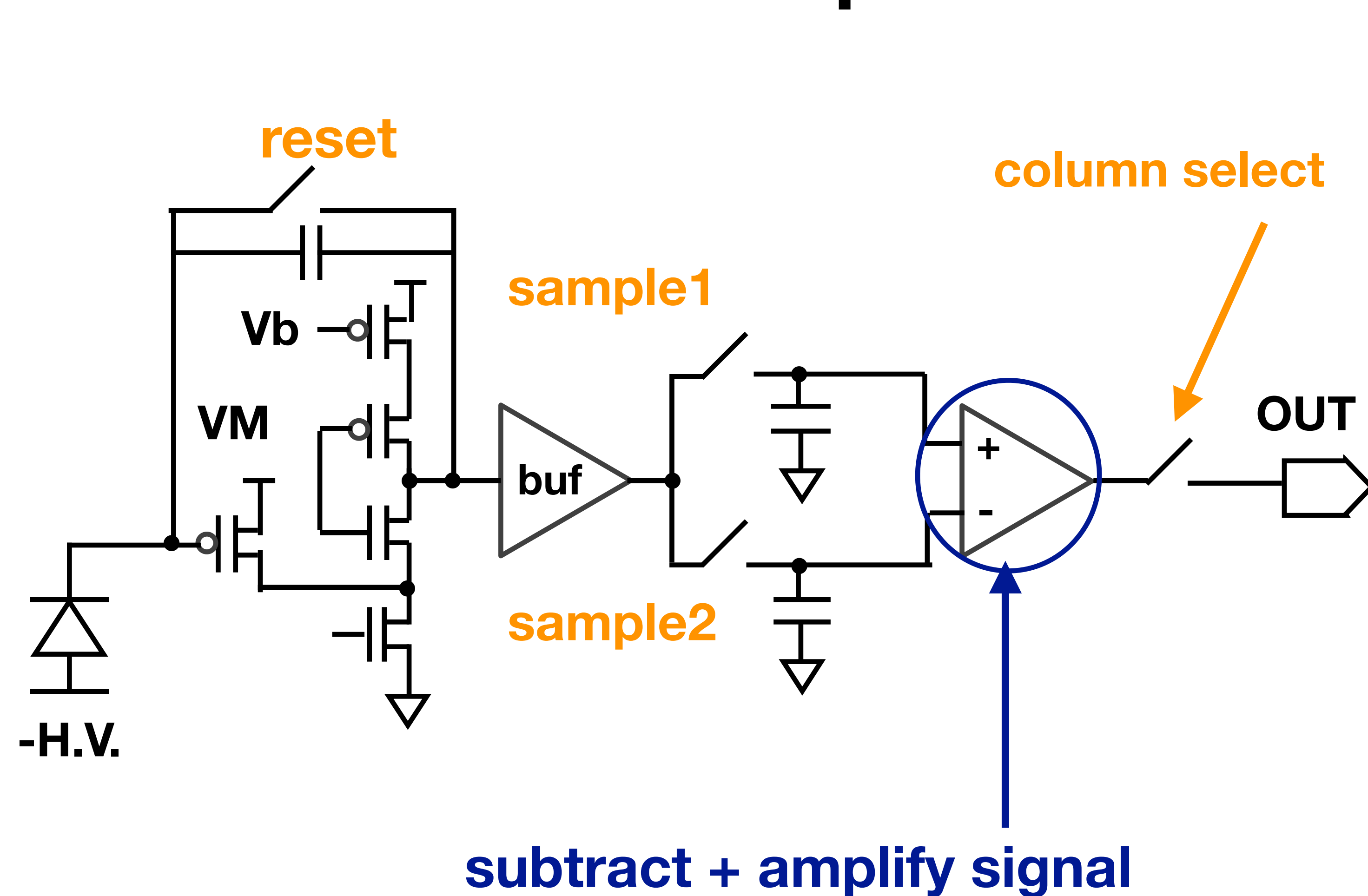
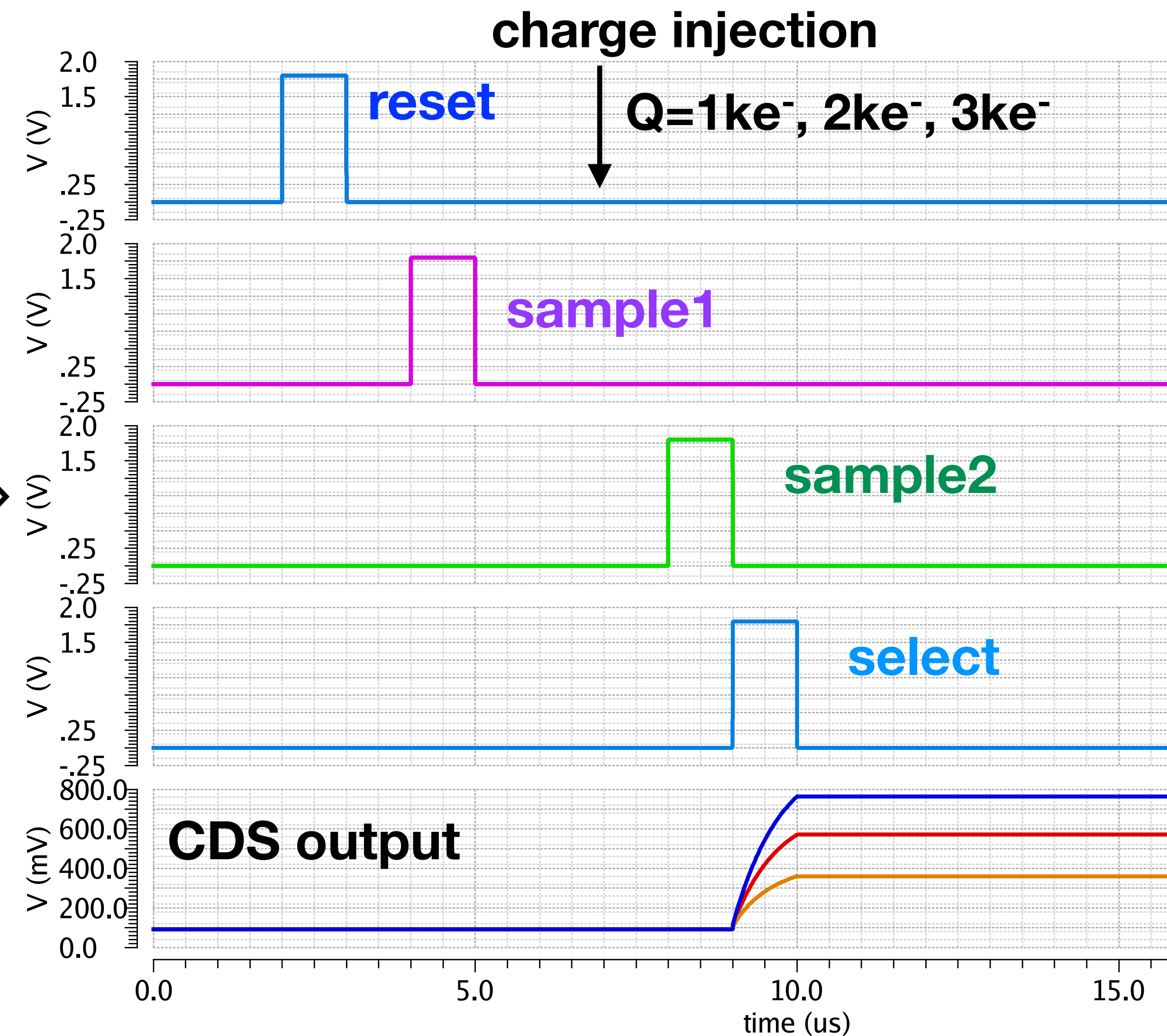
3. Folded-cascode + in pixel CDS





G. De Geronim et al. NIM A, 471 (2001) 192

- ✓ No fixed pattern noise in analog output
- ✓ No external amplifier needed
- ✓ Rolling shutter readout

Prototype-chip: XTB01

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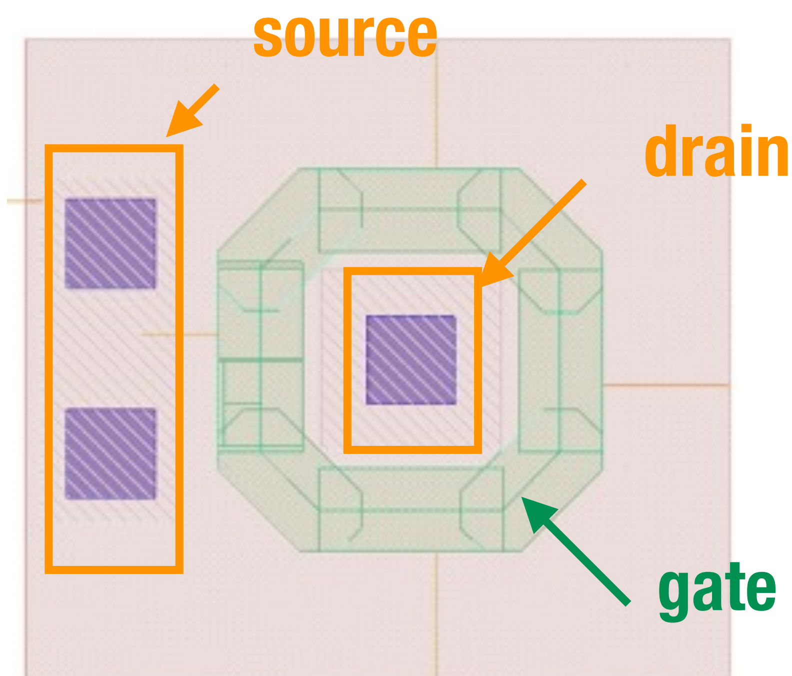
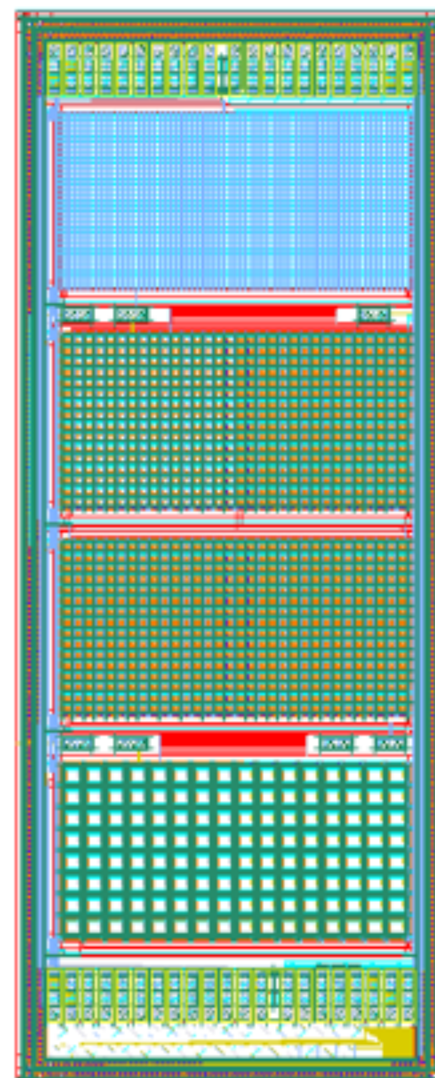
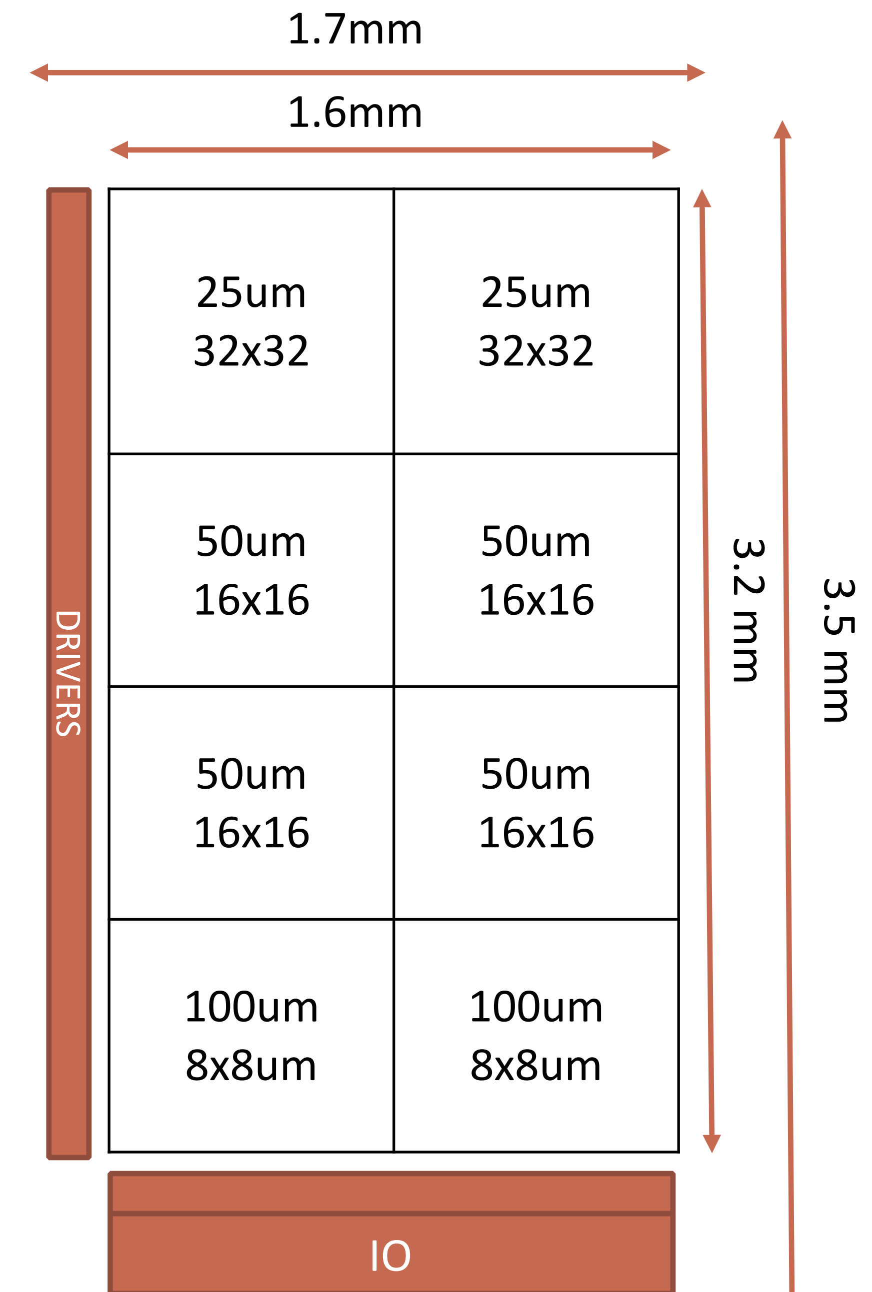
- ✓ Area: 5 × 2 mm^2
- ✓ Thickness: 300 um
- ✓ 4 matrixes with different pixel sizes: 100 × 100 um^2, 50 × 50 um^2 (x2), 25 × 25 um^2
- ✓ 3 types of readout
- ✓ Radiation test structure: normal + enclosed gate FETs

Enclosed gate FET



Submitted in Feb. 2013





Measurement setup

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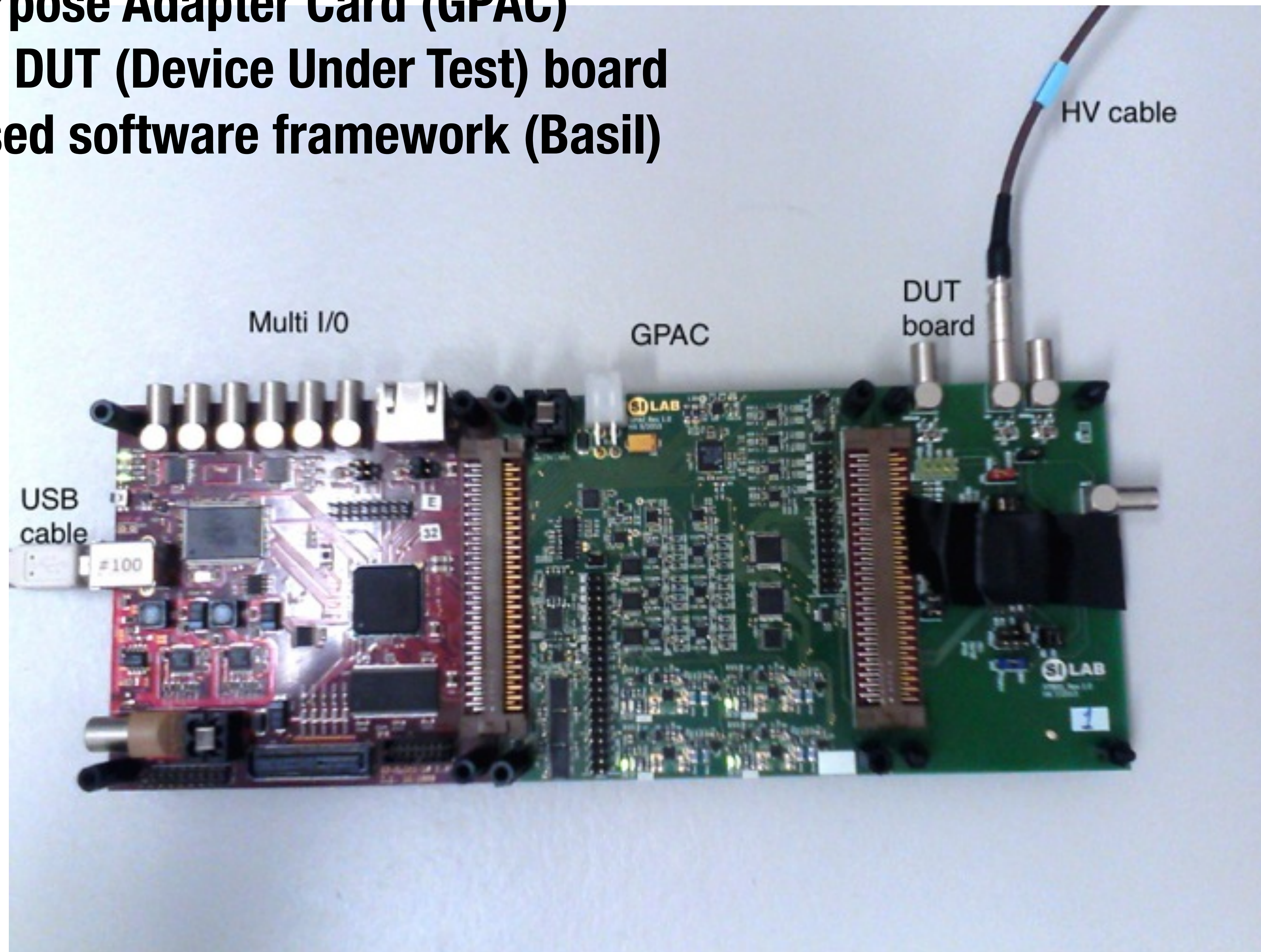
- ✓ Multi I/O board
- ✓ General Purpose Adapter Card (GPAC)
- ✓ Chip on the DUT (Device Under Test) board
- ✓ Python-based software framework (Basil)



Signals from 3T readout

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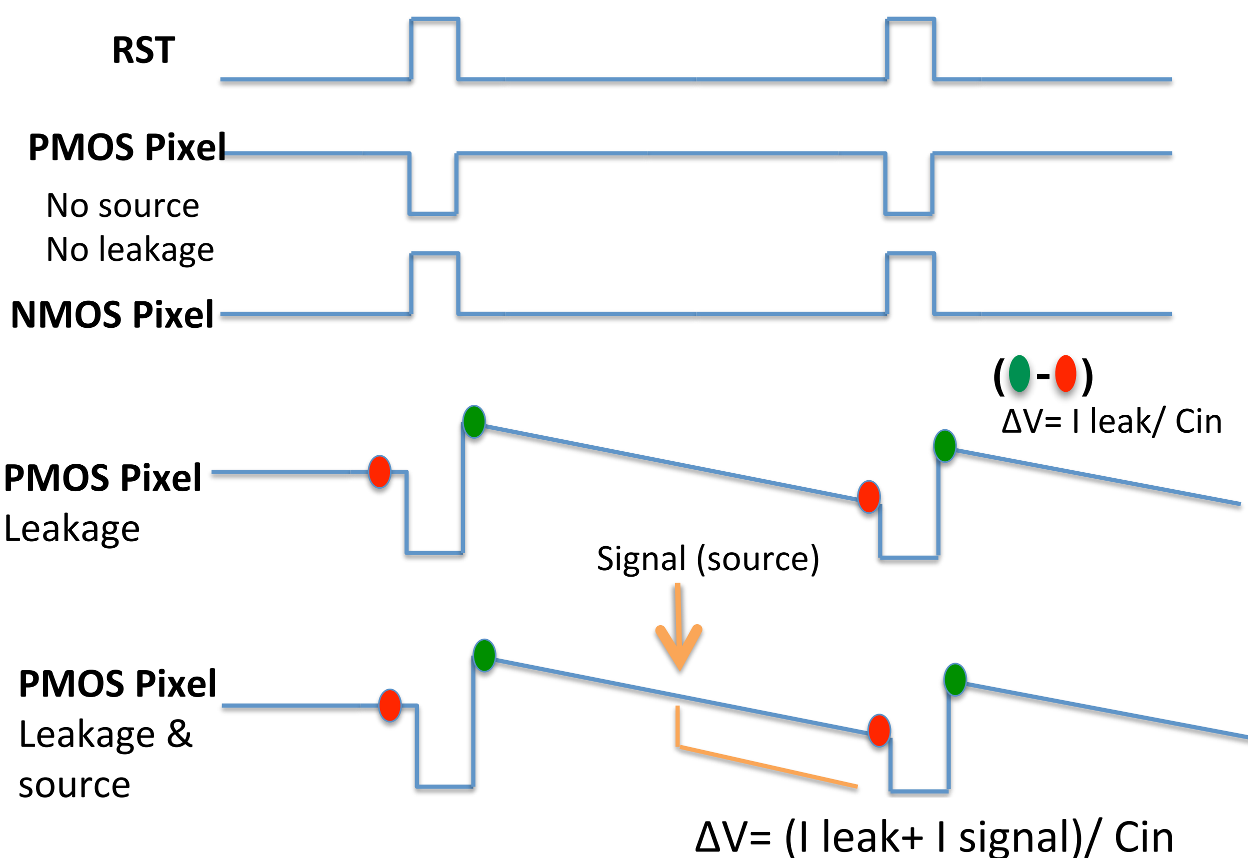

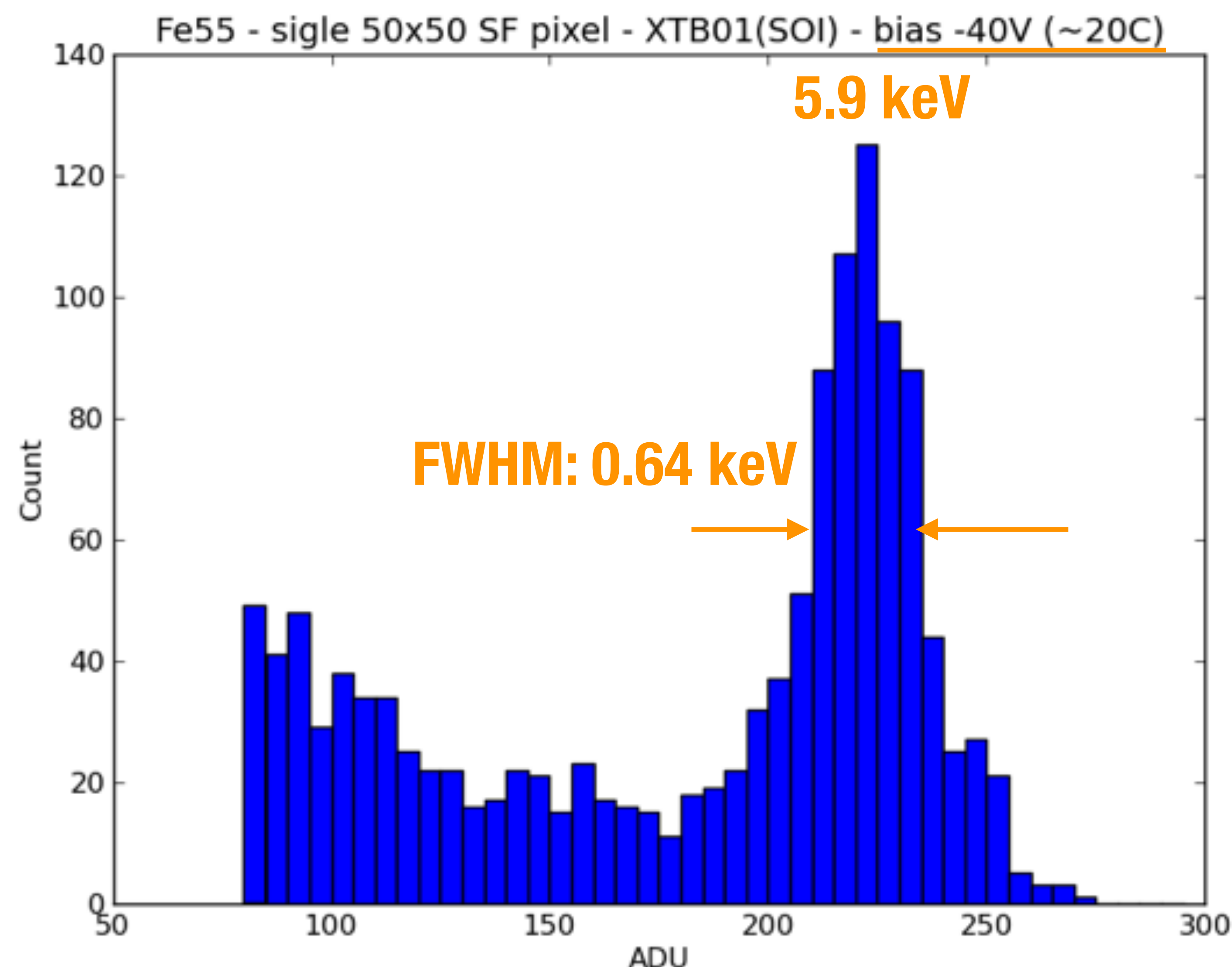

Spectrum was obtained only from 3T readout because of high leakage current. 😱

Leakage current

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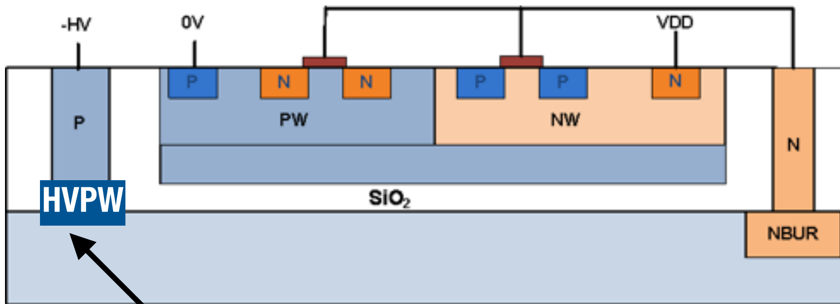
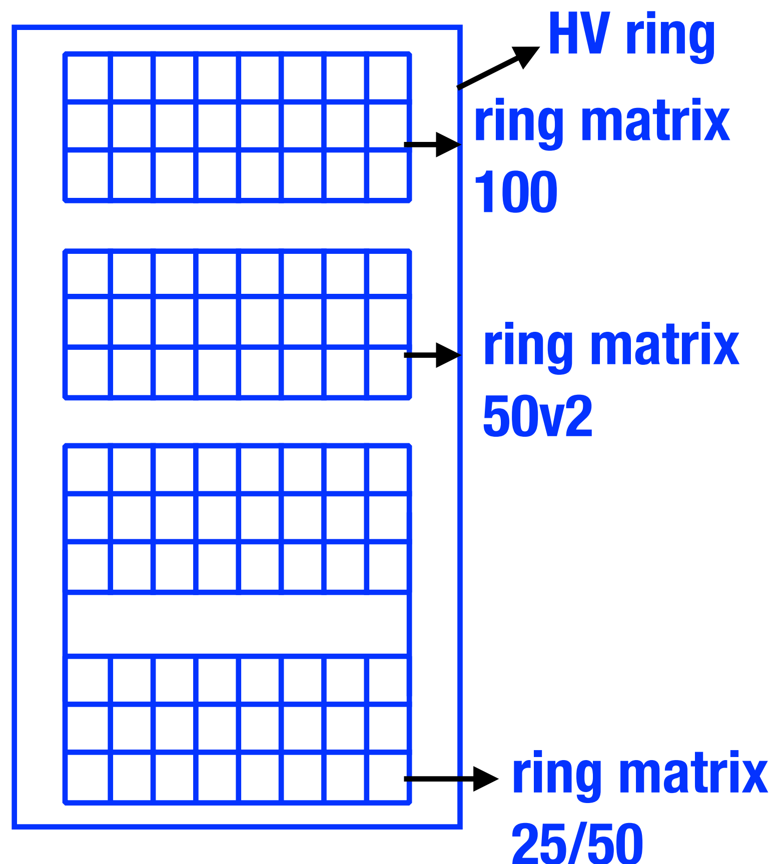
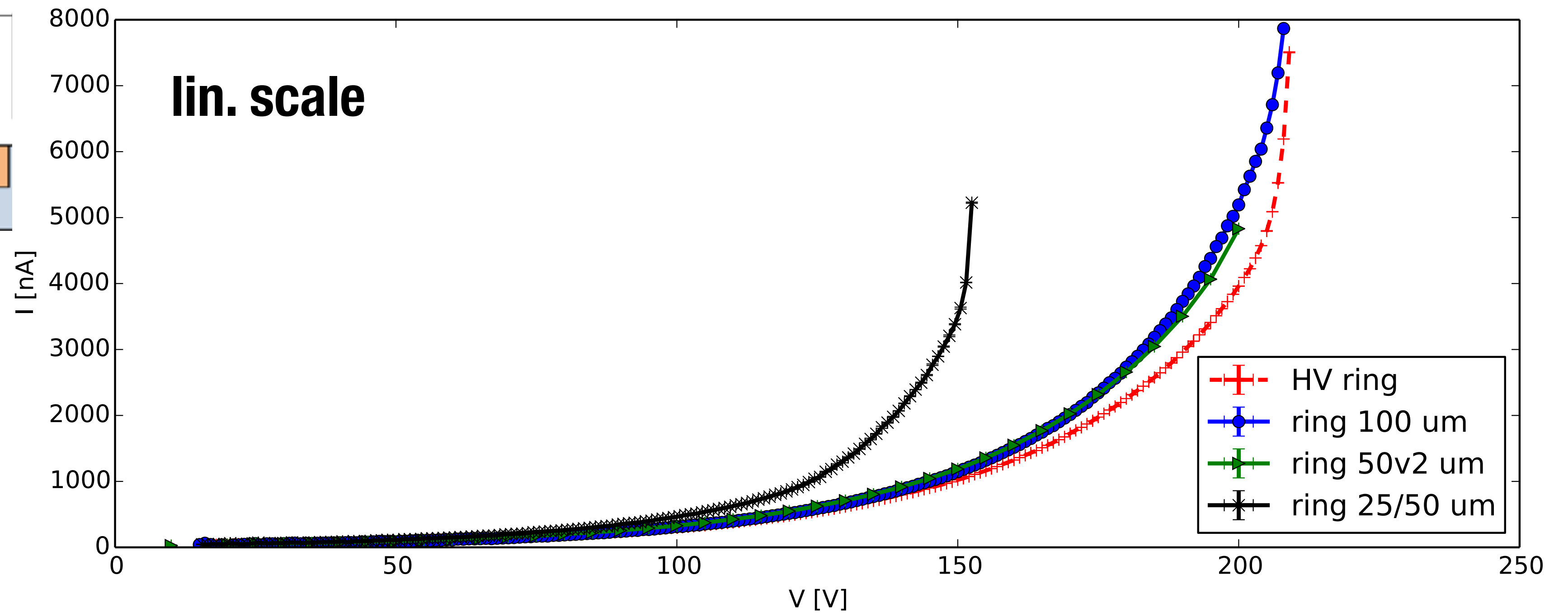
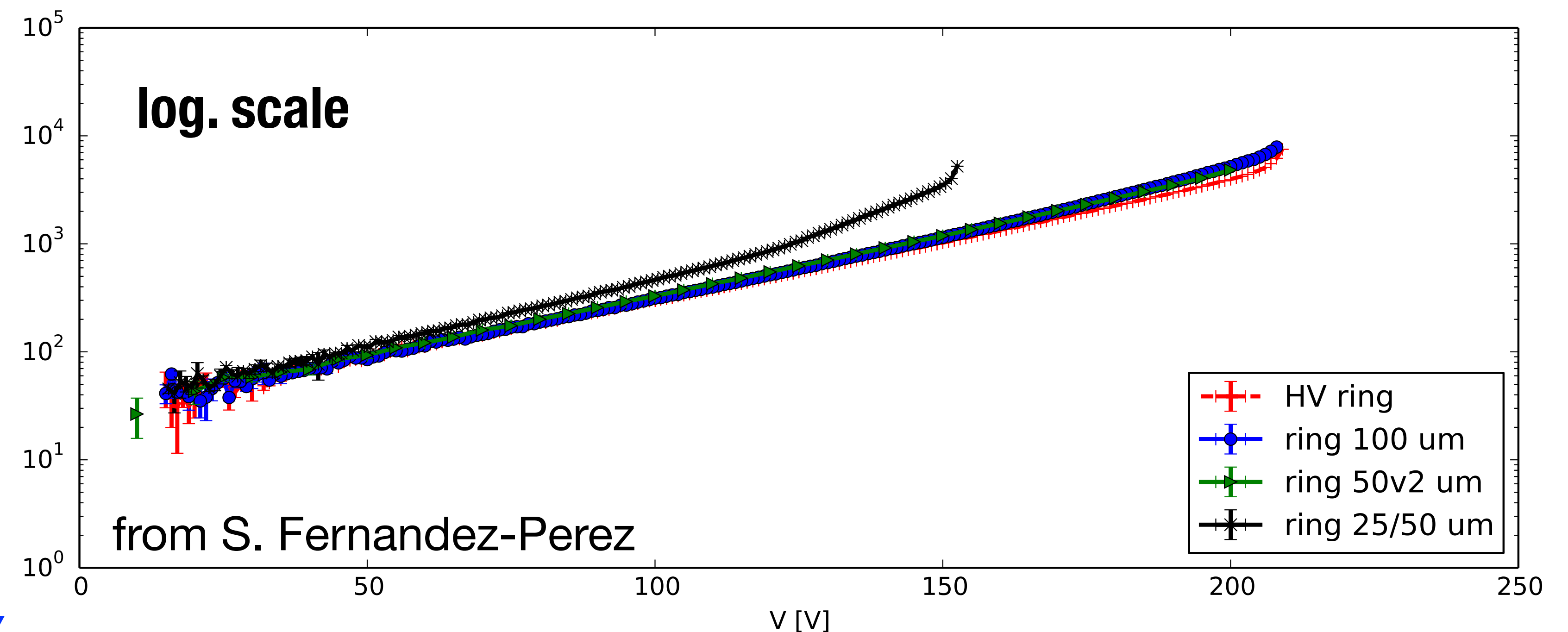


HV (bias) ring between pixels and around the chip



HV ring @ 20 degrees, Relative humidity < 8%





~10^3 times larger than expected (@ room T).

Temp. dependence

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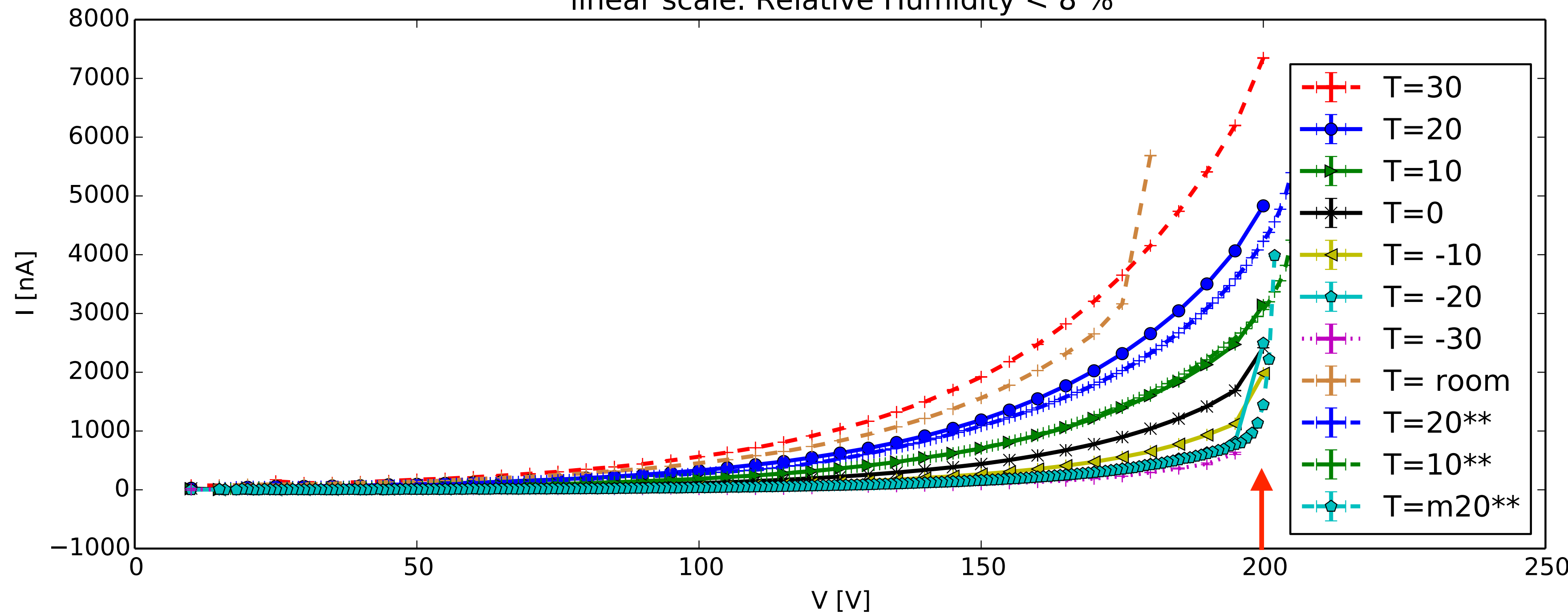
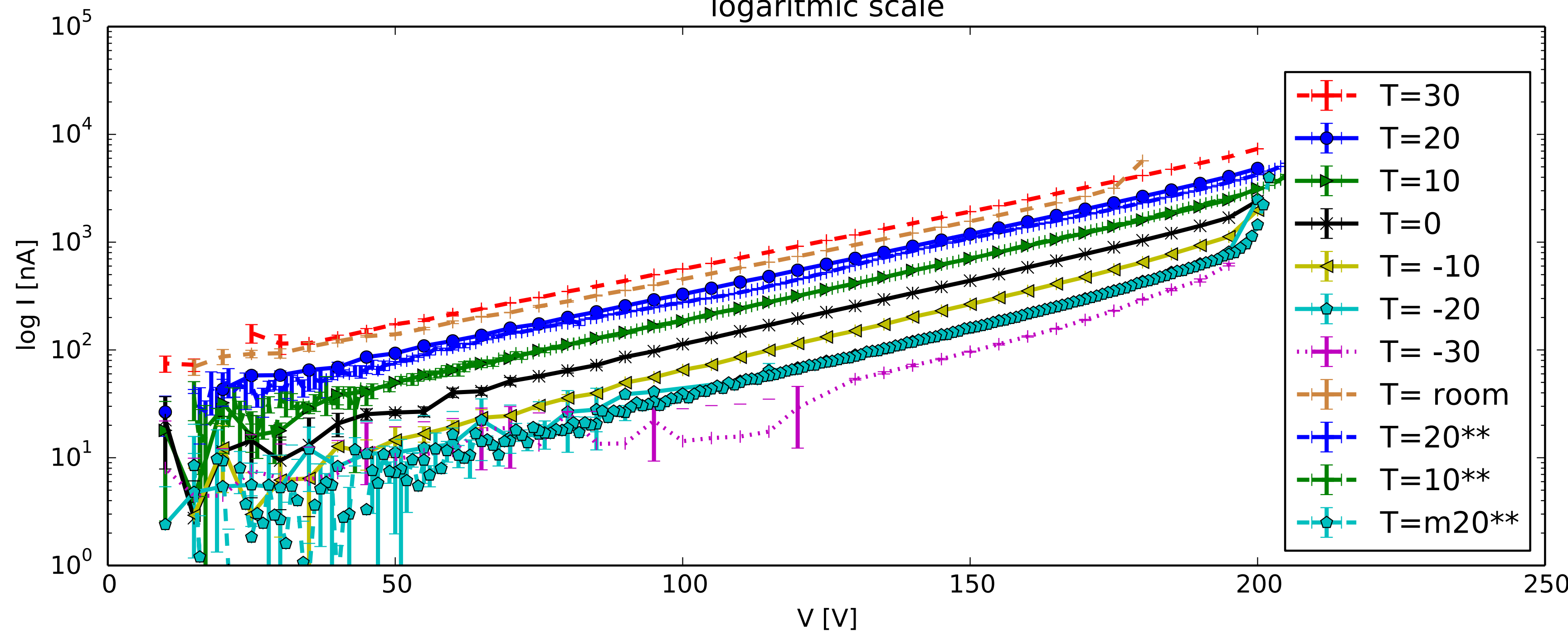
Matrix: 50 um x 50 um





$$I_{leak} \propto e^{-\frac{E_g}{kT}}$$

Eg: activation energy

- ✓ **Expected behavior with temperature.**
- ✓ **Matrix stands up to 200 V.**
- ✓ **Still 100 times larger…**

Leakage current after irradiation

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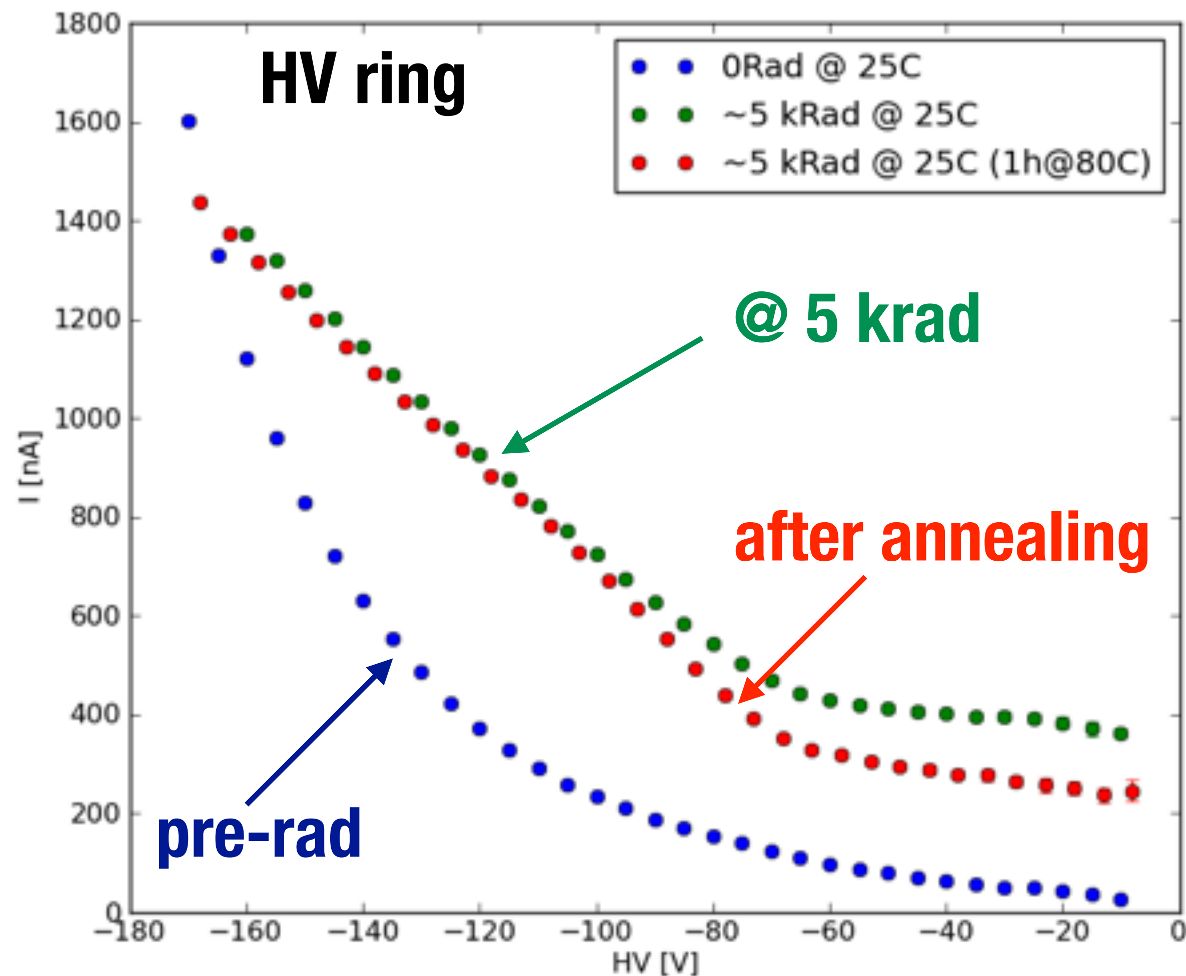
1 week irradiation with ^{90}Sr source



Charge accumulation in BOX affects the leakage current / breakdown voltage.

1 um +++ BOX (SiO_2)

Thermally grown oxides typically have from mid-10^{10} to 1-2x10^{11} positive charges per cm^2, localized within about 35 Å of the Si/SiO_2 interface.

Radiation can induce 1x10^{12} to 1x10^{13} positive charges per cm^2. (increased by 100 after irradiation)

Trap-assisted band-to-band tunneling?

In case of strong electric field inside the structure we also get impact ionization mechanism…

Oxide charge effect by TCAD sim.

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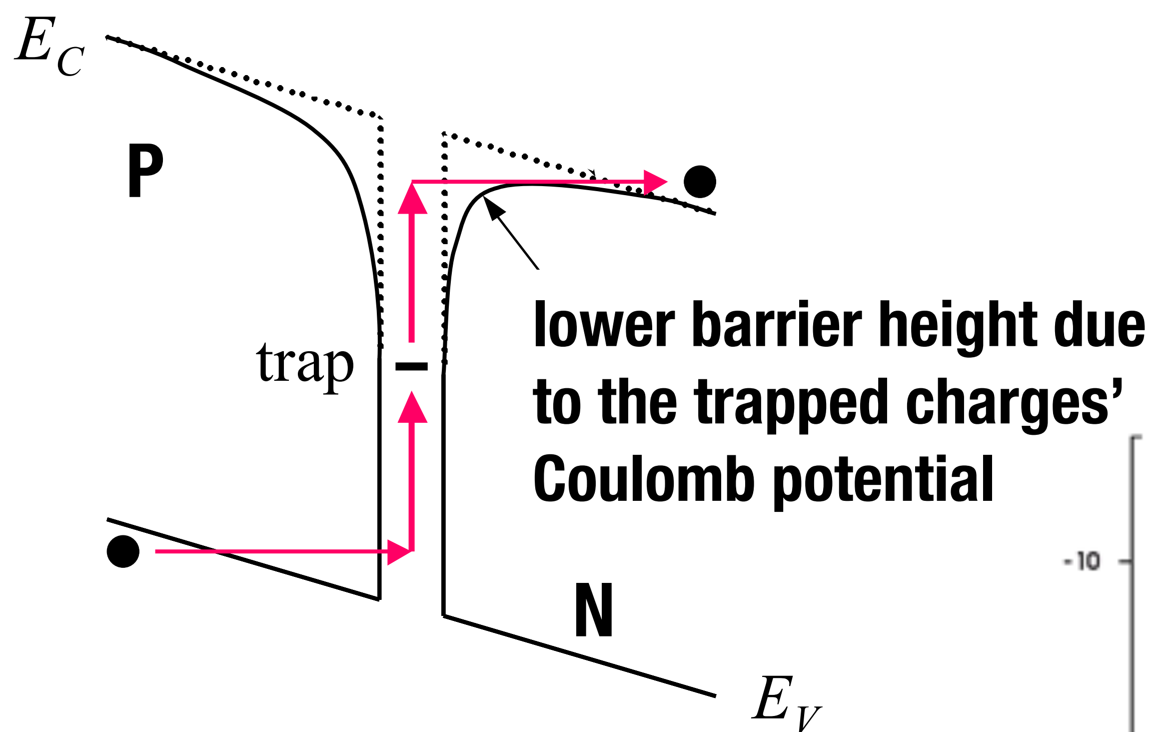
Trap-assisted band-to-band tunneling



-HV
0V
VDD
-HV
P
PW
NW
N
NBUR
SiO_2
HVPW
HVPW
Y
X
BOX
Doping Concentration [cm^-3]
5.015e+19
1.079e+13
2.323e+06
0.000e+00
-2.323e+06
-1.079e+13
-5.015e+19

from T. Hemperek

Oxide charges in BOX

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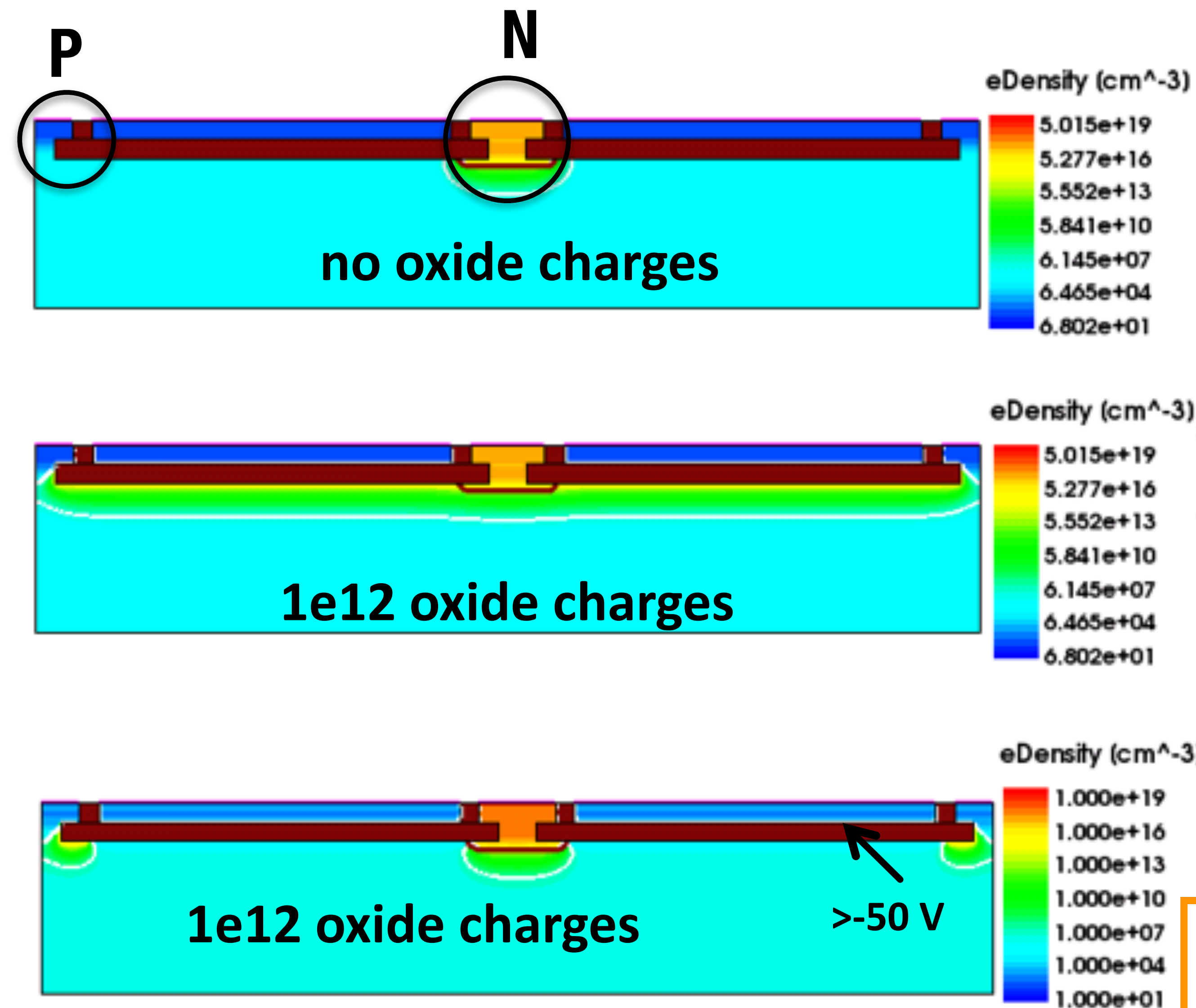

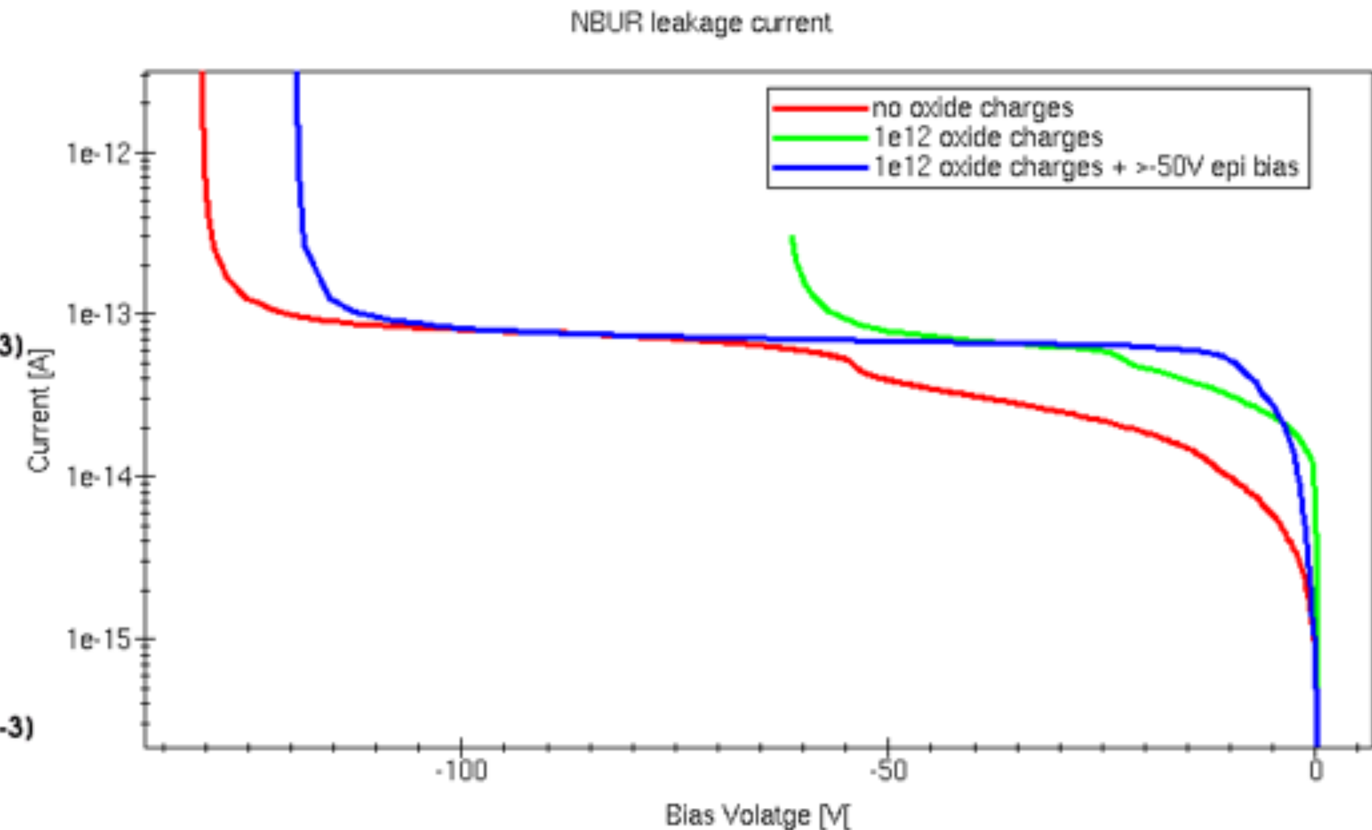

Epi bias mitigates the breakdown voltage.

Solutions to large I_{leak}

✓ P-stop – light p+ implant below oxide
✓ AC coupling to the readout

Total ionizing dose (TID) effects

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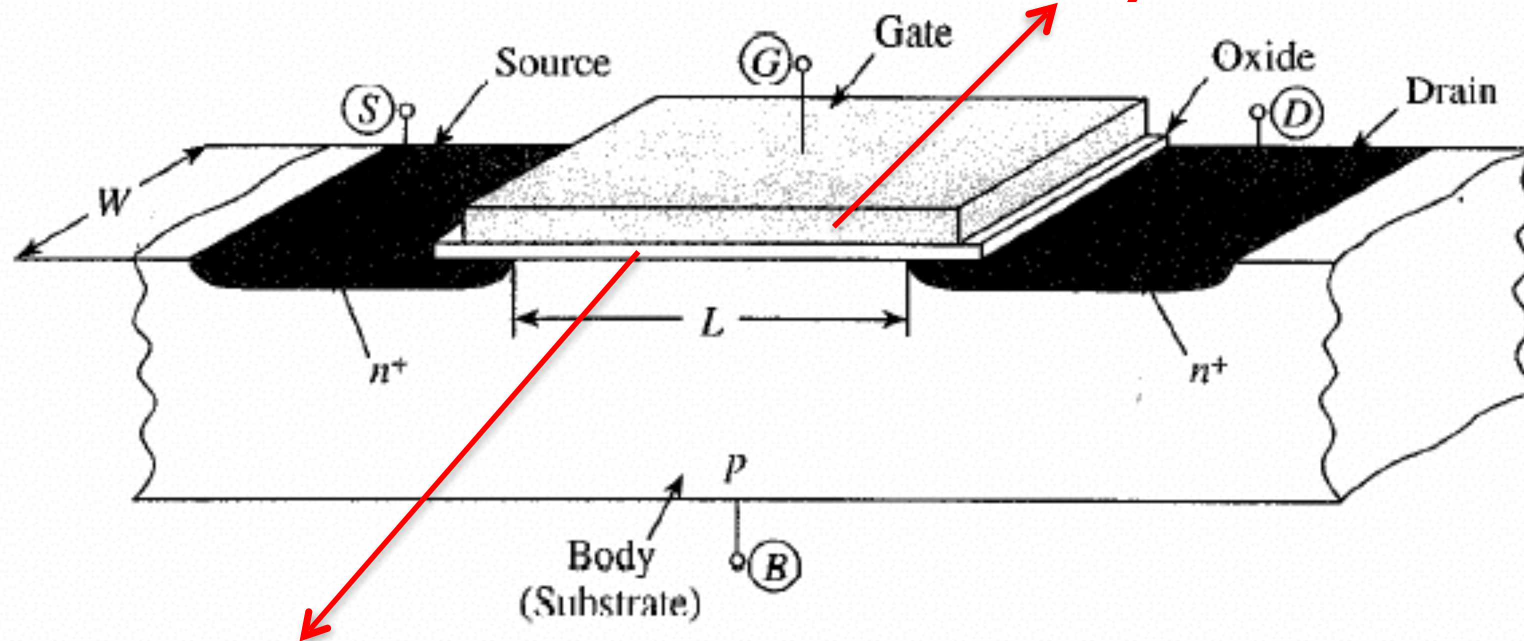
X-ray irradiation at CERN

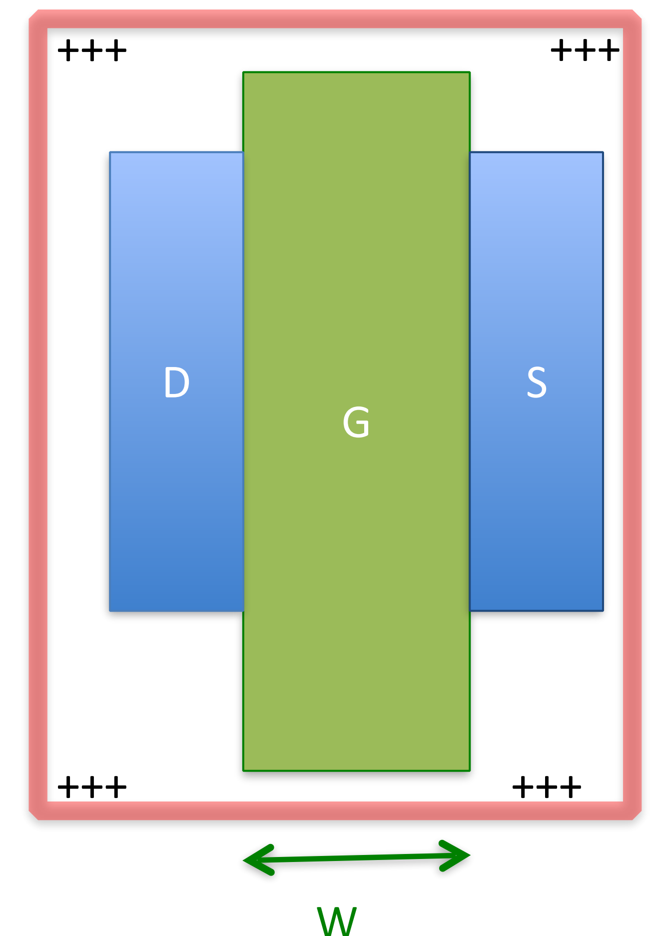
1) Positive charges in the gate oxide



2) Interface traps (Si02- Si)

3) STI effect
(Shallow Trench Isolation)

Top view of MOSFET



Either the STI oxide and STI interface traps influence the field of the gate, and therefore the electrical parameters.

Transistor threshold variation

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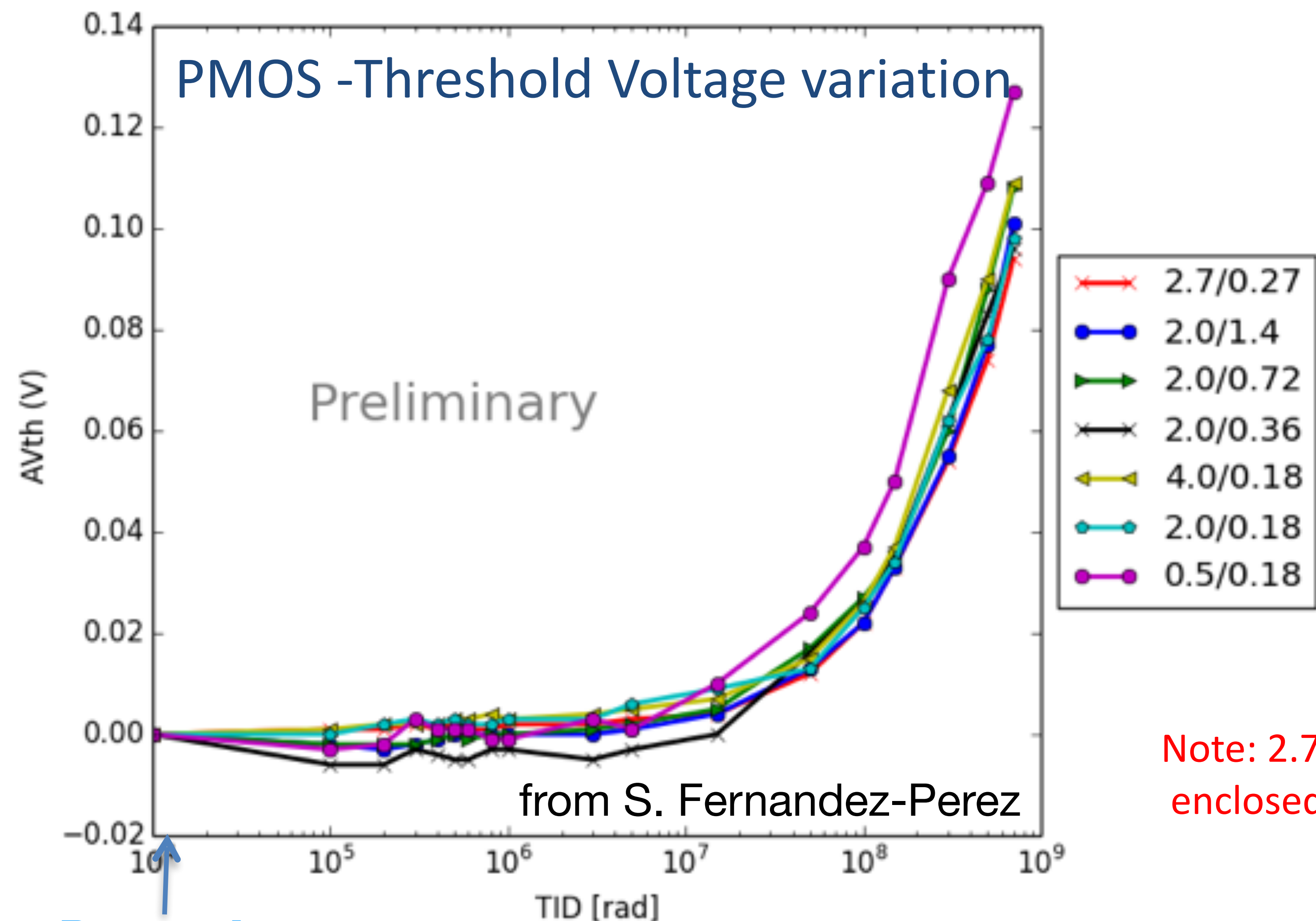

Note: 2.7/0.27 is an enclosed transistor

The threshold voltage increases with irradiation due to 2 effects:
Either the gate/STI oxide trapped charges and/or the gate/STI interface traps
ΔVth~120 mV @ 700 Mrad for PMOS, ΔVth~80 mV @ 700 Mrad for NMOS
(supply rail of 1.8 V)

→in the order of process variation

Transconductance variation

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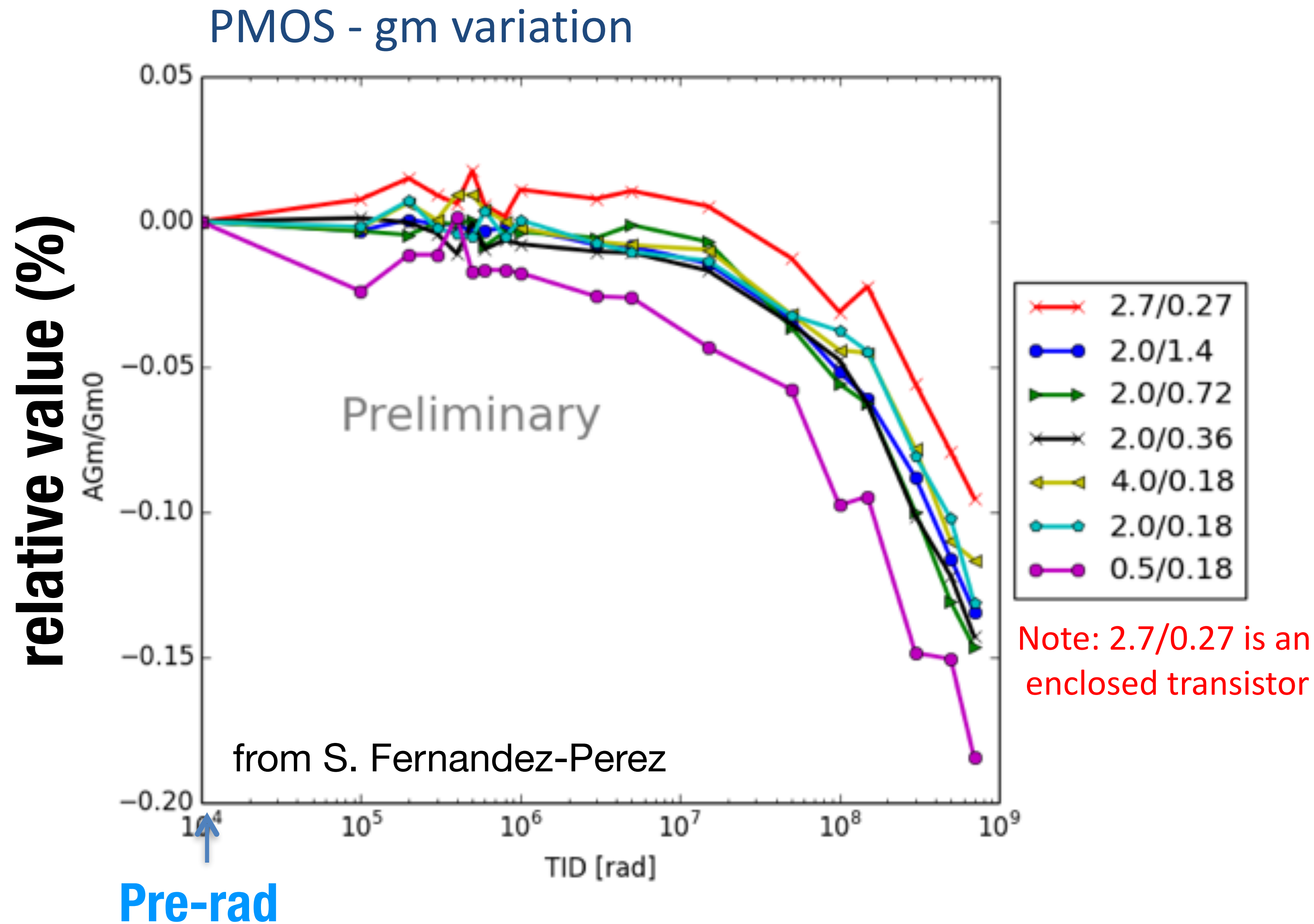

transconductance variation @ 700Mrad: 10-20% decrease for PMOS, 5% decrease for NMOS

- ✓Consistent with non SOI thin gate oxide technologies.
- ✓No BOX effects are observed.

Layout modification

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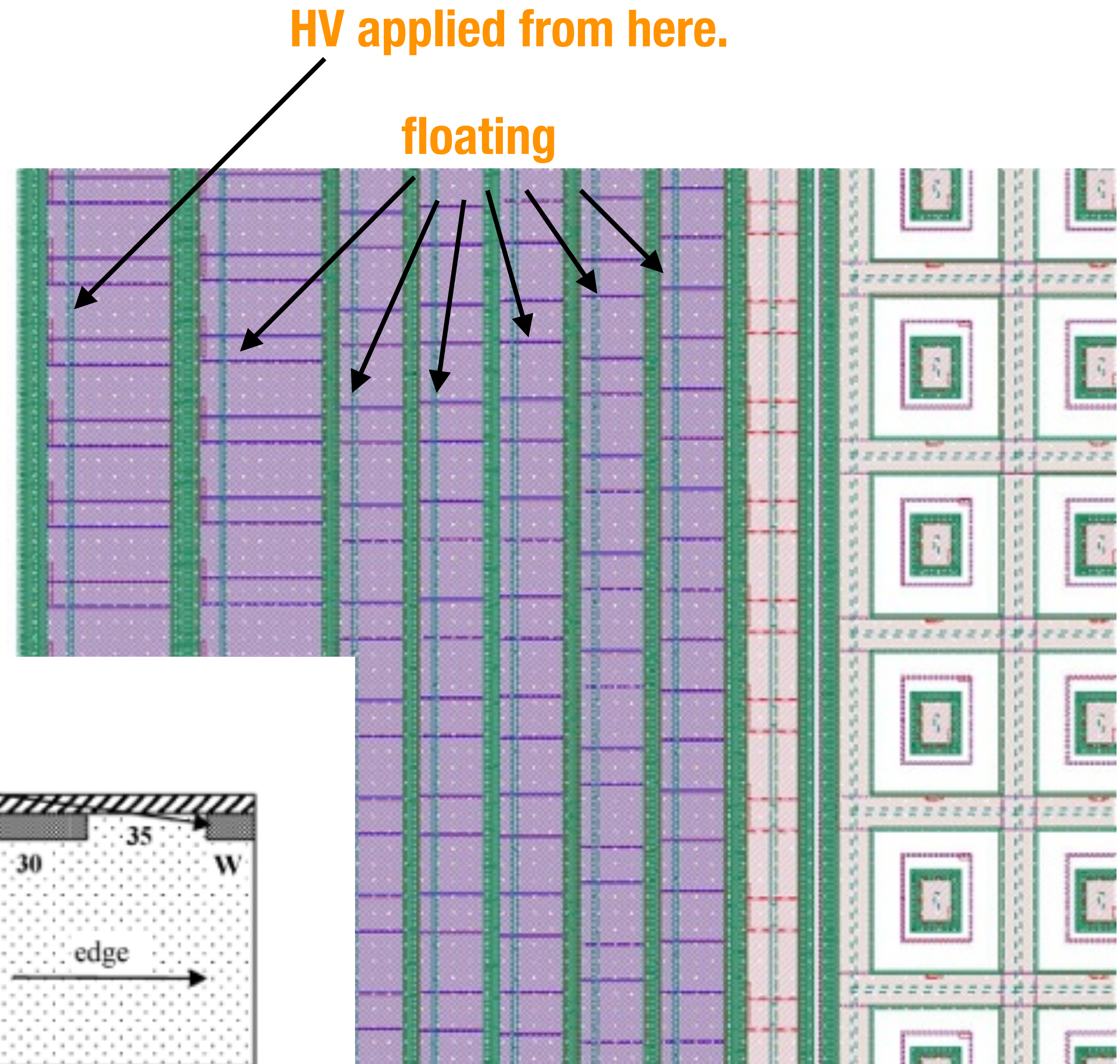
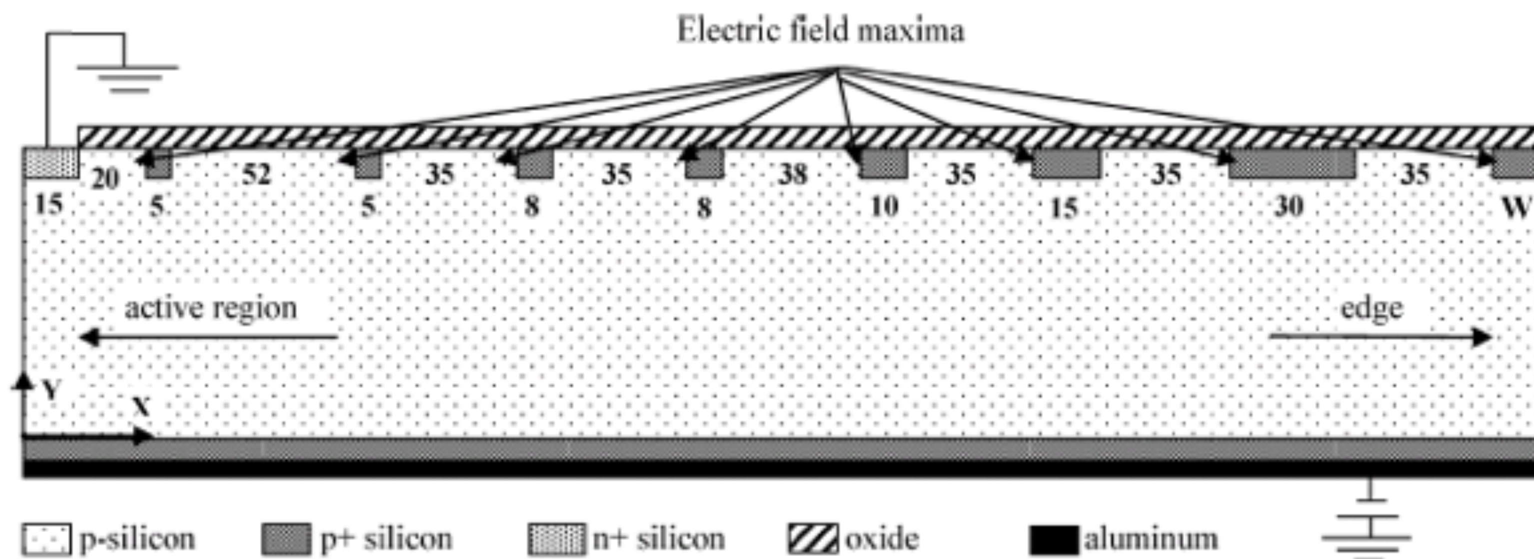
- ✓ HV (bias) from outside of matrix
- ✓ Increase # of GR rings to mitigate break down
- ✓ Increase # of DTI
- ✓ P-stop – light p+ implant bellow BOX
- ✓ Simple diodes only (no complex readout)



O. Koybasi et al. IEEE TNS, 57 (2010) 2978



Submitted in June 2014

Summary

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- ✓ The prototype-chip stands up to 200 V.
- ✓ Output from the 3T matrix works.
- ✓ Large leakage current might come from the charge accumulation in BOX and trap-assisted tunneling.
- ✓ Threshold voltage shifts of transistors are in the order of process variation up to 700Mrad.
- ✓ No effect of the BOX. All results are consistent with non SOI thin gate oxide technologies (e.g., FEI-4/IBM 130nm).
- ✓ We modified the diode layout and submitted in July 2014.

Thank you very much.